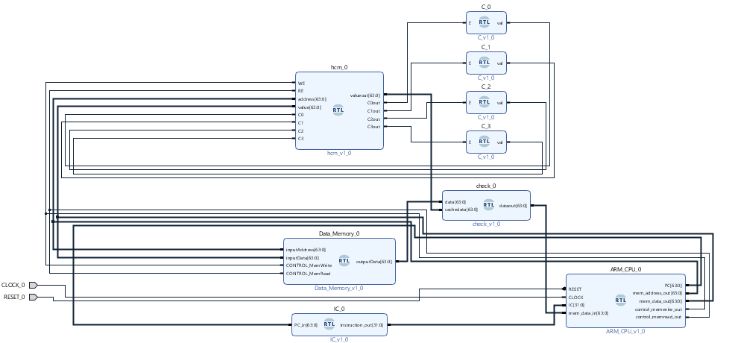
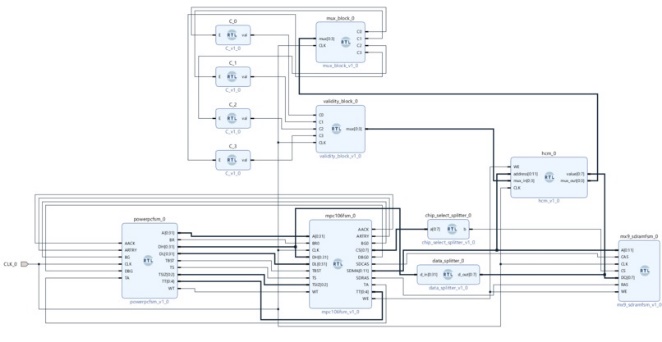
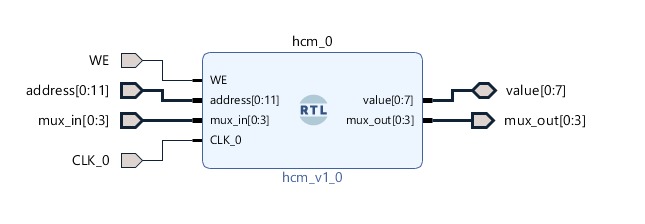
Information Technology Solutions

4 way set-associative cache memory module

Syncronication features

Capacitive times

Low-power demand



The module is working syncronised with the signals received from the processor. If a data is read/written in the cache, it appear also in memory (writeback memory).

In order to check if a block is valid or not, we use a set of capacitive timers. They charge and discharge depending on the use of a block. If the block is not used for a time, the condensatos discharges and the block is deleted. If a read/write operation occures, then the capacitor charges and the entry becomes/stays valid.

UFCache – new design of cache memory

Faster Memory

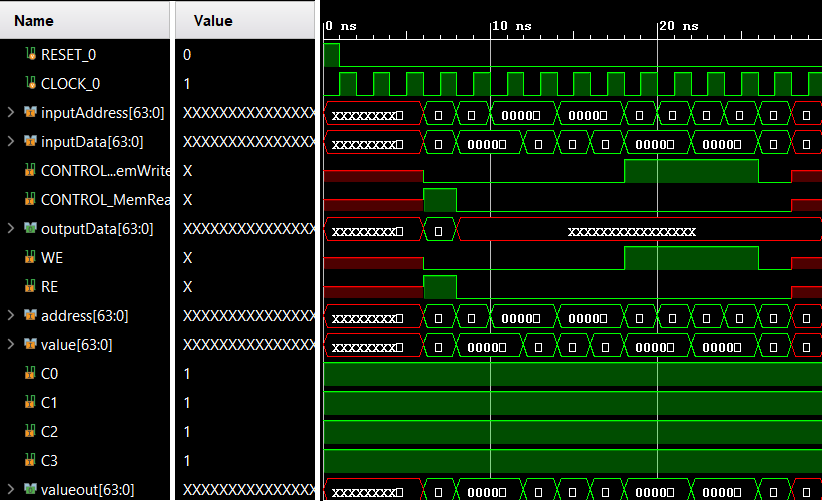
Enable the read/write operations with a set-associative cache module. Smaller association table in the cache implementation.

Lower Power Consumption

The module uses only power from operation read-write. Using transistors switch, it help to lower the sources needed for the circuit.

Store large amount of data

Efficient comparisons enable to enlarge the cache module.



As we can see, the data is transfered almost instantly between the cache module and the processor.

Bucharest, Romania

Phone +40771691920

technologies

Hackwired

Open-Source

The project is available on Github for further development at

<https://github.com/AlexandraChiritaACS/HotCache>

More information about the project can be found here

<https://devpost.com/software/hotcache>

Research

We would like to gather a team to work on this research project.

Collaboration

We have active online for support, proposals or collaboration of any sort.

RISC processor

RAM module

FPGA (optional)

Vivado 2018.3 (for customization)

Willingness to work for better good

Service Features and Benefits

System Requirements