Total No. of Printed Pages:4

T.E. (Computer) (Sem-V) (Revised Course 2016-2017)
EXAMINATION MAY/JUNE 2019
Automata Languages and Computation

[Duration : 3 Hours] **[Max. Marks : 100]**

Instructions
Please check whether you have got the right question paper.
1. Answer **any two** questions from **Part-A** (20 marks each)
2. Answer **any two** questions from **Part-B** (20 marks each)
3. Answer **any one** question from **Part-C** (20 marks each)
4. Make suitable assumptions if needed and state.

PART-A

Q.1 a) Prove that: $1.2.3 + 2.3.4 + ---- + n(n+1)(n+2) = 1/4\ (n+1)\ (n+2)(n+3)$ using mathematical induction. **06**

b) Illustrate the hierarchy of formal languages as defined by Chomsky. **05**

c) Construct DFA for the following languages: **06**
i) $L = \{W\ |n_a(W) mod\ 5 \neq n_b(W) mod\ 3\}$
ii) $L = \{W\ |n_a(W) = 2\ and\ n_b(w) >= 3\}$

d) Explain applications of finite automata **03**

Q.2 a) Obtain Regular Expression for the following languages:- **06**
i) $L = \{a^n b^m | n \geq 4\ and\ m \leq 3\}$
ii) $L = \{VUV \mid U, V \in \{a,b\}^*\ and\ |V| = 2\}$

b) Convert the following ΛNFA to DFA:- **06**

δ / states	Λ	a	b	c
→p	ϕ	{p}	{q}	{r}
q	{p}	{q}	{r}	ϕ
*r	{q}	{r}	ϕ	{p}

c) State pumping Lemma for Regular languages. Prove that the language: **05**
$L = \{O^n | n\ is\ perfect\ sqare\}$ is
Not regular

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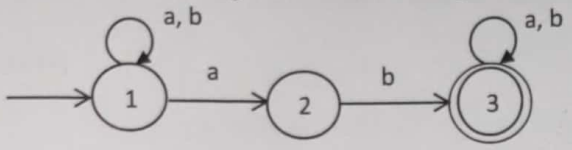
d) "The DFA or NFA for the language $L = \{a^n b^n | n \geq 0\}$ cannot be constructed". Is the statement true? Justify? **05**

Q.3 a) Convert the following NFA to DFA using subset construction technique. **06**



b) Prove that: "If L_1 and L_2 are Regular Language then $L_1 \cap L_2$ is also regular". **04**

c) Using mathematical induction prove that: for every $u, v \in \sum^+ (uv)^R = v^R u^R$ **06**

d) Design a DFA to accept strings of decimal numbers that are divisible by 3. **04**

PART-B

Q.4 a) Construct a CFG for the following Languages: **06**

i) $L = \{W \mid |w| \ mod \ 3 > 0 \text{ where } w \in \{a\}^*\}$

ii) $L = \{W \mid n_a(w) = n_b(w) + 1 \ and \ w \in \{a, b\}^*\}$

b) Design NPDA for the language:- **05**

$L = \{a^i b^j c^k | i, j, k \geq 0 \ and \ i = j + k\}$

Validate the string aaabbc

c) Convert the grammar 'G' into GNF whose productions are given below:- **05**

$S \rightarrow aSa \mid aSb \mid \Lambda$

$S \rightarrow aSb \mid aSbS \mid \Lambda$

d) Write a short note on ambiguity in CFG. Can it be removed? **04**

Q.5 a) Design a Turing machine that accepts all palindrome strings over $\sum = \{a, b\}^*$ **06**

b) Design a Turing Machine for the language **06**

$L = \{a^i b^j \mid i > j \ and \ i, j \geq 0\}$

c) Explain the technique of combining Turing machine with the help of an example. **06**

d) State Church – Turing thesis. **02**

Q.6 a) Design a Turing machine to compute the function $f(n) = n + y$ where n & y are positive integers. Assume Turing Machine to use unary notation **08**

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b) What is Linear Bounded Automata? **02**

c) Consider a grammar 'G' whose producilions are given as follows: **04**

$S \rightarrow S_1$

$S_1 \rightarrow S_1T \mid ab$

$T \rightarrow aT\ bb \mid ab$

Perform the following operations on the above grammar:-

1) Elimination of Left Recursion
2) Left Factoring

d) Construct a Bottom up PDA that accepts the following CFG: **06**

$$S \rightarrow XaY \mid YbX$$
$$X \rightarrow YY \mid aY \mid b$$
$$Y \rightarrow b \mid bb$$

PART-C

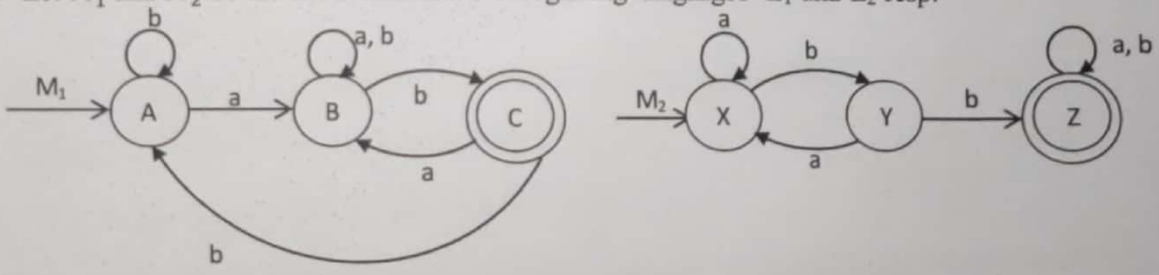
Q.7 a) Draw an Λ-NFA that recognizes the following regular expression over $\sum = \{0,1\}$ **04**
$(0+1)(01)^*(011)^*$

b) Construct a PDA that accepts the following language:- **06**
$L = \{X \mid n_a(x) = n_b(x)\ and\ X \in \{a,b\}^*\}$

c) Design a Turing machine to delete a symbol by changing the tape contents from $YaZ\ to\ YZ$ where **08**
$Y \in \{\Sigma U\{\Delta\}\}^*$, a$\in \{\Sigma U\{\Delta\}\}$ and $z \epsilon \Sigma^*$ Assume that $\Sigma = \{a,b\}$

d) What are null producilions? How are these eliminated? **02**

Q.8 a) Let M_1 and M_2 be the finite automata's recognizing languages L_1 and L_2 resp. **06**



Draw finite automata that accepts following languages:

i) $L_1 \cup L_2$

ii) $L_2 - L_2$

b) Design a Turing machine that performs multiplication of two integers represented in unary form. **08**

c) Prove that: **04**

$1(1!) + 2\,(2!) + \cdots + n(n!) = (n+1)! - 1$

d) What are useless symbols in a CFG? **02**

T.E. (Comp.) (Semester – V) (RC 2016-2017)
Examination, November/December 2018
AUTOMATA LANGUAGES AND COMPUTATION

Duration : 3 Hours Max. Marks : 100

Instructions : *1) Answer **any two** questions from Part – **A** (**20** marks **each**)*
*2) Answer **any two** questions from Part – **B** (**20** marks **each**)*
*3) Answer **any one** question from Part – **C** (**20** marks)*
4) Make suitable assumptions if needed and State.

PART – A

1. a) Prove that : "$\sqrt{2}$ is irrational" using any suitable mathematical proof technique of your choice. **6**

   b) Design a DFA for the language :

      i) $L = \{w / n_a(w) \bmod 5 \neq n_b(w) \bmod 3\}$

      ii) $L = \{a^n b^m | n \geq 4 \text{ and } m \leq 3\}$. **8**

   c) Write a short note on :

      i) Recursive v/s recursively enumerable languages.

      ii) Chomsky Hierarchy. **6**

2. a) Obtain regular expressions for the following languages :

      i) $L = \{a^n b^m | \ m \geq 1, n \geq 1, nm \geq 3\}$

      ii) $L = \{w | n_a(w) \bmod 3 = 0 \text{ where } w \in \{a, b\}^*\}$ **4**

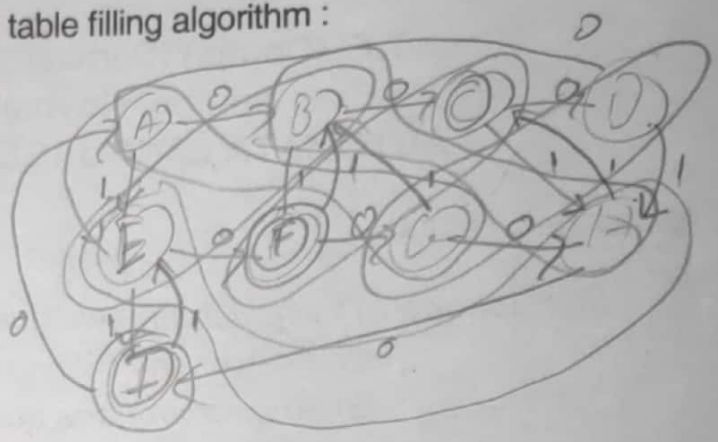
   b) Obtain Non deterministic finite automata for the following regular expression :

      $(a + b)^* aa (a + b)^*$. **6**

P.T.O.

c) Minimize the following DFA using table filling algorithm :

States \ δ	0	1
→ A	B	E
B	C	F
*C	D	H
D	E	H
E	F	I
*F	G	B
G	H	B
H	I	C
*I	A	E



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3. a) Design DFA for the language :
L = { W/|w| mod 3 = |w| mod 2 where w∈Σ* and Σ = {a}}. 6

b) Prove that : "if n ≥ 4 then $2^n \geq n^2$" using induction. 6

c) Construct a DFA from the given NFA : 6

States \ δ	0	1
→ q_0	$\{q_0, q_1\}$	$\{q_2\}$
q_1	$\{q_2\}$	$\{q_1\}$
*q_2	$\{q_1\}$	$\{q_2\}$

d) State pumping lemma for regular languages. 2

PART – B

4. a) Construct context free grammars for the following languages :
i) $L = \{0^m 1^m 2^n \mid m \geq 1 \text{ and } n \geq 0\}$
ii) $L = \{0^i 1^j \mid i \neq j, i \geq 0 \text{ and } j \geq 0\}$. 6

b) What is ambiguity in context free grammars ? Determine whether the following grammar is ambiguous.

$S \rightarrow a \mid Sa \mid bSS \mid SSb \mid SbS$. 6

c) Design a DPDA that accepts the language

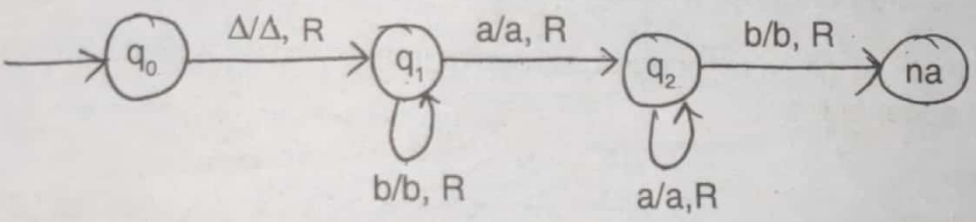
$L = \{a^n b^{2n} \mid n \geq 1\}$ validate the string aa bbbb. 8

5. a) Design a Turing machine that computes minimum of two unary numbers. 4

b) Design a Multitrack Turing Machine for

$L = \{a^n b^n c^n \mid n \geq 1\}$. 6

c) What is universal Turing machine ? Give encoding functions for UTM. Encode the following turing machine. 8



d) Explain non deterministic Turing machine. 2

6. a) Construct context free grammar for the language :

$L = \{a^{4n} \mid n \geq 1\}$ and convert it into CNF. 6

b) For the following Grammar :

$S \rightarrow aABB \mid aAA$

$A \rightarrow aBB \mid a$

$B \rightarrow bBB \mid A$

$C \rightarrow a$

Obtain push down automata. 6

c) Construct a turing machine that computes subtraction of two unary numbers. 8

PART – C

7. a) Design a deterministic finite automata for the following languages :

   i) $L = \{w(ab + ba) \mid w \in \{a, b\}^*\}$

   ii) $L = \{w | n_a(w) = 2 \text{ and } n_b(w) >= 3\}$. 6

   b) List closure properties of regular languages and prove that if L_1 and L_2 are regular languages then $L_1 - L_2$ is also regular. 8

   c) Construct NPDA to accept language $L = \{a^i b^j c^k \mid i, j, k > 0 \text{ and } i = j \text{ or } i = k\}$. 6

8. a) Design a Turing Machine for the language $L = \{SS \mid S \in \{a, b\}^*\}$. 8

   b) Construct a PDA corresponding to given context free grammar :

   $P \rightarrow PP \mid [P] \mid (p) \mid \wedge$

   Describe the behaviour of this PDA for the input string : ([ ]) [ ]. 6

   c) Prove that : "A given language L is regular if there exists a Finite automata M that accepts L". 6

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T.E. (Computer) (Sem-V) (Revised Course 2016-2017)
EXAMINATION MAY/JUNE 2019
VLSI Hardware Descriptive Language

[Duration : Three Hours] **[Max. Marks : 100]**

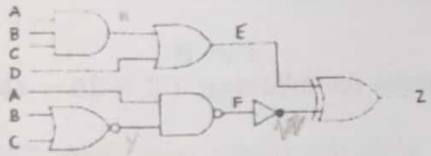
Instructions:
1. Answer **two** full questions from **Part A**. **two** full questions from **Part B** and **one** full question from **Part C**.
2. Make suitable assumptions wherever necessary.

Part A

Answer any two full questions from the following ($2 \times 20 = 40$ Marks)

Q.1 a) Explain the different data types in VHDL with examples. **06**

b) Write a VHDL description of the following combinational circuit using concurrent statements. Each gate has a 5-ns delay, excluding the inverter, which has a 2-ns delay. **06**



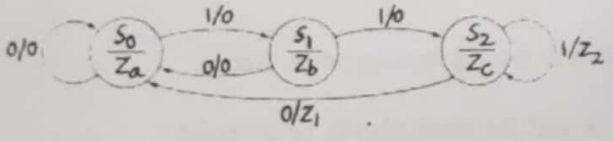
c) Find a minimum-row PLA table to implement the following sets of functions. **08**

$x(A,B,C,D) = \Sigma m(0,1,4,5,6,7,8,9,11,12,14,15)$
$y(A,B,C,D) = \Sigma m(0,1,4,5,8,10,11,12,14,15)$
$z(A,B,C,D) = \Sigma m(0,1,3,4,5,7,9,11,15)$

Q.2 a) Explain the working of BCD adder and write the VHDL description of the BCD adder. **08**

b) With a neat diagram explain the components of SM block. **07**

c) Convert the following state graph into a SM chart. **05**



Q.3 a) Draw the circuit represented by the following VHDL process. Use only two gates. **06**

```
process (clk, clr)
begin
 if clr = '1' then Q <= '0';
elsif clk' event and clk = '0' and CE = '1' then
 if C = '0' then Q <= A and B ;
 else Q <= A or B ; end if ;
end if ;
```

end process ;

Why is clr on the sensitivity list but C is not?

b) Implement the following state table using a ROM and two D flip-flops. Use a straight binary state assignment. **08**

(i) Show the block diagram and the ROM truth table. Truth table column headings should be in the order Q1 Q0 X D1 D0 Z.

(ii) Write VHDL code for the implementation. Use an array to represent the ROM table, and use two processes.

Present State	Next State X=0	Next State X=1	Output (Z) X=0	Output (Z) X=1
S_0	S_0	S_1	0	1
S_1	S_2	S_3	1	0
S_2	S_1	S_3	1	0
S_3	S_3	S_2	0	1

c) Derive SM chart for the binary multiplier. **06**

Part B

Answer any two full questions from the following: ($2 \times 20 = 40$ Marks)

Q.4 a) Show the implementation of the ring counter using simple FPGA building block. **07**

b) Explain the synthesis of case statement. **08**

c) Write a VHDL function which will return the largest integer in an array of N integers. The function call should be of the form LARGEST(ARR, N). **05**

Q.5 a) (i) Represent 25.625 in IEEE single precision floating-point format. **06**

(ii) Represent -15.6 in IEEE single precision floating-point format.

b) Multiply the following two floating-point numbers to give a properly normalized result. Assume 4-bit 2's complement format. F1=1.011, E1=1011, F2=0.110, E2=1101 **06**

c) Explain the syntax of VHDL procedure declaration. Write a VHDL procedure for adding bit vectors. **08**

Q.6 a) Two floating-point numbers are added to form a floating-point sum: **08**

$(F_1 \times 2^{E_1}) + (F_2 \times 2^{E_2}) = F \times 2^E$

Assume that F1 and F2 are normalized and the result should be normalized.

(i) List the steps required to carry out floating-point addition, including all special cases.

(ii) Illustrate these steps for F1=1.0101, E1=1001, F2=0.1010, E2=1000. Note that the fractions are 5 bits, including sign, and the exponents are 4 bits, including sign.

b) Explain the concept of scan path testing. **06**

c) Write short notes on: **06**

(i) signal attributes

(ii) array attributes

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Part C

Answer any One full questions from the following: (1 × 20 = 20 Marks)

Q.7

a) Write a VHDL process that is equivalent to the following concurrent statement: A<=B1 when C=1 else B2 when C=2 else B3 when C=3 else 0; **05**

b) Given F=A' B' + BC' and G=AC + B', write a complete VHDL module that realizes the functions F and G using an 8-word × 2-bit ROM. Include the array type declaration and the constant declaration that defines the contents of the ROM. **08**

c) Draw the SM chart for dice game. **07**

Q.8

a) Explain with diagrams the concept of carry chains and cascade chains in FPGA. **08**

b) Draw the SM Chart for floating point multiplication. **08**

c) The following VHDL code is part of a process. Assume that A=B= '0' before the code is executed. Give the values of the variable X1, X2, X3, and X4 immediately after the code is executed. **04**

```
wait until clock' event and clock= '1';
A <= not B;
A <= transport B after 5 ns;
wait for 5 ns;
X1 := A' event ;
X2 := A' delayed' event ;
X3 := A' last_event ;
X4 := A' delayed' last_event ;
```


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COMP 5 – 4 (16-17)

T.E. (Computer) (Semester – V) (RC 2016-17) Examination, Nov./Dec. 2018
VLSI HARDWARE DESCRIPTIVE LANGUAGE

Duration : 3 Hours Total Marks : 100

Instructions *: 1) Answer* ***two full*** *questions from Part –* ***A****,* ***two full*** *questions from Part –* ***B*** *and* ***one full*** *question from Part –* ***C****.*
2) Make suitable assumptions ***wherever*** *necessary.*

PART – A

Answer **any two full** questions from the following : **(2×20=40)**

1. a) With a neat diagram describe the steps in simulation of VHDL code. **6**

   b) Given the concurrent VHDL statements :

   B <= A and C after 3ns;

   C <= not B after 2ns;

   i) Draw the circuit the statements represent.

   ii) Draw a timing diagram if initially A = B = '0' and C = '1', and A changes to '1' at time 5 ns. **6**

   c) Find a minimum-row PLA to implement the following three functions :

   $f(A, B, C, D) = \sum m (3, 6, 7, 11, 15)$

   $g(A, B, C, D) = \sum m (1, 3, 4, 7, 9, 13)$

   $h(A, B, C, D) = \sum m (4, 6, 8, 10, 11, 12, 14, 15)$

   Use Karnaugh maps to find common terms. Give the logic equations with common terms underlined, the PLA table and also a PLA diagram. **8**

2. a) Explain the working of a 4 bit carry look ahead adder and write the VHDL description of the 4 bit carry look ahead adder. **8**

   b) Write the VHDL description of the multiplier controller. **6**

P.T.O.

c) Construct an SM chart equivalent to the following state table. Test only one variable in each decision box. Try to minimize the number of decision boxes. 6

Present State	Next State X_1X_2 = 00	01	10	11	Output (Z_1Z_2) X_1X_2 = 00	01	10	11
S_0	S_3	S_2	S_1	S_0	00	10	11	01
S_1	S_0	S_1	S_2	S_3	10	10	11	11
S_2	S_3	S_0	S_1	S_1	00	10	11	01
S_3	S_2	S_2	S_1	S_0	00	00	01	01

3. a) The following state table is implemented using a ROM and two D flip-flops (falling edge triggered) :

Q_1Q_2	$Q_1^+ Q_2^+$ X = 0	X = 1	Z X = 0	X = 1
00	01	10	0	1
01	10	00	1	1
10	00	01	1	0

i) Draw the block diagram.

ii) Write VHDL code that describes the system. Assume that the ROM has a delay of 10 ns and each flip-flop has a propagation delay of 15 ns. 8

b) Explain the working of the keypad scanner. 7

c) Explain the use of assert and report statements in VHDL. 5

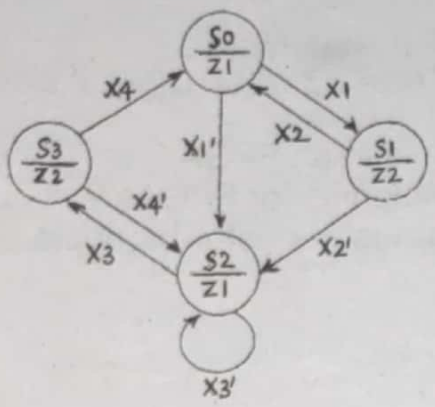
PART – B

Answer **any two full** questions from the following : **(2×20=40)**

4. a) Implement seven variable function using four input LUTs and 2 to 1 multiplexers. 8

b) Design a shift register using conditional compilation with generate statement. 6

c) For the given state graph :



i) Derive the simplified next-state and output equations by inspection. Use the following one-hot state assignment for flip-flops.

Q0 Q1 Q2 Q3 : S0, 1000 ; S1, 0100 ; S2, 0010 ; S3, 0001.

ii) How many Vertex slices are required to implement these equations ? 6

5. a) Convert the following decimal numbers in the IEEE single precision format.

i) 25.25.

ii) 2000.25 6

b) Explain the process of testing combinational logic. 6

c) Explain the major components of floating point multiplier with a neat diagram. 8

6 a) i) Add the floating-point numbers $0.111 \times 2^5 + 0.101 \times 2^3$ and normalize the result.

ii) Draw the SM chart for a floating-point adder that adds $(F_1 \times 2^{E1})$ and $(F_2 \times 2^{E2})$. Assume that the fractions are initially normalized (or zero) and the final result should be normalized (or zero). A zero fraction should have an exponent of –8. Set an exponent overflow flag (EV) if the final answer has an exponent overflow. Each number to be added consists of a 4-bit fraction and a 4-bit exponent, with negative numbers represented in 2's complement. Assume that all registers (F1, E1, F2 and E2) can be loaded in one clock time when a start signal (St) is received. If E1 > E2, the control signal GT = 1 and if E1 < E2, the control signal LT= 1. Define all other control signals used. 8

b) Explain the synthesis of if statement. 6

c) Explain the concept in scan testing. 6

PART – C

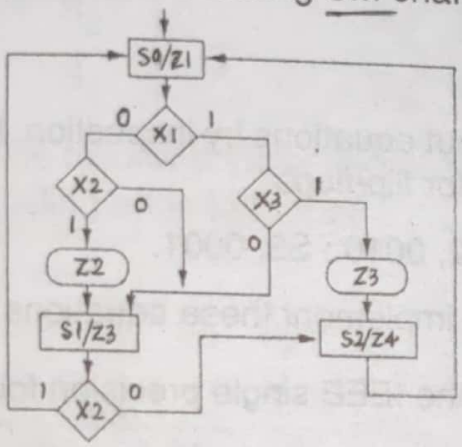
Answer **any one full** question from the following : **(1×20=20)**

7. a) Draw a circuit to implement the following VHDL statement :
A <= B1 when C1 = '1' else B2 when C2 = '1' else B3 when C3 = '1' else '0';
where all signals are of type bit. 5

b) i) What are the major programmable elements in an FPGA ?
ii) What are the different programming technologies for FPGAs ? 6

c) If gate delays are 5 ns, what is the delay of the fastest 4-bit ripple carry adder ? Explain your calculation. 4

d) Given the following SM chart,



Derive the next state and output equations, assuming the following state assignment :

$S_0 = 00$, $S_1 = 01$, $S_2 = 10$. 5

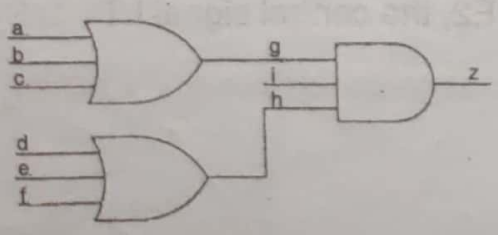
8. a) Generate optimized hardware for the following statement, assuming A is a 4-bit vector :

EQ3 <= (A = 3); 5

b) What is the biggest number that can be represented in the 8-bit 2's complement floating point format with 4 bits for exponent and 4 bits for fraction ? 4

c) Write an overloading function for the "<" operator for bit-vectors. Return a Boolean TRUE if A is less than B, otherwise return FALSE. Report an error if the bit-vectors are of different lengths. 6

d) Find a minimum set of tests that will test all single stuck-at-0 and stuck-at-1 faults in the following circuit. For each test, specify which faults are tested for s-a-0 and for s-a-1. 5



COMP 5 – 6 (16 – 17)

T.E. (Computer) (Semester – V) (RC 2016 – 17) Examination, November/December 2018
OPERATING SYSTEMS

Duration : 3 Hours | Total Marks : 100

Instruction : *Answer **any five full** questions selecting **any two** of **each** from Part – **A** and Part – **B** and **one** from Part – **C**.*

PART – A

Answer **any two** questions from the following :

1. a) What are Scheduling queues ? With the help of Queuing diagram explain the concept of scheduling processes. 6

   b) What are Threads ? List and explain different Multithreading models. 6

   c) Consider the following process table : 8

Process	Arrival Time (ms)	Burst Time (ms)	Priority
P1	6	1	1
P2	1	2	7
P3	2	3	3
P4	1	5	3
P5	4	5	2

   Draw the Gantt chart and find the average waiting time and average turnaround time when the processes are scheduled using :

   i) Pre-emptive Priority based scheduling algorithm.

   ii) Non-pre-emptive Priority based scheduling algorithm.

   Assume lower number means higher priority.

2. a) Explain various methods of Hardware support for mutual exclusion. 5

   b) List and explain different types of Semaphores. Give the implementation of the Readers- Writers problem using semaphores. 6

   c) What are its advantages of Monitors over Semaphores ? How is mutual exclusion achieved using Monitors ? 5

   d) List and explain the necessary conditions for a Deadlock to occur. 4

P.T.O.

3. a) Explain Deadlock detection algorithm with the help of suitable example. 6

b) What is Process ? With the help of a neat diagram, explain the five-state process model. List and describe the various state transitions. 6

c) Write short notes on (2x4=8)

i) Multilevel Feedback Queue Scheduling

ii) Real-Time Scheduling.

PART – B

Answer **any two** questions from the following :

4. a) With the help of neat diagram explain Hashed Page table structure. 5

b) Explain the Optimal page replacement algorithm with suitable example. 5

c) Discuss the basic file operations. 5

d) With the help of neat diagram explain Indexed allocation of disk space. 5

5. a) With the help of neat diagram explain steps for DMA transfer. 5

b) Write a shell program to generate Fibonacci series. 4

c) A disk drive has 250 cylinders numbered from 0 to 249. The drive is currently serving a request at cylinder 71 and the previous request was at cylinder 70. The queue of pending requests in FIFO order is 99, 52, 10, 72, 131, 107, 89, 66, 187, 85, 222, 244, 218. Starting from the current head position what is the total distance that the disk arm moves to satisfy all pending requests for each of the following algorithms ? Draw the arm movement chart. 8

i) SSTF ii) LOOK

iii) SCAN iv) C-SCAN

d) Explain the following shell commands 3

i) head ii) bc iii) echo

6. a) Discuss any two services related to Kernel I/O subsystem. 6

b) What is Thrashing ? What are the causes of Thrashing ? 5

c) Explain Acyclic-graph directory structure with relevant diagram. 5

d) Write shell program to generate squares of first 25 numbers. 4

PART – C

Answer **any one** questions from the following :

7. a) Write short note on Fair Share scheduling. **5**

   b) Give the implementation of Dining Philosopher problem using Monitors. **6**

   c) Explain Bankers Algorithm with the help of an example. **6**

   d) What are the functions of Dispatcher in context to CPU Scheduling ? **3**

8. a) With the help of neat diagram explain Inverted Page table structure. **5**

   b) Explain Interrupt-driven I/O cycle with necessary steps. **5**

   c) Consider the following page reference strings. **8**

   1, 2, 3, 4, 2, 4, 1, 5, 2, 6, 4, 1, 7, 6, 3, 2, 2, 7, 2, 3, 1, 7, 3

   How many page faults will occur for the following page replacement algorithms assuming a set of 4 page frames ?

   i) Optimal page replacement

   ii) FIFO page replacement.

   d) Explain the use of chmod command in Linux. **2**

COMP 5 – 1 (16-17)

T.E. (Computers) (Semester – V) (RC) (2016 – 17) Examination, Nov./Dec. 2018

DATA COMMUNICATION

Duration : 3 Hours | Total Marks : 100

Instructions : 1) *Attempt* ***two*** *questions from Part –* ***A*** *and Part –* ***B*** *and* ***one*** *question from Part –* ***C****.*

2) *Assume any suitable data* ***if*** *necessary.*

PART – A

1. a) Describe the components of an optical fiber cable. 5

b) Explain the various layers in the TCP/IP Protocol stack. 6

c) With reference to efficiency and delay compare circuit switched networks with datagram networks. 5

d) What is the difference between half-duplex and full-duplex transmission modes ? 4

2. a) Distinguish between multilevel TDM, multiple slot TDM and pulse-stuffed TDM. 5

b) Explain the effect of noise on twisted pair lines. 5

c) Encode the following sequence using NRZ-L, AMI, Differential Manchester and HDB3

1110110000111111010110 8

d) What is the difference between bit rate and baud rate ? 2

3. a) List the steps that take an analog signal to a PCM digital code. 7

b) List the disadvantages of Optical Fiber. 4

c) Differentiate between serial and parallel transmission. 4

d) What is spread spectrum ? Explain frequency hopping spread spectrum. 5

P.T.O.

PART – B

4. a) Compare and contrast Go Back N ARQ protocol with selective repeat ARQ. 6

   b) Explain HDLC frames with format. 6

   c) Explain concept of CRC encoder and decoder with example. 8

5. a) Explain connecting devices that operate at all five layers with neat diagram. 4

   b) Explain two dimensional parity check with example. 8

   c) How does VLAN provide extra security for a network ? 4

   d) Compare X.25 versus frame relay network. 4

6. a) Compare and contrast byte oriented and bit oriented protocols. 6

   b) Write note on transparent bridge. 6

   c) Explain FDMA and TDMA with diagram. 8

PART – C

7. a) Explain datawords and codewords in block coding with diagram 4

   b) Explain any three methods for converting digital data to analog signals. 8

   c) Explain how cellular telephony is used to provide stable communication between mobile devices. 8

8. a) Explain the concept of CSMA/CA. 4

   b) Explain the Stop and Wait protocol with neat diagram. 6

   c) List and explain the functions of the data link layer. 5

   d) Differentiate between TCP/IP and OSI model. 5

COMP 5 – 5 (16-17)

T.E. (Computer Engineering) (Semester – V) (RC 2016-17)
Examination, November/December 2018
DATABASE MANAGEMENT SYSTEM

Duration : 3 Hours Max. Marks : 100

Instructions : 1) *Attempt **five** questions, **any two** questions **each** from Part – **A** and Part – **B** and **one** question from Part – **C**.*
2) *Assume necessary data, **wherever** required.*

PART – A

Answer **any two** questions from the following : **(2×20=40)**

1. a) Consider the relations : **10**
PROJECT(projno, proj_name, chief_architect)
EMPLOYEE(empno, emp_name)
ASSIGNED(projno, empno)

Use relational algebra to express the following queries :
i) Get details of employees working on project CE100.
ii) Get the employee number of employees who work on all projects.
iii) Get details of project on which employee with name 'RAM' is working.
iv) Find the employee numbers of the employees who do not work on project CE200.
v) Get employee details who are working on both CE300 and CE400 projects.

b) Explain the following : **4**
a) DBMS Languages
b) Data independence.

c) Differentiate between : **6**
i) WHERE and HAVING clause
ii) Correlated query and nested query
iii) TRUNCATE and DELETE.

2. a) What is union compatibility ? Why do the UNION, INTERSECTION and DIFFERENCE operations require that the relations on which they are applied be union compatible ? **3**

b) Explain and illustrate with an example the three schema database architecture. **7**

P.T.O.

c) Consider student (std_id, std_name, date_of_birth, phone, dept_name). Write the SQL expression for the following : 10

i) Put the data for a student with student id200, name arun, birth date 1st February, 1985, phone number (01110 32818) and dept. name English in the student table.

ii) A constraint named less_than_20 was defined on the field date_of_birth of table student. Delete this constraint.

iii) List names of students in the departments other than maths and computer.

iv) Create a view stud_view containing dept_name and number of students in each department.

v) Delete the record for the students whose name begin with alphabet 'R' or whose names have second alphabet 'A' in their names.

3. a) Define DBMS. Explain the functions of DBMS. 6

b) With the help of an appropriate example explain Triggers, Views and Assertion. 6

c) Consider the two tables T1 (P,Q,R) and T2 (A,B,C) shown below : 5

Table T1

P	Q	R
a	1	–
c	2	10
t	2	–
a	–	–

Table T2

A	B	C
a	1	–
d	3	10
r	3	10
a	–	–

Show the results for the following operations :

i) $\sigma_{(P = a)}(T\ 1)$

ii) $\Pi_{(P, R)}(T1)$

iii) $T1 \cup T2$

iv) $T1 \cap T2$

v) $T1 - T2$

d) Let the following relation schemas be given : 3

$R = (A, B, C)$

$S = (D, E, F)$

Let the relations r(R) and s(S) be given. Give an expression in SQL that is equivalent to each of the following queries.

a) $\Pi_A(r)$

b) $\sigma_{(B = 17)}(r)$

c) $\Pi_{A, F}(\sigma_{(C = D)}(r \times s))$

PART – B

Answer **any two** questions from the following : **(2×20=40)**

4. a) Check if the following schedule are conflict serializable and/or view serializable. Show all your work. Explain the reasons of your answers clearly. **8**

   S1 : w2(x); w1(x); w3(x); r3(x); r1(y); w2(y); r2(y); r3(z)

   S2 : w2(x); r3(x); r5(z); w4(y); r2(y); w1(x); w4(z); r2(z); r1(x); w3(y); w3(z)

   b) In an organization several projects are undertaken. Each projects can employ one or more employees. Each employee can work on one or more projects. Each project is undertaken on the request of client. A client can request for several projects. Each project has only one client. A project can use a number of items and a item may be used by several projects. Draw an E-R diagram and convert it to a relational schema. **6**

   c) Explain the types of anomalies found in RDBMS. Justify with examples. **6**

5. a) Describe the various mapping constraints in ER diagram by giving suitable example. **8**

   b) Explain multiversion two phase locking using certified locks. **5**

   c) Let R = (A, B, C, D) a relation and F = {AB –> C, C –> D, D –> A} a set of dependencies for this relation. **7**

      1) Find the candidate keys in R.
      2) Find the possible violations of R when {A, B} is defined as primary key.
      3) If R is not in BCNF, give a decomposition of R in relations that will be in BCNF.

6. a) Explain the concept of generalization and aggregation in ER diagrams. Give one example for each one of them. **6**

   b) A relation R (A, C, D, E, H) satisfies the following FDs : **4**

      F = {A –> C, AC –> D, E –> AD, E –> H}

      Find the canonical cover for this set of FDs.

   c) What are result equivalent schedules ? Explain with example. **4**

   d) Explain the ACID properties in transaction with an example. **6**

PART – C

Answer **any one** question from the following : **(1×20=20)**

7. a) Composite and multivalued attributes can be nested to any number of levels. Suppose we want to design an attribute for a STUDENT entity type to keep track of previous college education. Such an attribute will have one entry for each college previously attended and each such entry will be composed of college name, start and end dates, degree entries (degrees awarded at that college, if any) and transcript entries (courses completed at that college, if any). Each degree entry contains the degree name and the month and year the degree was awarded and each transcript entry contains a course name, semester, year and grade. Design an attribute to hold this information. Use the ER conventions. **5**

b) Explain the division operator in relational algebra by giving an example. **4**

c) Explain the following : **6**

i) Serial schedule

ii) Wait-for graph for deadlock detection

iii) Cascading rollback

d) Explain the role of aggregate functions in SQL queries. **5**

8. a) Consider the given schedule S_1 with transactions T_1 and T_2; if the value of X at the beginning of the transactions is 100, what will be the value of X at the end of the transactions ? Also, find the problem with the given schedule. **4**

Transaction T1	Transaction T2
READ X	
X : = X – 20	
	READ X
	X : = X – 30
WRITE X	
	WRITE X

b) All candidate keys are superkeys, whereas all superkeys are not candidate keys. Justify this statement with a suitable example. **4**

c) Consider two sets of functional dependencies

F1 = {A –> C, AC –> D, E –> AD, E –> H) and F2 = {A –> CD, E –> AH}. Are they equivalent ? **5**

d) Define data model. Explain different types of data models. **7**

T.E. (Computer) (Semester – V) (RC-2016-17) Examination, Nov./Dec. 2018

CRYPTOGRAPHY AND CODING THEORY

Duration : 3 Hours | Total Marks : 100

Instructions : *1) Answer **any two** questions from Part – **A**.*
*2) Answer **any two** questions from Part – **B***
*3) Answer **any one** question from Part – **C**.*
*4) **Assume** suitable data **whenever** necessary.*

PART – A

1. a) What is Vigenere Cipher. Encrypt the word "sheislistening" using the key "PASCAL" using vigenere cipher. Also show the Decryption process. **4**

   b) For the given congruence $49x \equiv 5000 \pmod{999}$. **5**

   Determine the following :

   i) Total number of existing solutions

   ii) The value of x.

   c) Determine the value of x for the simultaneous congruence equations by applying the Chinese remainder theorem. **5**

   $x \equiv 5 \pmod 6$

   $2x \equiv -3 \pmod{11}$

   $x \equiv 3 \pmod{17}$.

   d) Apply Modular Exponentiation on the following **6**

   $(54^{27} + 8)^{120} \bmod 67$.

2. a) Alice wants to encrypt a message "hello" to be send to Bob using the affine function by choosing the value of $\alpha = 7$ and $\beta = 2$. Explain how Bob retrieves the message. **6**

   b) Give the structure of Rijndael Algorithm (AES).

   Explain how Encryption/Decryption is performed using this algorithm. **8**

   c) Apply Linear Congruential Generator on the following set of data a = 4 b = 5 n = 17 and the $x_0 = 7$ (Seed value). **4**

   d) Evaluate $2^{53} \bmod 11$ using Fermat theorem. **2**

P.T.O.

3. a) With the help of a block diagram, explain the simplified DES algorithm. Also trace the algorithm with the following boxes on the 8-bit plain text 10111101 and the 10 bit key 1010000010. 8

P10									
3	5	2	7	4	10	1	9	8	6

P8							
6	3	7	4	8	5	10	9

IP							
2	6	3	1	4	8	5	7

IP – 1							
4	1	3	5	7	2	8	6

E/P							
4	1	2	3	2	3	4	1

P4			
2	4	3	1

b) Explain the algorithm used to determine the primitive roots of a number. Using the same determine the primitive roots of 13. 6

c) Calculate GCD (1547,560) using Euclids algorithm. Also determine the values of x and y which will satisfy the linear Diophantine equation. 6

PART – B

4. a) Perform Solovay strassen primality testing for the following number $n = 341$ and $a = 2$. 6

b) Rama wants to send a message ($M = 5$) to Sudarshan with the value of $n = 77$ and he chooses the public component $e = 13$. 5

Apply the Rivest, Shamir and Adleman Encryption Algorithm and also show, how Sudarshan retrieves the original message from Rama with the given algorithm.

c) Users A and B use the Diffie-Hellman key exchange a common prime $q = 11$ and a primitive root $\alpha = 7$. 5

i) If user A has private key $X_A = 3$. What is A's public key Y_A ?

ii) If user B has private key $X_B = 6$. What is B's public key Y_B ?

iii) What is the shared secret key ?

d) Using Fermat factorization method, find factors for $n = 5959$. 4

5. a) An adversary intercepts two encrypted messages C1 = 3 and C2 = 10 encrypted using E1Gamal public key {11, 2, 8}. The adversary comes to know that the random integer k = 8 is chosen. How does he determine the plaintext ? 5

b) What are the different operations and constants used in the SHA1 algorithm ? 5

c) Use Quadratic sieve factoring method to find factors for n = 1649. 4

d) What are error correcting codes ? Explain q-ary code and Hamming Code. Determine the set of codeword's on the given alphabet A = {0, 1} for set defined over A^3. 6

6. a) For a (6, 3) cyclic code, generating polynomial is $g(x) = [1 + x + x^3]$. Find all the code vectors and determine the minimum Hamming distance. How many errors can be corrected/detected by the above coding scheme ? 8

b) Using Pollard (p-1) factoring method find the factors of n = 391 where the Bound value B = 8. 5

c) Using Miller-Rabin Primality test, check if 349 is prime or composite, where a = 2. 4

d) Explain how hashing and signing is done on a long message. 3

PART – C

7. a) What is Cryptanalysis ? Explain Cryptanalysis of Caesar cipher. 4

b) With the help of diagrams, explain the Data Encryption Algorithm on 64 bit plaintext to generate the 64 bit Ciphertext. 7

c) Elaborate on Timing Attack on RSA. 2

d) Find the solution of $3^x \equiv 17 \bmod 101$ for the discrete log problem using Pohling Helman method. 7

8. a) State Eulers Theorem. Use Eulers Theorem to determine the last 3 digits of 7^{803}. 4

b) Explain CBC and OFB modes of operation of block ciphers. 5

c) A linear (6, 3) block code has the generator matrix : 6

$$G = \begin{bmatrix} 1 & 0 & 0 & 1 & 1 & 0 \\ 0 & 1 & 0 & 0 & 1 & 1 \\ 0 & 0 & 1 & 1 & 1 & 1 \end{bmatrix}$$

Find the code for the following message vectors.

i) [1 0 1] ii) [1 1 1]

How many errors can this scheme correct ? Introduce single bit error in the first bit from left and find the error syndrome.

d) What is ISBN code ? Explain the process of assigning ISBN codes. 5