Features

- Meets wetting (sealing) current requirements per ITU-T G.991.2
- Integrated bridge rectifier for polarity correction
- Uses inexpensive opto-coupler for dc signalling
- Electronic inductor, breakover, and latch circuits
- Current limiting and excess power protection circuits
- ANSI SHDSL and ISDN compatible
- MLT and SARTS compatible
- Compatible with portable test sets
- Excellent linearity
- Compatible with GlobespanVirata and Conexant SHDSL transceiver chip set families
- Small 16-pin SOIC package
- Pin compatible with Agere LH1465AAE

Applications

- Router and bridge customer premises equipment
- Leased line equipment
- T1/E1 network line cards and repeaters
- Network Termination 1 (NT1) equipment
- Mechanized Loop Test (MLT) networks
- Switched Access Remote Test System (SARTS) networks

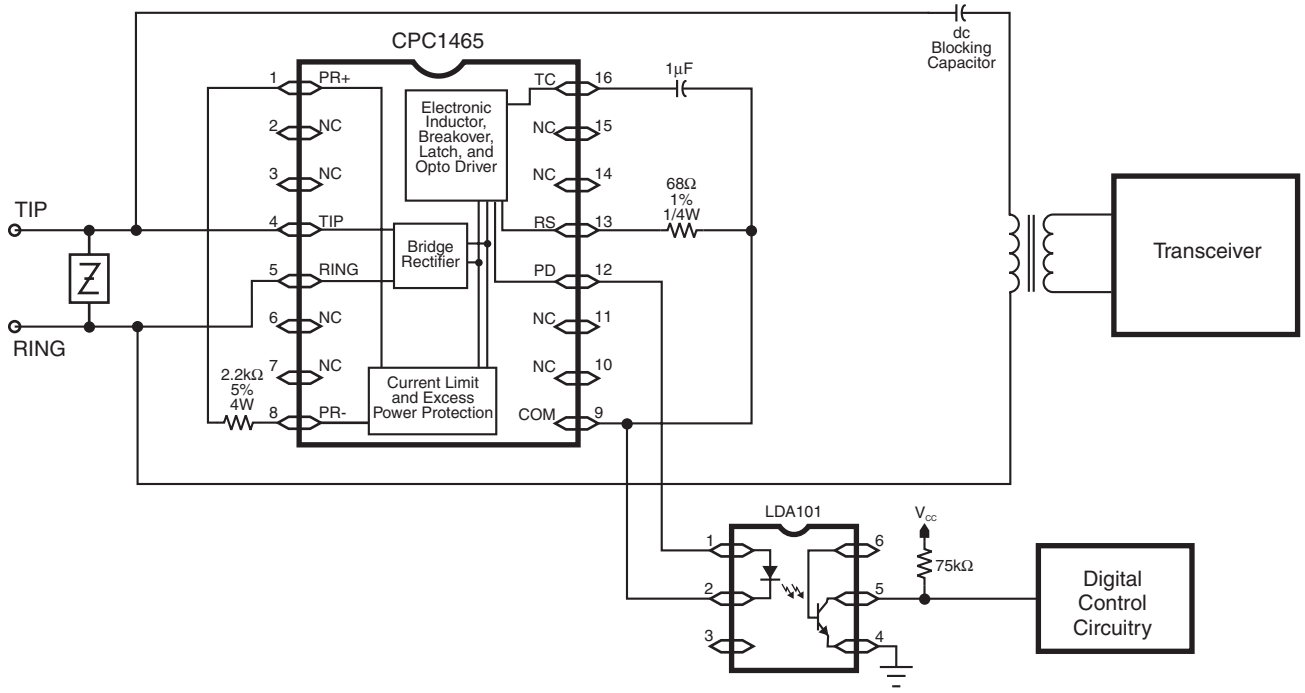
Description

The CPC1465 is a dc termination IC used in Single-pair High-speed Digital Subscriber Line (SHDSL) and Integrated Services Digital Network subscriber line (ISDN) equipment. It provides a polarity insensitive dc termination for DSL loop sealing current and a recognizable device signature for MLT systems. The CPC1465 passes the low frequency ISDN signalling information to the NT1 via Clare's inexpensive LDA101 optocoupler.

Ordering Information

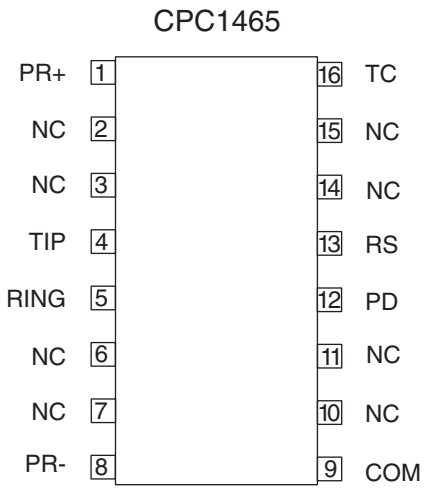
Part Number	Description
CPC1465D	DC Termination IC, 16-pin SOIC, in tubes
CPC1465DTR	DC Termination IC, 16-pin SOIC, in tape and reel

Figure 1. CPC1465 Typical 2-Wire dc Termination Application



1. Specifications

1.1 Package Pinout



1.2 Pinout

Pin	Name	Description
1	PR+	Protection resistor positive side
2	NC	No connection
3	NC	No connection
4	TIP	Tip lead
5	RING	Ring lead
6	NC	No connection
7	NC	No connection
8	PR-	Protection resistor negative side
9	COM	Common
10	NC	No connection
11	NC	No connection
12	PD	Photo-diode (LED input current)
13	RS	Current limiting resistor
14	NC	No connection
15	NC	No connection
16	TC	Timing capacitor

1.3 Absolute Maximum Ratings at 25°C

Parameter	Minimum	Maximum	Unit
Operating temperature	-40	+85	°C
Storage temperature	-40	+125	°C
Operating relative humidity	5	95	%
Pin soldering temperature (15 seconds max)	-	+220	°C
Power dissipation	-	1	W
Maximum Voltage (T to R, R to T)*	-	300	V

**Clare recommends the use of room-temperature-vulcanizing silicone RTV sealant on the tip and ring pins (pins 4 and 5) to guard against the possibility of arcing.*

Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

1.4 Electrical Characteristics at T_A = 25°C

Unless otherwise specified, minimum and maximum values are production testing requirements. Typical values are characteristic of the device and are the result of engineering evaluations. In addition typical values are provided for information purposes only and are not part of testing requirements.

1.4.1 DC Characteristics, Normal Operation, (see Figure 2 on page 5) and (see Figure 3 on page 5)

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Unit
Activate/Non-activate Voltage	Off State	V_{AN}	30.0	35.0	39.0	V
Breakover current	-	I_{BO}	-	0.5	1	mA
DC Voltage drop	Active State, 1 mA ≤ I_{SL} ≤ 20 mA	V_{ON}	-	12.5	15	V
DC leakage current	V_{OFF} = 20 V	I_{LKG}	-	1.5	5	µA
Hold/Release current	Active State	$I_{H/R}$	0.1	0.5	1.0	mA
Minimum on current	V_{ON} < 54 V	I_{MIN1}	20	38	-	mA
Minimum on current	54 V ≤ V_{ON} ≤ 100 V for 2 seconds, source resistance 200 Ω to 4 kΩ	I_{MIN2}	9.0	45	-	mA
Minimum on current	V_{ON} > 100 V	I_{MIN3}	0	0.1	-	mA
Maximum on current	V_{ON} ≤ 70 V	I_{MAX1}	-	38.4	70	mA
Maximum on current	V_{ON} > 70 V	I_{MAX2}	-	-	$\frac{V_{ON}}{1k\Omega}$	mA
Photodiode drive current	Active State	I_{PD}	0.2	0.3	10	mA

1.4.2 AC Characteristics, Normal Operation, (see Figure 4 on page 6) and (see Figure 5 on page 6)

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Unit
ac impedance	200 Hz to 50 kHz	Z_{MT}	10	38	-	kΩ
Linearity distortion	f = 200 Hz to 40 kHz, I_{SL} = 1 mA to 20 mA, V_{APP} ≤ 10.5 V_{PP}	D1	75	78	-	dB
Linearity distortion	f = 200 Hz to 40 kHz, I_{SL} = 1 mA to 20 mA, V_{APP} ≤ 12 V_{PP}	D2	50	70	-	dB

1.4.3 Transition Characteristics, Normal Operation, (see Figure 6 on page 7)

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Unit
Activate time	(see Figure 7 on page 7)	t1	3.0	13	50	ms
Deactivate time	(see Figure 8 on page 7)	t2	3.0	-	100	ms

Figure 2. I-V Requirements Template, 0 V to 50 V

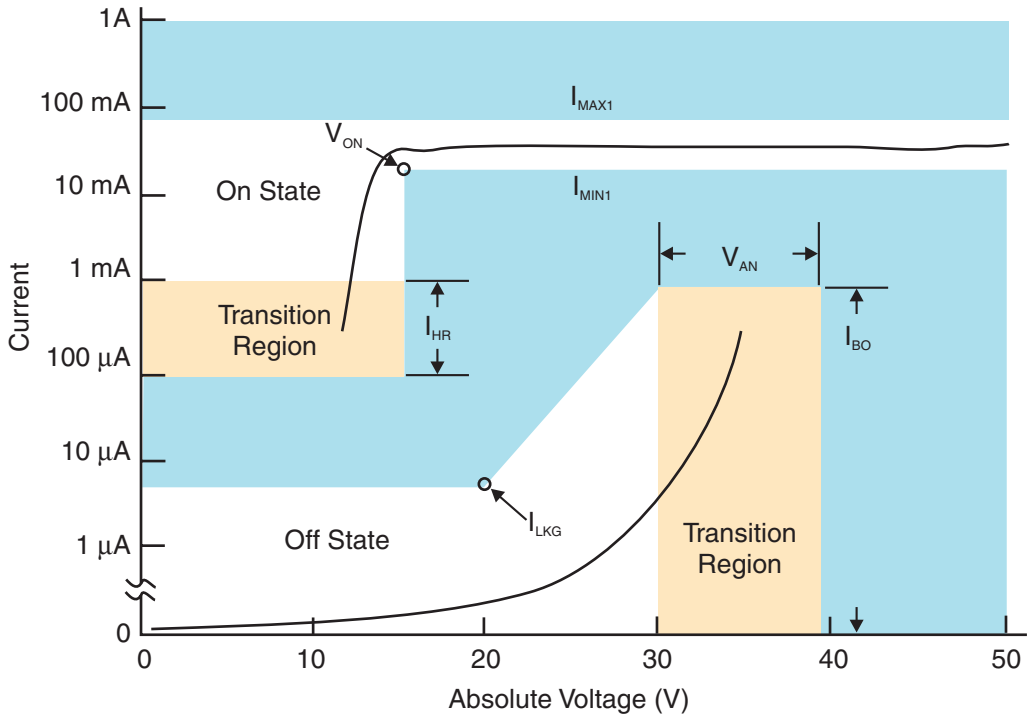


Figure 3. I-V Requirements Template, 0 V to 250 V

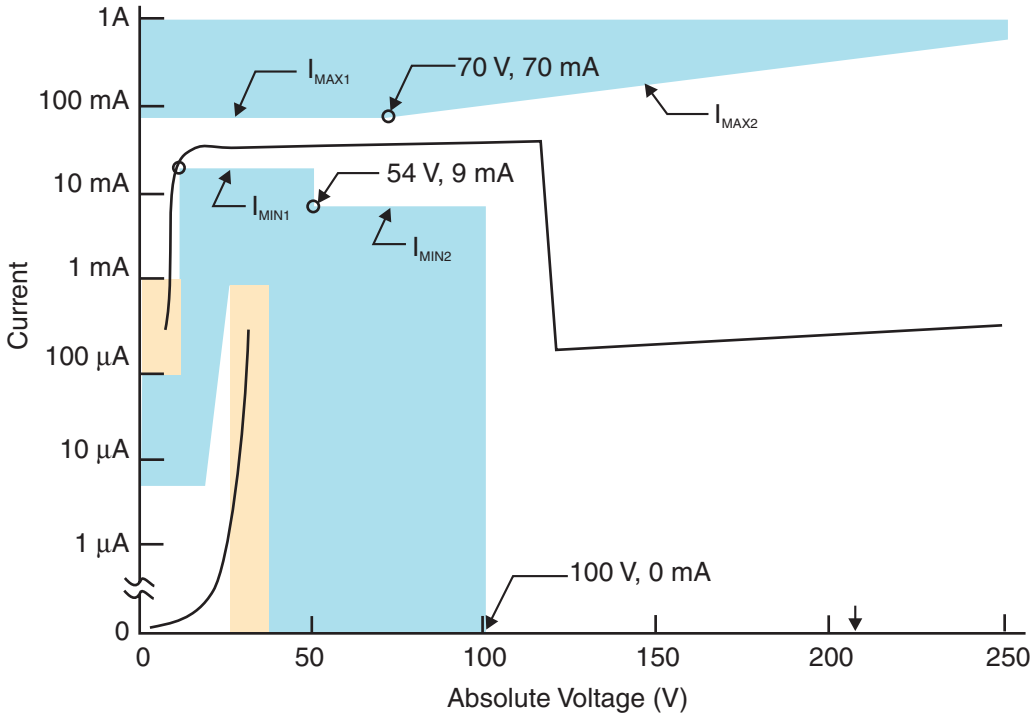
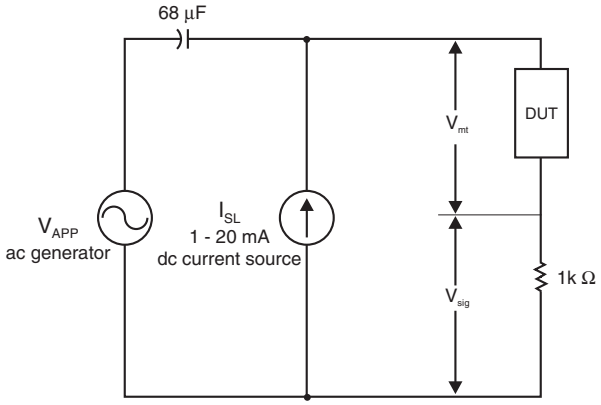


Figure 4. Test Circuit for ac Impedance and Linearity



$$Z_{mt} = \frac{1000 \times V_{mt}}{V_{sig}}$$

$$\text{Linearity} = 20\log\left[\frac{V_{mt}}{V_{sig2ndHarmonic}}\right] + 20\log\left[\frac{1000}{67.5}\right]$$

Figure 5. Linearity Requirement Template

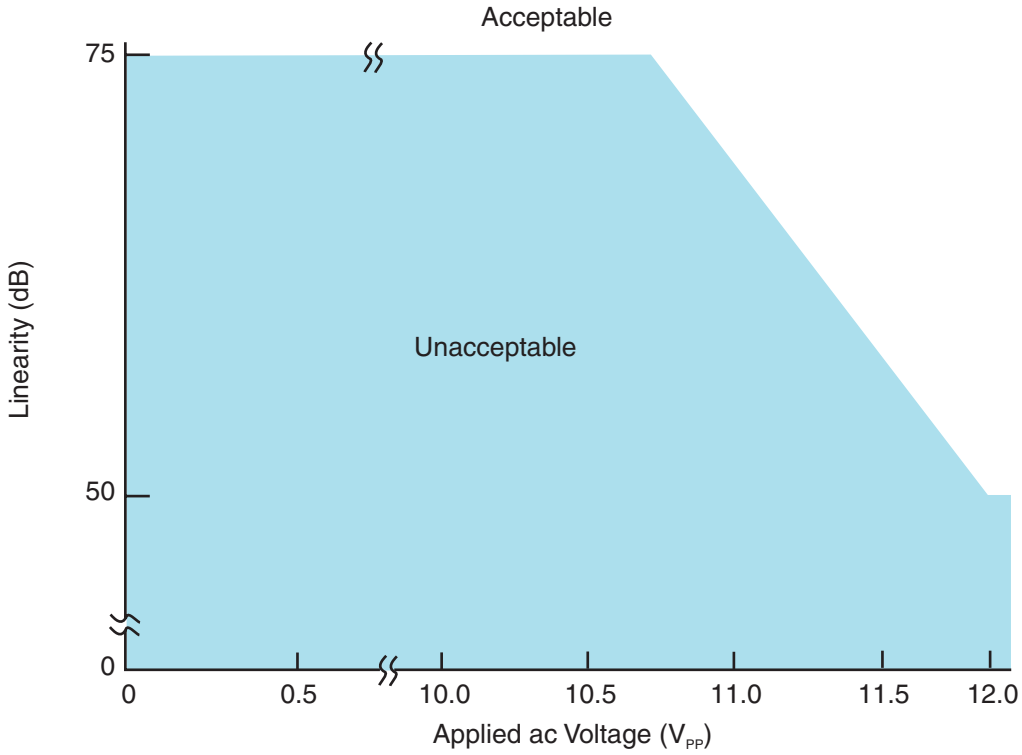


Figure 6. Test Circuit for Activate and Deactivate Times

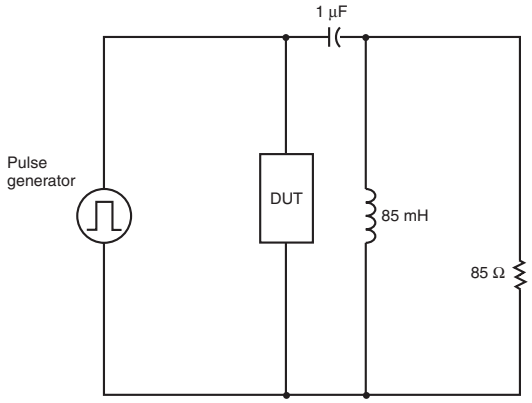


Figure 7. Applied Waveform for Activation Test

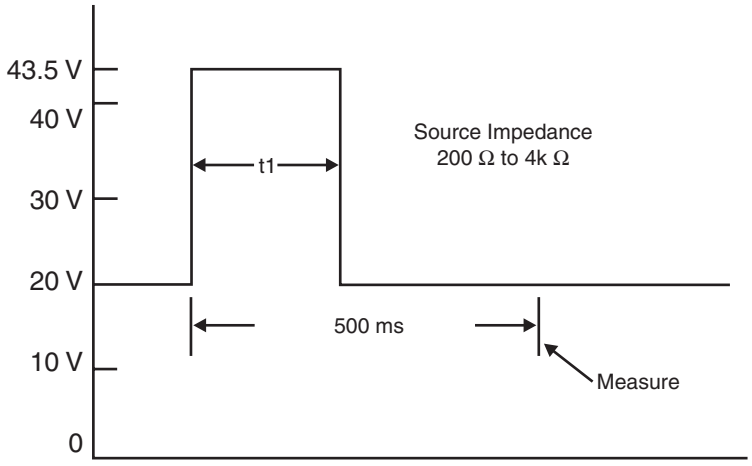
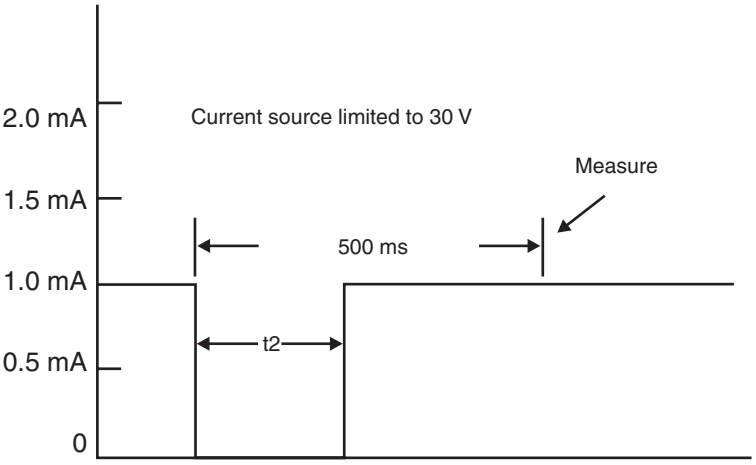


Figure 8. Applied Waveform for Deactivation Test



1.5 Application Signalling Characteristics

These tests assume crowbar protection across the CPC1465 limiting peak potentials to 250 V.

1.5.1 LED Trigger Characteristics During MLT Signalling, (see Figure 9 on page 9)

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Unit
Applied ac Voltage	-	-	60	-	62	V_{PEAK}
Applied ac frequency	-	-	2	-	3	Hz
Number of half-cycles applied	-	1	6	-	10	-
Total loop resistance	-	-	900	-	4500	Ω
Required opto-coupler response						
Number of pulses per half-cycle applied	-	-	-	1	-	-
Pulse width (opto on)	(see Figure 9 on page 9)	T_{ON}	10	-	-	ms
Pulse width (opto off)		T_{OFF}	10	-	-	ms

1.5.2 LED Trigger Characteristics During Dial Test Set Signalling, (see Figure 9 on page 9)

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Unit
Applied dc battery Voltage	-	-	-43.5	-	-56	V_{DC}
Frequency (pulses per second)	-	-	4	-	8	-
Percent break	-	-	40	-	60	%
Number of pulses	-	-	6	-	10	-
Total Loop Resistance	-	-	200	-	4000	Ω
Required opto-coupler response						
Number of pulses per make/break applied	-	-	-	1	-	-
Pulse width (opto on)	(see Figure 9 on page 9)	T_{ON}	10	-	-	ms
Pulse width (opto off)	(see Figure 9 on page 9)	T_{OFF}	10	-	-	ms

Figure 9. Test Circuit for LED Operation

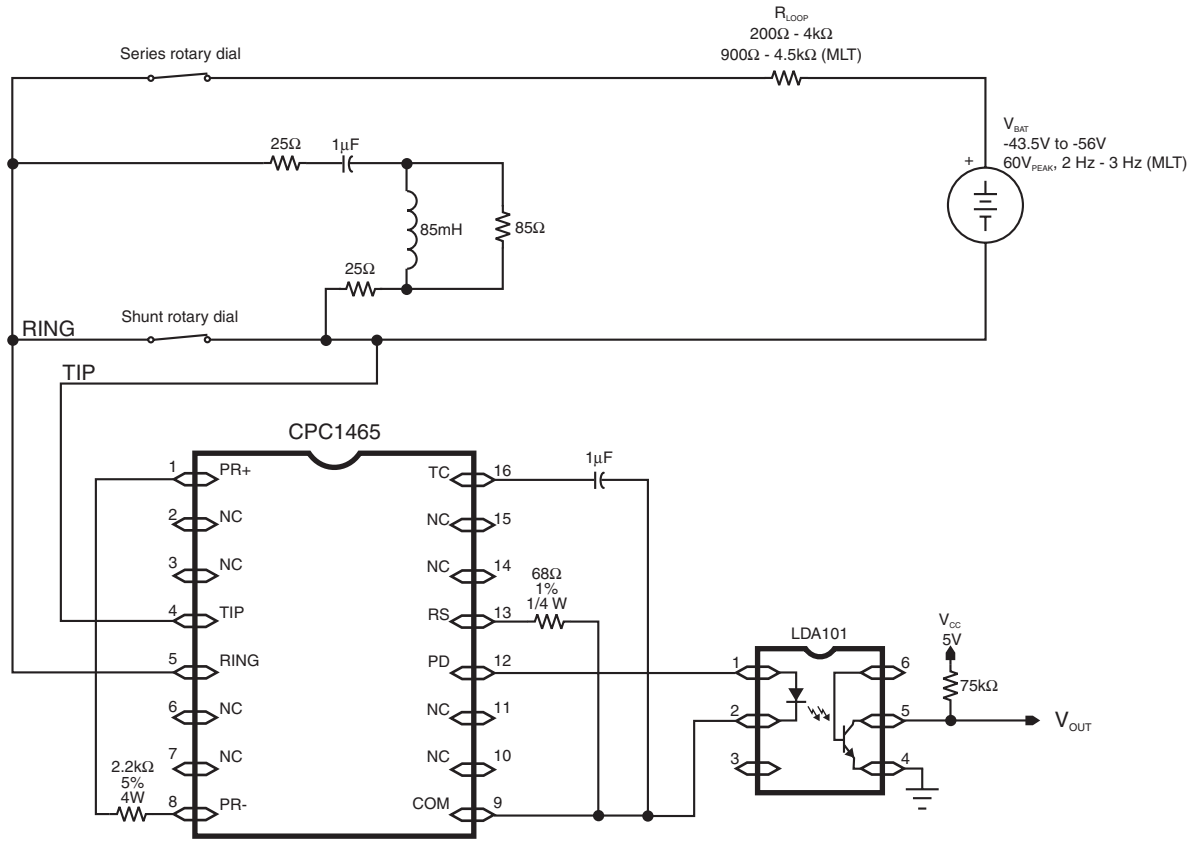
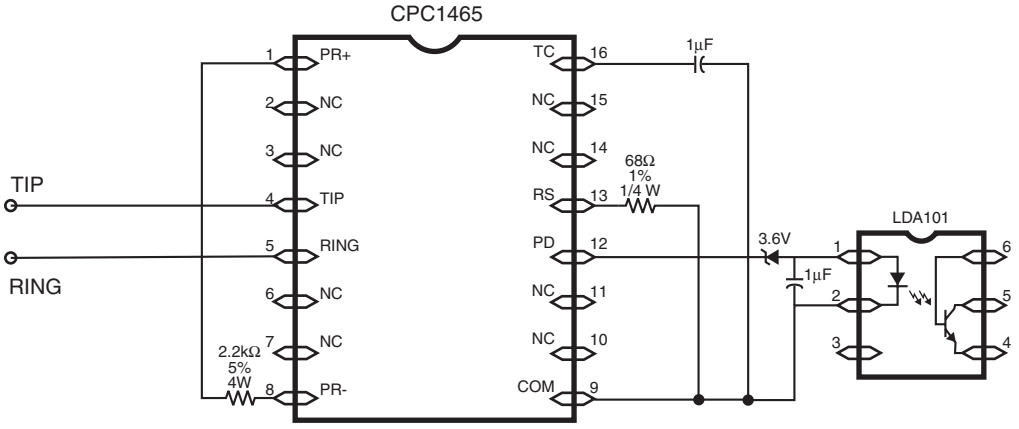


Figure 10. Typical ISDN NT1 Application Diagram



2. Functional Description

2.1 Introduction

The CPC1465 can be used for a number of designs that require a dc hold circuit such as SHDSL applications and ISDN NT1 applications. Typical SHDSL applications will use a circuit design similar to the one shown in Figure 1, “CPC1465 Typical 2-Wire dc Termination Application” on page 1 while the typical ISDN NT1 circuit design will be similar to the one shown in Figure 10, “Typical ISDN NT1 Application Diagram” on page 9.

The DC Termination IC performs two functions in an NT1; as an electronic inductor which provides a low impedance dc termination with a high impedance ac termination, and second as part of the dc signalling system for testing line capability. The CPC1465 meets or exceeds the requirements for an NT1 dc termination as described in ANSI T1.601-1991.

2.1.1 Surge Protection

The CPC1465 requires few external components **(see Figure 1 on page 1)**. Although the CPC1465 is current limited, it is not an over voltage surge protector. Clare recommends the use of a crowbar-type surge protector that limits the line voltage applied to the CPC1465 to 250 V. The protection device must be able to withstand the surge requirements specified by the appropriate governing agency in regions where the product will be deployed. Teccor, Inc. and Bourns, Inc. make suitable surge protectors for most applications. Devices such as Teccor’s P1800SC or P2000SC Sidactors and Bourns’ TISP4220H3 or TISP4240H3 thyristors should provide suitable protection.

2.1.2 Bridge Rectifier

The bridge rectifier in the CPC1465 ensures that the device is polarity insensitive and provides consistent operational characteristics if the tip and ring leads are reversed.

2.1.3 Trigger

The dc tip-lead to ring-lead I-V characteristics of the CPC1465 are shown in “I-V Requirements Template, 0 V to 50 V” on page 5, and in “I-V Requirements Template, 0 V to 250 V” on page 5. Application of battery voltage to the loop causes the CPC1465 to conduct when the voltage exceeds approximately 35 V. With sufficient voltage across the tip-lead and ring-lead terminals, the CPC1465 will conduct about 150 µA of dc current for approximately 20 ms, then it turns on. The CPC1465 remains on as long as the loop current exceeds a nominal 0.5 mA.

The CPC1465 turn-on and turn-off timing circuits assure that the device will not turn on if a voltage greater than 43.5 V is applied for less than 3 ms, and that it will not turn off if loop current is interrupted for less than 3 ms.

2.1.4 Activation and Deactivation

Current for the opto-coupler LED flows when the current in the CPC1465 exceeds 1 mA. The CPC1465 will turn on if a voltage above 43.5 V is applied for more than 50 ms, and it will turn off if 1 mA loop current is interrupted for more than 100 ms. See “Test Circuit for Activate and Deactivate Times” on page 7, “Applied Waveform for Activation Test” on page 7, and “Applied Waveform for Deactivation Test” on page 7 for more information.

LED current is interrupted when loop current is interrupted. The current in the on state is determined by the battery voltage feed circuit and the loop resistance.

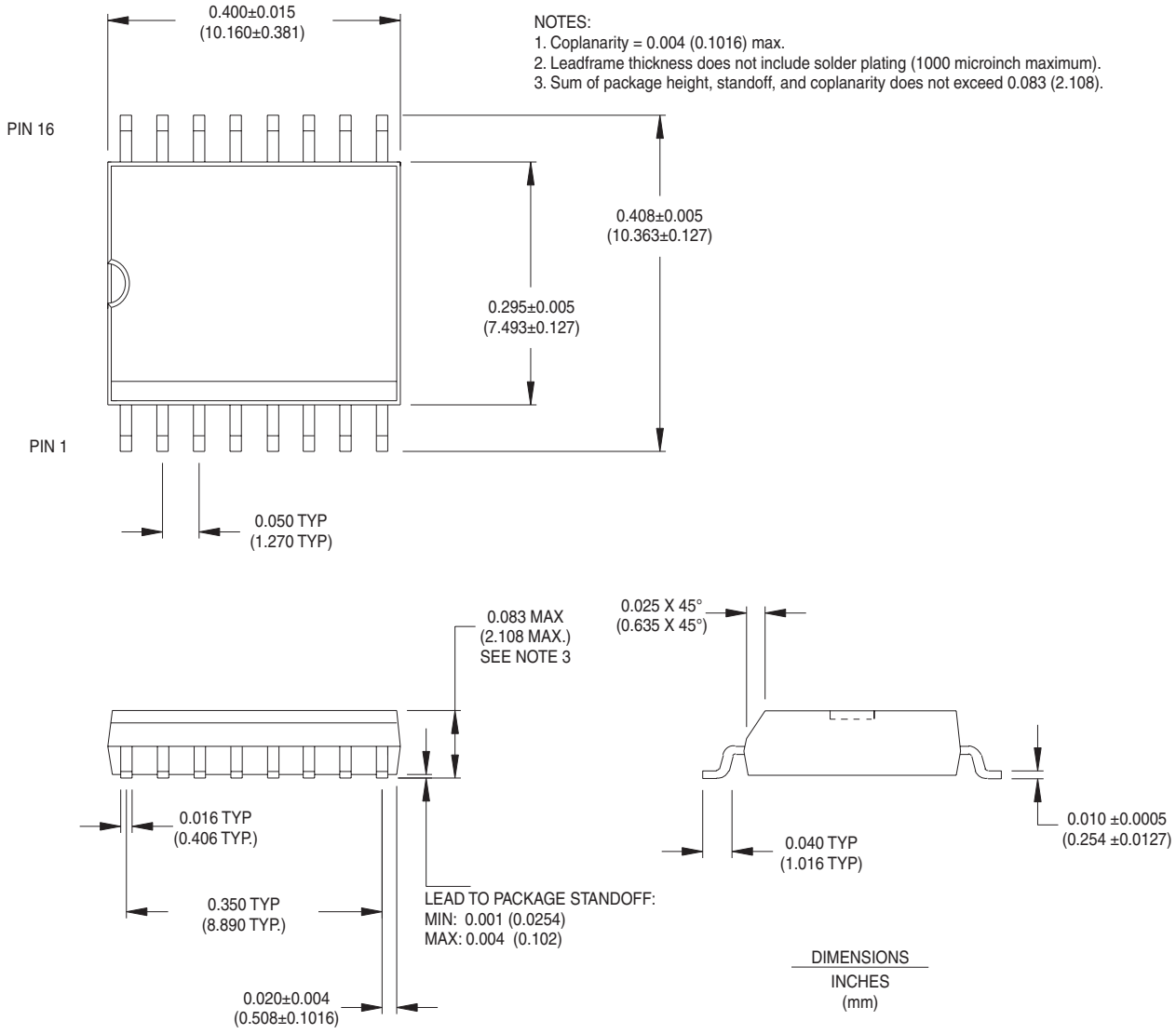
2.1.5 Fault Conditions

If loop resistance is low or if the applied voltage is very high, the CPC1465 limits loop current to less than 70 mA. While limiting current, the CPC1465 shunts current through the 2.2 kΩ resistor to prevent excess heating of the CPC1465.

Voltage in excess of 100 V applied to the tip and ring interface will cause the CPC1465 to shut down with very little current flow. Removal of the excessive voltage automatically resumes normal operation.

3. Manufacturing Information

Figure 11. Mechanical Dimensions



NOTE: The CPC1465 uses a slightly different package than the LH1465AAE. Some adjustment to printed-circuit-board pad layout may be needed for existing applications.

Figure 12. Printed Circuit Board Layout Pattern

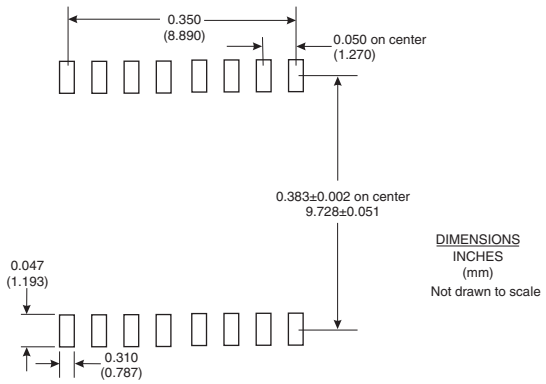
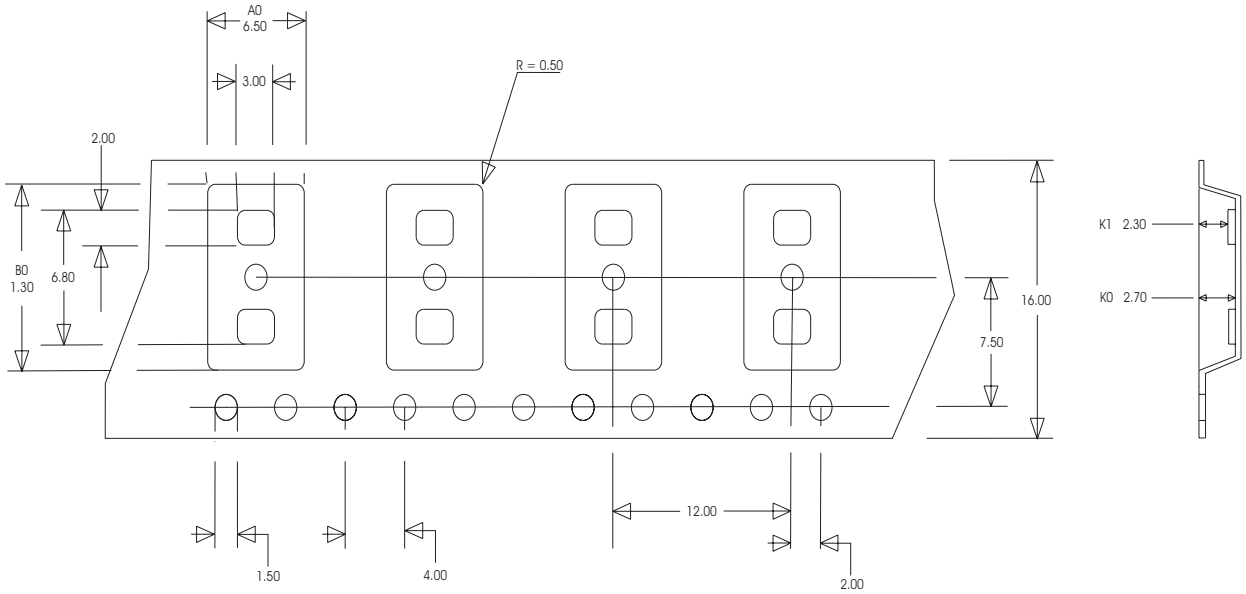


Figure 13. Tape and Reel Packaging



A0 =	6.5 mm
B0 =	10.3 mm
K0 =	2.3 mm
K1 =	2.7 mm

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS AND CARRY TOLERANCES OF EIA STANDARD 481-2.
2. THE TAPE COMPLIES WITH ALL "NOTES" FOR CONSTANT DIMENSIONS LISTED ON PAGE 5 OF EIA-481-2.

3.1 Soldering

3.1.1 Moisture Reflow Sensitivity

Clare has characterized the moisture reflow sensitivity for this product using IPC/JEDEC standard J-STD-020A. Moisture uptake from atmospheric humidity occurs by diffusion. During the solder reflow process, in which the component is attached to the PCB, the whole body of the component is exposed to high process temperatures. The combination of moisture uptake and high reflow soldering temperatures may lead to moisture induced delamination and cracking of the component. To prevent this, this component must be handled in accordance with IPC/JEDEC standard J-STD-020A per the labelled moisture sensitivity level (MSL), level 1.

3.1.2 Reflow Profile

The maximum ramp rates, dwell times, and temperatures of the assembly reflow profile should not exceed those specified in IPC standard IPC-9502, table 2. Soldering processes are limited to 220 °C component body temperature.

3.2 Washing

Clare does not recommend ultrasonic cleaning of this part.

Specifications: DS-CPC1465 - Rev. 1.0

2/11/2004