

## Multilayer Ceramic Chip Capacitors

### Introduction

Multilayer Surface Mount Ceramic Capacitors are constructed by screen printing alternative layers of internal metallic electrodes onto ceramic dielectric materials and firing into a concrete monolithic body, then completed by application of metal end terminations which are fired to assure permanent bonding with the individual internal electrodes.

Multilayer ceramic capacitors have various features such as large capacitance values in small sizes and excellent high frequency characteristics.

Moreover, chip capacitors can be used on surface mount assembly equipment. Our fully integrated manufacturing and total quality control systems ensure unprecedented high standards of quality and reliability.

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### Chip Capacitor Selection

Selection of the most suitable capacitor for any application is based on the following:

#### **Dielectric Type**

The choice of dielectric is largely determined by the temperature stability required.

#### **COG (NPO)**

Capacitance change with temperature is 0-30ppm/°C which is less than -0.3%/°C from -55°C to +125°C. Typical capacitance change with life is less than -0.1% for NPOs, one-fifth that shown by most other dielectrics. NPO formulations show no aging characteristics.

#### **X7R/X5R**

Its temperature variation of capacitance is within  $\pm 15\%$  from -55°C to +125°C (-55°C to +85°C for X5R). The capacitance change is non-linear.

#### **Z5U**

Despite their capacitance instability, Z5U formulations are very popular because of their small size, temperature range low ESL, low ESR and excellent frequency response. These features are particularly important for decoupling application where only a minimum capacitance value is required.

#### **Y5V**

Y5V formulations are for general purpose use in a limited temperature range. They have a wide temperature characteristic of +22% - 82% capacitance change over the operating temperature range of -30°C to +85°C. Y5Vs high dielectric constant allows the manufacture of very high capacitance values (up to 22MF) in small physical sizes.

#### **Capacitance Value & Tolerance**

Determined by circuit requirements. Note that chip prices decrease with lower capacitance value and looser tolerance.

#### **Voltage**

Determined by circuit requirements. Units are designed to exceed the withstanding voltage specification, i.e., the user need not incorporate an additional safety margin.

#### **Capacitor Size**

Select the smallest unit permitted by the circuit constraints that provides the required capacitance and voltage rating. All Cal-Chip capacitors conform to EIA specifications.

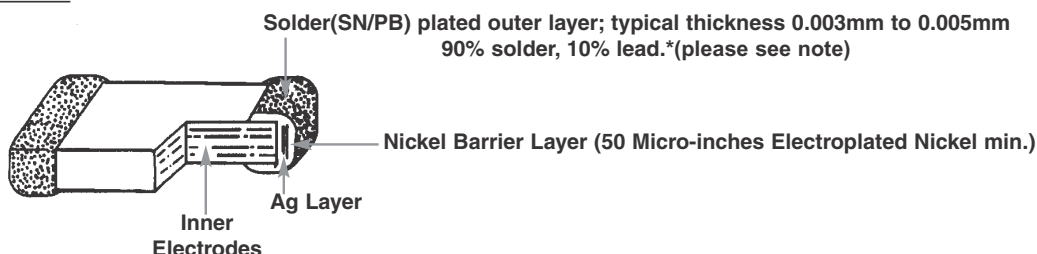
#### **Capacitor Termination**

Termination choice is largely determined by the chip attachment method. Silver-palladium is adequate for most applications involving soldering or solder reflow.

Nickel barrier is standard and recommended for units exposed to repeated solder cycles, to minimize leaching of the termination.

## Multilayer Ceramic Chip Capacitors

### Construction



### Example

GMC21	CG	102	J	50	N	T				
Size Code	Dielectric	Capacitance (pF)	Capacitance Tolerance (EIA Code)	Voltage	Termination	Packaging Code				
	<table><tr><td>CG (COG) (NPO)</td></tr><tr><td>X7R or X5R</td></tr><tr><td>Z5U</td></tr><tr><td>Y5V</td></tr></table>	CG (COG) (NPO)	X7R or X5R	Z5U	Y5V					
CG (COG) (NPO)										
X7R or X5R										
Z5U										
Y5V										
Capacitance values are represented in 3 digits, and expressed in pF. The first two digits are significant, and the third is the number of zeros. The letter "R" is used as a decimal point.										
0R5		0.5pF	B ±0.1pf for ≤ 10pF		6r3 6.3 DC					
5R0		5pF	C ±0.25pF for ≤ 10pF		10 10 DC					
100		10pF	D ±0.5pF for ≤ 10pF		16 16 DC					
101		100pF	F ±1%		25 25 DC					
102		1000pF	G ±2%		50 50 DC					
103		.01mF	J ±5%		100 100 DC					
104		.1mF	K ±10%		200 200 DC					
105		1.0mF	M ±20%			N Nickel Barrier				
106		10mF	Z -20%~+80%			T Tape and Reel				

\*Note for Lead Free: Cal-Chip is beginning to phase in Lead-Free products. Upon checking availability with the factory, please specify "TLF" at the end of the part number, so the sales team knows you require lead-free product. When you receive the parts you will notice "LF" at the end of the Lot Code indicating the parts are lead-free.

Multilayer Ceramic Chip Capacitors

**0201**

DIMENSION (MM)

**GMC02**

<b>L</b>		0.6 ± 0.03						
<b>W</b>		0.3 ± 0.03						
<b>T(MAX)</b>		0.3 ± 0.03						
<b>BW</b>		0.15 ± 0.05						
dielectric		NPO/COG	X5R		X7R		Y5V/Z5U	
Rated Voltage		25	6.3	10	6.3	10	16	6.3
Cap. Range								
0.5pF	0R5							
1.0	1R0							
1.2	1R2							
1.5	1R5							
1.8	1R8							
2.2	2R2							
2.7	2R7							
3.3	3R3							
3.9	3R9							
4.7	4R7							
5.6	5R6							
6.8	6R8							
8.2	8R2							
10	100							
12	120							
15	150							
18	180							
22	220							
27	270							
33	330							
39	390							
47	470							
56	560							
68	680							
82	820							
100	101							
120	121							
150	151							
180	181							
220	221							
270	271							
330	331							
390	391							
470	471							
560	561							
680	681							
820	821							
1.0nF	102							
1.2	122							
1.5	152							
1.8	182							
2.2	222							
2.7	272							
3.3	332							
3.9	392							
4.7	472							
5.6	562							
6.8	682							
8.2	822							
10	103							
12	123							
15	153							
18	183							
22	223							
27	273							
33	333							
39	393							
47	473							
56	563							
68	683							
82	823							
100	104							
120	124							
150	154							
180	184							
220	224							
270	274							
330	334							
390	394							
470	474							
560	564							
680	684							
820	824							
1.0uF	105							
2.2	225							

## Multilayer Ceramic Chip Capacitors

## 0402 & 0603

**GMC04**

## GMC10

Type	0402															0603															
Length (L1) mm	1.0±0.05															1.6±0.2															
inches	0.04±0.002															0.063±0.008															
Width (W) mm	0.5±0.05															0.8±0.2															
inches	0.02±0.002															0.031±0.008															
Thickness (H) mm	0.5±0.1															0.8±0.2															
inches	0.02±0.004															0.031±0.008															
Termination Band (L2+L3) mm	Min 0.1					Max 0.35					Min 0.1					Max 0.4															
inches	0.004					0.014					0.004					0.015															
Band Gap (L4)mm (Min)	0.3 0.012															0.6 0.015															
Dielectric	COG		X5R			X7R					Y5V & Z5U					COG		X5R			X7R					Y5V & Z5U					
Rated Voltage d.c.	25	50	6.3	10	16	6.3	10	16	25	50	6.3	10	16	25	50	25	50	100	6.3	10	16	6.3	10	16	25	50/100	6.3	10	16	25	50
Cap Range	Code																														
0.5pF	0R5																														
1.0	1R0																														
1.2	1R2																														
1.5	1R5																														
1.8	1R8																														
2.2	2R2																														
2.7	2R7																														
3.3	3R3																														
3.9	3R9																														
4.7	4R7																														
5.6	5R6																														
6.8	6R8																														
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3.9	395																														
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5.6	565																														
6.8	685																														
8.2	825																														
10	106																														
15	156																														
22	226																														
33	336																														
47	476																														

**COG/NPO**[illegible]

**COG/NPO (cont.)**[illegible]

Multilayer Ceramic Chip Capacitors

X7R

GMC21				GMC31				GMC32				GMC40				GMC43				GMC45				GMC55				GMC57					
Type		0805				1206				1210				1808				1812				1825				2220				2225			
Length	mm	2.0±0.3				3.2±0.3				3.2±0.3				4.57±0.25				4.5±0.35				4.5±0.35				5.7±0.4				5.7±0.4			
	Inches	0.08±0.012				0.125±0.012				0.125±0.012				0.18±0.01				0.18±0.014				0.18±0.014				0.225±0.016				0.225±0.016			
Width	mm	1.25±0.2				1.6±0.2				2.5±0.3				2.03±0.25				3.2±0.3				6.3±0.4				5.0±0.4				6.3±0.4			
	Inches	0.05±0.008				0.063±0.008				0.10±0.012				0.08±0.01				0.125±0.012				0.25±0.016				0.197±0.016				0.25±0.016			
Thickness	mm	1.5				1.8				2.8				3.0				3.0				3.2				3.5				3.5			
	Inches	0.059				0.071				0.110				0.118				0.118				0.126				0.138				0.138			
Termination Band	mm	Min	Max			Min	Max			Min	Max			Min	Max			Min	Max			Min	Max			Min	Max			Min	Max		
	mm	0.25	0.75			0.25	0.75			0.25	0.75			0.25	0.75			0.25	0.75			0.25	0.75			0.25	0.75			0.25	0.75		
	Inches	0.01	0.03			0.01	0.03			0.01	0.03			0.01	0.03			0.01	0.03			0.01	0.03			0.01	0.03			0.01	0.03		
Band Gap	mm	0.5				1.4				1.4				2.0				2.2				2.2				2.9				2.9			
	Inches	0.019				0.055				0.055				0.078				0.087				0.087				0.114				0.114			
Rated Voltage d.c.		6.3	10	16	25	6.3	10	16	25	10	16	25	10	16	25	10	16	25	10	16	25	10	16	25	10	16	25	10	16	25	10	16	25
Cap. Range	Code																																
0.5pF	0R5																																
1.0	1R0																																
1.2	1R2																																
1.5	1R5																																
1.8	1R8																																
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Multilayer Ceramic Chip Capacitors

X7R (cont)

			GMC21			GMC31			GMC32			GMC40			GMC43			GMC45			GMC55			GMC57		
Type			0805			1206			1210			1808			1812			1825			2220			2225		
Length	mm		2.0±0.3			3.2±0.3			3.2±0.3			4.57±0.25			4.5±0.35			4.5±0.35			5.7±0.4			5.7±0.4		
	Inches		0.08±0.012			0.125±0.012			0.125±0.012			0.18±0.01			0.18±0.014			0.18±0.014			0.225±0.016			0.225±0.016		
Width	mm		1.25±0.2			1.6±0.2			2.5±0.3			2.03±0.25			3.2±0.3			6.3±0.4			5.0±0.4			6.3±0.4		
	Inches		0.05±0.008			0.063±0.008			0.10±0.012			0.08±0.01			0.125±0.012			0.25±0.016			0.197±0.016			0.25±0.016		
Thickness	mm		1.5			1.8			2.8			3.0			3.0			3.0			3.5			3.5		
	Inches		0.051			0.063			0.07			0.08			0.07			0.07			0.07			0.07		
Termination Band			Min	Max		Min	Max		Min	Max		Min	Max		Min	Max		Min	Max		Min	Max		Min	Max	
	mm		0.25	0.75		0.25	0.75		0.25	0.75		0.25	0.75		0.25	0.75		0.25	0.75		0.25	0.75		0.25	0.75	
	Inches		0.01	0.03		0.01	0.03		0.01	0.03		0.01	0.03		0.01	0.03		0.01	0.03		0.01	0.03		0.01	0.03	
Band Gap	mm		0.5			1.4			1.4			2.0			2.2			2.2			2.9			2.9		
	Inches		0.019			0.055			0.055			0.078			0.087			0.087			0.114			0.114		
Rated Voltage d.c.			50	100	200	50	100	200	50	100	200	50	100	200	50	100	200	50	100	200	50	100	200	50	100	200
Cap. Range	Code																									
0.5pF	0R5																									
1.0	1R0																									
1.2	1R2																									
1.5	1R5																									
1.8	1R8																									
2.2	2R2																									
2.7	2R7																									
3.3	3R3																									
3.9	3R9																									
4.7	4R7																									
5.6	5R6																									
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4.7	475																									
6.8	685																									
10	106																									
22	226																									



**X5R**

[illegible]

**Y5V/Z5U**[illegible]

Multilayer Ceramic Chip Capacitors

Y5V/Z5U (cont)

			GMC21			GMC31			GMC32			GMC40			GMC43			GMC45			GMC55			GMC57		
Type		0805			1206			1210			1808			1812			1825			2220			2225			
Length	mm	2.0±0.3			3.2±0.3			3.2±0.3			4.57±0.25			4.5±0.35			4.5±0.35			5.7±0.4			5.7±0.4			
	Inches	0.08±0.012			0.125±0.012			0.125±0.012			0.18±0.01			0.18±0.014			0.18±0.014			0.225±0.016			0.225±0.016			
Width	mm	1.25±0.2			1.6±0.2			2.5±0.3			2.03±0.25			3.2±0.3			6.3±0.4			5.0±0.4			6.3±0.4			
	Inches	0.05±0.008			0.063±0.008			0.10±0.012			0.08±0.01			0.125±0.012			0.25±0.016			0.197±0.016			0.25±0.016			
Thickness	mm	1.5			1.8			2.8			3.0			3.0			3.2			3.5			3.5			
	Inches	0.059			0.07			0.110			0.118			0.118			0.126			0.138			0.138			
Termination Band	mm	Min	Max		Min	Max		Min	Max		Min	Max		Min	Max		Min	Max		Min	Max		Min	Max		
	Inches	0.25	0.75		0.25	0.75		0.25	0.75		0.25	0.75		0.25	0.75		0.25	0.75		0.25	0.75		0.25	0.75		
Band Gap	mm	0.5			1.4			1.4			2.0			2.2			2.2			2.9			2.9			
	Inches	0.019			0.055			0.055			0.078			0.087			0.087			0.114			0.114			
Rated Voltage d.c.		50	100	200	50	100	200	50	100	200	50	100	200	50	100	200	50	100	200	50	100	200	50	100	200	
Cap. Range	Code																									
0.5pF	0R5																									
1.0	1R0																									
1.2	1R2																									
1.5	1R5																									
1.8	1R8																									
2.2	2R2																									
2.7	2R7																									
3.3	3R3																									
3.9	3R9																									
4.7	4R7																									
5.6	5R6																									
6.8	6R8																									
8.2	8R2																									
10	100																									
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820	824																									
1.0uF	105																									
2.2	225																									
3.3	335																									
4.7	475																									
6.8	685																									
10	106																									
22	226																									
33	336																									
47	476																									
68	686																									
100	107																									

### Multilayer Ceramic Chip Capacitors

#### COG Dielectric

Ultra stable class I dielectric: linear temperature coefficient, low loss, negligible change of electrical properties with time, voltage and frequency.

Operating Temperature Range	Temperature Coefficient	Temperature Voltage Coefficient ( $\Delta C_{Max}$ @ $V_{DCW}$ )	Dissipation Factor	Insulation Resistance	Dielectric withstanding Voltage	Aging Rate	Test Parameters
-55°C to +125°C	0±30ppm/°C	0±30ppm/°C	0.1% Max, 0.02% Typical	<ul style="list-style-type: none"> <li>• 25°C, <math>V_{DCW}</math>: &gt;100GΩF or 1000ΩF, whichever is less</li> <li>• 125°C, <math>V_{DCW}</math>: &gt;10GΩF or 100ΩF, whichever is less</li> </ul>	3 X $V_{DCW}$	0% per decade hour	<ul style="list-style-type: none"> <li>• <math>C \leq 1000pF</math> f=1MHz V=1.0Vrms ±0.2Vrms T=25°C</li> <li>• <math>C &gt; 1000pF</math> f=1KHz V=1.0Vrms ±0.2Vrms T=25°C</li> </ul>

#### X7R Dielectric

Stable class II dielectric (EIA X7R)

Operating Temperature Range	Temperature Coefficient	Temperature Voltage Coefficient ( $\Delta C_{Max}$ @ $V_{DCW}$ )	Dissipation Factor	Insulation Resistance	Dielectric withstanding Voltage	Aging Rate	Test Parameters
-55°C to +125°C	±15%	X7R Not Applicable	2.5% Max, 1.8% Typical	<ul style="list-style-type: none"> <li>• 25°C, <math>V_{DCW}</math>: &gt;100GΩFor 1000ΩF, whichever is less</li> <li>• 125°C, <math>V_{DCW}</math>: &gt;10GΩF or 100ΩF, whichever is less</li> </ul>	2.5 X $V_{DCW}$	<2% per decade hour	1KHz, 1.0Vrms ±0.2Vrms 25°C values > or = to 10uF 1.0Vrms 120Hz

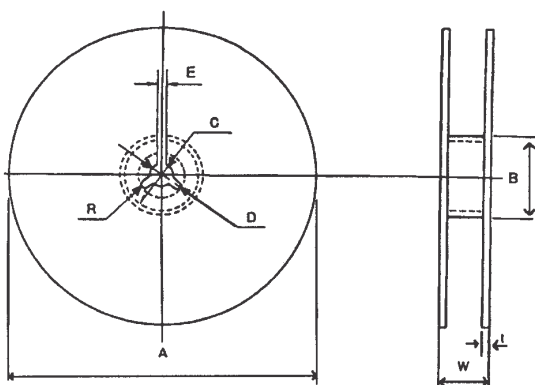
## Multilayer Ceramic Chip Capacitors - Z5U (Y5V) Dielectric

High capacitance per unit volume: general purpose product

Operating Temperature Range	Temperature Coefficient	Dissipation Factor	Insulation Resistance	Dielectric withstanding Voltage	Aging Rate	Test Parameters
-30°C to +85°C	+22% -82%	3.0% Max, 2.0% Typical	10GΩ or 100ΩF whichever is less, 25°C, V <sub>DCW</sub>	2.5 X V <sub>DCW</sub>	3.0% per decade hour	1KHz, 1Vrms 25°C values > or = to 10uF 1.0Vrms 120Hz

### Packaging (Taping)

(Reel Type-Size)



#### Standard Reel

Unit:mm

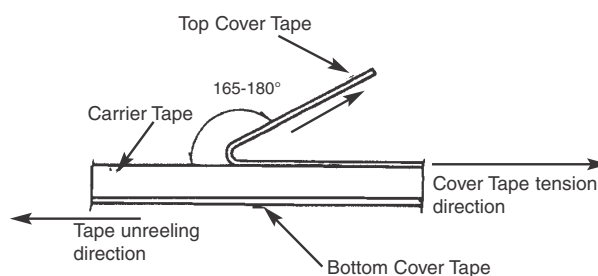
A	B	C	D	E	W	t	R
ø178 ±2.0	ø50 min.	ø13.0 ±0.5	ø21.0 ±0.8	2.0 ±0.5	14.9 ±1.5	0.8 ±0.2	1.0

#### 10000 units per reel OPTIONAL

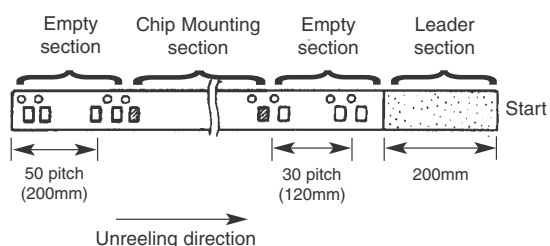
Unit:mm

A	B	C	D	E	W	t	R
ø250 ±2.0	ø50 min.	ø13.0 ±0.5	ø21.0 ±0.8	2.0 ±0.5	10.0 ±1.5	0.8 ±0.2	1.0

#### Carrier Tape (Standard)



- To peel off the cover tape by the method shown in the right figure apply a peel-off force of 20 gf - 60 gf (card board); 35 gf - 75 gf (plastic tape).
- The cover tape should not touch the top or bottom of the chip.
- If the cover tape has been peeled off it may be difficult to remove the chip due to punch-hole clearance, dirt, and debris. Make sure therefore that no paper waste will adhere to and block the absorption nozzle.
- If the cover tape has been peeled off from the top, stick it back on with a suitable adhesive.
- Follow the illustration for the start and end of the winding operation.



## Multilayer Ceramic Chip Capacitors

- Cardboard carrier tape for 0402, 0603 type and 0805/1206 type

Unit: mm

Type A	B W	F E	P <sub>1</sub> P <sub>2</sub>	P <sub>0</sub> D <sub>0</sub>	t <sub>1</sub> t <sub>2</sub>								Mounting Hole	Quantity per Reel
0402	0.7±0.2	1.3±0.2	8.0±0.3	3.5±0.05	1.75±0.1	2.0±0.05		4.0±0.1	ø1.5 <sup>+0.1</sup> <sub>-0</sub>	1.1 max	1.4 max	Angular Punch Hole	10000	
0603	1.1±0.2	1.9±0.2				4000								
0805	1.65±0.2	2.4±0.2				4000 to 5000*								
1206	2.0±0.2	3.6±0.2				4000 to 5000*								

\*Dependent on chip thickness

- Embossed plastic carrier tape for 0805/1206 type and 1210 type

Unit: mm

Type	A	B	W	F	E	P <sub>1</sub>	P <sub>2</sub>	P <sub>0</sub>	D <sub>0</sub>	t <sub>1</sub>	t <sub>2</sub>	Mounting Hole	Quantity per Reel
0805	1.45±0.2	2.3±0.2	8.0±0.3	3.5±0.05	1.75±0.1	4.0±0.1	2.0±0.05	4.0±0.1	ø1.5 <sup>+0.1</sup> <sub>-0</sub>	0.6 max	2.5 max	Angular Embossed Hole	2000 to 5000*
1206	2.0±0.2	3.6±0.2											2000 to 5000*
1210	2.9±0.2	3.6±0.2											2000 to 4000*

\*Dependent on chip thickness

- Embossed plastic carrier tape for 1812, 1825, 2220 and 2225 type

Unit: mm

Type	A	B	W	F	E	P <sub>1</sub>	P <sub>2</sub>	P <sub>0</sub>	D <sub>0</sub>	t <sub>1</sub>	t <sub>2</sub>	Mounting Hole	Quantity per Reel
1812	3.6±0.2	4.9±0.2	12.0±0.3	5.5±0.05	1.75±0.1	8.0±0.1	2.0±0.05	4.0±0.1	ø1.5±0.1	0.6 max.	6.5 max.	Angular Embossed Hole	
1825	6.8±0.3	4.9±0.2											1000
2220	5.5±0.3	6.2±0.3											1000
2225	6.8±0.3	6.2±0.3											1000

\*Dependent on chip thickness

**Tape and Reel Packing Quantities**

Chip Size	178 mm (7") Reel	330 mm (13") Reel
0402	10,000	N/A
0603	4,000	16,000
0805	4,000	12,000
1206	4,000	15,000
1210	2,000 , 4,000	8,000
1812	1,000	4,000
1825	1,000	4,000
2220	1,000	4,000
2225	1,000	4,000

The tape and reel packing quantities apply to voltages up to 200V rating only.

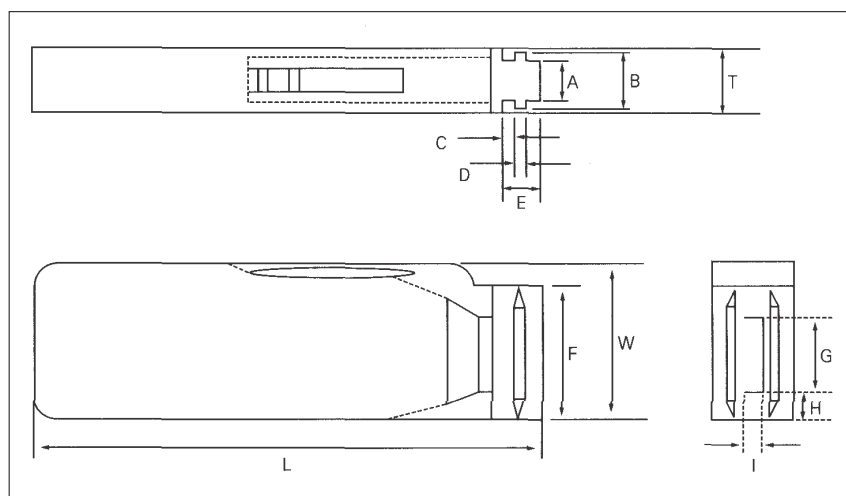
The 0402 and 0603 size chips have similar width and thickness dimensions.

## Multilayer Ceramic Chip Capacitors

### BULK CASE

- Bulk case packaging can reduce the stock space and transportation costs.
- The bulk feeding system can increase the productivity.
- It can eliminate the components loss.

### • Structure and Dimension



Symbol	A	B	T	C	D	E
Dimension	6.8±0.1	8.8±0.1	12±0.1	1.5 <sup>+0.1</sup> <sub>-0</sub>	2 <sup>+0</sup> <sub>-0.1</sub>	4.7±0.1

Symbol	F	W	G	H	L	I
Dimension	31.5 <sup>+0.2</sup> <sub>-0</sub>	36 <sup>+0</sup> <sub>-0.2</sub>	19±0.35	7±0.35	110±0.7	5±0.35

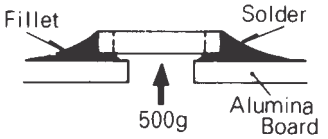
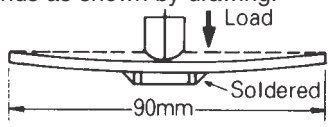
### • Quantity

Size	04(0402)	10(0603)	21(0805)	
			T≤0.85mm	T≥1.0mm
Quantity	80,000	15,000	10,000	5,000



## Multilayer Ceramic Chip Capacitors

### RELIABILITY AND TEST CONDITIONS

Item	Specification	Test Method
<b>Capacitance</b>	Within tolerance shown by part number code	<ul style="list-style-type: none"> <li>Class (I)  <math>C &lt; 1000\text{pF}</math>: <math>1\text{MHz} \pm 10\%</math>,  <math>0.5</math> to <math>5\text{Vrms}</math>  <math>C \geq 1000\text{pF}</math>: <math>1\text{KHz} \pm 10\%</math>,  <math>1.0 \pm 0.2\text{Vrms}</math> </li> <li>Class (II)  <math>1\text{KHz} \pm 10\%</math>, <math>1.0 \pm 0.2\text{Vrms}</math>  values <math>&gt;</math> or <math>=</math> to <math>10\mu\text{F}</math> <math>1.0\text{Vrms}</math> <math>120\text{Hz}</math> </li> </ul>
<b>Dissipation Factor (<math>\tan\delta</math> or Q)</b>	<ul style="list-style-type: none"> <li>Class (I)  <math>C &lt; 30\text{pF}</math>: <math>Q \geq 400 + 20 \times C</math>  <math>C \geq 30\text{pF}</math>: <math>Q \geq 1000</math> </li> <li>Class (II)  <math>X7R</math>: <math>DF \leq 2.5\%</math>  <math>Y5V/Z5U</math>: <math>DF \leq 3.0\%</math> </li> </ul>	
<b>Insulation Resistance (IR)</b>	$\text{NPO-XR7}$ : $C \leq 50,000\text{pF}$ : $IR \geq 100\text{G}\Omega$ $C > 50,000\text{pF}$ : $IR \geq 500\text{M}\Omega$ . Per $U_f$ . $Y5V/Z5U$ : $IR \geq 10\text{G}\Omega$	Apply rated voltage for 60 seconds at room temperature and normal humidity. (70% RH max)
<b>Dielectric Withstanding Voltage</b>	There shall be no evidence of damage or flash over during the test	Apply 3 x rated voltage (Class I) or 2.5 x rated voltage (Class II) to both terminations for 5 seconds. Charge and discharge current are less than 50mA.
<b>Termination Adherence</b>	No mechanical damage	 <p>Care shall be taken to avoid thermal shock. 500g of steady pull is applied in direction of arrow for 1 minute.</p>
<b>Bend Strength</b>	No mechanical damage	<p>After soldering capacitor on the glass-epoxy PWB, 2 mm of bending shall be applied for 10 seconds as shown by drawing.</p> 
<b>Life Test (High Temperature Loading Test)</b>	$\Delta C$	<ul style="list-style-type: none"> <li>Class (I)  No more than <math>\pm 3\%</math> or <math>\pm 0.3\text{pF}</math> whichever is less </li> <li>Class (II)  <math>X7R</math>: <math>\pm 10\%</math> max  <math>Y5V/Z5U</math>: <math>\pm 30\%</math> max </li> </ul>
	Q or DF	<ul style="list-style-type: none"> <li>Class (I)  <math>C &lt; 10\text{pF}</math>: <math>Q &gt; 200 + 10 \times C</math>  <math>10 \leq C &lt; 30\text{pF}</math>: <math>Q \geq 275 + 5/2 \times C</math>  <math>C \geq 30\text{pF}</math>: <math>Q \geq 350</math> </li> <li>Class (II)  <math>X7R</math>: <math>DF \leq 5.0\%</math>  <math>Y5V/Z5U</math>: <math>DF \leq 7.5\%</math> </li> </ul>
	IR	$1000\text{M}\Omega$ or $50\Omega\text{F}$ , min whichever is less

### Multilayer Ceramic Chip Capacitors

#### RELIABILITY AND TEST CONDITIONS

Item	Specification	Test Method
<b>Moisture Test</b>	$\Delta C$ <ul style="list-style-type: none"> <li>Class (I) No more than <math>\pm 5\%</math> or <math>\pm 0.5\text{pF}</math> whichever is larger</li> <li>Class (II) X7R: <math>\pm 10\%</math> Y5V/Z5U: <math>\pm 30\%</math></li> </ul>	<p>The capacitors shall be subjected to <math>40^\circ\text{C}</math>, 90-95%RH for 500 hours.</p> <p>After above testing condition, samples shall be kept in room temperature for 24 hours (Class I) or 48 hours (Class II), and then shall be measured.</p>
	Q or DF <ul style="list-style-type: none"> <li>Class (I) <math>C &lt; 10\text{pF}</math>: <math>Q &gt; 200 + 10 \times C</math> <math>10 \leq C &lt; 30\text{pF}</math>: <math>Q \geq 275 + 5/2 \times C</math> <math>C \geq 30\text{pF}</math>: <math>Q \geq 350</math></li> <li>Class (II) X7R: <math>DF \leq 5.0\%</math> Y5V/Z5U: <math>DF \leq 7.5\%</math></li> </ul>	
	IR           1000M $\Omega$ or 50 $\Omega\text{F}$ , whichever is less	
<b>Moisture Resistance Test</b>	$\Delta C$ <ul style="list-style-type: none"> <li>Class (I) No more than <math>\pm 7.5\%</math> or <math>\pm 0.75\text{pF}</math> whichever is larger</li> <li>Class (II) X7R: <math>\pm 10\%</math> Y5V/Z5U: <math>\pm 30\%</math></li> </ul>	<p>Apply rated voltage at <math>40^\circ\text{C}</math>, 90-95%RH for 500 hours.</p> <p>The surge current shall not exceed 50mA. After testing with above condition, samples shall be kept in room temperature for 24 hours (Class I) or 48 hours (Class II), and then shall be measured.</p>
	Q or DF <ul style="list-style-type: none"> <li>Class (I) <math>C &lt; 30\text{pF}</math>: <math>Q &gt; 100 + 100/3 \times C</math> <math>C \geq 30\text{pF}</math>: <math>Q \geq 200</math></li> <li>Class (II) X7R: <math>DF \leq 5.0\%</math> Y5V/Z5U: <math>DF \leq 7.5\%</math></li> </ul>	
	IR           500M $\Omega$ or 25 $\Omega\text{F}$ , min whichever is less	
<b>Temperature Cycle</b>	$\Delta C$ <ul style="list-style-type: none"> <li>Class (I) No more than <math>\pm 2.5\%</math> or <math>\pm 0.25\text{pF}</math> whichever is larger</li> <li>Class (II) X7R: <math>\pm 5\%</math> Y5V/Z5U: <math>\pm 20\%</math></li> </ul>	<p>Perform 5 cycles as follow:</p> <ol style="list-style-type: none"> <li>Room temperature. Dwell for 15 minutes.</li> <li>Minimum operating temperature, dwell for 30 minutes.</li> <li>Room temperature, dwell for 30 minutes.</li> <li>Maximum operating temperature, dwell for 30 minutes.</li> </ol> <p>After above testing condition, samples shall be kept in room temperature for 24 hours (Class I) or 48 hours (Class II), and then shall be measured.</p>
	Q or DF           To satisfy the specified initial value.	
	IR           To satisfy the specified initial value.	
<b>Solderability</b>	Termination area shall be at least 95% covered with a new solder coating. There shall be no crack and ceramic exposure of terminated surface by melting.	<p>The capacitors are completely immersed during <math>4 \pm 0.5</math> seconds in the molten solder with a temperature of <math>230 \pm 5^\circ\text{C}</math></p> <p>*Solder: Sn 63.</p>
<b>Resistance to Solder Heat Test</b>	$\Delta C$ <ul style="list-style-type: none"> <li>Class (I) No more than <math>\pm 2.5\%</math> or <math>\pm 0.25\text{pF}</math> whichever is larger</li> <li>Class (II) X7R: <math>\pm 5\%</math> Y5V/Z5U: <math>\pm 20\%</math></li> </ul>	<p>Immerse into molten solder at <math>270 \pm 5^\circ\text{C}</math> for <math>3 \pm 0.5</math> seconds. Preheat before immersion.</p> <ol style="list-style-type: none"> <li><math>80 \sim 100^\circ\text{C}</math> for 2 minutes.</li> <li><math>150 \sim 180^\circ\text{C}</math> for 2 minutes.</li> <li><math>270 \pm 5^\circ\text{C}</math> for <math>3 \pm 0.5</math> seconds.</li> </ol> <p>The capacitance measurement shall be made after sample keeping at room temperature for 24 hours.</p>
	Q or DF           To satisfy the specified initial value.	
	IR           To satisfy the specified initial value.	

APPLICATION MANUAL FOR  
SURFACE MOUNTING

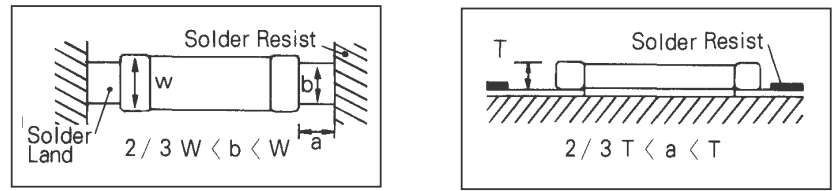
1. Temperature / Humidity Control

Since dew condensation may occur by the differences in temperature when the products are take out of storage, it is important to maintain a temperature-controlled environment.

2. Design of Solder Land Pattern

When designing printed circuit boards, the shape and size of the solder lands must allow for the proper amount of solder on the capacitor. The amount of solder at the end terminations has a direct effect on the probability that the chip will crack. The greater amount of solder, the larger amount of stress on the chip, and the more likely that it will break. Use the following illustrations as guidelines for proper solder land design.

Recommendation of solder land shape and size.



3. Adhesives

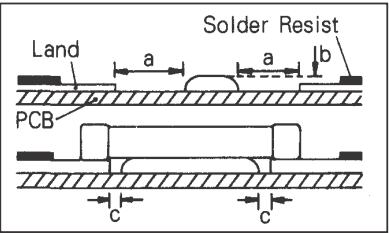
MLCCs generally require the use of an adhesive to adhere the chips to the circuit board prior to wave soldering.

3-1. Requirements for Adhesives

- They must have enough adhesion so that the chips will not fall off or move during the handling of the circuit board.
- They must maintain their adhesive strength when exposed to soldering temperatures.
- They should not spread or run when applied to the circuit board.
- They should have a long pot life.
- They should harden quickly.
- They should not corrode the circuit board or chip material.
- They should be a good insulator.
- They should be non-toxic, and not produce harmful gases, nor be harmful when touched.

3-2. Application Method

It is important to use the proper amount of adhesive. Too little will cause poor adhesion to the circuit board, and too much may strain the conductor pattern, thereby causing defective soldering. The following illustrations show the proper quantity of adhesive.



(Unit: mm)

Type	21	31
a	0.2 min	0.2 min
b	70~100μm	70~100μm
c	>0	>0

3-3. Adhesive Hardening Characteristics

To prevent oxidation of the terminations, the adhesive must harden at 160°C or less, within 2 minutes or less.

## Multilayer Ceramic Chip Capacitors

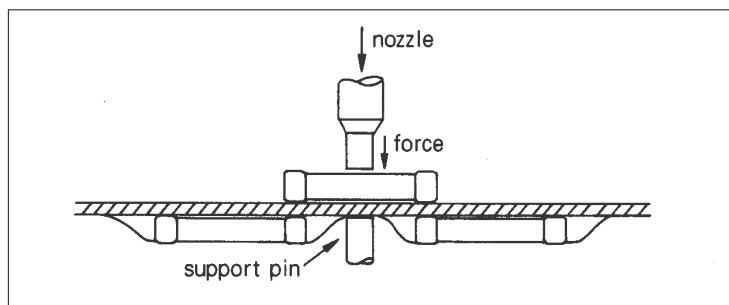
### 4. Mounting

#### 4-1. Mounting Head Pressure

Excessive pressure will cause chip capacitors to crack. The pressure between nozzle and chip capacitor will be 300g maximum during mounting.

#### 4-2. Bending Stress

Bending of printed circuit board by mounting head when double-sided circuit boards are used, chip capacitors first are mounted and soldered onto one side of the board. When the capacitors are mounted onto the other side, it is important to support the board as shown in the illustration. If the circuit board is not supported, it may bend, causing the already installed capacitors to crack.



### 5. Flux

Although highly activated flux gives better solderability, substances which increase activity may also degrade the insulation of the chip capacitors. To avoid such degradation, it is recommended that a mildly activated rosin flux (less than 0.2% chlorine) be used.

### 6. Soldering

Since a multilayer chip ceramic capacitor comes into direct contact with melted solder during soldering, it is exposed to potentially damaging mechanical stress caused by the sudden temperature change. The capacitor may also be subject to silver migration, and to contamination by the flux. Because of these factors, soldering technique is critical.

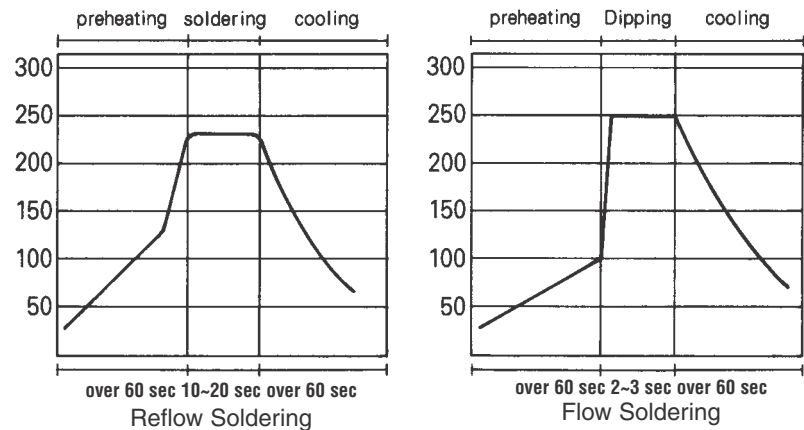
#### 6-1. Soldering Methods

Method	Classification	
Reflow Soldering	Mass reflow	<ul style="list-style-type: none"> <li>• IR/Convection</li> <li>• VPS (Vapor phase)</li> </ul>
	Selective reflow	<ul style="list-style-type: none"> <li>• Hot air/gas</li> <li>• Laser</li> </ul>
Flow Soldering	Dual Wave	

#### 6-2. Soldering Profile

To avoid the crack problem by sudden temperature change, follow the temperature profile in the adjacent graph.

Multilayer Ceramic Chip Capacitors



6-3. Manual Soldering

Manual Soldering can pose a great risk of creating thermal cracks in chip capacitors. The hot soldering iron tip comes into direct contact with the end terminations, and operator's carelessness may cause the tip of the soldering iron to come into direct contact with the ceramic body of the capacitor. Therefore the soldering iron must be handled carefully, and close attention must be paid to the selection of the soldering iron tip and to temperature control of the tip.

6-4. Amount of Solder

Too much solder		Cracks tend to occur due to large stress
Amount of solder is adequate		
Not enough solder		Weak holding force may cause bad connections or detaching of the capacitor

6-5. Cooling

Natural cooling using air is recommended. If the chips are dipped into solvent for cleaning, the temperature difference ( $\Delta T$ ) must be less than 100°C.

6-6. Cleaning

If rosin flux is used, cleaning usually is unnecessary. When strongly activated flux is used, chlorine in the flux may dissolve into some types of cleaning fluids, thereby affecting the chip capacitors. This means that the cleaning fluid must be carefully selected, and should always be new.

7. Notes for Separating Multiple, Shared PC Boards

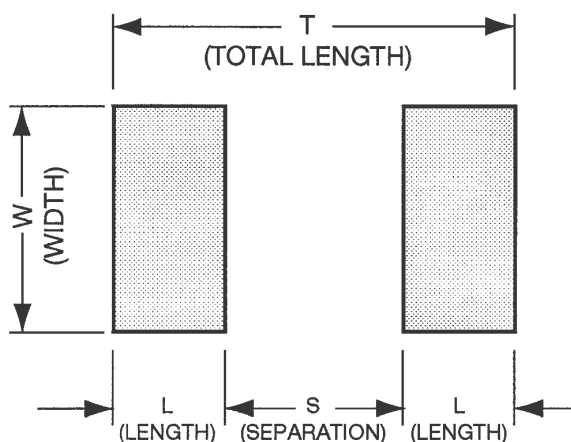
A multi-PC board is separated into many individual circuit boards after soldering has been completed. If the board is bent or distorted at the time of separation, cracks may occur in the chip capacitors. Carefully choose a separation method that minimizes the bending of the circuit board.

#### APPLICATION INFORMATION ON SOLDER PAD DESIGN FOR SURFACE MOUNT CHIP CAPACITOR

#### Recommended Pad Dimensions

Chip Size	Dimensions (inches)			
	L	W	S	T
0402*	0.021	0.022	0.017	0.059
0603*	0.035	0.030	0.030	0.100
0805	0.040	0.050	0.040	0.120
1206	0.040	0.065	0.080	0.160
1210	0.040	0.100	0.080	0.160
1812*	0.050	0.120	0.130	0.230
1825*	0.050	0.250	0.130	0.230
2220	0.050	0.250	0.130	0.230
2225*	0.050	0.250	0.170	0.270
3640*	0.060	0.400	0.300	0.420

\*These sizes are recommended for use with IR and vapor phase soldering only.



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