Low Inductance Capacitors

Introduction

As switching speeds increase and pulse rise times decrease the need to reduce inductance becomes a serious limitation for improved system performance. Even the decoupling capacitors, that act as a local energy source, can generate unacceptable voltage spikes: V = L (di/dt). Thus, in high speed circuits, where di/dt can be quite large, the size of the voltage spike can only be reduced by reducing L.

Figure 1 displays the evolution of ceramic capacitor toward lower inductance designs over the last few years. AVX has been at the forefront in the design and manufacture of these newer more effective capacitors.

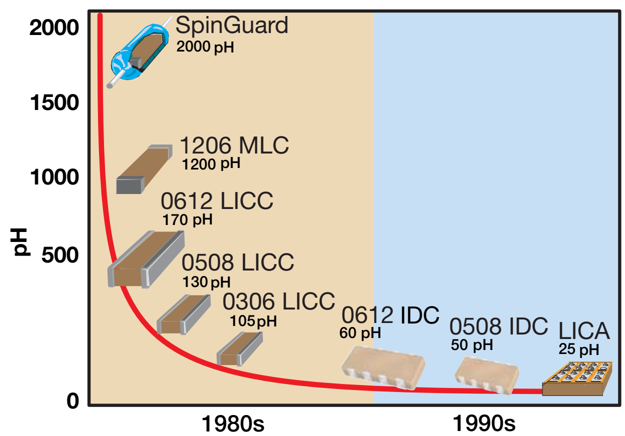


Figure 1. The evolution of Low Inductance Capacitors at AVX (values given for a 100 nF capacitor of each style)

LOW INDUCTANCE CHIP CAPACITORS

The total inductance of a chip capacitor is determined both by its length to width ratio and by the mutual inductance coupling between its electrodes. Thus a 1210 chip size has lower inductance than a 1206 chip. This design improvement is the basis of AVX's low inductance chip capacitors, LI Caps, where the electrodes are terminated on the long side of the chip instead of the short side. The 1206 becomes an 0612 as demonstrated in Figure 2. In the same manner, an 0805 becomes an 0508 and 0603 becomes an 0306. This results in a reduction in inductance from around 1200 pH for conventional MLC chips to below 200 pH for Low Inductance Chip Capacitors. Standard designs and performance of these LI Caps are given on pages 55 and 56.

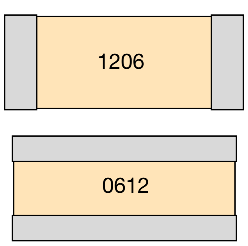
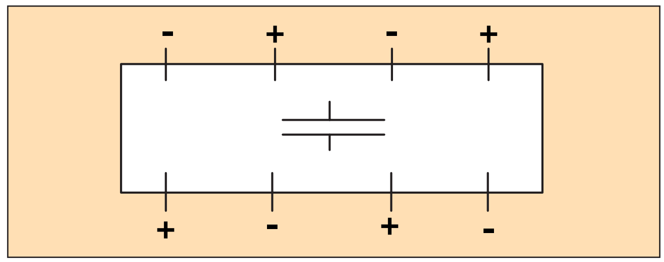


Figure 2. Change in aspect ratio: 1206 vs. 0612

INTERDIGITATED CAPACITORS

Multiple terminations of a capacitor will also help in reducing the parasitic inductance of the device. The IDC is such a device. By terminating one capacitor with 8 connections the ESL can be reduced even further. The measured inductance of the 0612 IDC is 60 pH, while the 0508 comes in around 50 pH. These FR4 mountable devices allow for even higher clock speeds in a digital decoupling scheme. Design and product offerings are shown on pages 59 and 60.



LOW INDUCTANCE CHIP ARRAYS (LICA®)

Further reduction in inductance can be achieved by designing alternative current paths to minimize the mutual inductance factor of the electrodes (Figure 3). This is achieved by AVX's LICA® product which was the result of a joint development between AVX and IBM. As shown in Figure 4, the charging current flowing out of the positive plate returns in the opposite direction along adjacent negative plates. This minimizes the mutual inductance.

The very low inductance of the LICA capacitor stems from the short aspect ratio of the electrodes, the arrangement of the tabs so as to cancel inductance, and the vertical aspect of the electrodes to the mounting surface.

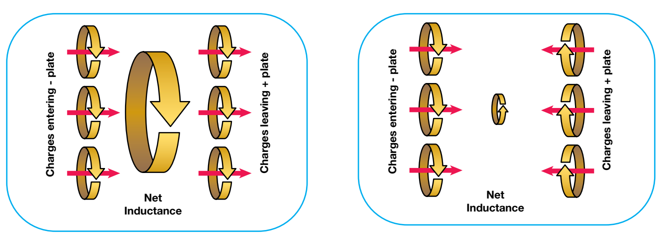


Figure 3. Net Inductance from design. In the standard Multilayer capacitor, the charge currents entering and leaving the capacitor create complementary flux fields, so the net inductance is greater. On the right, however, if the design permits the currents to be opposed, there is a net cancellation, and the inductance is much lower.

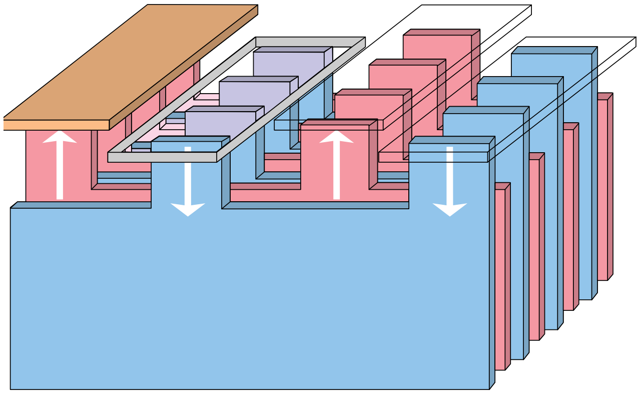


Figure 4. LICA's Electrode/Termination Construction. The current path is minimized – this reduces self-inductance. Current flowing out of the positive plate, returns in the opposite direction along the adjacent negative plate – this reduces the mutual inductance.

Also the effective current path length is minimized because the current does not have to travel the entire length of both electrodes to complete the circuit. This reduces the self inductance of the electrodes. The self inductance is also minimized by the fact that the charging current is supplied by both sets of terminals reducing the path length even further!

The inductance of this arrangement is less than 30 pH, causing the self-resonance to be above 100 MHz for the same popular 100 nF capacitance. Parts available in the LICA design are shown on pages 60 and 61.

Figure 5 compares the self resonant frequencies of various capacitor designs versus capacitance values. The approximate inductance of each style is also shown.

Active development continues on low inductance capacitors. C4 termination with low temperature solder is now available for plastic packages. Consult AVX for details.

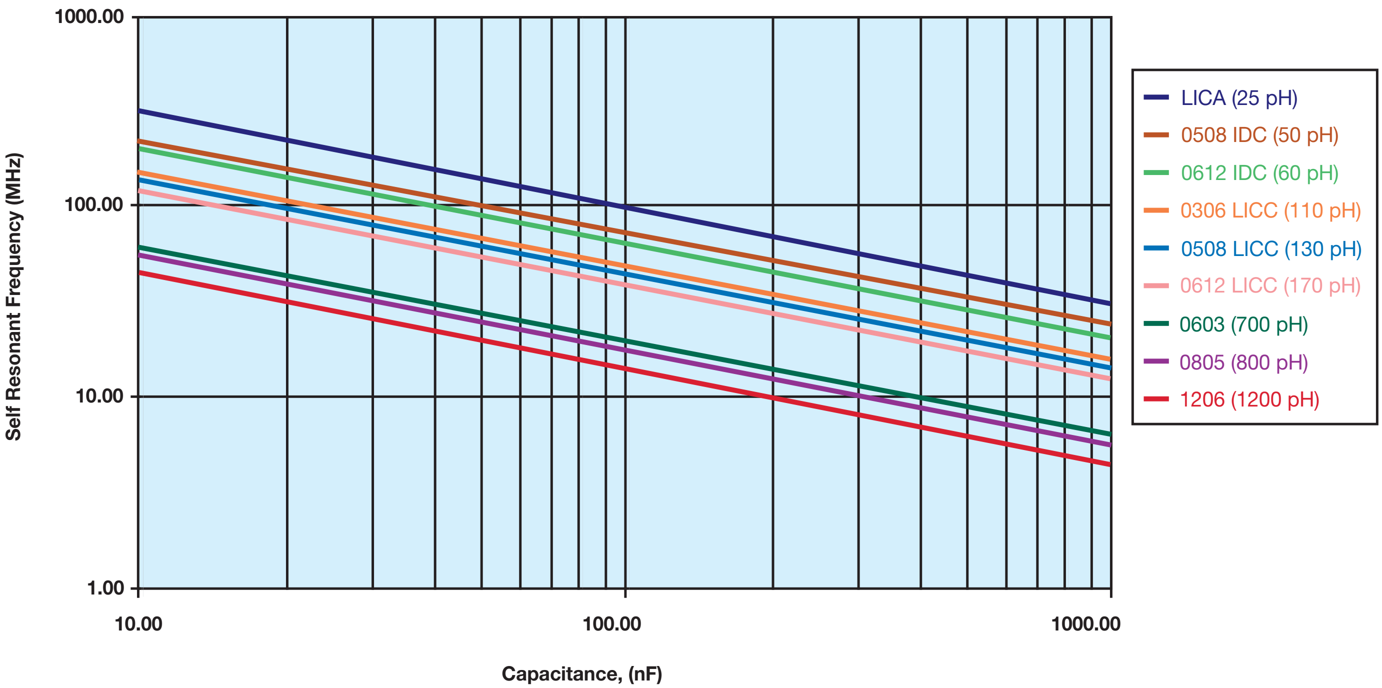


Figure 5. Self Resonant Frequency vs. Capacitance and Capacitor Design

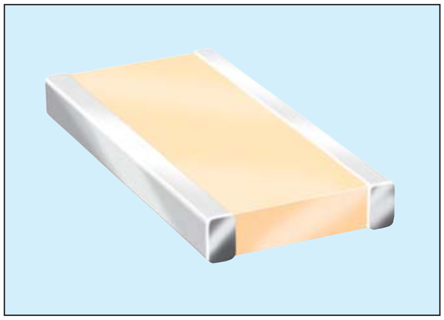
Low Inductance Capacitors (RoHS)

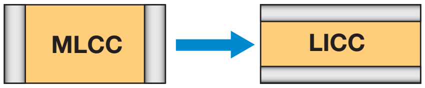
0612/0508/0306 LICC (Low Inductance Chip Capacitors)

GENERAL DESCRIPTION

The total inductance of a chip capacitor is determined both by its length to width ratio and by the mutual inductance coupling between its electrodes.

Thus a 1210 chip size has a lower inductance than a 1206 chip. This design improvement is the basis of AVX's Low Inductance Chip Capacitors (LICC), where the electrodes are terminated on the long side of the chip instead of the short side. The 1206 becomes an 0612, in the same manner, an 0805 becomes an 0508, an 0603 becomes an 0306. This results in a reduction in inductance from the 1nH range found in normal chip capacitors to less than 0.2nH for LICCs. Their low profile is also ideal for surface mounting (both on the PCB and on IC package) or inside cavity mounting on the IC itself.





HOW TO ORDER

0612	Z	D	105	M	A	T	2	A*
Size	**Voltage**	**Dielectric**	**Capacitance Code (In pF)**	**Capacitance Tolerance**	**Failure Rate**	**Terminations**	**Packaging**	**Thickness**
0306 0508 0612	6 = 6.3V Z = 10V Y = 16V 3 = 25V 5 = 50V	C = X7R D = X5R	2 Sig. Digits + Number of Zeros	K = ±10% M = ±20%	A = N/A	T = Plated Ni and Sn	Available 2 = 7" Reel 4 = 13" Reel	Thickness mm (in) 0.56 (0.022) 0.61 (0.024) 0.76 (0.030) 1.02 (0.040) 1.27 (0.050)

NOTE: Contact factory for availability of Termination and Tolerance Options for Specific Part Numbers.

PERFORMANCE CHARACTERISTICS

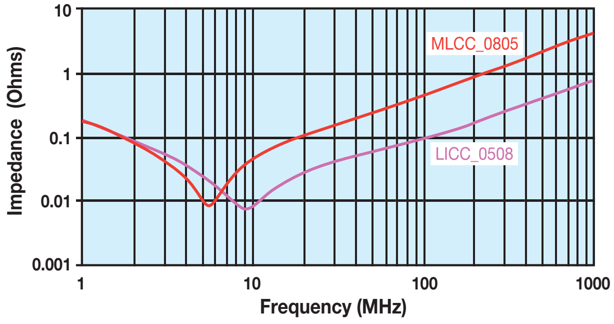
Capacitance Tolerances	K = ±10%; M = ±20%
Operation Temperature Range	X7R = -55°C to +125°C; X5R = -55°C to +85°C
Temperature Coefficient	±15% (0VDC)
Voltage Ratings	6.3, 10, 16, 25 VDC
Dissipation Factor	6.3V = 6.5% max; 10V = 5.0% max; 16V = 3.5% max; 25V = 3.0% max
Insulation Resistance (@+25°C, RVDC)	100,000MΩ min, or 1,000MΩ per µF min.,whichever is less

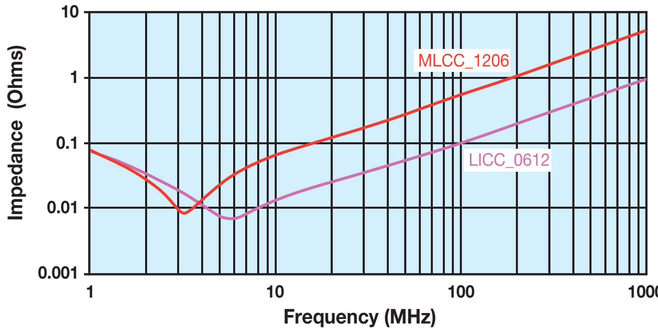
TYPICAL INDUCTANCE

Package Style	Measured Inductance (pH)
1206 MLCC	1200
0612 LICC	**170**
0508 LICC	**130**
0306 LICC	**105**

*Note: See Range Chart for Codes

TYPICAL IMPEDANCE CHARACTERISTICS





Low Inductance Capacitors (RoHS)

0612/0508/0306 LICC (Low Inductance Chip Capacitors)

SIZE	0306					0508					0612				
Packaging	Embossed					Embossed					Embossed				
Length MM (in.)	0.81 ± 0.15 (0.032 ± 0.006)					1.27 ± 0.25 (0.050 ± 0.010)					1.60 ± 0.25 (0.063 ± 0.010)				
Width MM (in.)	1.60 ± 0.15 (0.063 ± 0.006)					2.00 ± 0.25 (0.080 ± 0.010)					3.20 ± 0.25 (0.126 ± 0.010)				
WVDC	6.3	10	16	25	50	6.3	10	16	25	50	6.3	10	16	25	50
CAP (μF) 0.001	A	A	A	A		S	S	S	S	V	S	S	S	S	V
0.0022	A	A	A	A		S	S	S	S	V	S	S	S	S	V
0.0047	A	A	A	A		S	S	S	S	V	S	S	S	S	V
0.010	A	A	A	A		S	S	S	S	V	S	S	S	S	V
0.015	A	A	A	A		S	S	S	S	V	S	S	S	S	W
0.022	A	A	A	A		S	S	S	S	V	S	S	S	S	W
0.047	A	A	A			S	S	S	V	A	S	S	S	S	W
0.068	A	A	A			S	S	S	A	A	S	S	S	V	W
0.10	A	A	A (X5R)			S	S	V	A	A	S	S	S	V	W
0.15	A	A				S	S	V			S	S	S	W	W
0.22	A	A				S	S	A			S	S	V	W	
0.47						V	V	A (X5R)			S	S	V		
0.68						A	A				V	V	W		
1.0						A	A				V	V	A		
1.5						A (X5R)					W	W			
2.2											A	A			
3.3											A (X5R)				
4.7															
10															

Solid = X7R   (hatched) **= X5R**

mm (in.)

0306	
Code	Thickness
A	0.61 (0.024)

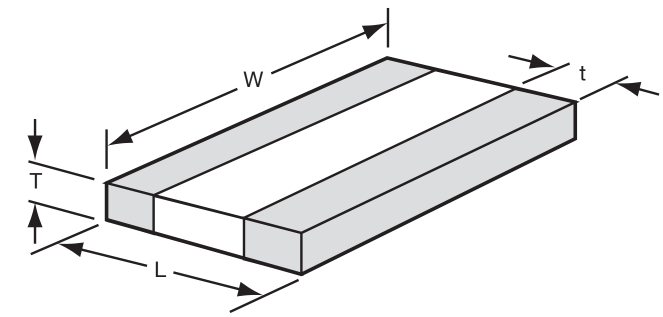
mm (in.)

0508	
Code	Thickness
S	0.56 (0.022)
V	0.76 (0.030)
A	1.02 (0.040)

mm (in.)

0612	
Code	Thickness
S	0.56 (0.022)
V	0.76 (0.030)
W	1.02 (0.040)
A	1.27 (0.050)

PHYSICAL DIMENSIONS AND PAD LAYOUT



PHYSICAL CHIP DIMENSIONS

mm (in)

	L	W	t
0612	1.60 ± 0.25 (0.063 ± 0.010)	3.20 ± 0.25 (0.126 ± 0.010)	0.13 min. (0.005 min.)
0508	1.27 ± 0.25 (0.050 ± 0.010)	2.00 ± 0.25 (0.080 ± 0.010)	0.13 min. (0.005 min.)
0306	0.81 ± 0.15 (0.032 ± 0.006)	1.60 ± 0.15 (0.063 ± 0.006)	0.13 min. (0.005 min.)

T - See Range Chart for Thickness and Codes

PAD LAYOUT DIMENSIONS

mm (in)

	A	B	C
0612	0.76 (0.030)	3.05 (0.120)	.635 (0.025)
0508	0.51 (0.020)	2.03 (0.080)	0.51 (0.020)
0306	0.31 (0.012)	1.52 (0.060)	0.51 (0.020)