Digital IC Design

Session 5: Gate Level Modeling 2(Complex Design: Lab and Assignment)

2024 | Nineplus Infotech X Anseong Polytechnic University
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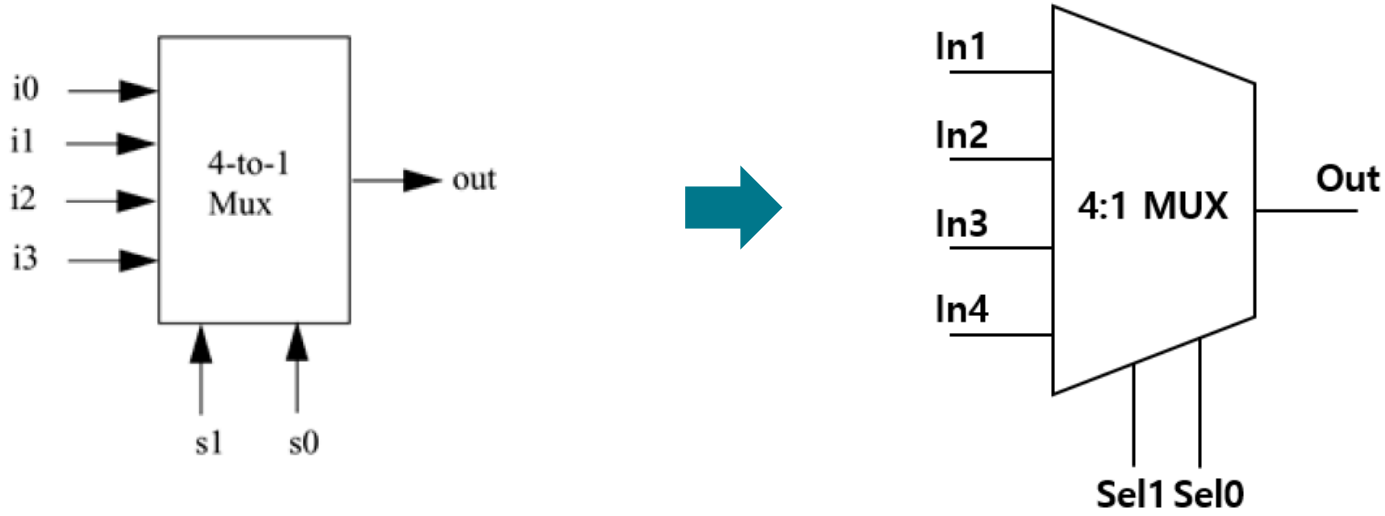
cadence

LAB

- Do a 4X1 selector(multiplexer) using gate level modeling
- Verify the DUT with testbench.
- Think about the problem concerning such modeling.

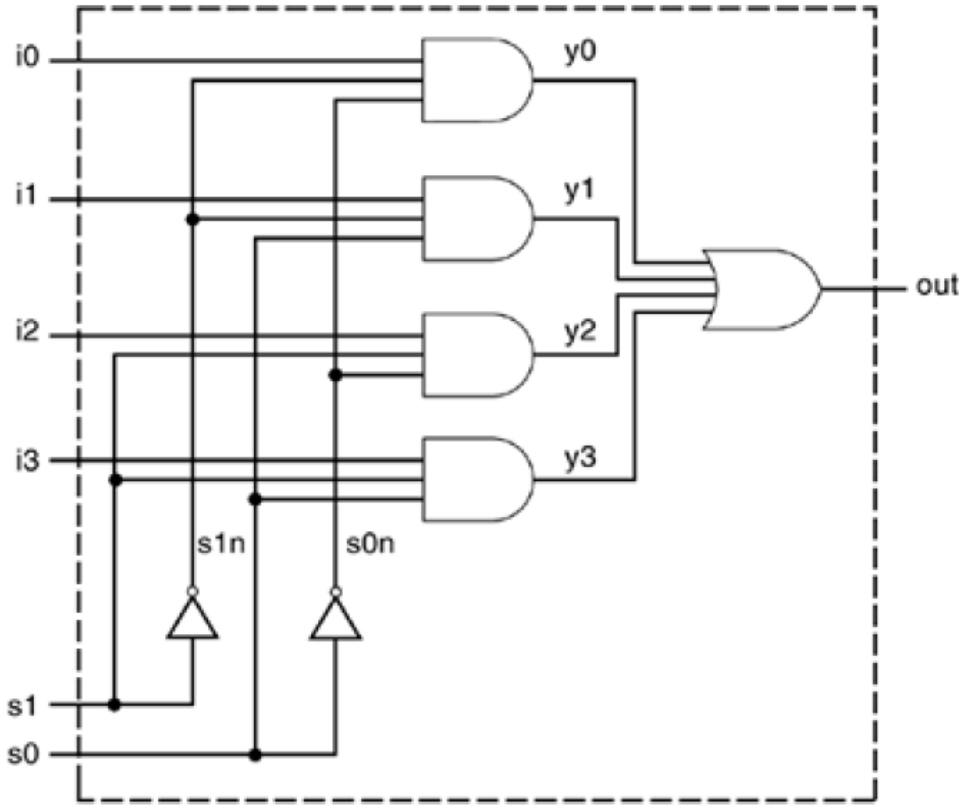
1. Logic Symbol



2. Truth Table

s1	s0	i0	i1	i2	i3	out
0	0	0				0
0	0	1				1
0	1		0			0
0	1		1			1
1	0			0		0
1	0			1		1
1	1				0	0
1	1				1	1

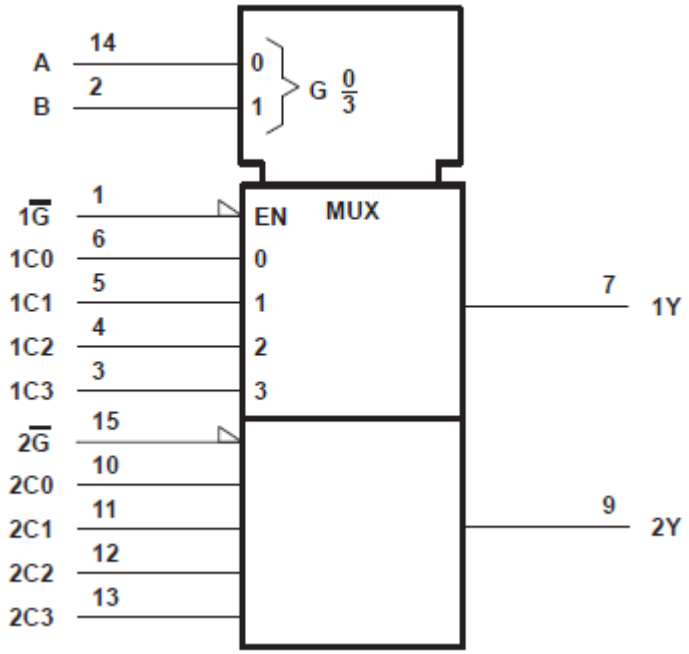
3. Implemented Logic Diagram



Assignment

- Do the same thing with “sn54als153” referring to the data sheet

1. Logic Symbol



2. Truth Table

FUNCTION TABLE

INPUTS						STROBE $\overline{G}$	OUTPUT Y
SELECT		DATA					
B	A	C0	C1	C2	C3		
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.

3. Implemented Logic Diagram

logic diagram (positive logic)