# Digital IC Design

## Week1: Brief History of Semiconductor Fabrication and Process of Semi Custom IC

2024 | Nineplus Infotech X Anseong Polytechnic University
*Sr Research Engineer, William Woo*

cadence

# 1. Intro

# 강사소개

*우승안 (William Woo)*

- Senior Research Engineer: Semi Custom Design
- BA, Sungkunkwan University
- MA, Incheon University: Accelerator Design / CUDA Architecture
- Nineplus Infotech Inc.
- Interest: OOP Design(C++), Firmware Control, Linux System

- https://github.com/codefoolosopher/Digital_Design
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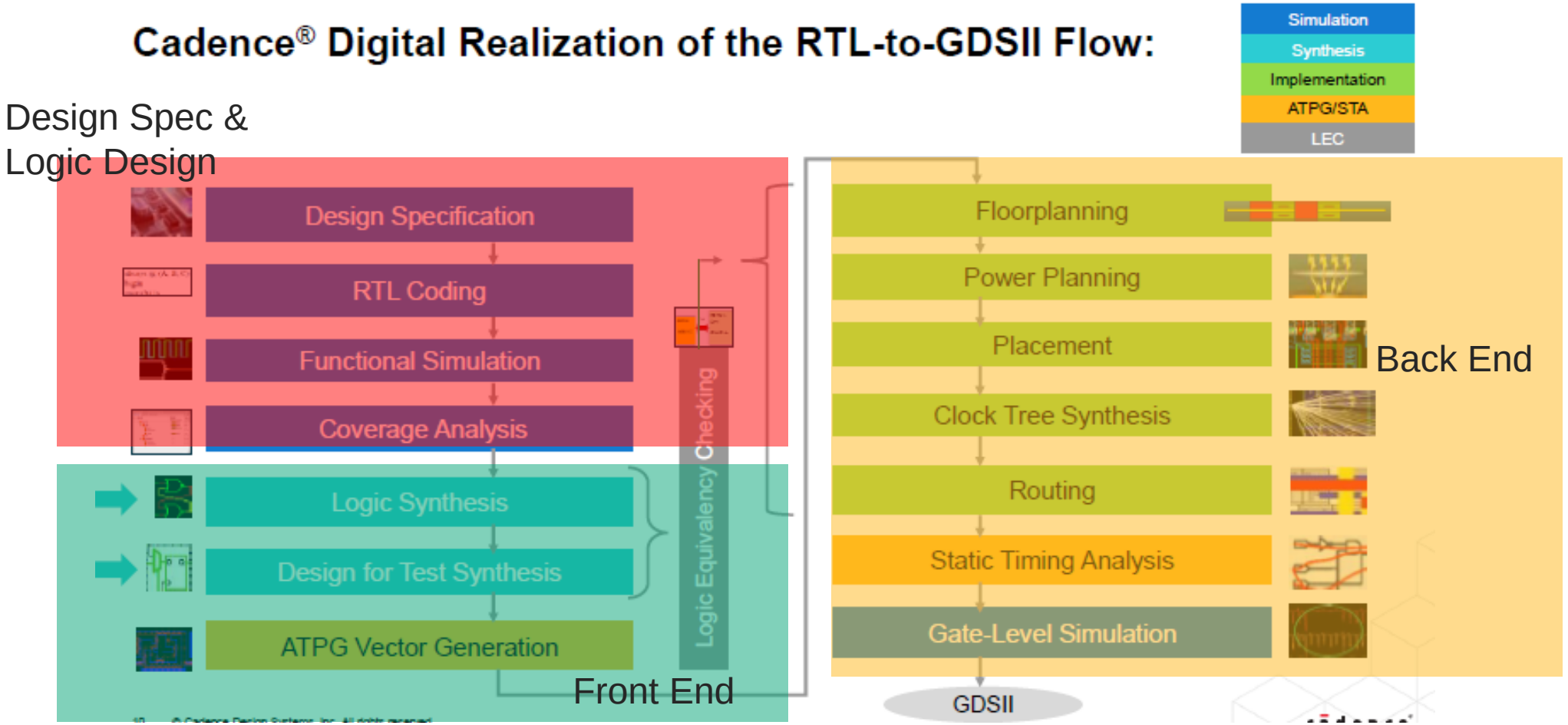
- Office Hour: (Thu.) 15:00 ~ 18:00 / (Fri.) 16:00 ~ 18:00

# 강의소개: Digital IC Design

*What is Digital IC?*

# 강의소개: Digital Realization of the RTL-to-GDSII Flow



# 강의소개: Course Overview

- 본 과목은 NCS 교과임
- 강의는 Semi Custom Design 기준으로 Cadence Solution 활용하여 진행
- 각 수업마다 Lecture + LAB으로 구성
- 교재
  - 강의: 자체 교재(강의안) 및 LAB 제공
  - Self Study: “Verilog HDL 설계”(신경욱, 한빛아카데미)
- 평가는 총 3회
  - 1회차(10%): 이론
  - 2회차(20%): 이론 + 실습(Design)
  - 3회차(40%): 실습(Design + Front End Flow)
- 학습 능력과 진도에 따라 (온라인) 보강이 있을 수 있음
- Office Hour시간: 상담 및 개별 보충

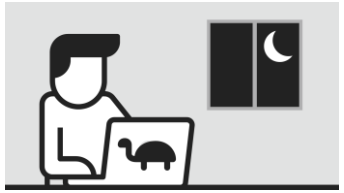
# THINK

## Self Checking

# Roadmap for Your Success

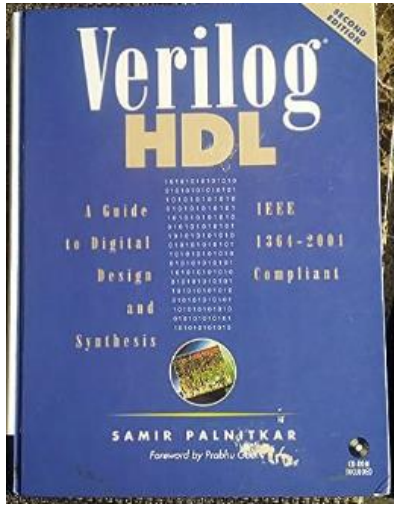
C Programming → Signals and Systems → Logic Circuit

**Digital System Design with HDL** → Computer Architecture → Embedded Processor(Firmware)

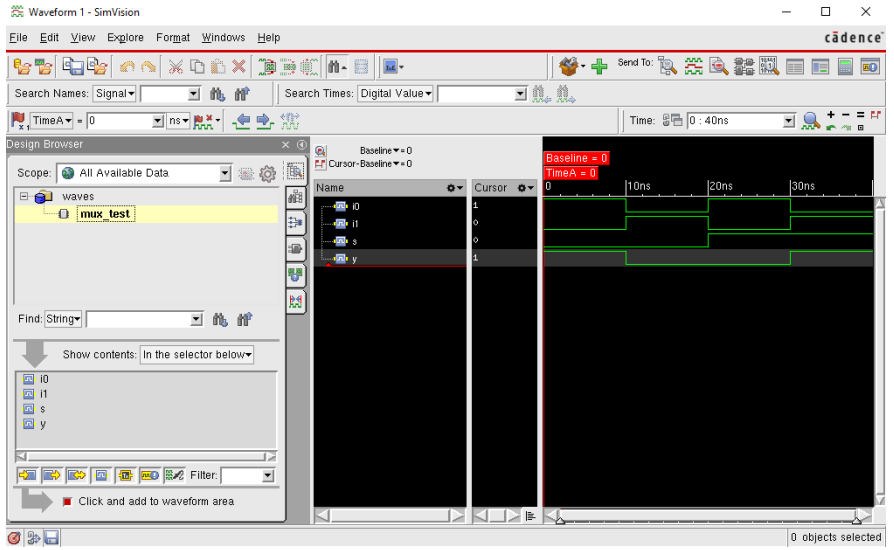


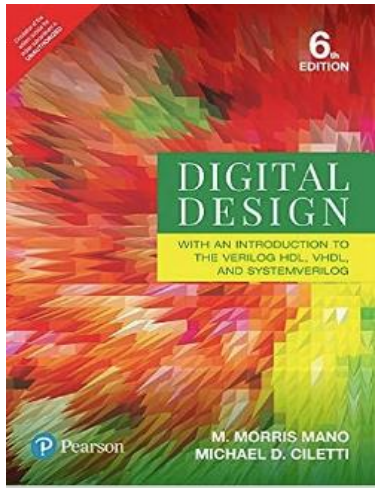
Network | Vision | AI algorithm… → VLSI | SoC Design → System Verilog | UVM

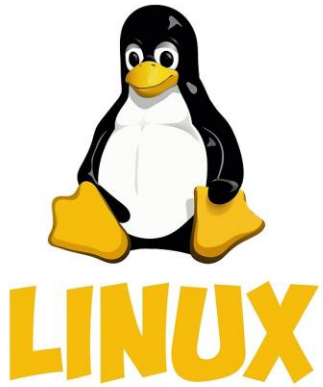
# Study Guide for Beginner

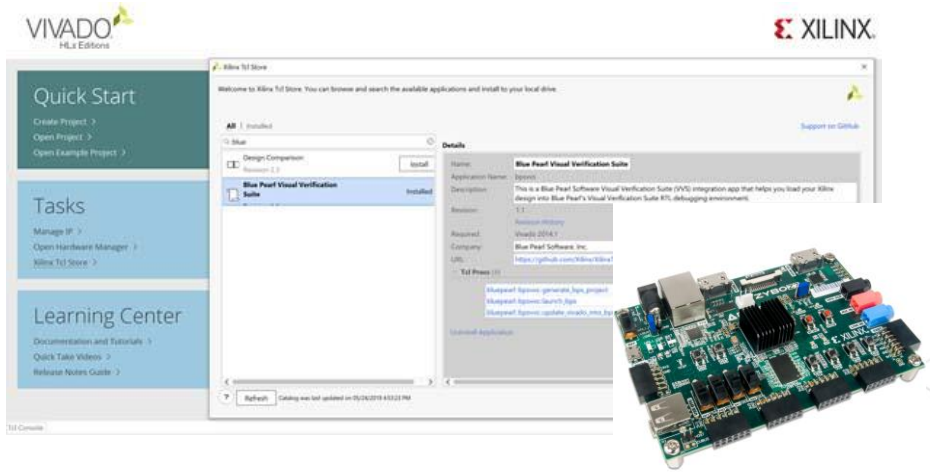






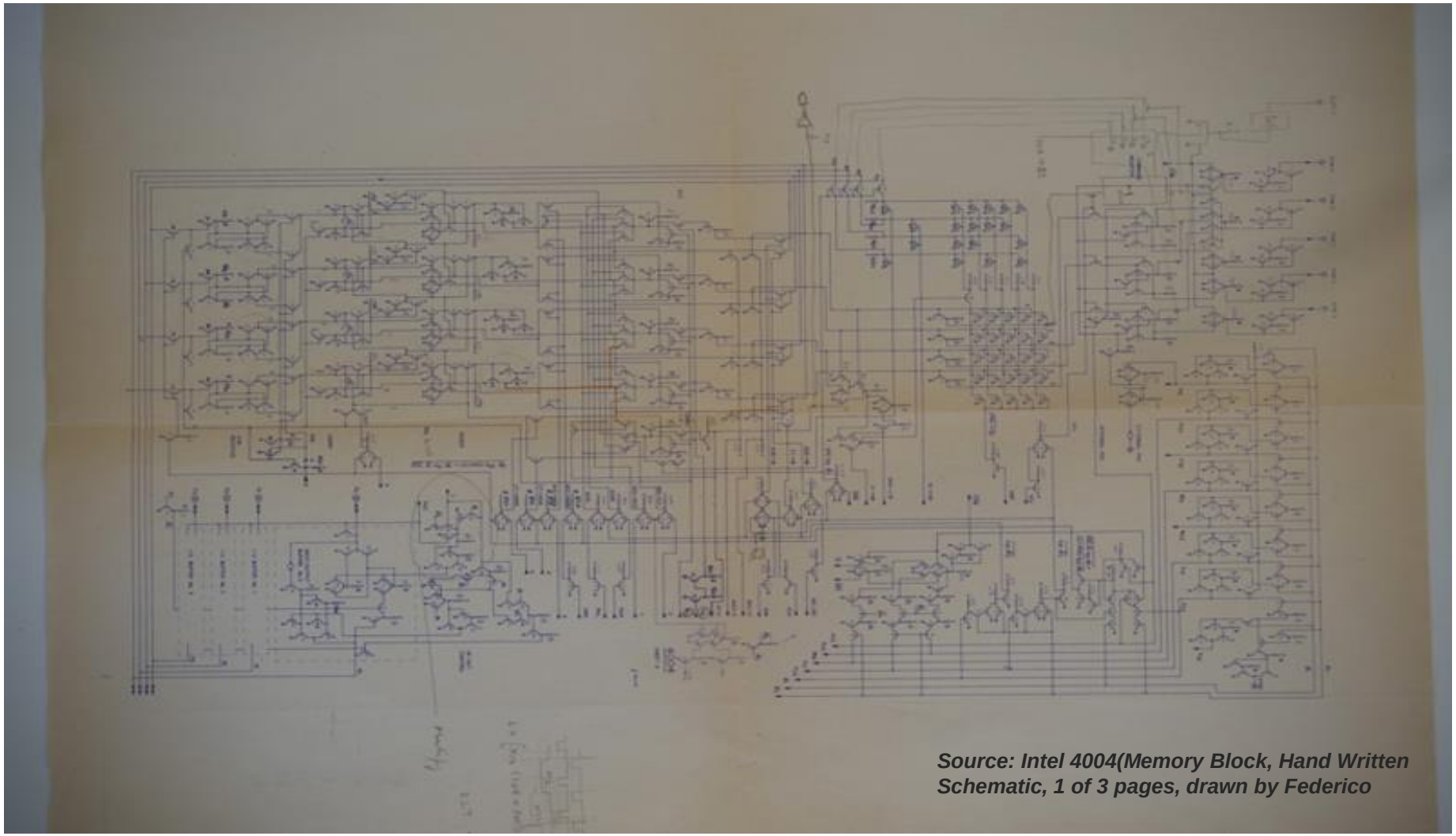



# 2. History of IC Development and HDL Emerging

# THINK

Why on earth does we need
Hardware Descriptive Language?

# Old Schematic & Design Methodology: Intel 4004

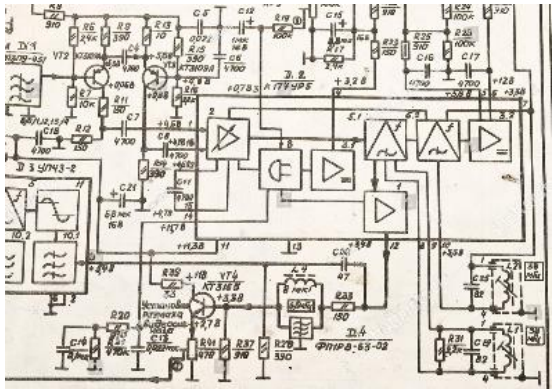


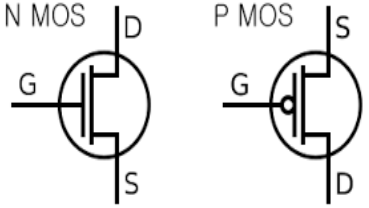
*Source: Intel 4004(Memory Block, Hand Written Schematic, 1 of 3 pages, drawn by Federico*

# THINK

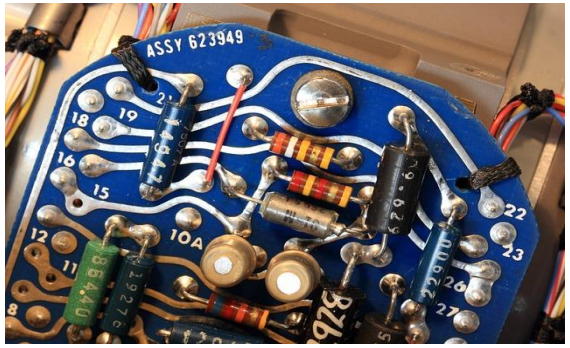
사람들은 어떻게 하드웨어를
만들어 왔을까?

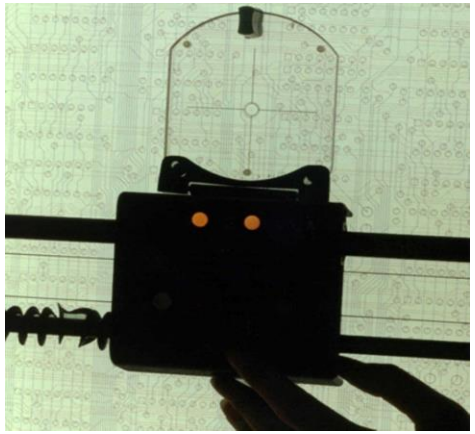
# Development of Circuit Design Concept






1966, IBM360/37 mainframe-powered CAD at Fairchild

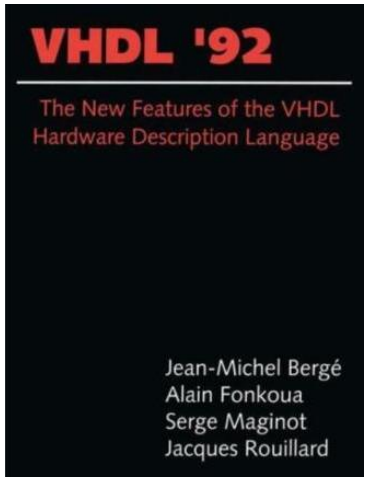


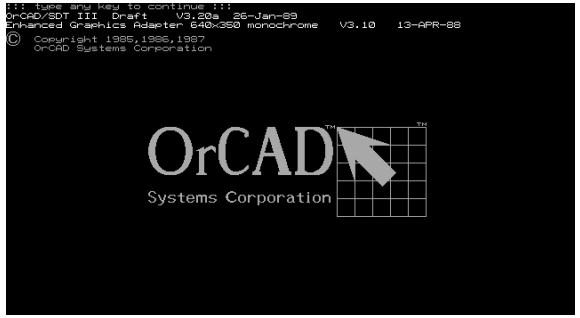



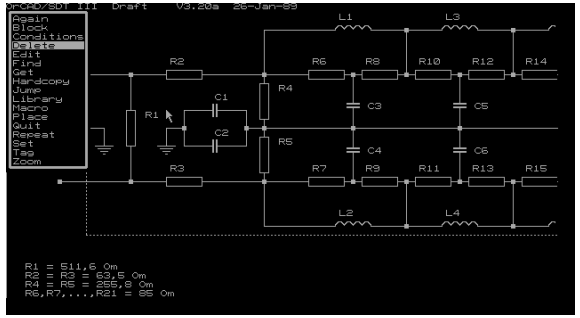
Mask layout drawing hand digitizing system at Intel

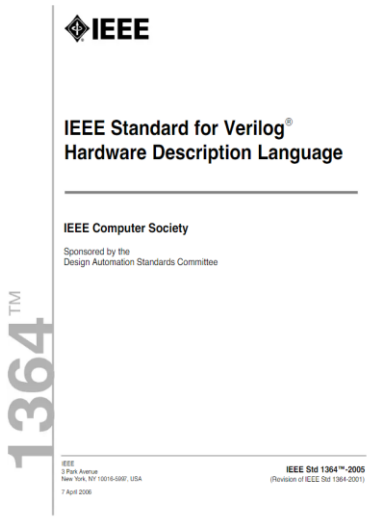
*Source: National Instrument | pixabay | Wikipedia | Computer History Museum*

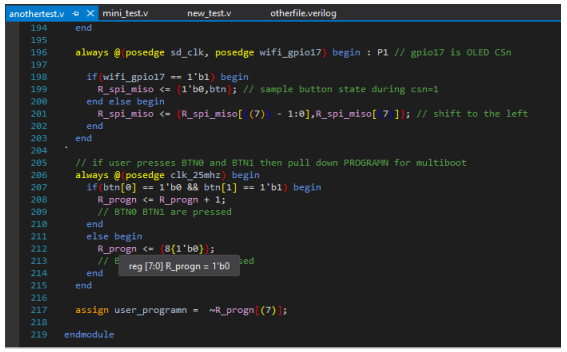
# Development of Circuit Design Concept

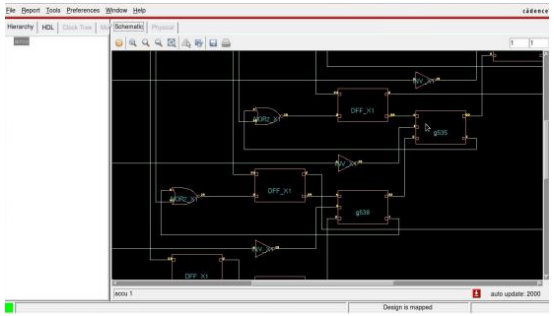


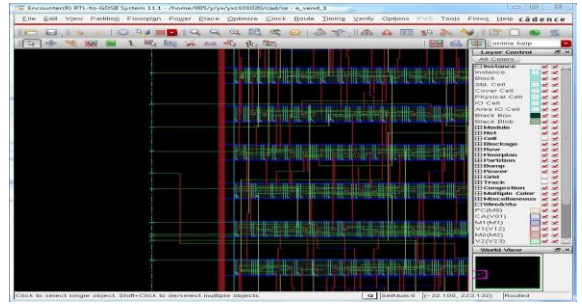



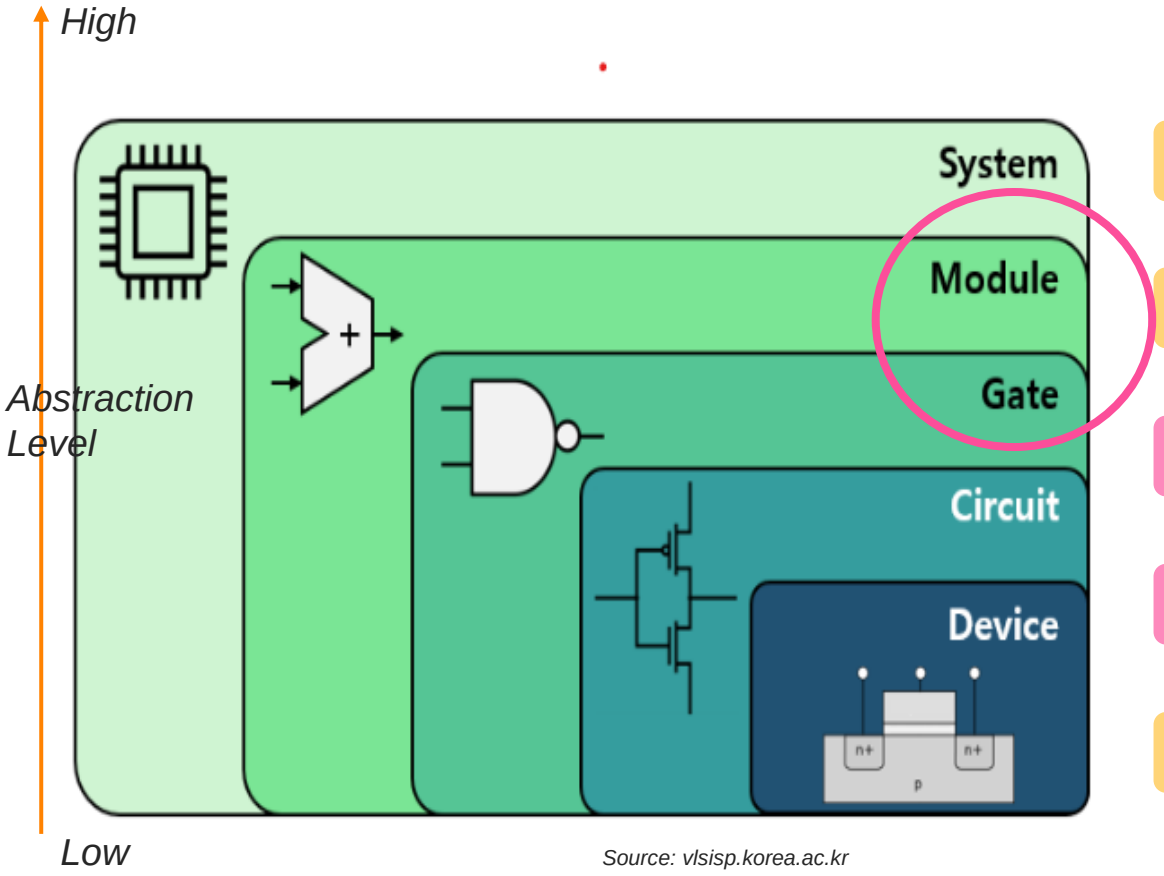






# Diverse viewpoint to scrutinize chip designs




Source: vlsisp.korea.ac.kr

**Device Level**

- 소자의 설계

**Circuit Level**

- TR기반의 회로설계

**Gate Level**

- Logic Gate기반의 회로설계

**RTL(Module) Level**

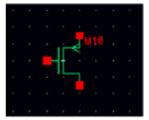
- 레지스터간 데이터 흐름 / 논리 연산 모델링 기반 회로설계

**System Level**

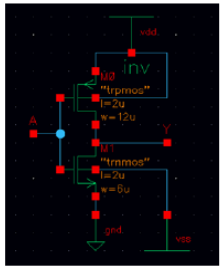
- 시스템 모듈 및 인터페이스를 통한 전체 시스템 설계

# How to realize semiconductor chip? | Full Custom

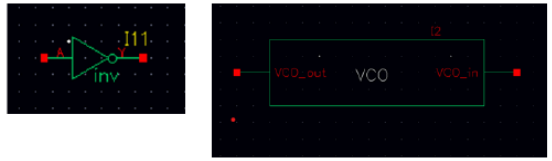
- Full Custom IC
  - Circuit 수준에서 설계 진행
  - Transistor / Resistor / Capacitor 기반



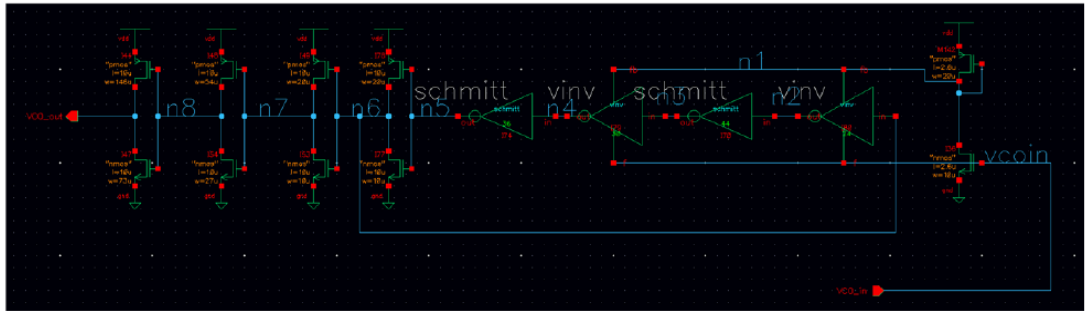
Primitive



Schematic using primitives

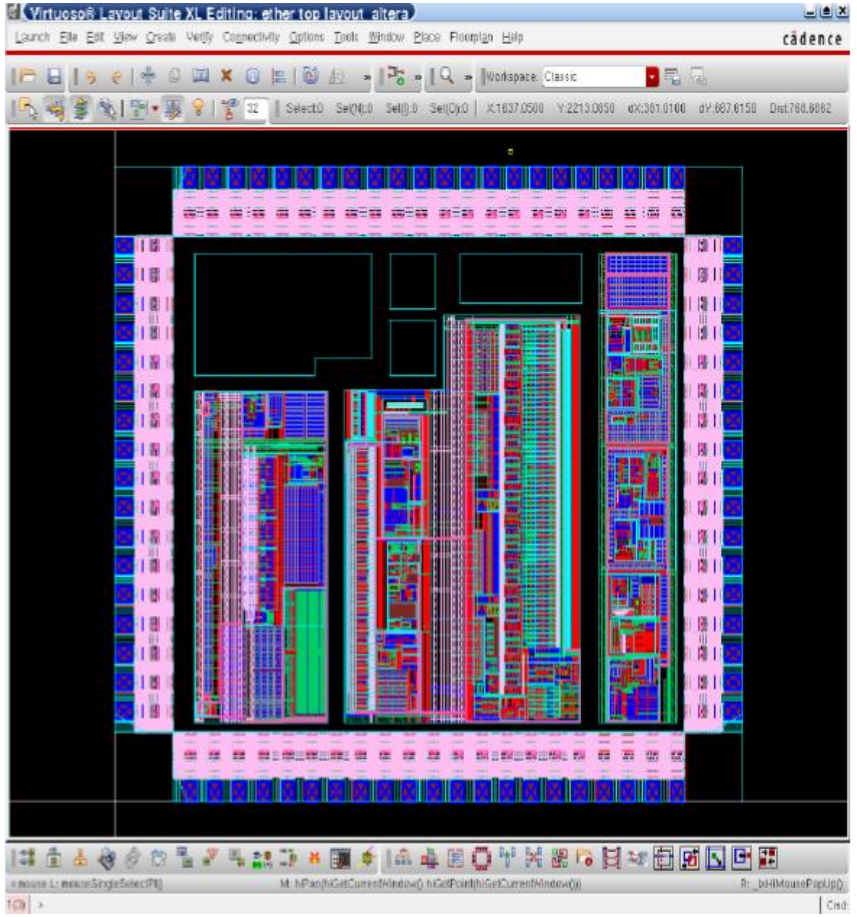


Symbols for inv and vco




Vco schematic using primitives and hierarchical symbols

Logic Design

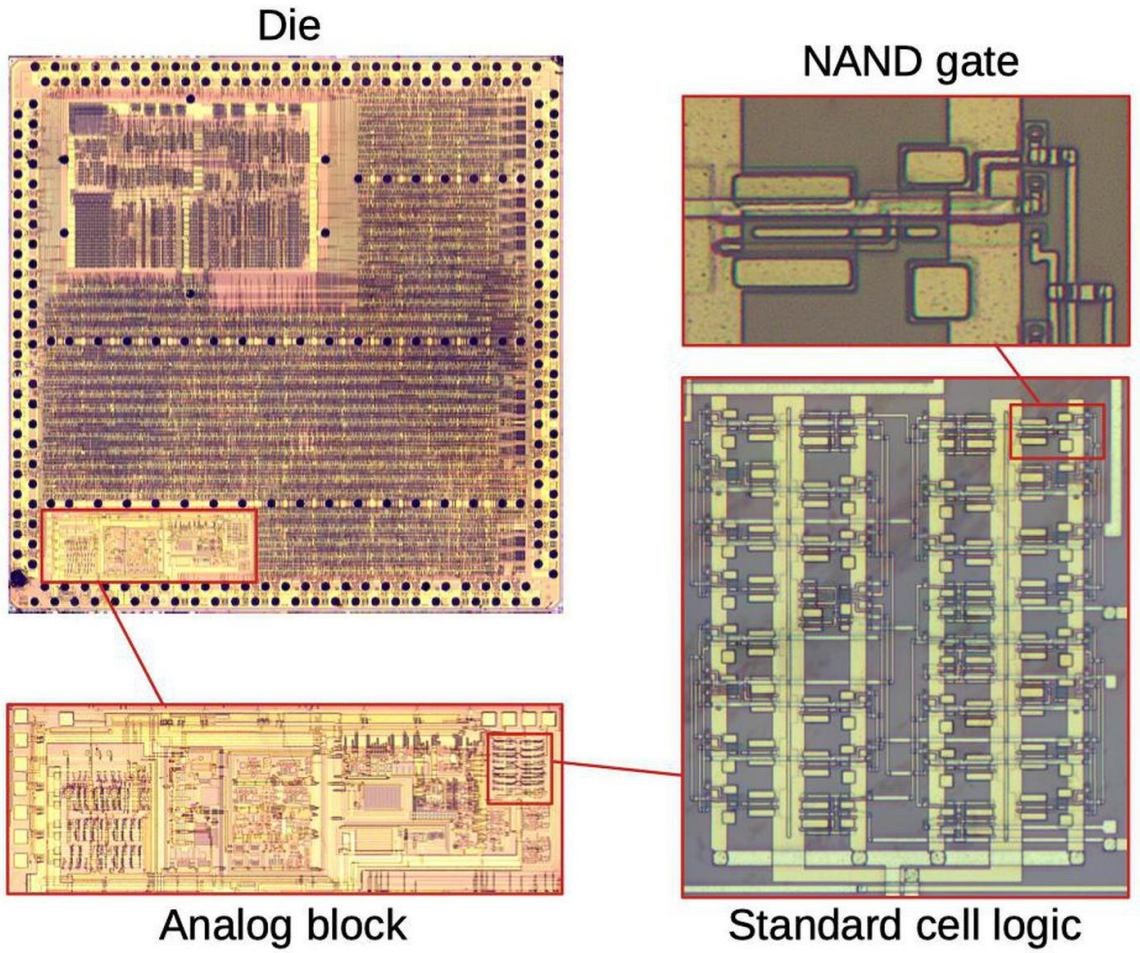



Physical Implementation: Layout

# How to realize semiconductor chip? | **Semi Custom IC**

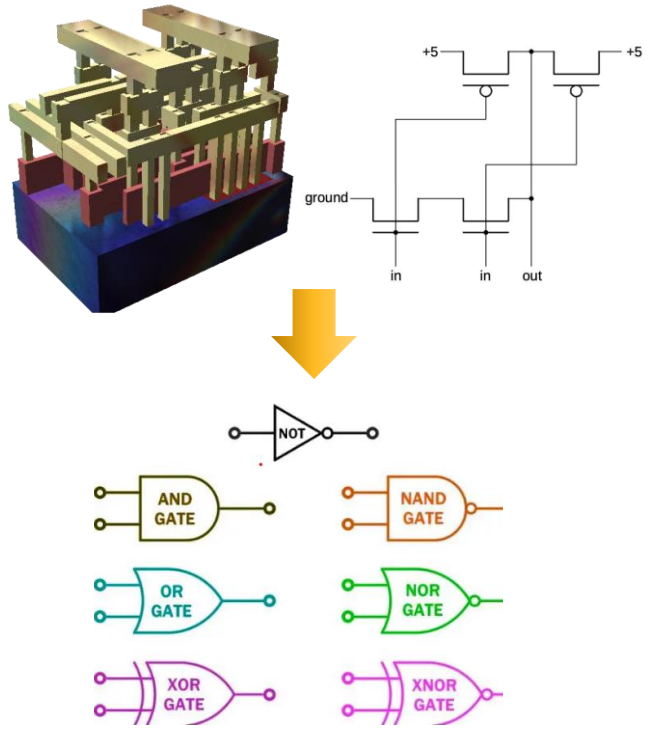
- Semi Custom IC
  - Gate Level 수준에서 설계 진행
  - Standard Cell 기반

* Standard Cell: 미리 만들어 놓은 논리 게이트 소자

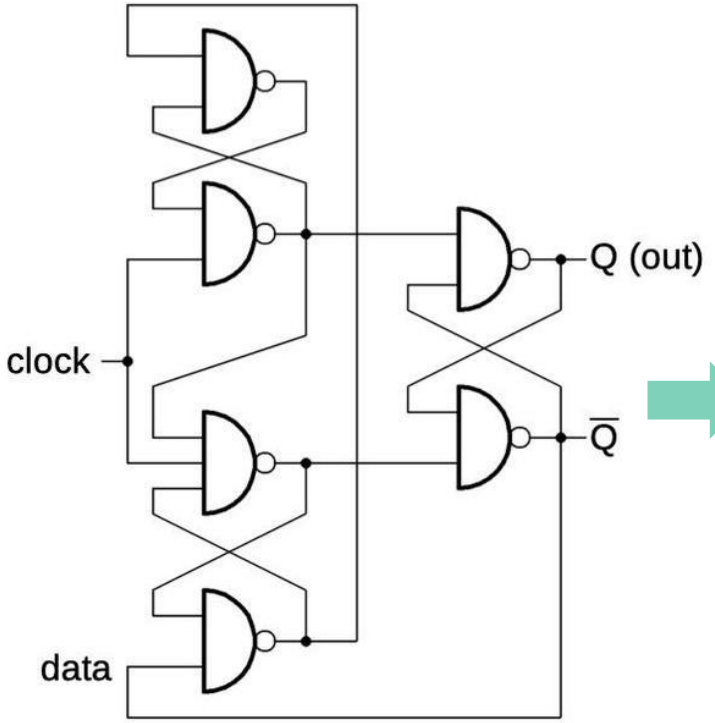



*Source: IBM*

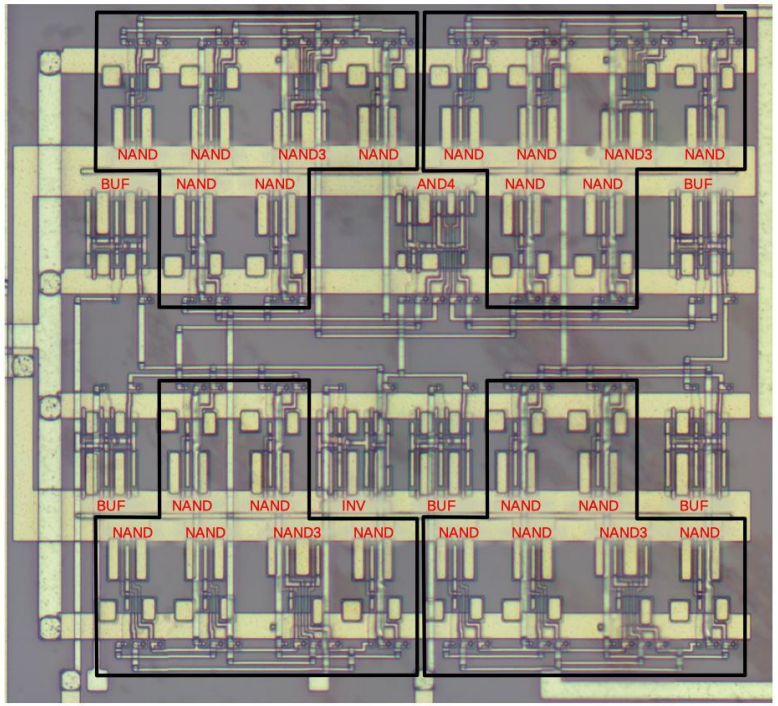
# How to realize semiconductor chip? | **Semi Custom IC**




Standard Cell Library




Logic HW Design




Implementation: Place & Route

# How to realize semiconductor chip? | **FPGA**

- FPGA(Field Programmable Gate Array)
  - Gate Level 수준에서 설계 진행
  - Standard Cell이 미리 구현되어 있음

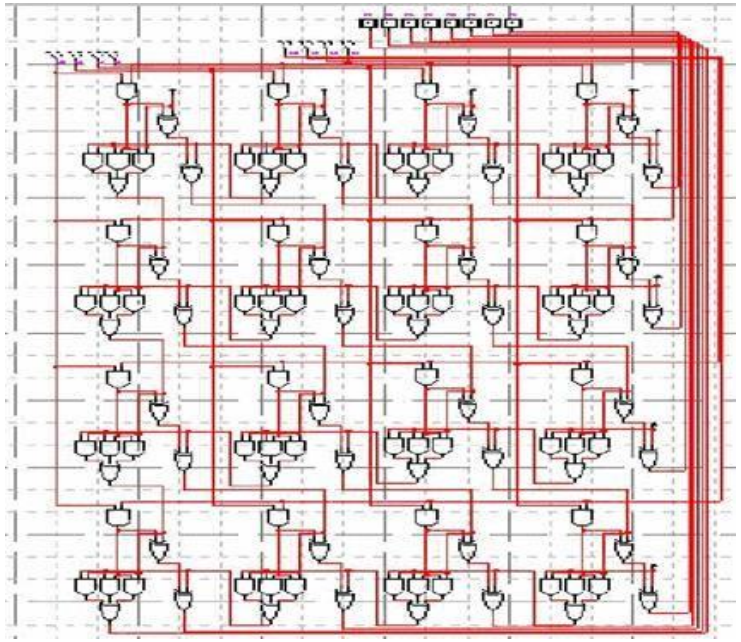
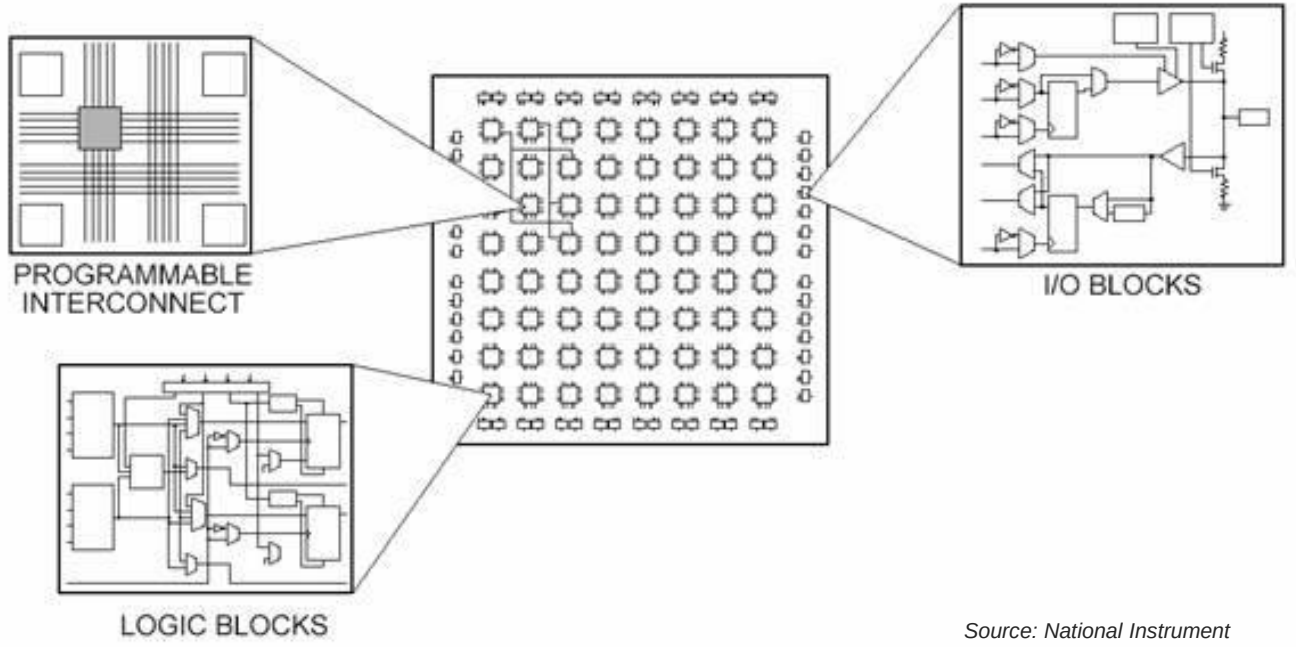
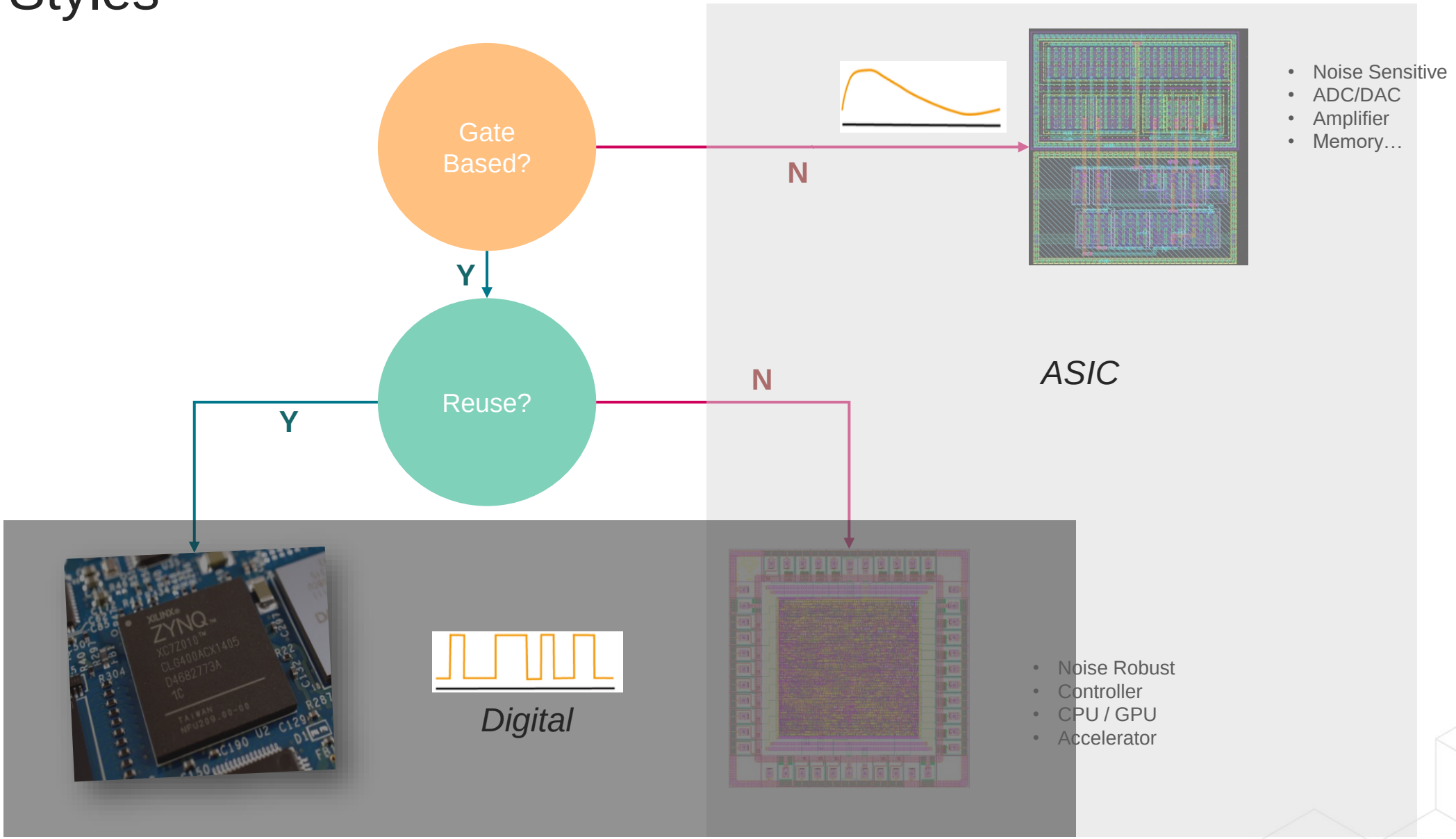


Fig. 4 X 4 multiplexer schematic




*Source: National Instrument*

# Design Styles



# ASIC | FPGA



https://wordcloud.kr/

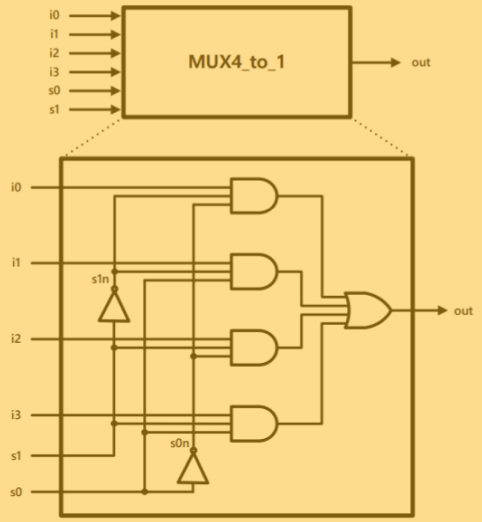
# Semi Custom Design Process

HDL

```
module mux4_to_1
(out, i0, i1, i2, i3, s1, s0);

output wire out;
input wire i0, i1, i2, i3;
input wire s0, s1;

assign out = (~s1 & ~s0 & i0) | (~s1 & s0 & i1) |
             (s1 & ~s0 & i2) | (s1 & s0 & i3);

endmodule
```

Design Concept & Logic Design

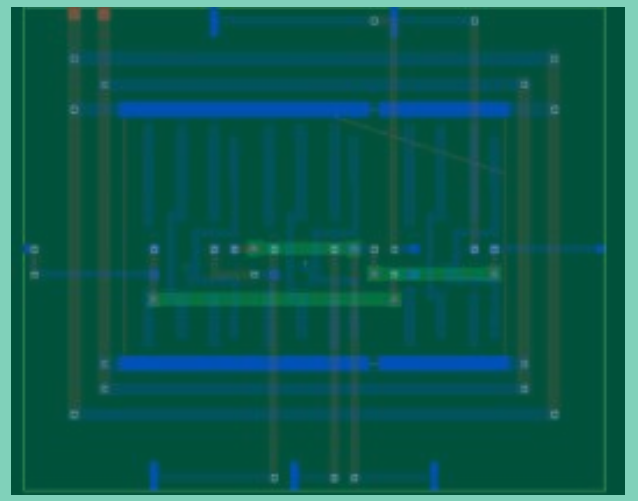
Netlist: list of primitive gates




Logic Synthesis

***Front End***

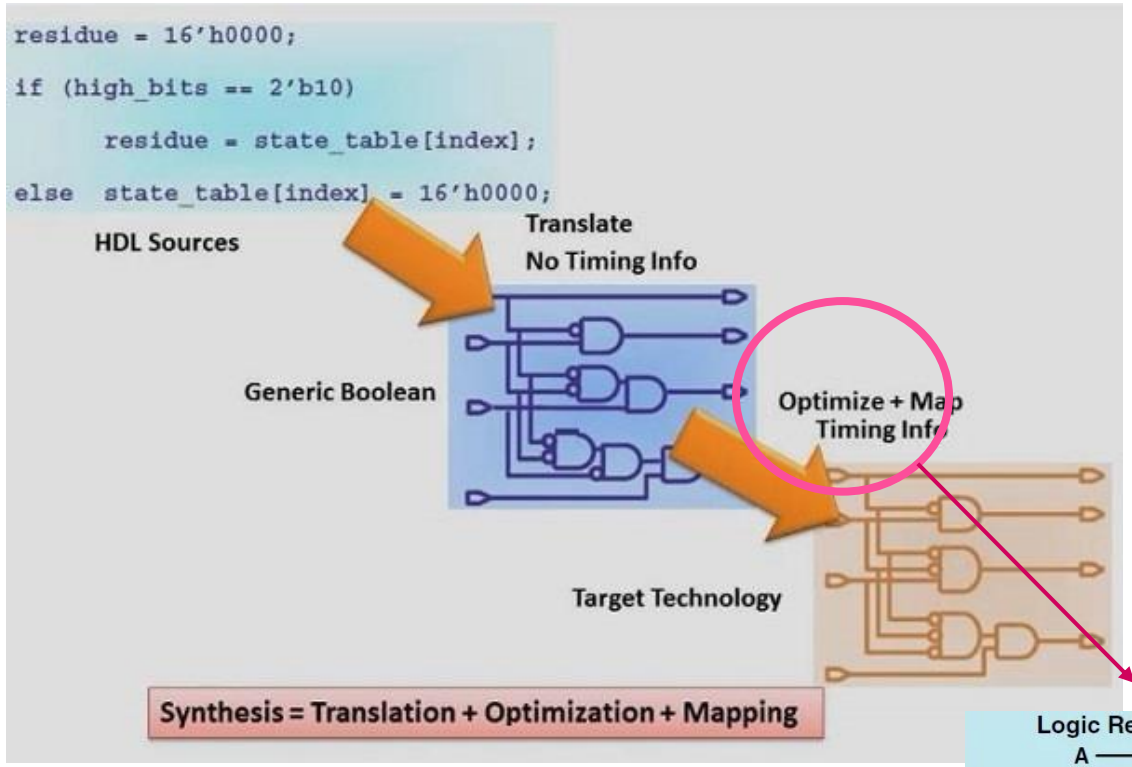
Layout

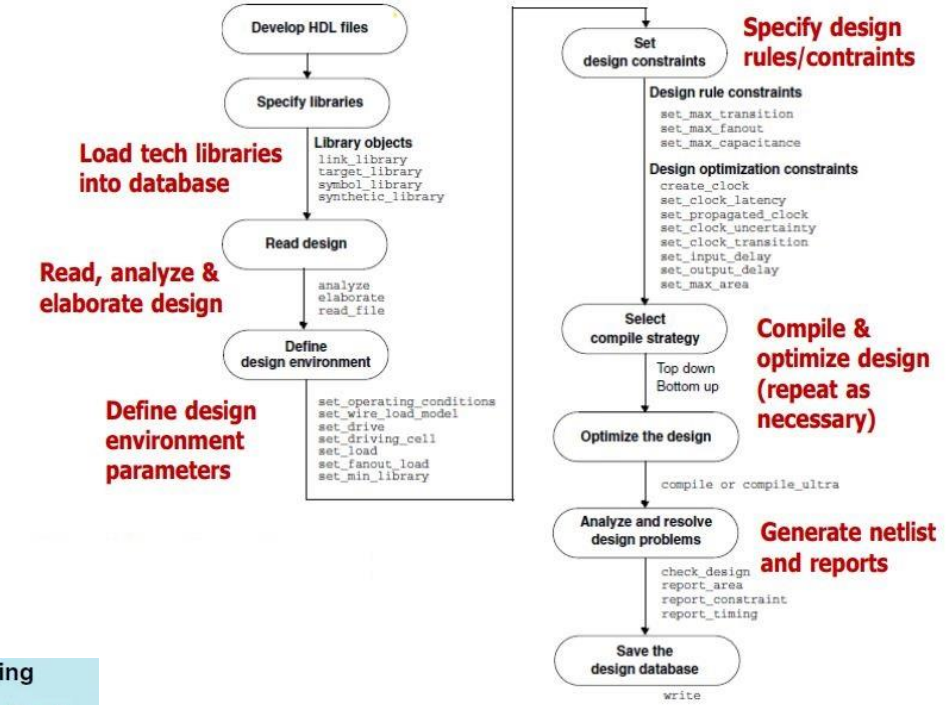


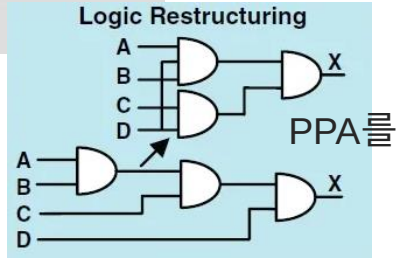
Physical Implementation:
Place and Route(PNR)

***Back End***

# Logic Synthesis: power of EDA tools

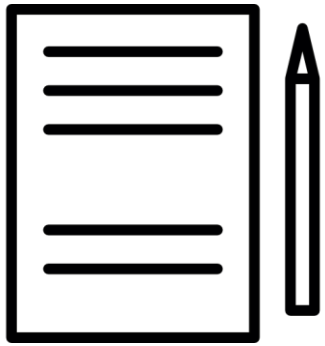



PPA를 고려한 logic reconstructing

# What if no EDA Tools?



[What if no EDA tools?]

# Advantages of HDL-based design

## 효율성

- 설계오류 수정이 쉽다
- 합성에 의한 회로 생성과 설계의 변경이 쉽다

## QoR 향상

- 다양한 설계기법에 의한 최적화
- 선택적인 최적화를 통한 합성

## 독립성

- 특정 ASIC제조업체에 종속되지 않음
- 동일한 HDL설계의 다른 라이브러리를 이용한 합성
- 신속한 prototyping 가능

## 비용

- 상위레벨 설계도구 사용에 따른 설계 생산성 증가
- 설계기간 단축 →설계비용 감소
- 설계자산 재사용

## 표준성

- IEEE표준으로 학계 및 산업계에서 설계 및 설계 정보 교환수단으로 사용

## 관리

- 구조적 설계 이용한 기능별 분할 설계 및 문서화 용이

# LAB

*System Setup*

# Homework

- Chapter1: ~pp.30