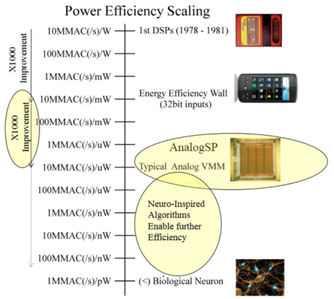
Android Interface for FPAA Device

Benjamin Bolte, Sahil Shah, Siwan Kim and Jennifer Hasler

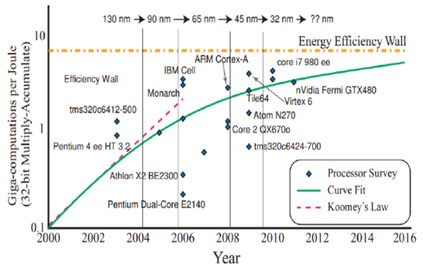
CADSP Cooperative Analog and Digital Signal Processing

Georgia Institute of Technology

FPAAs are computationally efficient

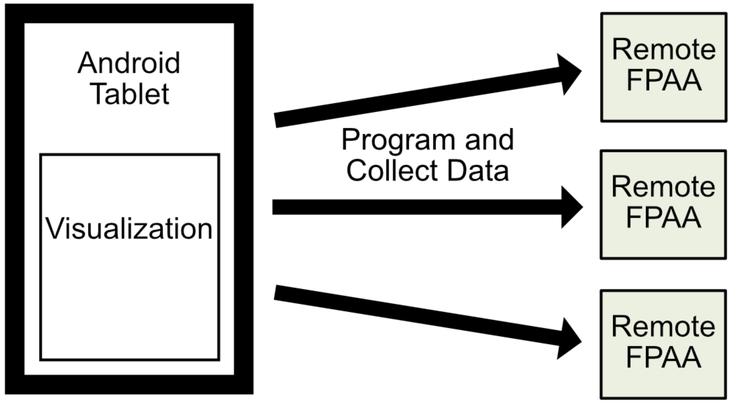


Hasler et. all 2013



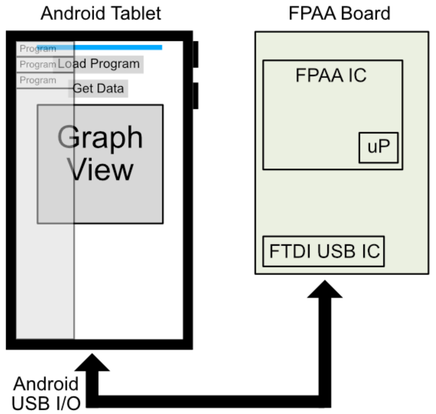
Marr et. all 2012

Tablet interface gives portability and ease of data collection

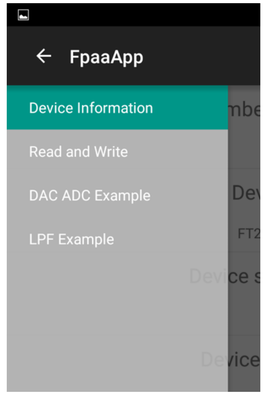


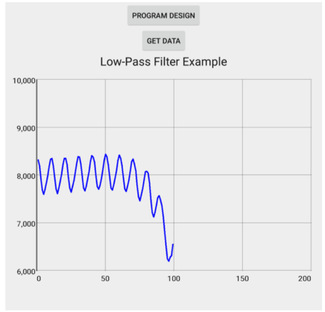
Parameter	Value	Parameter	Value
Number of CABs	98	Number of CLBs	98
On Chip μP	Open Source MSP430	μP clock frequency	0 - 50MHz
C block Line Capacitance	160fF	S Block Line Capacitance	160fF
V_{dd} (analog)	2.5V	V_{dd} (digital)	2.5V, 3.3V
V_{dd} Injection	6.0V	V_{dd} Tunneling	12V
Program Memory	16k x 16	Data Memory	16k x 16
CMOS Process	Standard 350nm	Die Size	12mm x 7mm
General Digital I/O	16 (in), 16(out)	SPI ports	5
General Analog I/O	125	Analog Parameters	359,014

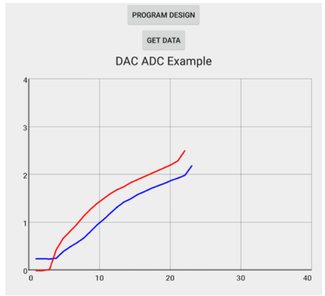
Tablet-Board Communication



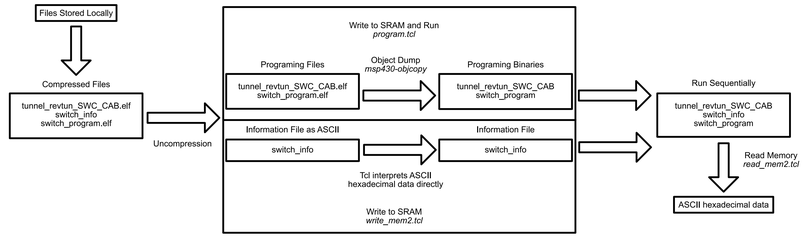
Choose between different programs to run on-chip



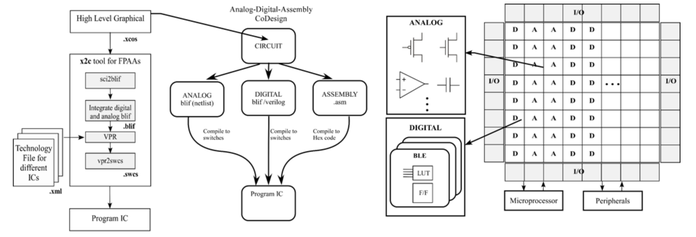


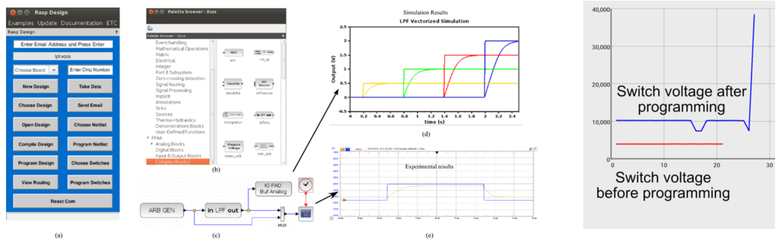


Programming flow integrates with high-level design tools



CAD tools used to enable Hardware-Software Codesign





REFERENCES

[1] S. Nedevschi, R. K. Patra, and E. A. Brewer, "Hardware speech recognition for user interfaces in low cost, low power devices," in 42nd Annual Conf. on Design Automation (DAC), 2005, pp. 684–689.

[2] S. George, S. Kim, S. Shah, J. Hasler, M. Collins, F. Adil, R. Wunderlich, S. Nease, and S. Ramakrishnan, "A programmable and configurable mixed-mode FPAA SOC," Accepted to IEEE Transactions on VLSI, Oct 2015.

[3] J. Gehring, "Graphview - open source graph plotting library for android."

[4] J. Hasler and B. Marr, "Finding a roadmap to achieve large neuromorphic hardware systems," Frontiers in Neuromorphic Engineering (2013)

[5] H. B. Marr, B. Degnan, P. Hasler, and D. Anderson, "Scaling Energy Per Operation via an Asynchronous Pipeline," IEEE Trans. on VLSI 2013

Integrated Circuits and Electronics Communications ICE