Android Interface for FPAA Device

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CADSP Cooperative Analog and Digital Signal Processing

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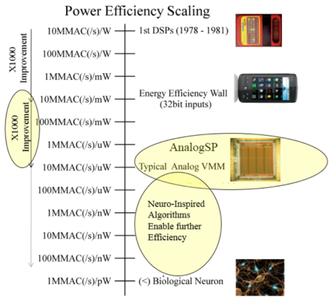
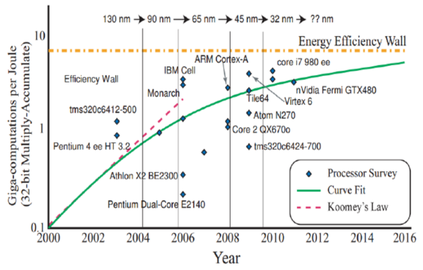
FPAAs are computationally efficient

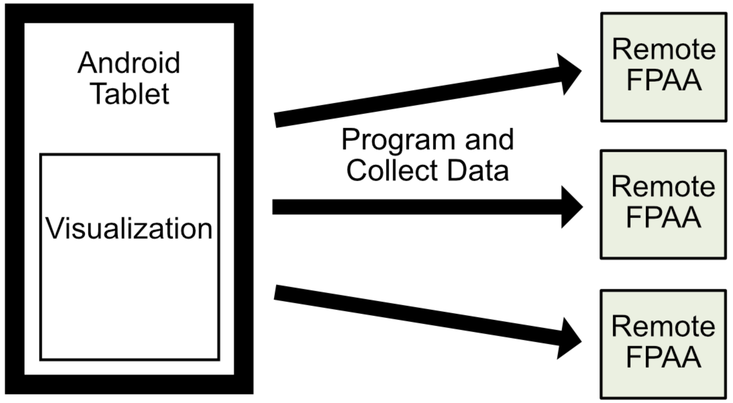


Hasler et. all 2013



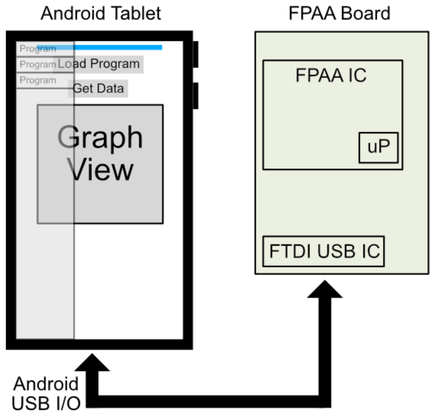
Marr et. all 2012

Tablet interface gives portability and ease of data collection

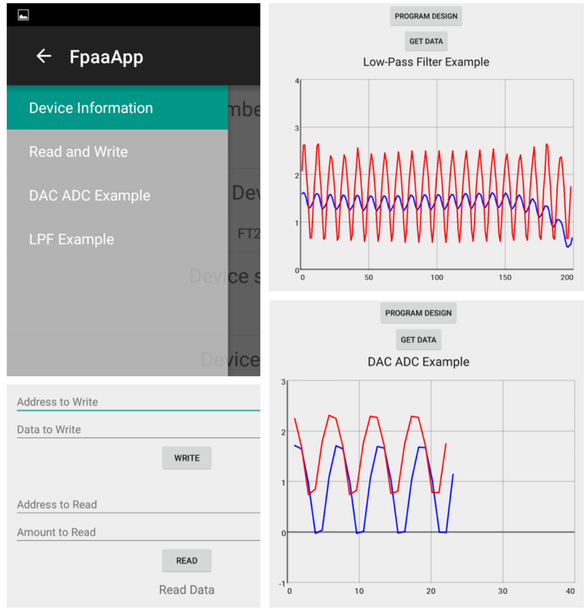


Parameter	Value	Parameter	Value
Number of CABs	98	Number of CLBs	98
On Chip μP	Open Source MSP430	μP clock frequency	0 - 50MHz
C block Line Capacitance	160fF	S Block Line Capacitance	160fF
V_{dd} (analog)	2.5V	V_{dd} (digital)	2.5V, 3.3V
V_{dd} Injection	6.0V	V_{dd} Tunneling	12V
Program Memory	16k x 16	Data Memory	16k x 16
CMOS Process	Standard 350nm	Die Size	12mm x 7mm
General Digital I/O	16 (in), 16(out)	SPI ports	5
General Analog I/O	125	Analog Parameters	359,014

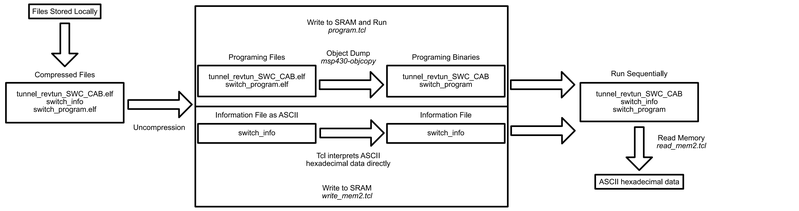
Tablet-Board Communication

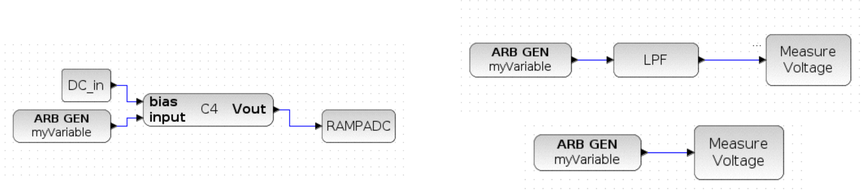


Choose between different programs to run on-chip

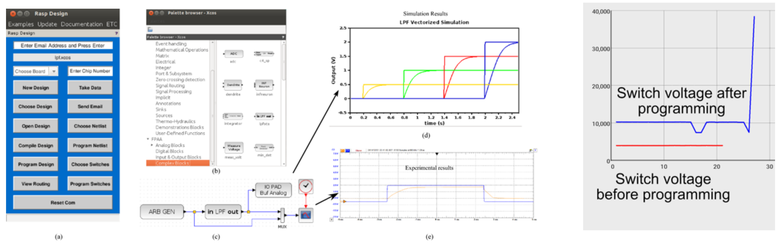


Programming flow integrates with high-level design tools





CAD tools used to enable Hardware-Software Codesign



Code available at https://github.com/codekansas/FpaaApp

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