Deliverable D6.2 – SYCLOPS IPR Management, Business Models, and Business Plan M12

GRANT AGREEMENT NUMBER: 101092877

Project acronym:	**SYCLOPS**
Project full title:	**Scaling extreme analYtics with Cross architecture acceLeration based on OPen Standards**
Call identifier:	**HORIZON-CL4-2022-DATA-01-05**
Type of action:	**RIA**
Start date:	**01/01/2023**
End date:	**31/12/2025**
Grant agreement no:	**101092877**

DXX - IPR Management, Business Models, and Business Plan M12

Executive Summary: This report presents the initial version of the IPR Management, Business Models and Business Plan of the SYCLOPS Project. It sheds light on the key aspects pertaining to the management and protection of intellectual property and lays down the main components of the relevant methodology to be applied.

WP:	WP6		
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Participating Partners:	All Partners		
Version:	1.0	**Status:**	Draft
Deliverable Type:	R - Document	**Dissemination Level:**	SEN
Official Submission Date:	31.12.23	**Actual Submission Date:**	31.01.2024

Disclaimer

The SYCLOPS consortium consists of the following partners:

No.	Partner Organisation Name	Partner Organisation Short Name	Country
1	EURECOM	EUR	FR
2	INESC ID - INSTITUTO DE ENGENHARIADE SISTEMAS E COMPUTADORES, INVESTIGACAO E DESENVOLVIMENTO EM LISBOA	INESC	PT
3	RUPRECHT-KARLS-UNIVERSITAET HEIDELBERG	UHEI	DE
4	ORGANISATION EUROPEENNE POUR LA RECHERCHE NUCLEAIRE	CERN	CH
5	HIRO MICRODATACENTERS B.V.	HIRO	NL
6	ACCELOM	ACC	FR
7	CODASIP S R O	CSIP	CZ
8	CODEPLAY SOFTWARE LIMITED	CPLAY	UK

Document Revision History

Version	Description	Contributions
0.1	Template & outline	**Raja Appuswamy, EUR**
0.2	First draft with CSIP contributions	**Jamie Broome, CSIP**
0.3	Second draft with all contributions	**ALL**
1.0	Final submission-ready draft	**Raja Appuswamy, EUR**

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Statement of Originality

This deliverable contains original unpublished work except where clearly indicated otherwise. Acknowledgement of previously published material and of the work of others has been made through appropriate citation, quotation or both.

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Executive Summary

Sound Innovation and Intellectual Property Rights (IPR) management is critical in order to enable the successful exploitation and market deployment for all SYCLOPS assets. Therefore, the SYCLOPS consortium places great emphasis in managing IPR in the framework of the project, with a view to effectively pave the way for the smooth exploitation and sustainability of its results following its completion.

The current report presents the M12 release of the IPR Management, Business Models and Business Plan of the SYCLOPS Project. It sheds light on the key terms pertaining to the management and protection of intellectual property and lays down the main components of the relevant methodology to be applied throughout the project. Preliminary description of expected project results, along with initial identification of the contributing partners, protection types and access rights are provided within the report. Initial considerations of Background and Foreground IP Knowledge, as currently perceived by the project partners is also presented.

This report will be further elaborated and updated on a regular basis as the project progresses. The final version (M36) of the IPR Strategy will be delivered by the end of the project, to guide post- project exploitation of SYCLOPS' results.

1 Introduction

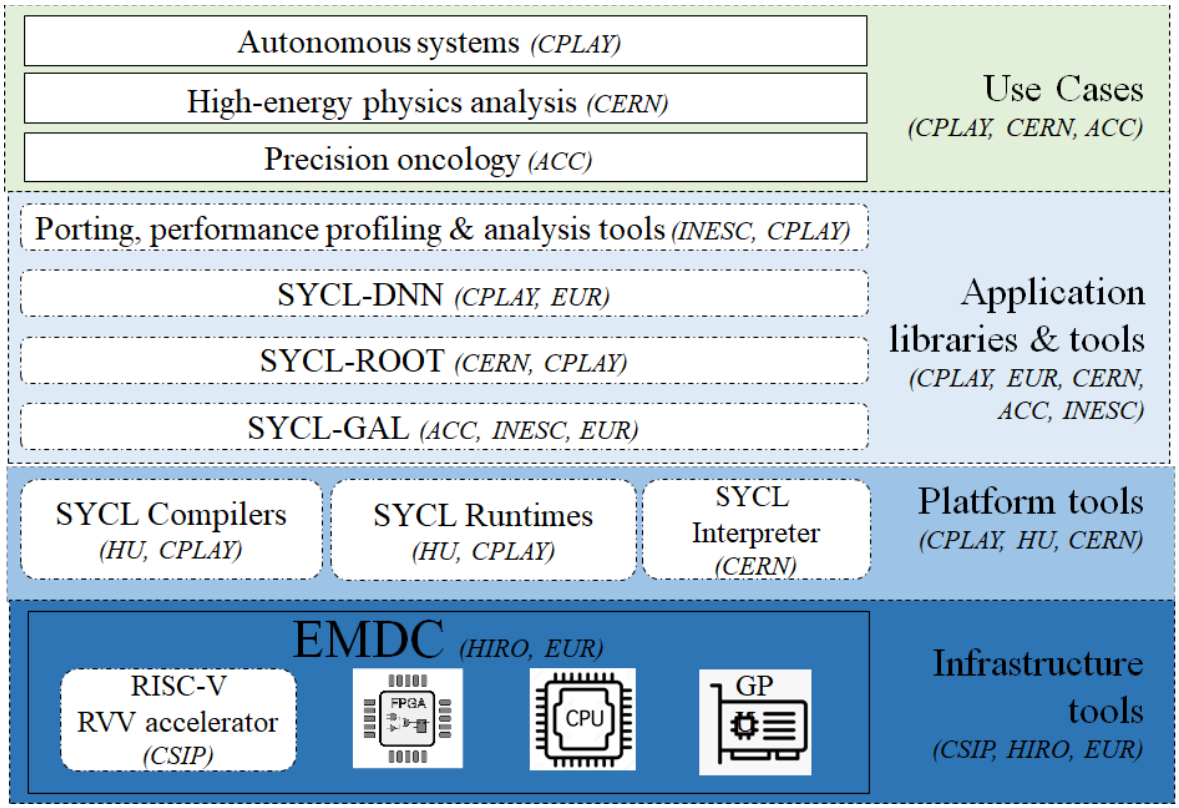
The AI acceleration market place today is dominated by a handful of large US-based industry players with proprietary solutions. In order to make the EU autonomous in its ability to process and analyze data at extreme scales, it is necessary to foster a healthy, open portable ecosystem of solutions in the future. This, in turn, makes it necessary to have open standards that allow European hardware and software vendors to innovative rapidly while being interoperable. RISC-V is gaining momentum as an open alternative for developing custom hardware accelerators, and SYCL is gaining momentum as an open alternative as a high-level, cross-vendor, cross-architecture programming model. However, historically, these standards have evolved independently with little interaction. **SYCLOPS brings together these two for the first time with the goal of demonstrating that an entirely open, standards-based approach to AI acceleration is feasible and performance-competitive with other proprietary solutions.** Through these standards, we will reinforce European leadership in AI acceleration by foster the development of an open, inter-operable European ecosystem of AI acceleration solutions that will counter the hegemony of a few large US-based technology players.

This report presents the M12 release of the IPR Management, Business Models and Business Plan of the SYCLOPS Project. It is structured as follows. In Section 2, we provide an overview of the SYCLOPS architecture and provide an overview of exploitable outcomes. In Section 3, we describe our methodology towards IPR management and elaborate in detail IPR handling mechanisms for each relevant partner. In section 4, we provide an overview of business models of various SYCLOPS partners and explain how SYCLOPS will directly contribute to the products of the four SMEs involved.

2 SYCLOPS Overview & Exploitable Outcomes

Figure 1 below shows the overall architecture of the SYCLOPS AI acceleration stack.

Figure 1: SYCLOPS hardware-software stack



Infrastructure layer. The SYCLOPS infrastructure layer is the bottom-most layer of the stack and provides heterogeneous hardware with a wide range of accelerators from several vendors. A key accelerator in this layer will be the RISC-V accelerator designed by our partner CSIP. CSIP will advance their processor description language *codAL* and their EDA tool *Codasip Studio* to offer native support for design, verification and implementation of RISC-V processors with customizable vector units. Using these tools, CSIP will develop an RVV accelerator. In order to demonstrate (i) an end-to-end integration of open standards, and the cross-architecture, and (ii) the cross-vendor performance portability of SYCLOPS, our partner HIRO will package the RISC-V accelerator with CPU and GPU from several other leading processor manufactures (Intel, AMD, NVIDIA) and build modular, *energy-efficient edge microdatacenter (EMDC)*. A key novelty of the EMDC will be the investigation of scaling down Compute Express Link (CXL) technology to a microdatacenter form factor.

Platform layer. The second layer from the bottom, the platform layer, provides the software required to compile, execute, and interpret SYCL applications over processors in the infrastructure layer. SYCLOPS contains *oneAPI DPC++*, an industry-standard, commercial SYCL compiler from CPLAY, and *AdaptiveCPP* (previously hipSYCL), an open-source SYCL compiler toolchain from UHEI. In terms of SYCL interpreters, SYCLOPS contains *Cling* from CERN, a state-of-the-art C++ interpreter that is being used as an interactive code development environment for exploratory analysis.

Application libraries and tools layer. While the platform layer described above enables direct programming in SYCL, the libraries layer enables API-based programming by providing pre-designed, tuned libraries for various deep learning methods for scalable point cloud analysis (*SYCL-DNN*), mathematical operators for scalable High-Energy Physics (HEP) analysis (*SYCL-ROOT*), and data parallel algorithms for scalable genomic analysis (*SYCL-GAL*).

The exploitation of SYCLOPS results will strengthen Europe's position in the burgeoning AI acceleration market on both an industry level and policy level. Table 1 provides a summarized listing of potential exploitable outcomes that we have identified.

Table 1: Exploitable SYCLOPS outcomes

Exploitable outcome	Target partner & potential users
Infrastructure tools for simple, fast, cost-effective customization of RISC-V accelerators.	• CSIP will enhance their EDA suite that will be offered as a product to hardware developers for designing RISC-V accelerators • CSIP will enhance its processor offerings with new RVV accelerators and expand into high-performance AI acceleration market.
Infrastructure services for energy-efficient data analytics at the edge	• The CXL-enabled EMDC is fundamentally important to our partner HIRO's exploitation, since the datacenter Industry is quickly transitioning to this new standard.
Improved compilers for SYCL-based cross-architecture programming.	• CPLAY will advance their SYCL compiler which has already been used by various embedded, IoT, HPC customers • UHEI will enhance their AdaptiveCPP compiler toolchain and it will be made available to researchers. Improvements to RISC-V LLVM backend will be upstreamed to enable further research in open hardware technologies and to benefit industrial RISC-V implementations
Improved productivity for data scientists and education using Cling with SYCL	• Direct integration of SYCL implementations with Cling interpreter will enable further research, experiments and exploitations by HEP community and CERN • Cling Jupyter notebook environment will simplify education of SYCL/C++ and the importance of standards and performance portability when targeting new platforms and accelerators
Improved end-to-end pipelines for use cases based on SYCLOPS' cross-architecture acceleration libraries	• ACC will use SYCL-GAL to develop accelerated multi-omics pipeline • SYCL-DNN integrated in oneAPI will be used to customize product offerings in automotive/drone space by CPLAY.

3 SCYLOPS IPR Management

Throughout the SCYLOPS project, IPR management will build on the pillars of identifying a common understanding concerning the background, foreground, ownership (including joint ownership), access and usage rights, dissemination and exploitation during and after the project. In this respect, the SYCLOPS IPR management plan applies on a comprehensive framework that separates the IP management processes of the project in the following stages:

1. Grant preparation stage
2. Project implementation stage
3. Post-project stage

Since this deliverable is being drafted at M12 of project SYCLOPS, we focus only on the first two stages here. This report will be updated on a regular basis as the project progresses. The final version (M36) of the IPR Strategy will be delivered by the end of the project to guide post- project exploitation of SYCLOPS results.

3.1 Grant Preparation Stage

At the Grant Agreement preparation stage, both the Grant Agreement and the Consortium Agreement documents have been drafted to include a description of several issues related to IPR. Their unique provisions represent a reference point for IPR issues within the project.

3.1.1 Grant Agreement

The Grant Agreement constitutes a contract that sets out the key rules and conditions of the project. It is signed between the EC and the SYCLOPS partners and represents the main contractual basis for SYCLOPS while its main points and sections which refer to IPR are included in article 16 “Intellectual property rights (IPR) — background and results —access rights and rights of use”. Under this scheme, the management of the SYCLOPS IP is regulated, whereas access rights and obligations related to the background are set. In addition, the Grant Agreement defines issues concerning the ownership and protection of the project generated results, as well as their exploitation and dissemination outcomes. Lastly, the SYCLOPS GA defines transferability and access rights to results.

3.1.2 Consortium Agreement

The Consortium Agreement constitutes a contract among the partners of the SYCLOPS consortium that aims to define rights and obligations during the partnership for the purposes of carrying out the project’s foreseen actions and activities. The Consortium Agreement minimizes the probability of later disputes as it provides rules and responsibilities during the project and defines the access rights to be granted to the partners concerning the project. In addition, it outlines rights and responsibilities among the consortium members concerning issues of the IP.

The SYCLOPS Consortium Agreement main points and sections referring to IPR are included in:

- **Section 8 “Results”**, that sets out provisions on ownership and joint ownership of results, as well as on their transfer and dissemination.
- **Section 9 “Access Rights” and Section 10 “Non-disclosure of information”,**

which clarify the access rights governing principles along with the access rights for the exploitation, communication, and dissemination purposes.

- **Attachment 1 "Background included"** that presents the initial list of usable background.

3.2 Project Implementation Stage

During the first year, the consortium members collectively identified an initial list of IP that will be developed in the project based on the list of exploitable items mentioned earlier.

Table 2: List of software to be developed in SYCLOPS

Exploitable outcome	Software Developed	Partners	Open source/ proprietary
Infrastructure tools for simple, fast, cost-effective customization of RISC-V accelerators.	Upgraded Codasip Studio	CSIP	Proprietary
	Updated Codespace	CSIP	Proprietary
	Updated CodAL support for RVV	CSIP	Proprietary
Infrastructure services for energy-efficient data analytics at the edge	CXL-based EMDC modules	HIRO	Proprietary
Improved compilers for SYCL-based cross-architecture programming.	Updates to oneAPI DPC++ compiler (https://github.com/intel/llvm,) oneAPI Construction Kit (https://github.com/codeplaysoftware/oneapi-construction-kit,) SYCLomatic conversion tool (https://github.com/oneapi-src/SYCLomatic,) and Unified Runtime (https://github.com/oneapi-src/unified-runtime)	CPLAY	Open Source
	Updates to AdaptiveCPP compiler (https://github.com/AdaptiveCpp/AdaptiveCpp) & a new graph runtime	UHEI	Open Source
Improved productivity for data scientists and education using Cling with SYCL	SYCL-enabled Cling interpreter (https://root.cern/cling/)	CERN	Open Source
Improved end-to-end pipelines for use cases	New library SYCL-GAL for accelerating genomics	ACC	Open Source

based on SYCLOPS' cross-architecture acceleration libraries	Extensions to SYCL-DNN (https://github.com/codeplaysoftware/portDNN) for supporting new workloads	CPLAY	Open Source
	New library SYCL-ROOT for acceleration HEP	CERN	Open Source

The table shown above lists software that will be developed during the SYCLOPS project together with relevant partners and licensing (open source or proprietary) envisioned.

3.2.1 Open source and standards

First of all, SYCLOPS partners unanimously view open source technologies as the most beneficial route to reach a wide use of many SYCLOPS results. Especially since the project builds upon open standards SYCL and RISC-V, and open source software initiatives like AdaptiveCPP, Cling, and oneAPI, it seems natural to provide higher impact for the project by releasing contributions to such pre-existing open source projects following their open source licenses. In addition, the newly developed SYCL-GAL and SYCL-ROOT libraries will also be made open source. However, our four SME partners have proprietary hardware/software that will be a part of SYCLOPS. Thus, the next section addresses IPR issues for each of these partners on a case-by-case basis.

3.2.2 Proprietary Hardware & Software Management

Specific components of four partners were identified as proprietary: (i) EMDC modules from HIRO, (ii) Codasip Studio/CodeSpace/CoDAL from CSIP, (ii) ACORAN compiler suite from CPLAY, and (iii) multi-omics pipeline from ACC. We provide a description of each partner's IP and partner-specific IPR handling measures adopted in the first year here.

3.2.2.1 HIRO

HIRO-MicroDataCenters BV is a European SME developing powerful edge-as-a-service infrastructure that will enable European Industries to participate in the data economy with infrastructure deployed at the edge of the network. Compute Express Link (CXL) is known as the "breakthrough" CPU-to-device, cache-coherent interconnect for processors, memory expansion, accelerators and targeting extremely low latency for new cache and memory transactions. In the SYCLOPS project, HIRO will build a prototype CXL capable server using off the shelf components to test the SYCL software and test the use of memory coherency in the orchestrated workloads of a heterogeneous platform. HIRO will also develop a CXL capable module for their own EMDC and demonstrate its functionality. Furthermore, HIRO's Kubernetes based workload orchestration software will be structured and adjusted to match the CloudEdgeIot standard of cloud software stacks and tested in the orchestration of SYCL containers. The experimentation with CXL in datacenter technology is fundamentally important to HIRO' exploitation, since the datacenter Industry is quickly transitioning to this new standard.

IPR protection measures. HIRO will be the exclusive designer and developer of the CXL EMDC component. As per IPR regulations in CA, the results obtained from this endeavour shall be owned by HIRO, who will be the sole partner carrying out the work.

3.2.2.2 Codasip

CSIP's primary business model is to license both Studio/CodAL as well as our RISC-V processors designed with Studio/CodAL. This license includes all rights to use the EDA tool and IP during the license period and for the purpose defined in the license agreement. Financially, the typical license agreement includes an annual price per seat for Studio/CodAL and both an up-front fee and royalty per chip for the IP. IP created by the customer using CSIP's tool and IP is owned exclusively by the customer, subject to a background IP license and EDA subscription with CSIP.

IPR protection measures. For the SYCLOPS Project all intellectual property of Studio/CodAL, Codespace and CSIP's RISC-V processors is considered background IP owned solely by CSIP. We expect development work on these products to be done only by CSIP. SYCLOPS partners, in contrast, will predominantly be "users" of our IP. To this end, CSIP is already providing EDA tools and RISC-V processor IP cores to SYCLOPS beneficiaries on a license and royalty free basis and strictly only to meet the needs of the project. Any foreground intellectual property results created with CSIP EDA tooling and processor IP will be the property of the beneficiary or beneficiaries who created it under the terms outlined in the Grant Agreement and the Consortium Agreement.. After the project, if further work is necessary that requires the use of CSIP's EDA tool or IP, the beneficiary must obtain the necessary commercial EDA and IP licenses from CSIP. Beneficiaries outside of the SYSCLOPs member who are granted access to CSIP EDA tools and/or RISC-V IP license must sign appropriate non-disclosure agreements (NDAs) and license agreements with CSIP. For any 3rd Party use of CSIP IP directly or indirectly from the SYCLOPS program, CSIP will enter into a commercial license agreement with that party.

3.2.2.3 Codeplay

After the official start of project SYCLOPS, Intel acquired Codeplay. Hence, the proprietary ACORAN ComputeCPP compiler described in the SYCLOPS proposal has been discontinued. This has replaced by open-source DPC++ as the SYCL implementation used in SYCLOPS. DPC++ is an open-source, state-of-the-art SYCL compiler and runtime with a much larger developer and user community (commercial and research) than ComputeCPP. Thus, all contributions from Codeplay in SYCLOPS including the DPC++ compiler, SYCL-DNN library, CUDA-to-SYCL code conversion utility (SYCLomatic), Unified Runtime, and oneAPI Construction Kit for porting SYCL to RISC-V are all expected to be open source in nature.

IPR protection measures. There are no specific IPR issues for the SYCLOPS project from CPLAY's point of view.

3.2.2.4 ACCELOM

ACC has developed easy-to-deploy, reproducible multi-omics software pipelines that use novel, peer-reviewed, statistical machine learning techniques (G2, dNET) to integrate multiple molecular datasets from a host to analyze association patterns between molecular levels. The pipeline consists of two major parts: (i) secondary analysis that starts from reads generated by sequencing instrument to analysis-ready variants, and (ii) tertiary analysis of identified variants with various statistical techniques. The secondary analysis stage of the pipeline is a collection of open-source software tools for sequence alignment (BWA-MEM, Accel-Align), post-alignment preprocessing (GATK), and variant calling (GATK, Deepvariant). The tertiary stage contains proprietary algorithms. In SYCLOPS, the goal is to develop SYCL-GAL for accelerating the secondary analysis stage.

IPR protection measures. ACC will work together with EUR for accelerating alignment, and post-alignment preprocessing, and with INESC for variant calling. In order to promote the update of SYCL in the genomics community, SYCL-GAL will be entirely open source. ACC also recognizes that the results potentially jointly created with EUR and INESC will be jointly owned by all contributing project partners when appropriate. Such joint inventions and all related patent applications and patents shall be jointly owned by the contributing parties. Thus, if SYCL-GAL is turned into a commercial offering, depending on which components jointly developed are used commercially based on evaluation in SYCLOPS, IPR agreements will be made using the Consortium Agreement as the guiding legal framework.

4 Business Model and Business Plan

Conceptually, there are two major approaches for building AI and analytics accelerators. The specialization approach starts with one or few models that provide state-of-the-art accuracy and performance for a given task. The core algorithms behind those models are analyzed and a combined hardware—software stack is designed to accelerate them. The generalization approach, in contrast, starts with a flexible, customizable yet general-purpose hardware and software stack that provides well-established interfaces and APIs. AI algorithms are then programmed against the API. The two strategies target different stakeholders in the marketplace. The specialization strategy is geared towards providing the highest efficiency for focused application verticals where AI algorithms have matured, and their performance/accuracy has reached a threshold that is sufficient for practical deployment. The generalization strategy, in contrast, is more suitable for building an ecosystem of solutions covering a broad range of applications where new AI models and user requirements are evolving at a rapid pace. Given this distinction, it is obvious that the generalization strategy yields a much larger market compared to specialization. This is validated by a report from Omdia[1] that estimates that NVIDIA, with its customizable GPU hardware and the immensely successful CUDA software ecosystem, dominates AI accelerator market with an 80% share and a business worth over $4B.

Given recent advances in RISC-V and SYCL we believe that we are at an inflection point--a new ecosystem of AI acceleration solutions based on the generalization offered by these standards has started. The key stakeholders in this ecosystem are the hardware and software developers who develop customized AI solutions for various application verticals, and they are the target user group of the technology developed in this project. SYCLOPS aims to reinforce Europe leadership in both framing and monetizing this ecosystem by bringing together partners who are playing a key role in framing these standards with the goal of clearly demonstrating that an entirely open approach to AI acceleration can yield efficiency comparable to state-of-the-art solutions.

Based on the initial foreground IP identification study, SYCLOPS will contribute to the advancement of business offerings of all four SMEs involved in SYCLOPS in different ways.

4.1.1.1 HIRO

A Powerful Edge Infrastructure (hardware and software) will help Europe to break free from the oligopoly of Google, Apple, Facebook, Amazon, and Microsoft (GAFAM), whose business models are all built around centralisation and control of infrastructure. In stark contrast, multiple technologies like VR, AR, Blockchain, Cybernetics, AI, 5G, Digital Twins, Real Time CyberPhysical Systems are maturing. In all these case, large volumes of data need to be stored and processed. In order to save costs, bandwidth and multiple round trip latencies, such storage and processing of data must be done locally where data is generated. Thus, Europe's data economy requires a powerful edge infrastructure running data spaces where data producers and data consumers freely can share and monetize their data supported by additional service providers for security, governance, AI training, data product management, networking, etcetera.

[1] AI Processors for Cloud and DataCenter Forecast Report. Omdia. 2021

Market feedback based on our customers and collaborators has identified bottlenecks that limit the growth of edge data centres:

- Lack of standardisation in Edge-native (designed for the Edge) hardware
- Absence of an outsourcing cost model to enable a shift from CAPEX (capital expenditure) to a more repeatable OPEX (operational expenditure) model
- Absence of advanced security features
- Above average PUE (Power Usage Effectiveness) performance

HIRO-MicroDataCenters BV is a European SME's developing powerful edge-as-a-service infrastructure and addressing these concerns by driving the innovation of hardware and of software at the edge, and will enable European Industries to participate in the data economy with infrastructure deployed at the edge of the network.

- *Standardisation:* HIRO is actively involved in the standardisation of hardware and software for the powerful edge infrastructure (more information in Section 2.1.7 deliverable "D6.3. Communication, Networking and Dissemination Plan and Activities M12").
- *Service levels:* HIRO is working on an OPEX model of exploitation that could have similarities with the OPEX model of large cloud providers.
- *Security:* HIRO incorporates security by design in their projects and is creating security from the hardware level up, by incorporating hardware based security features (such trust zones, security chips, encryption technologies). All hardware and software is designed, manufactured and programmed in Europe.
- *Power Usage Effectiveness:* A standard used by the datacenter industry to prove their efficiency in bringing maximum power to their server processors, memories, switches, etc. and using as little power possible for other supportive functions such as cooling, light, power transformation, spinning disks, etc. State-of-the-art datacenters by GAFAM have a PUE of around 1.15-1.2, most co-location and edge datacenters have a PUE of 1.6-2.0. HIRO has developed a cooling technology that allows them to cool an edge datacenter with PUE 1.03.

Through SYCLOPS, HIRO plans to take the first steps towards the design of its CXL-enabled EMDC. Largely used for applications like AI and machine learning, CXL enables efficient peer-to-peer communications, allows CPUs and accelerators to access each other's memory with coherency. Memory coherency paves the way for higher performance via resource sharing, less complexity of the software stack, and lower overall system cost. CXL also enables fine-grained resource sharing across multiple compute domains, leading to an efficient disaggregated architecture. This approach leads to better platform flexibility, higher density, and better resource utilization, with datacenter designers able to tap into resources based on the needs of particular workloads. Thus, we expect CXL-enabled EMDC to become a new standardized driving force in realizing AI at the edge. Through SYCLOPS, HIRO plans to be at the forefront of this technology with differentiated EMDC offerings that can compete with GAFAM.

4.1.1.2 Codasip

CSIP is a European deep tech company specializing in Electronic Design Automation (EDA) software tools used to create semiconductor processors. CSIP uses its EDA tool called Studio, along with its complementary C-based processor description language called CodAL, to design processors based on the open RISC-V ISA. A key benefit of RISC-V, besides being an open

ISA, is that users can also customize the ISA, which is frequently referred to or related to "software driving processor design" or "heterogeneous compute" or "domain specific processing". We call such design Custom Compute. Studio/CodAL are designed specifically to facilitate Custom Compute, which is becoming increasingly important because of the end of Moore's Law. The output of Studio is a Hardware Development Kit (HDK) and a Software Development Kit (SDK). The HDK includes standard a standard RTL description of the processor along with test bench framework to support integration and creation of a System on Chips (SoCs). The SDK includes a LLVM compiler and tool change to support creation of software tuned to run on the processor. The combination of an HDK and SDK is unique in the industry and particularly well designed for RISC-V and to optimally enable Custom Compute.

CSIP's primary business model is to license both Studio/CodAL as well as our RISC-V processors designed with Studio/CodAL. This license includes all rights to use the EDA tool and IP during the license period and for the purpose defined in the license agreement. Financially, the typical license agreement includes an annual price per seat for Studio/CodAL and both an up-front fee and royalty per chip for the IP. IP created by the customer using CSIP's tool and IP is owned exclusively by the customer, subject to a background IP license and EDA subscription with CSIP.

Through SYCLOPS, CSIP will transform codAL and Studio into powerful tools that can be used to develop advanced RISC-V accelerators with RVV extension support. As RVV requires application-specific customization, extensions will be made at both the codAL language level and the Studio API level to facilitate the mapping of applications to customized RISC-V architectures. Today, CSIP licenses Studio/CodAL, and has a portfolio of RISC-V microprocessor cores targeting the embedded segment. We expect RVV customization to further expand the addressable market for CSIP by covering the high-performance segment. By extending codAL and Studio to offer native support for RVV, CSIP will be able to target this new high-performance end of the market. As CSIP only designs accelerators and does not fabricate them, its business model is also aligned and synergistic with parallel European efforts like EPI.

Recently, research and consulting group Semico published a market survey and analysis report of the Semiconductor Intellectual Property (SIP) and System-on-a-chip (SoC) markets. They forecasted that RISC-V-based AI SoCs will have a CAGR for units of 73.6% by 2027. Their latest covers the impact of RISC-V on the SIP market, and provides projections regarding the growth of RISC-V SIP revenue in the near future. As a part of our business plan, we intend to engage Semico by acquiring their market survey and potentially expanding on it.

4.1.1.3 Codeplay

As mentioned earlier, after the official start of project SYCLOPS, Intel acquired Codeplay. Hence, the ACORAN ComputeCPP compiler described in the SYCLOPS proposal has been discontinued. This has replaced by open-source DPC++ as the SYCL implementation used in SYCLOPS. DPC++ is an open-source, state-of-the-art SYCL compiler and runtime with a much larger developer and user community (commercial and research) than ComputeCPP. Many algorithms and components from ComputeCPP have been, or are being integrated, into DPC++ improving platform support and performance. Thus, SYCLOPS will have a direct impact on compiler toolchains from Intel.

Further, the change from ComputeCPP to DPC++ does not alter the exploitation/commercialization plan or the technologies to be developed. To facilitate commercial exploitation the aim is to rapidly build and advance an open-source, standards-

based accelerated software ecosystem for AI, HPC, Automotive and other applications that runs with competitive performance on as many processors as possible. This open-source ecosystem is then customized in Intel customer projects (by building closed-source solutions) to (i) support new or proprietary specialized platforms (ongoing internal projects), and (ii) tune performance of ecosystem algorithms and tools (there are customer projects currently ongoing but also being negotiated)

4.1.1.4 ACCELOM

ACC is an innovative European SME specializing in multi-omics data analysis. So far, ACC's business plan has not involved selling software directly to customers. Instead, ACC specializes in bespoke consulting services that require specialized statistical and machine learning techniques for extracting insights from genotypic and phenotypic data. As mentioned before, ACC relies on a custom-built computational pipeline for their analysis. The pipeline consists of two parts: (i) secondary analysis part that uses open-source tools from GATK, and (ii) tertiary analysis part that relies on proprietary machine learning methods.

In SYCLOPS, SYCL-GAL will predominantly accelerate the secondary analysis part. The development of SYCL-GAL creates the possibility of starting a new product line involving direct sale of software pipeline (both secondary and tertiary). Preliminary market analysis has already revealed two key competitors, namely, NVIDIA with their Clara Parabricks software suite, and Illumina with the EDICO Dragen pipeline. Both these solutions are proprietary with vendor lock in and require special-purpose hardware. SYCL-GAL will be the first cross-vendor, cross-platform open-source solution. Thus, it will certainly be of interest to the genomics community, and we expect its open-source nature to promote the adoption of SYCL. At the end of SYCLOPS, we expect SYCL-GAL to be at TRL level 3 or 4. Thus, we do not expect it to be ready for commercial deployment. However, through SYCLOPS, we intend to demonstrate that SYCL-GAL will be able to achieve appreciable acceleration, and offer performance comparable to its competitors.

Further, ACC has forged a key partnership with India's largest biobank for molecular biomarker identification in precision oncology. Towards the end of SYCLOPS, once SYCL-GAL has been developed fully, integrated into our pipeline, and evaluated thoroughly, we plan to rely on our Indian partnership to advertise SYCLOPS in general, and SYCL-GAL in particular, to doctors, bioinformatics, and healthcare IT audience among others in India with the goal of gauging an interest in such a software.

5 Conclusion

This document constitutes the M12 update of the IPR Management, Business Models, and Business Plan. We presented the IPR methodology employed in SYCLOLPS, as well as an overview of the exploitable outcomes. Based on these outcomes, we then identified background and foreground IP during the grant preparation and first-year implementation phases of the project. We focused on proprietary software belonging to SME partners in SYCLOPS and outlined IPR management on a case-by-case basis.

As the project transitions into the second year, we will continue to track IP as it is created in the project and protect it using GA & CA as guidelines. We outlined the business models of each of our SMEs together with a preliminary identification of how SYCLOPS will transform their products in this deliverable. In the future, we plan to perform market surveys as and when appropriate (in particular for RISC-V market covered by Codasip) and use it to refine the business plan of relevant SMEs.