**VERIFICATION PLAN FOR AHB TO APB BRIDGE**

**BLOCK DIAGRAM:**

**CLK**

**APBBUS**

**AHB BUS**

**HCLK PCLK**

**BRIDGE**

**HWRITE**

**PADDR [31:0]**

**HSIZE[2:0]**

**PWDATA[31:0]**

**HTRANS[1:0]**

**PRDATA[31:0]**

**HWDATA[31:0]**

**HBURST[2:0]**

**PSEL**

**HRSDATA[31:0]**

**HREADY**

**PENABLE**

**HADDR[31:0] PWRITE**

**HRESETn PRESETn**

**RESETn**

The AHB to APB works as an interface between high speed AHB and low performance APB buses. It acts as an AHB slave and APB master, The AHB to APB bridge is designed for single master and single slave.

The AHB signals works on clock signal HCLK. The AHB bus contains active low asynchronous rest signal HRESETn. Master initiates READ or WRITE transfers, during WRITE transfer HWRITE is HIGH and HADDR address of slave is written with data HWDATA. The type of transfer whether IDLE, BUSY, NONSEQ OR SEQ depends upon signal HTRANS. The data transfer can be either single, wrapping burst or incrementing burst which is based on signal HBURST. The data transfer size depends upon HSIZE, whether the transfer is completed or not is indicated by HREADY. If HREADY is LOW, then HADDR and HWDATA are extended. During READ transfer HWRITE becomes LOW and HRDATA in HADDR address of slave is read. If HREADY is LOW then HRDATA is read once HREADY becomes HIGH.

The APB signals works on clock signal HCLK. The APB bus contains active low asynchronous reset signal PRESETn, Slave performs READ or WRITE transfer when initiated by master. During WRITE transfer, PWRITE should be HIGH and PSEL is HIGH indicating that slave is selected, into the address PADDR of slave PWDATA is written and at the second clock edge of transfer PENABLE goes HIGH. During READ transfer, PWRITE is LOW and PSEL is HIGH, from PADDR address of slave PRDATA is read and PENABLE becomes HIGH at the second clock edge transfer.

**Top**

**Test**

**Virtual Sequence ENV**

**nV**

**Virtual AHB interface virtual APB interface**

**SCOREBOARD**

ARD

**VIRTUALSEQUENCER**

**AHB AGENT APB AGENT**

Virtual s

**virtual sequencer**

**M-SEQUENCER**

**AHB FIFO**

**APB SEQR**

**APB FIFO**

**AHB SEQR**

**APB SEQR**

**AHB**

**SEQR**



**APB SEQR**

**AHB SEQR**

**APB MON**

**APB DRV**

**AHB MON**

**AHBDRV**

**APB SEQR**

**AHB**

**SEQR**

**static AHB interface static APB interface**

**DUV**

**FEATURES:**

* HRESETn, PRESETn active low asynchronous reset for AHB signals.
* HTRANS 00 IDLE

01 BUSY

10 NONSEQ

11SEQ

* HSIZE 000 8bits

001 16bits

010 32bits

011 64bits

100 128bits

101 256bits

110 512bits

111 1024bits

* HBURST 000 SINGLE

001 INCR

010 WREADY

011 INCR4

100 WRAP8

101 INCR8

110 WRPA16

111 INCR16

* HREADY- when LOW then HADDR and HWDATA are extended
* PENABLE- HIGH at every second clock cycle of transfer
* HWRITE- HIGH during WRITE transfer from AHB TO APB

LOW during READ transfer from AHB to APB

* PWRITE- HIGH during WRITE transfer from APB to AHB

LOW during READ transfer from APB to AHB

* PSEL – HIGH during READ or WRITE transfer

**TRANSACTORS:**

* AHB Agent - drives WRITE transfer signals to bridge and monitors READ signals from bridge.
* APB Agent – drives WRITE transfer signals (to AHB) to bridge monitors READ transfer signals (from APB) from bridge.
* Virtual Sequencer, Virtual Sequence
* Scoreboard compares AHB monitor and APB monitor transfers.

**COVERAGE:**

* **AHB COVERAGE**

Coverpoint HWDATA [31:0]

Coverpoint HADDR [31:0]

Coverpoint HWRITE

Coverpoint HTRANS

Coverpoint HRDATA [31:0]

Cross HADDR \* HWRITE \* HTRANS

* **APB COVERAGE**

Coverpoint PWDATA [31:0]

Coverpoint PADDR [31:0]

Coverpoint PWRITE

Coverpoint PSEL

Coverpoint PENABLE

Coverpoint PRDATA [31:0]

Cross PADDR \* PWRITE \* PSEL

* **TESTCASES**

Sequential burst transfer

Non sequential burst transfer

Single transfer

Combination of both sequential and non-sequential burst transfers