AXI Slave Module Specification Sheet

1. Overview

This AXI slave module is designed to interface with an AXI master to facilitate read and write operations. It conforms to the AXI3/AXI4 protocol and supports multiple channels for address, data, and response communication.

2. Features

- Protocol Support: AXI3/AXI4
- Burst Types: Fixed, Incremental, Wrapping
- Data Transfer Sizes: 1, 2, 4 bytes
- Burst Lengths: AXI4 (1-256)
- Unique Transaction IDs

3. Signal Description

Global Control Signals

Signal Name	Direction	Description
clk	Input	Clock signal for synchronous operations.
resetn	Input	Active-low reset signal.

Write Address Channel

Signal Name	Direction	Description
Awvalid	Input	Indicates that the master is sending a new address.
awready	Output	vice Indicates that the slave is ready to accept the address.
Awid[3:0]	Input	Unique ID for each transaction.
awlen[3:0]	Input	Burst length.

awsize[2:0]	Input	Transaction size.
Awaddr[31:0]	Input	Write address of the transaction.|
Awburst[1:0]	Input	Burst type (fixed, INCR, WRAP).

Write Data Channel

Signal Name	Direction	Description
wvalid	Input	Indicates that the master is sending new data.
wready	Output	Indicates that the slave is ready to accept data.
Wid[3:0]	Input	Unique ID for each transaction.
Wdata[31:0]	Input	Data being written.
wstrb	Input	Indicates which lanes have valid data.
wlast	Output	Last transfer in the write burst

Write Response Channel

Signal Name	Direction	Description
bready	Input	Master is ready to accept the response.
bvalid	Output	Slave has a valid response.
Bid[3:0]	Output	Unique ID for the transaction.
Bresp[1:0]	Output	Status of the write transaction.

Read Address Channel

Signal Name	Direction	Description
arready	Output	Read address ready signal from the slave.
Arid[3:0]	Input	Read address ID.
Araddr[31:0]	Input	Read address signal.
Arlen[3:0]	Input	Length of the burst.
Arsize[2:0]	Input	Number of bytes in a transfer.
arburst	Input	Burst type (fixed, incremental, wrapping).
arvalid	Input	Address read valid signal.

Read Data Channel

Signal Name	Direction	Description
rid[3:0]	Output	Read data ID.
Rdata[31:0]	Output	Read data from the slave.
Rresp[1:0]	Output	Read response signal.
Rlast	Output	Last transfer in the read burst.
rvalid	Output	Read data valid signal.
rready	Output	Master is ready to accept the data.

4. FSM States

The module includes finite state machines (FSMs) for managing write address, write data, and write response channels.

- Write Address FSM:
  - awidle: Idle state.
  - awstart: Start state, waiting for awvalid.
  - awreadys: Ready state, storing address.

- Write Data FSM
  - (States would follow the similar pattern as Write Address FSM)

- Write Response FSM:

  - (States would follow the similar pattern as Write Address FSM)

5. Compliance

This module adheres to the AXI4 specifications, ensuring compatibility with industry-standard AXI masters.