– CSE –

I Design a most optimal interface circuit with 8051 to meet the following requirement.

i) 2K x 8bit ROM – 3 NO.s (Code Memory)
ii) 4K x 8bit RAM – 4 NO.s (Data Memory)
iii) Two, Single bit Switches and two, Single bit LEDs.

– 20M

II) Design a most optimal interface circuit, with all intermediate logic CKTs., using the following device, for 8085 processor

i) 4K x 4bit RAM – 5 NO.s
ii) 2K x 4bit ROM – 2 NO.s
iii) 2K x 8bit ROM – 1 NO.
iv) A Single bit Switch at FFE0
v) A Single bit LED at FFD0
vi) A printer at address F8H

– 20M

iii) With a neat timing diagram, explain DCX instruction, in detail. If the periodicity of clock is 0.5μs, how much time the processor takes to execute the instruction? — 10M

iv) With an algorithm and ALP for 8085, implement "Bubble Sort" algorithm. Explain the program using an example. — 10M

v) Write an ALP for 8085, with an algorithm to implement a 'PULSE WAVE' with ON time — 20ms and OFF time 2 sec. — 10M

vi) With a neat block schematic representation, explain "Mirror memory" or "fold-back memory" in 8085. What are its advantages and disadvantages — 10M

vii) Write Short notes on

a) The architecture of 8085 processor.
b) Computer - A digital State machine.
c) Instruction cycle, M/c cycle and T-states
d) Addressing modes — 20M