| Roll No | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|

# राष्ट्रीय प्रौधोगिकी संस्थान गोवा

# NATIONAL INSTITUTE OF TECHNOLOGY GOA

Farmagudi, Ponda, Goa, 403401

Programme Name: B.Tech.

End Semester Examinations, December-2020

Course Name: Operating Systems | Course Code: CS300

Date: 22/12/2020 | Time: 2:30- 5:30 PM

Duration: 03 Hours | Max. Marks: 100

ANSWER ALL QUESTIONS

**Q.1** **a.** Differentiate kernel mode and user mode function in context of protection (security) system? **[03 Marks]**

**b.** A variable V=0 is shared by four concurrent processes A, B, C, D. The processes A and B reads V from memory and increments it by one, stores it to memory, and then terminates. The processes C and D reads V from memory and decrements it by two, stores it to memory, and then terminates. Before reading V, each process invokes the wait operation on a counting semaphore S and invokes the signal operation on the semaphore S after storing V to memory. Semaphore S is initialized to two. What is the maximum possible value of V after all processes complete execution? **[04 Marks]**

**c.** Consider three CPU-intensive processes require 10, 20 and 30 time respectively and they arrive at 0, 2 and 6 time respectively. If OS implements shortest remaining time first scheduling algorithm, how many context switches are needed? Justify your answer. **[05 Marks]**

**d.** Differentiate capability lists and access lists. **[03 Marks]**

**Q.2** **a.** Consider a computer with 46 bit virtual address, 32–bit physical address, and a three–level paged page table organization. The page table base register stores the base address of the first–level table (T1), which occupies exactly one page. Each entry of T1 stores the base address of a page of the second–level table (T2). Each entry of T2 stores the base address of a page of the third–level table (T3). Each entry of T3 stores a page table entry (PTE). The PTE is 32 bits in size. The processor used in the computer has a 1 MB 16 way set associative virtually indexed physically tagged cache. The cache block size is 64 bytes. What is the size of a page in KB in this computer? **[10 Marks]**

**b.** Consider a disk with 16 recording surfaces (0-15) having 16384 cylinders (0-16383) and each cylinder has 64 sectors (0-63). Each sector can store 512 bytes. Data are organized cylinder-wise. A file of size 42797 KB is stored in the disk and the starting disk location of the file is <1200, 9, 40>. What is the cylinder number of the last sector of the file, if it is stored in a contiguous manner? **[10 Marks]**

**Q.3** **a.** A computer has six tape drives and m processes which are competing for tape drives. Each process may need two drives. What is the maximum value of m for the system to be deadlock free? **[05 Marks]**

**b.** Consider the following page reference string: 1, 2, 3, 4, 2, 1, 5, 6, 2, 1, 2, 3, 7, 6, 3, 2, 1, 2, 3, 6. How many page faults would occur for the following replacement algorithms? LRU replacement, FIFO replacement and Optimal replacement. Assume three, five and seven frames. **[09 Marks]**

**c.** Consider a demand paging based system, in which the degree of multiprogramming is fixed at four. The system is measured to determine utilization of CPU and the paging disk. The results are one of the following alternatives. For each case, what is happening? Can the degree of multiprogramming be increased to increase the CPU utilization? Is the paging helping? **[06 Marks]**

Case 1. CPU utilization 13 percent; disk utilization 97 percent
Case 2. CPU utilization 87 percent; disk utilization 3 percent
Case 3. CPU utilization 13 percent; disk utilization 3 percent

**Q.4** **a.** Consider a single level paging scheme with a TLB. Assume no page fault occurs. It takes 20 ns to search the TLB. If TLB hit ratio is 50% and effective memory access time is 170 ns, what is the main memory access time? **[07 Marks]**

**b.** Consider a disk with 4 platters (0 to 3), 200 cylinders (0 to 199), and 256 sectors per track (0 to 255). Consider the following 6 disk requests of the form [sector number, cylinder number, platter number] are received by the disk controller at the same time: [120, 72, 2], [180, 134, 1], [60, 20, 0], [212, 86, 3], [56, 116, 2], [118, 16, 1]. Currently head is positioned at sector number 100 of cylinder 80, and is moving towards higher cylinder numbers. The average power dissipation in moving the head over 100 cylinders is 20 milliwatts and for reversing the direction of the head movement once is 15 milliwatts. Power dissipation associated with rotational latency and switching of head between different platters is negligible. Calculate the total power consumption in milliwatts to satisfy all of the above requests using the Shortest Seek Time First disk scheduling algorithm? **[08 Marks]**

**Q.5** **a.** Consider a paging system that uses 1-level page table stored in main memory and a TLB for address translation. Each main memory access takes 100 ns and TLB lookup takes 20 ns. Each page transfer to/from the disk takes 5000 ns. Assume that the TLB hit ratio is 95%, page fault rate is 10%. Assume that for 20% of the total page faults, a dirty page has to be written back to disk before the required page is read from disk. TLB update time is negligible. What is an average memory access time in ns? **[08 Marks]**

**b.** Consider a file consists of 100 blocks. Assume that the file control block (and the index block, in the case of indexed allocation) is already in memory. Calculate how many disk I/O operations are required for contiguous, linked, and indexed (single-level) allocation strategies, if, for one block, the following conditions hold? In the contiguous-allocation case, assume that there is no room to grow at the beginning but there is room to grow at the end. Also assume that the block information to be added is stored in memory. **[12 Marks]**

a. The block is added at the beginning.
b. The block is added in the middle.
c. The block is added at the end.
d. The block is removed from the beginning.
e. The block is removed from the middle.
f. The block is removed from the end.

**c.** Differentiate capability lists and access lists. **[05 Marks]**

**d.** What is thrashing? How to address thrashing problem. **[05 Marks]**

----------ALL THE BEST----------