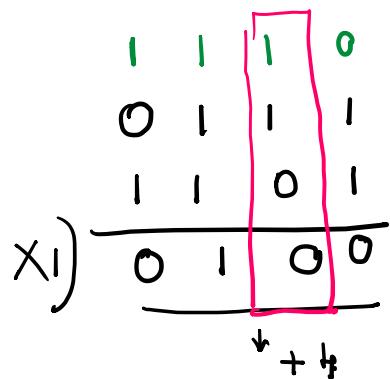


DESIGN ADDERS

- 2's complement
- 1-bit addition
- n-bit addition

$$\begin{array}{r}
 x \\
 + y \\
 \hline
 z \\
 c
 \end{array}
 \quad
 \begin{array}{r}
 +7 \\
 +(-3) \\
 \hline
 +4
 \end{array}$$



$$\begin{array}{c}
 C_{i+1} \quad C_i \\
 \bar{x}_i \\
 y_i \\
 \hline
 s_i
 \end{array}$$

\bar{x}_i	y_i	C_i	s_i	$\bar{x}_i y_i C_i$	C_{i+1}	
0	0	0	0	$\bar{x}_i y_i C_i$	0	
0	0	1	1	$\bar{x}_i \bar{y}_i C_i$	0	
0	1	0	1	$\bar{x}_i y_i \bar{C}_i$	0	
0	1	1	0	$\bar{x}_i y_i C_i$	1	
1	0	0	1	$x_i \bar{y}_i \bar{C}_i$	0	
1	0	1	0	$x_i \bar{y}_i C_i$	1	$x_i C_i$
1	1	0	0	$x_i y_i C_i$	1	$x_i y_i$
1	1	1	1	$x_i y_i C_i$	1	$y_i C_i$

$$S_i = \bar{x}_i \bar{y}_i c_i + \bar{x}_i y_i \bar{c}_i + x_i \bar{y}_i \bar{c}_i + x_i y_i c_i$$

$$S_i = \bar{x}_i + y_i + c_i$$



$2T$

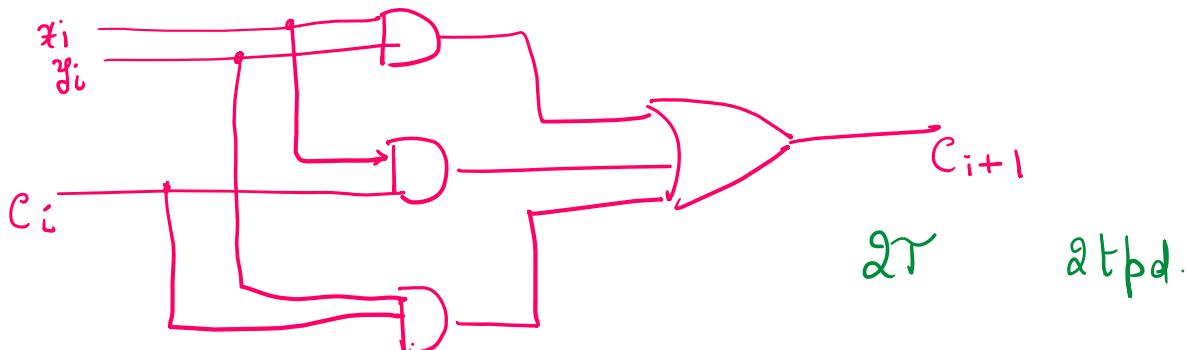
$2t_{pd}$

T : Propagation delay through a logic gate

$$C_{i+1} = \bar{y}_i c_i + x_i c_i + \bar{x}_i y_i$$

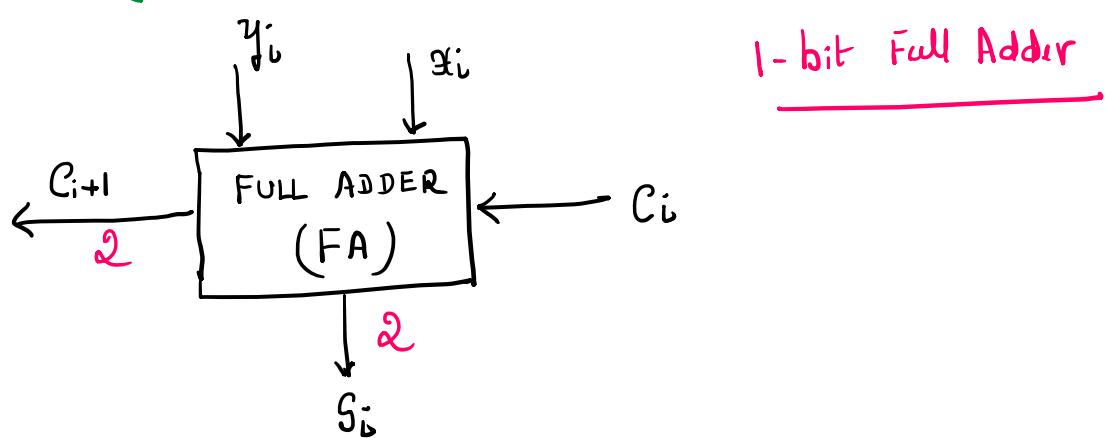
$$C_{i+1} = \bar{x}_i y_i + x_i c_i + \bar{y}_i c_i$$

$T \approx t_{pd}$



Delay through a digital circuit:

Ripple X
 Component \rightarrow IC \rightarrow Gate Propagation Delay
 - No of gate propagation levels

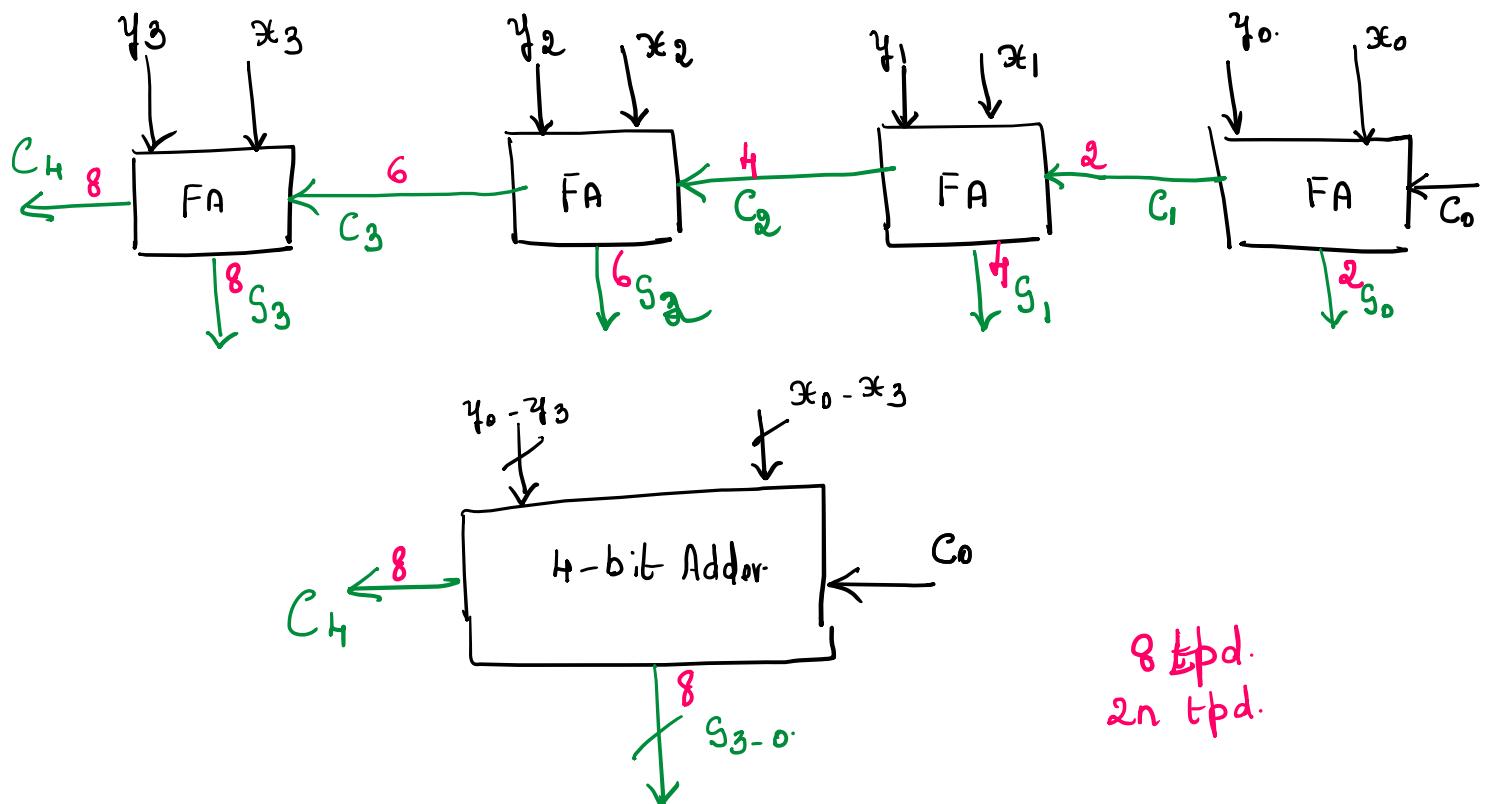
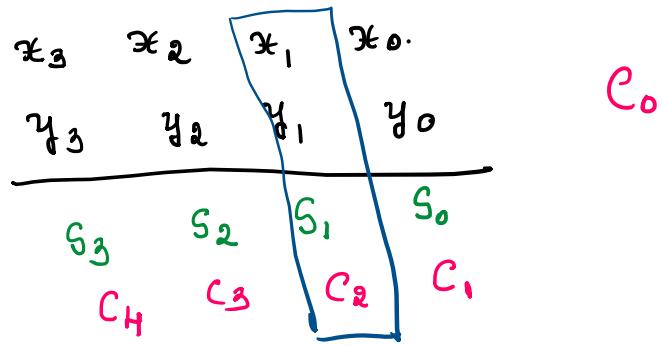


n-bit Addition

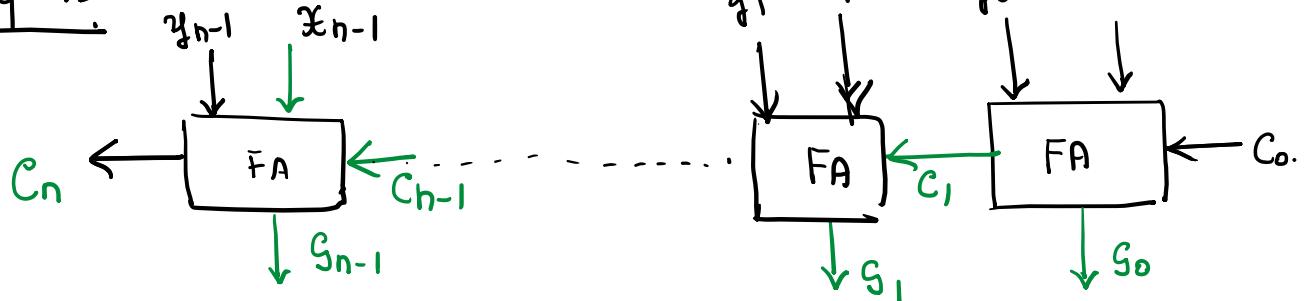
$$\begin{array}{r} 7 \\ + (-3) \\ \hline 4 \end{array}$$

$$\begin{array}{r} 1110 \\ 0111 \\ \hline 1101 \\ \hline 0100 \end{array}$$

$n=4$ x, y
 Ripple Carry (RCA) Adder



Arbitrary n



$2n t_{pd}$

Overflow

i) Unsigned number addition:

$$C_n = 1$$

2) Signed addition

- x, y have same sign } SOP $\begin{matrix} x_{n-1} \\ y_{n-1} \\ s_{n-1} \end{matrix}$
 - s has different sign }

$$O_{\text{Overflow}} = x_{n-1} y_{n-1} \overline{s_{n-1}} + \overline{x_{n-1}} \overline{y_{n-1}} s_{n-1}$$

$x_i y_i \geq 0$
 $x_i s_i \leq 0$

- C_{n-1}, C_n : They are different

C_n	C_{n-1}	Overflow
0	0	0
0	1	1
1	0	1
1	1	0

$O_{\text{Overflow}} = C_n \oplus C_{n-1}$

2-bit pd.

RCA:

$$\underline{2n + 2 \text{ bit pd.}}$$

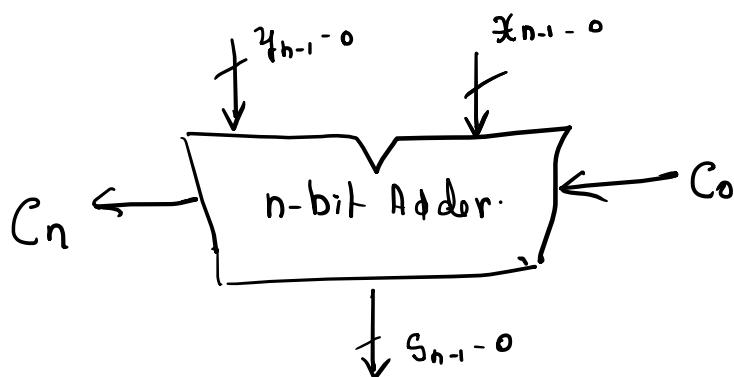
$$\underline{2n}$$

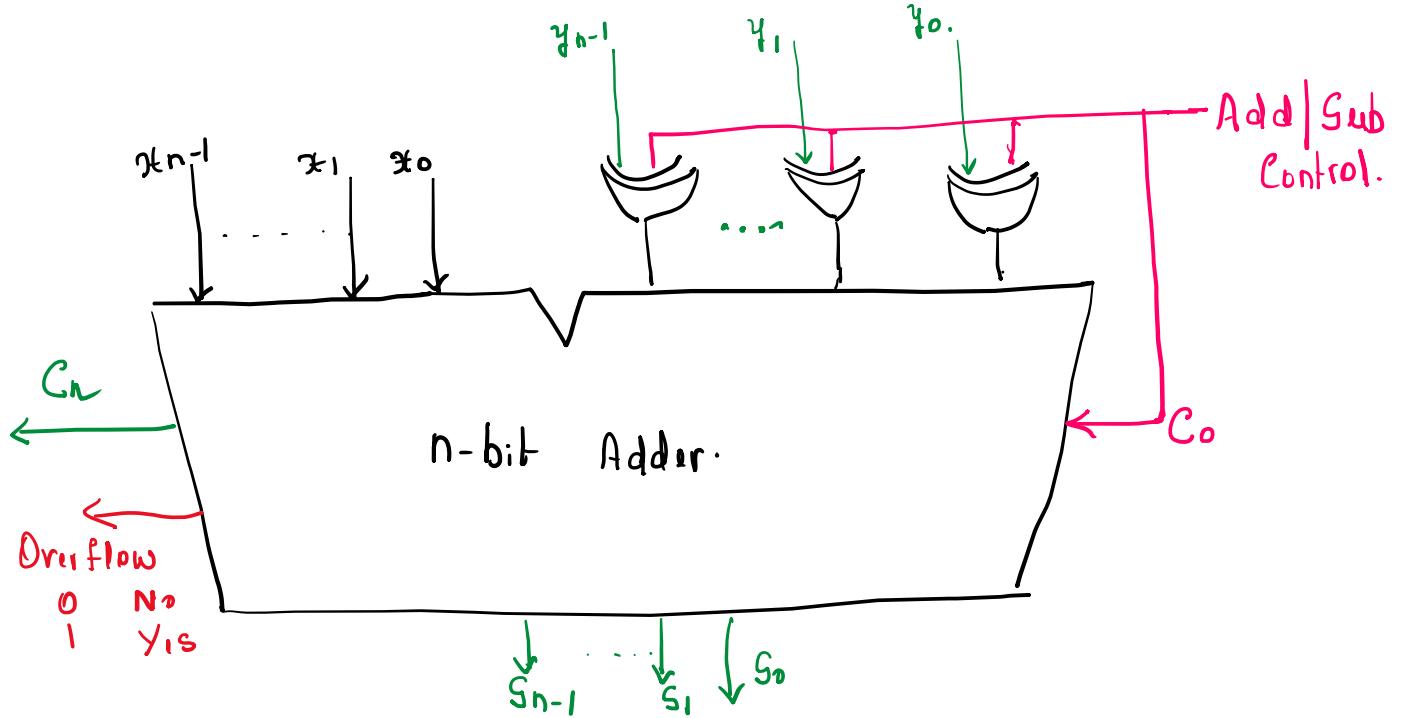
Subtraction

$$x - y \Rightarrow \underline{x + y''}$$

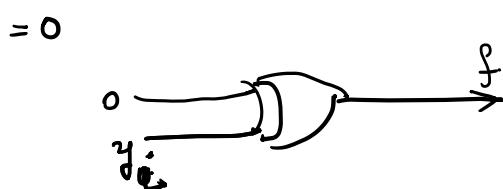
$$x + y$$

$$x - y$$





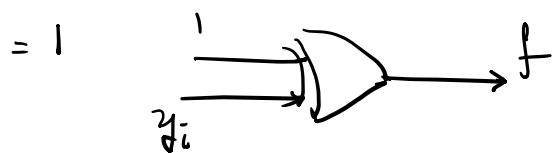
Add/Sub Control.



0	y_i	f
0	0	0
0	1	1

$$f = y_i$$

No complement



1	y_i	f
1	0	1
1	1	0

$$f = \bar{y}_i$$

Complemented.

Add/Sub

$y_{n-1} \dots y_2 y_1 y_0$

$\bar{y}_{n-1} \dots \bar{y}_2 \bar{y}_1 \bar{y}_0$

$\textcircled{1} C_o$

y

n -bit RCA

- Addition
- Subtraction

1-bit FA
↓
 n -bit

8-bit 1 bit
 4 bit
 1 bit
16-bit 4 bit
 8-bit

$2n$ tpd : Dday through n -bit RCA

$n=4$ 8 tpd.
 $n=32$ 64 tpd.

} Very large. → Reduce Dday.

Approach 1

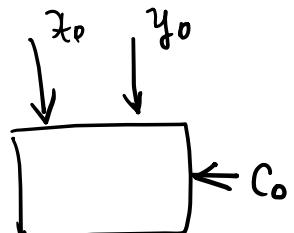
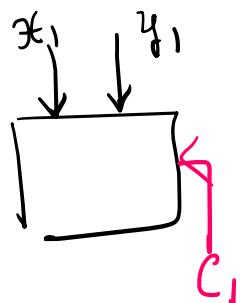
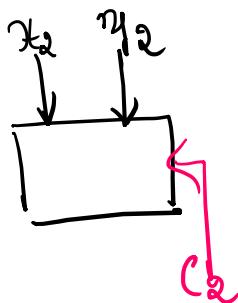
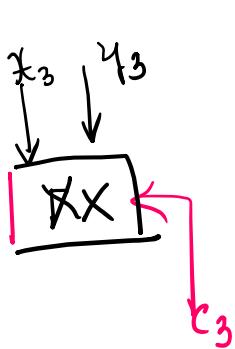
Fastest possible electronic technology

8 tpd. γ

Approach 2

Augmented logic gate network

RCA → $2n$



↑

6 tpd. → c3

8 tpd.

m tpd. << 6

Carry Look-Ahead Adder (CLA)

- Carry generation Process

$$G_i = x_i \oplus y_i \oplus c_i$$

$$C_{i+1} = x_i y_i + x_i c_i + y_i c_i$$

$$= \frac{x_i y_i}{G_i} + \frac{(x_i + y_i) c_i}{P_i}$$

$$\boxed{C_{i+1} = G_i + P_i c_i}$$

Stage i
 G_i : Generator
 P_i : Propagator } Carry

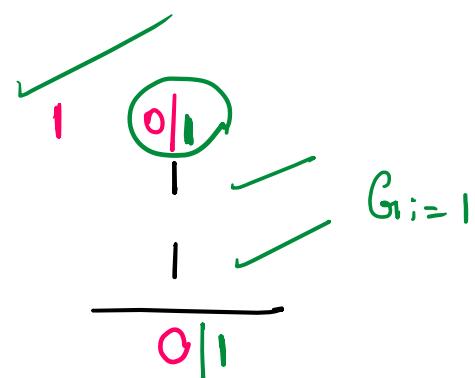
G_i : Generator

$$G_i = x_i y_i$$

$$\underline{G_i = 1}, \quad C_{i+1} = 1 \quad \text{irrespective of } c_i$$

$$x_i = 1 \quad y_i = 1$$

$$\begin{array}{r} c_{i+1} \quad c_i \\ x_i \quad y_i \\ \hline g_i \end{array}$$



P_i : Propagator

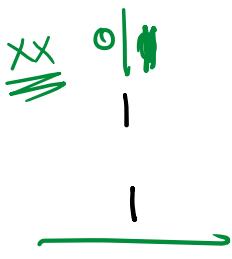
$$P_i = x_i + y_i$$

$$P_i = 1 \quad x_i = 1 \quad | \quad y_i = 1$$

$$\begin{array}{r} 0 \quad 0 \\ | \\ \hline 0 \end{array}$$

$$\begin{array}{r} 1 \quad 1 \\ | \\ \hline 0 \end{array}$$

$$P_i = 1 \quad C_{i+1} = 1, \quad C_i = 1$$



$$x_i = 1, \quad y_i = 1$$

$$G_{i+1}$$

$$n = 4$$

$$\begin{array}{cccc} x_3 & x_2 & x_1 & x_0 \\ y_3 & y_2 & y_1 & y_0 \\ \hline s_3 & s_2 & s_1 & s_0 \\ c_4 & c_3 & c_2 & c_1 \end{array}$$

$$C_{i+1} = G_i + P_i C_i$$

$$G_0 = x_0 y_0$$

$$P_0 = x_0 + y_0$$

$$C_1 = G_0 + P_0 C_0$$

$$G_1 = x_1 y_1$$

$$P_1 = x_1 + y_1$$

$$\begin{aligned} C_2 &= G_1 + P_1 C_1 \\ &= G_1 + P_1 [G_0 + P_0 C_0] \\ &= G_1 + P_1 G_0 + \underline{P_1 P_0 C_0} \end{aligned}$$

$$G_2 = x_2 y_2$$

$$P_2 = x_2 + y_2$$

$$\begin{aligned} C_3 &= G_2 + P_2 C_2 \\ &= G_2 + P_2 G_1 + P_2 P_1 G_0 + \\ &\quad \underline{P_2 P_1 P_0 C_0} \end{aligned}$$

$$G_3 = x_3 y_3$$

$$P_3 = x_3 + y_3$$

$$C_4 = G_3 + P_3 C_3$$

$$\begin{aligned} &= G_3 + P_3 G_2 + P_3 P_2 G_1 \\ &\quad + P_3 P_2 P_1 G_0 + \underline{P_3 P_2 P_1 P_0 C_0} \end{aligned}$$

All G_i and P_i functions can be generated - 1 tpd.

1 - logic gate

Once G_i, P_i s are available.
2 tpd. $\rightarrow C_{i+1}$

Approach 1

$$G_{ii}, P_i, C_{i+1}, G_i$$

Approach 2

$$P_i = x_i + y_i$$

$$P_i = 1$$

$$\left. \begin{array}{ll} x_i = 1 & y_i = 0 \\ x_i = 0 & y_i = 1 \end{array} \right\} x_i \oplus y_i$$

$$P_i = x_i \oplus y_i$$

$$P_i = 1$$

$$\frac{x_i = 1 \quad y_i = 1}{P_i = 0}$$

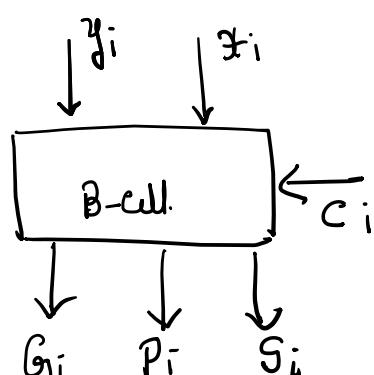
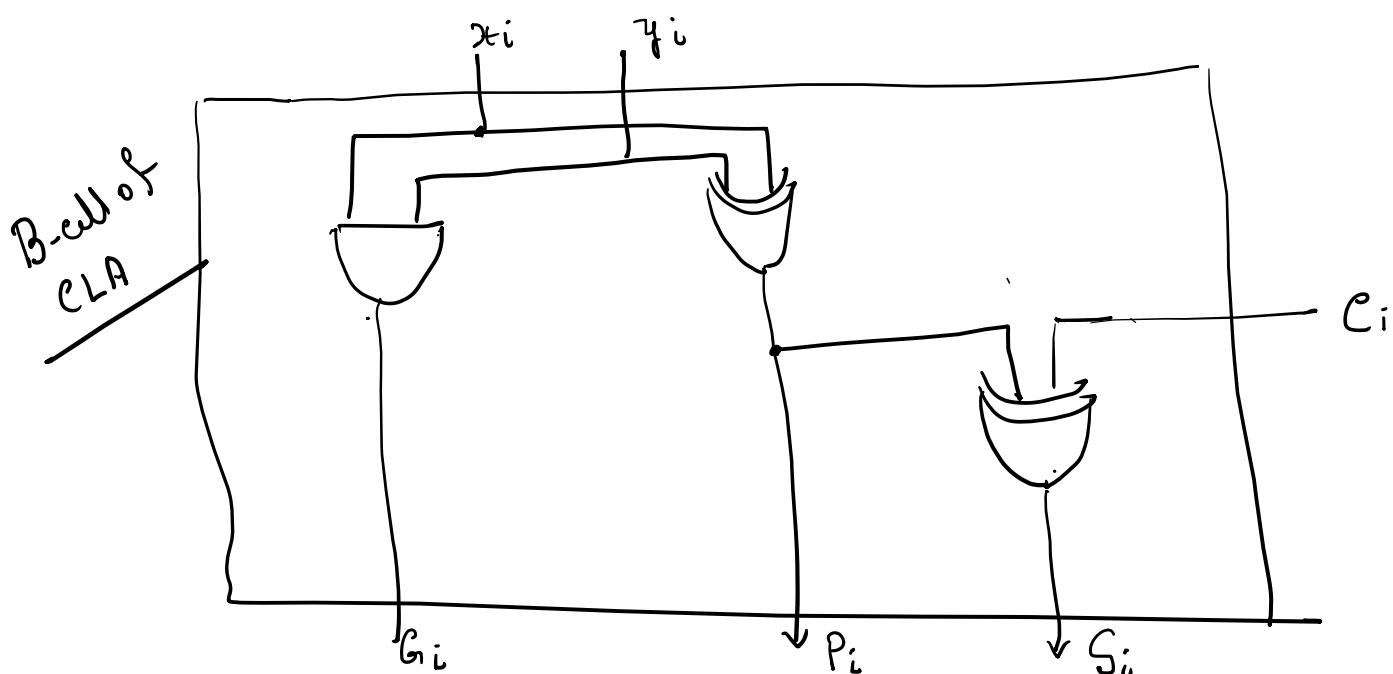
$$\frac{x_i = 0 \quad y_i = 1}{x_i \oplus y_i}$$

$\hookrightarrow G_i = 1$

$$G_i = x_i \oplus y_i \oplus C_i$$

$$S_i = P_i \oplus C_i$$

$$P_i = x_i \oplus y_i$$



4-bit CLA : 4 B-cells

Delay through the n-bit CLA

16-bit CLA → 16 B cells ←
→ 4-bit CLA