

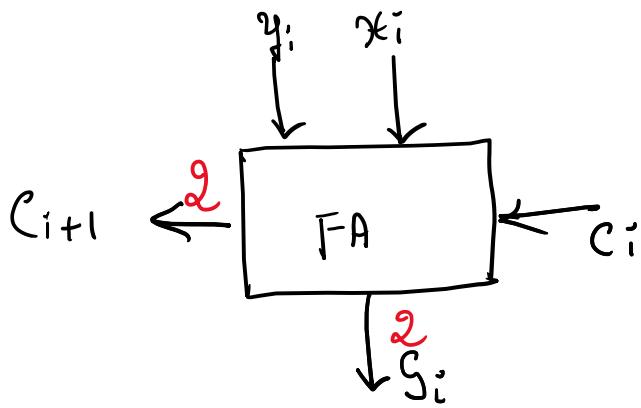
ARITHMETIC CIRCUITS

- Adders - subtractors
- 1-bit adder \rightarrow FA
- n -bit adders \Rightarrow n FAs
- Overflow
- Adder circuit/network \rightarrow Subtraction

Delay through a Circuit

- Electronic technology used (IC) in designing of logic gate
- Number of gates in the path from input to outputs
- Number of logic-gate delays along the longest signal propagation path through the network
 - 1 logic level : $1 \frac{t_{pd}}{}$

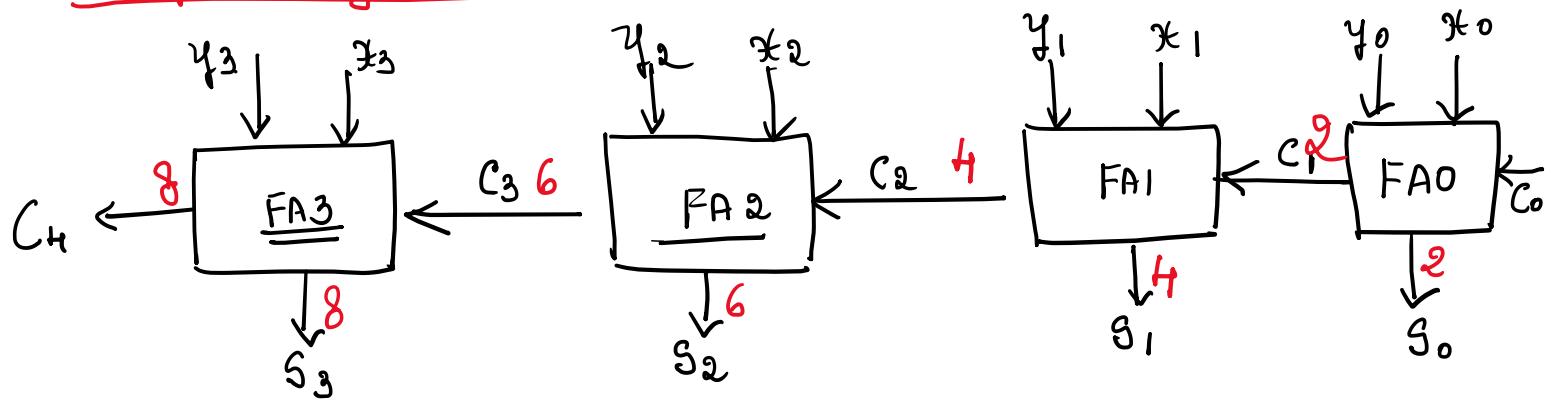
Delay through a FA



$$C_{i+1} : S_0 P \\ : 2 t_{pd.}$$

$$S_i = x_i \oplus y_i \oplus c_i \\ : 2 t_{pd.}$$

Delay through a RCA : 4-bit



Delay through a 4-bit RCA : $8t_{pd}$
 $= \underline{2} \times 4 t_{pd}$

n-bit RCA : $2n t_{pd}$

Overflow : $C_n \oplus C_{n-1}$ } $2 t_{pd}$
 $2n+2 t_{pd}$

Delay through a n-bit RCA : $2n t_{pd}$.

Higher.

Approaches to reduce the delay

① Fastest possible electronic technology in implementing RCA

② Augmented Circuit

- Inspect : What is causing the delay.

→ Carry propagation one level to other bit position to next

↑
Precompute carry

Carry Look Ahead Adder → CLA

- Spend up carry generation
 - Propagation of carry

$$S_i = x_i \oplus y_i \oplus C_i$$

$$\begin{aligned} C_{i+1} &= x_i y_i + x_i C_i + y_i C_i \\ &= \frac{x_i y_i}{G_i} + \frac{(x_i + y_i) C_i}{P_i} \end{aligned}$$

$$\underline{C_{i+1} = G_i + P_i C_i}$$

$$G_i = x_i y_i \quad \text{Generate function}$$

$$P_i = x_i + y_i \quad \text{Propagate function}$$

For bit position
 $\frac{i}{\text{stage } i}$

Generate function

$$C_{i+1} = G_i + P_i C_i$$

$$G_i = 1 \quad C_{i+1} = 1 \quad \text{irrespective of } C_i$$

$$G_i = x_i y_i \quad G_i = 1 \Rightarrow x_i = 1 \quad y_i = 1$$

$$G_i = \begin{cases} 0 & \\ 1 & \end{cases}$$

$$\begin{array}{c} x_i = 1 \\ y_i = 1 \\ \hline S_i & 0 \\ C_{i+1} & 1 \end{array}$$

$$\begin{array}{c} x_i = 1 \\ y_i = 1 \\ \hline S_i & 1 \\ C_{i+1} & 1 \end{array}$$

Propagate function

$$C_{i+1} = G_i + P_i C_i$$

$$P_i = x_i + y_i \quad P_i = 1, \quad x_i = 1 \quad \left| \begin{array}{l} y_i = 1 \\ x_i = 1, y_i = 1 \end{array} \right.$$

\downarrow

$$C_{i+1} = 1 \quad \text{if} \quad C_i = 1$$

$C_i \quad $ $x_i \quad 1$ $y_i \quad 0$ \hline $S_i \quad 0$ $C_{i+1} \quad 1$	$C_i \quad $ $x_i \quad 0$ $y_i \quad 1$ \hline $S_i \quad 0$ $C_{i+1} \quad 1$	$C_i \quad $ $x_i \quad 1$ $y_i \quad 1$ \hline $S_i \quad 1$ $C_{i+1} \quad 1$
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$$P_i \neq 1 \quad \begin{array}{r} x_i \quad 0 \\ y_i \quad 0 \\ \hline S_i \quad 1 \\ C_{i+1} \quad 0 \end{array}$$

$P_i = \underline{\text{Propagate function}}$

n-bit Adder

4-bit adder

$$\begin{array}{r} X \quad x_3 \quad x_2 \quad x_1 \quad x_0 \\ Y \quad y_3 \quad y_2 \quad y_1 \quad y_0 \\ \hline S \quad s_3 \quad s_2 \quad s_1 \quad s_0 \\ C \quad c_4 \quad c_3 \quad c_2 \quad c_1 \end{array}$$

$$G_0 = x_0 y_0 \quad P_0 = x_0 + y_0 \quad \underline{C_1} = G_0 + P_0 C_0$$

$$G_1 = x_1 y_1 \quad P_1 = x_1 + y_1 \quad \underline{C_2} = G_1 + P_1 C_1 \\ = G_1 + P_1 [G_0 + P_0 C_0] \\ = G_1 + P_1 G_0 + P_1 P_0 \underline{C_0}$$

$$G_2 = x_2 y_2 \quad P_2 = x_2 + y_2 \quad \underline{C_3} = G_2 + P_2 C_2 \\ = G_2 + P_2 G_1 + P_2 P_1 G_0 \\ + P_2 P_1 P_0 \underline{C_0}$$

$$G_3 = x_3 y_3 \quad P_3 = x_3 + y_3 \quad \underline{C_4} = G_3 + P_3 C_3 \\ = G_3 + P_3 G_2 + P_3 P_2 G_1 \\ + P_3 P_2 P_1 G_0 \\ + P_3 P_2 P_1 P_0 \underline{C_0}$$

P_i, G_i : 1 Gate delay

2 levels of logic

2 tpd.

3 tpd's: $C_1 \ C_2 \ C_3 \ C_4$

Design ①

C_{iS}

$$G_i = x_i \oplus y_i \oplus C_i$$

↳ 3 input XOR gate.

Design ②

$$P_i = x_i + y_i$$

$$P_i = \cancel{x_i + y_i}$$

$$P_i = 1$$

$$\begin{array}{ll} x_i = 1 & y_i = 0 \\ x_i = 0 & y_i = 1 \end{array}$$

$$\begin{array}{ll} x_i = 1 & y_i = 1 \end{array}$$

$$G_i = 1$$

$$C_{i+1} = \underline{G_i} + \underline{P_i C_i}$$

$$S_i = x_i + y_i + C_i$$

$$P_i = x_i + y_i$$

\checkmark XOR

$$\begin{array}{c} S_i = P_i + C_i \\ \hline T \end{array}$$

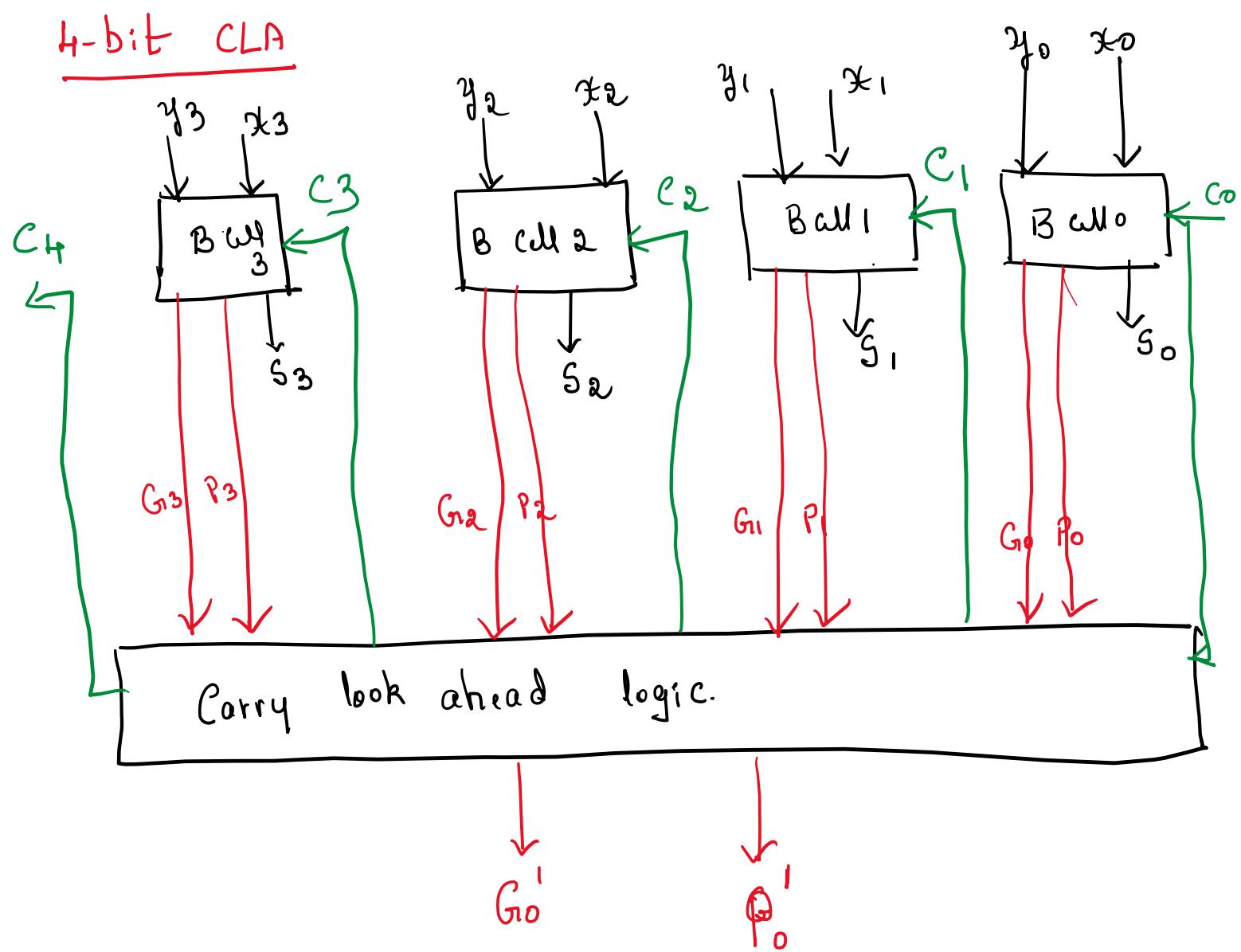
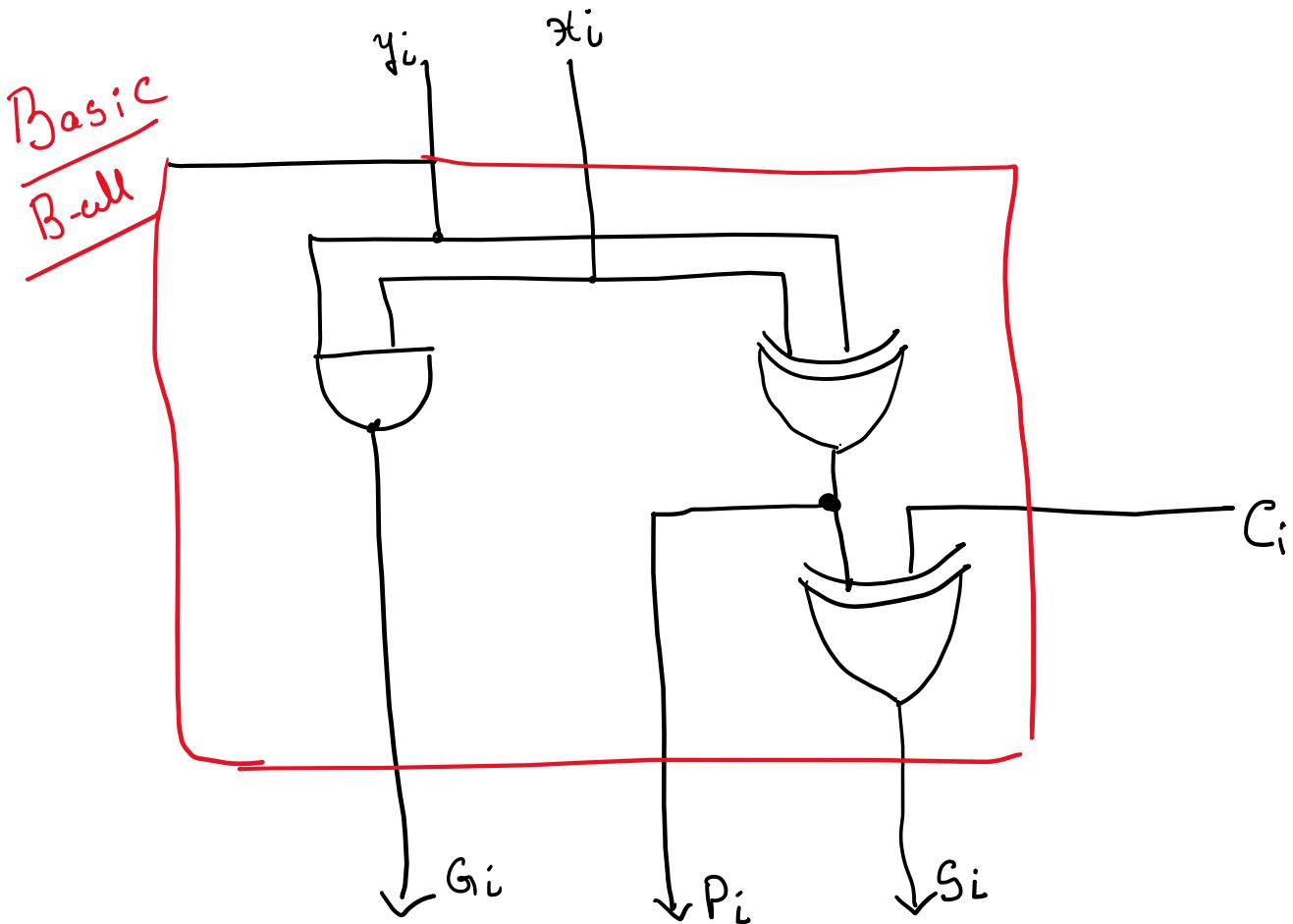
\checkmark XOR

$$P_i = x_i + y_i$$

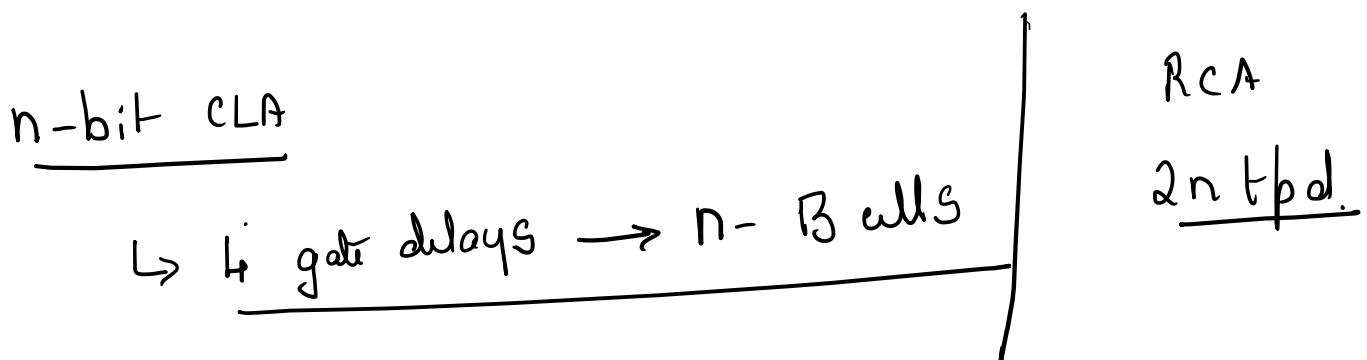
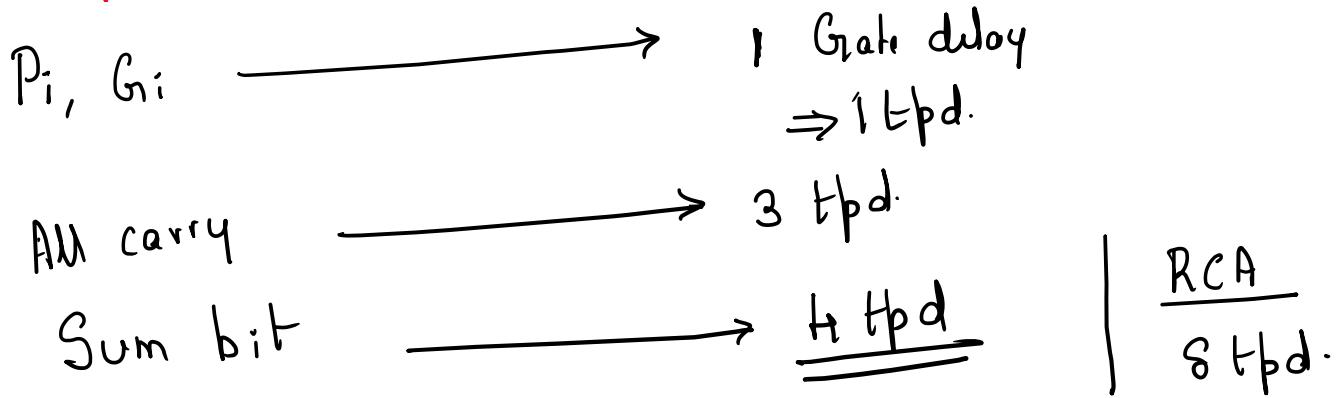
$$G_i = \underline{x_i + y_i}$$

AND \checkmark

Basic Cell - CLA



Delay through k-bit CLA



Extending to longer operands : 8-bit

$$C_4 = G_{13} + P_3 G_{12} + P_3 P_2 G_{11} + P_3 P_2 P_1 G_{10} + \underline{\underline{P_3 P_2 P_1 P_0 C_0}}^{15} \quad 5 \text{ tpd}$$

$$\begin{aligned} C_5 &= G_4 + P_4 C_4 \\ &= G_4 + P_4 G_{13} + P_4 P_3 G_{12} + P_4 P_3 P_2 G_{11} + P_4 P_3 P_2 P_1 G_{10} \\ &\quad + P_4 P_3 P_2 P_1 P_0 C_0 \end{aligned}$$

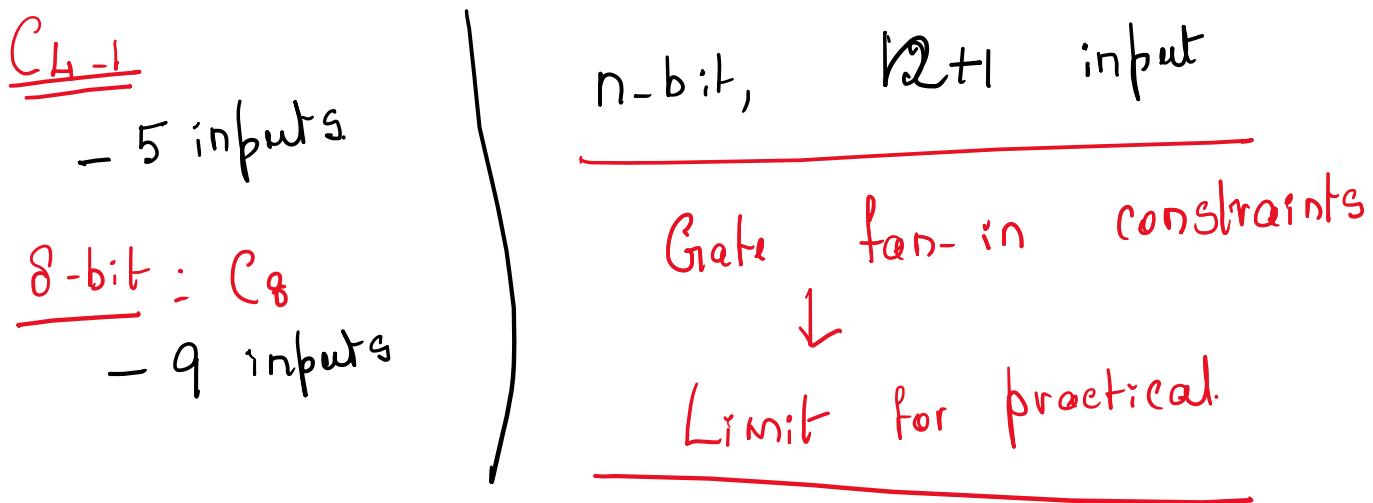
$$C_6 = G_5 + P_5 C_5$$

$$\begin{aligned} &= G_5 + P_5 G_{14} + P_5 P_4 G_{13} + P_5 P_4 P_3 G_{12} + P_5 P_4 P_3 P_2 G_{11} \\ &\quad + P_5 P_4 P_3 P_2 P_1 G_{10} + P_5 P_4 P_3 P_2 P_1 P_0 C_0 \end{aligned}$$

$$C_7 = G_6 + P_6 C_6$$

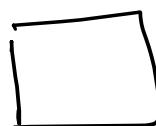
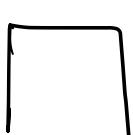
$$\begin{aligned}
 &= G_6 + P_6 G_{15} + P_6 P_5 G_{14} + P_6 P_5 P_4 G_3 + P_6 P_5 P_4 P_3 G_2 \\
 &\quad + P_6 P_5 P_4 P_3 P_2 G_1 + P_6 P_5 P_4 P_3 P_2 P_1 G_0 + P_6 P_5 P_4 P_3 P_2 P_1 P_0 C_0
 \end{aligned}$$

$$\begin{aligned}
 C_8 &= G_7 + P_7 C_7 \\
 &= G_7 + P_7 G_6 + P_7 P_6 G_5 + P_7 P_6 P_5 G_4 + P_7 P_6 P_5 P_4 G_3 + P_7 P_6 P_5 P_4 P_3 G_2 \\
 &\quad + P_7 P_6 P_5 P_4 P_3 P_2 G_1 + P_7 P_6 P_5 P_4 P_3 P_2 P_1 G_0 + \underline{P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0 C_0} \quad 9.
 \end{aligned}$$



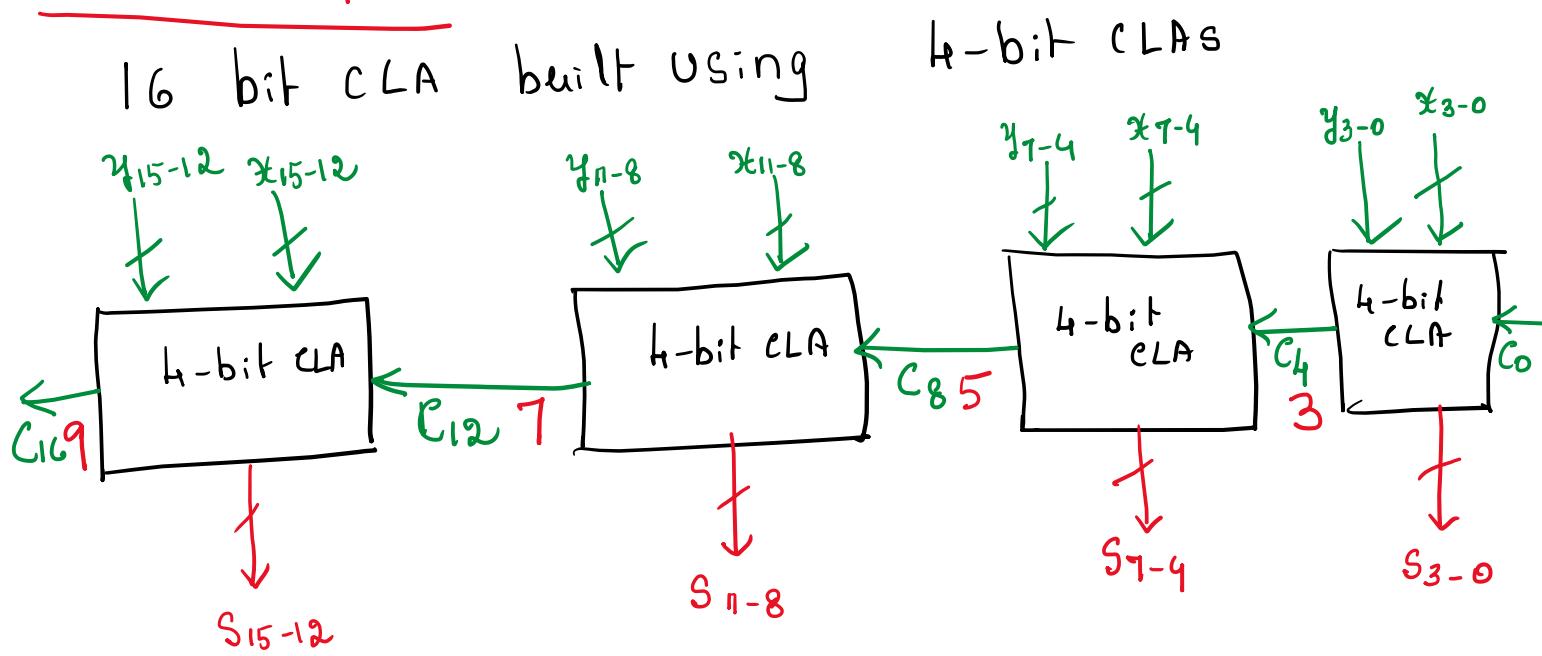
→ longer operands →

Suppose - l -bit CLA $\rightarrow l+1$ inputs		4 5
$\begin{array}{l} - n\text{-bit CLA} \\ \rightarrow l\text{-bit CLA} \\ - \frac{n}{l} = k \end{array}$		16 4-bit CLA $n = kl$ $k = 4$



Building a n -bit $\xrightarrow{\text{CLA}}$ Using k 1-bit CLA, $n = k \cdot l$.

Cascade style I \rightarrow Ripple Carry Style



$P_i, G_i \rightarrow$ 1 Gate delay

Initial Carry $\rightarrow C_4 \rightarrow 2 \text{ tpd}$ after P_i and G_i

Remaining Carry $\rightarrow C_8, C_{12}, C_{16} \rightarrow$ 2 tpd more
once the inputs
are available

$$\frac{9 \text{ tpd}}{(4-1) \times 2 + 3}$$

$$= \underline{\underline{9}}$$

Sum bit \rightarrow 11 additional gate delay
 $= \underline{\underline{10 \text{ tpd}}}$

RCA-16 bit $\Rightarrow \underline{\underline{32 \text{ tpd}}}$

Each stage: l -bit CLA

$$\text{No of stages: } k = \frac{n}{l}$$

$$\text{Carry generation: } \left(\frac{n}{l} - 1\right)2 + 3$$

$$\text{Sum} + 1$$

$$\begin{array}{c} \text{32-bit adder using } k \text{ bit CLAs} \\ \hline n = 32 \quad l = 4 \quad k = 8 \end{array}$$

$$C_i : \left(\frac{n}{l} - 1\right) \times 2 + 3 = \left(\frac{32}{4} - 1\right) 2 + 3 \\ = 14 + 3 \\ = \underline{\underline{17}}$$

$$S_i = 17 + 1 = \underline{\underline{18 \text{ tpd}}}$$

$$RCA : 32 \times 2 = \underline{\underline{64 \text{ tpd}}}$$

Design of Adders

Adder \rightarrow n-bit addition

$$\begin{array}{c} \text{RCA} \\ \hline \xrightarrow{\quad} \underline{2n \text{ tpd}} \end{array}$$

$$\begin{array}{c} \text{CLA} \\ \hline \frac{n=4}{P_i, G_i} \end{array}$$

Delay: $\frac{1}{4}$ tpd.

$$\begin{array}{c} P_i, G_i = \frac{1}{4} \\ S_i = \frac{1}{4} \\ \hline \end{array} \quad \left| \quad 2n - \text{RCA} \right.$$

✓

Longer operands
- Large 'n'

Gates fan-in constraint

$(n+1)$ input

n -bit Adder.

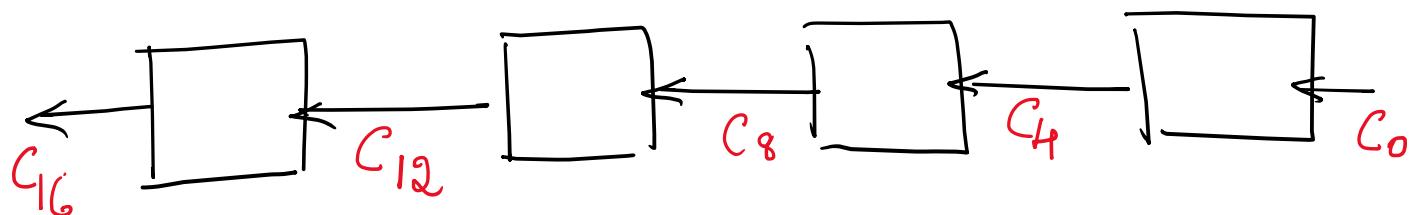
$n \rightarrow k \times l$
↳ l -bit CLA
 k of them

Cascade Style I - Ripple Carry way

$$n = 16$$

$$l = 4$$

$$k = 4$$



$$k = \frac{n}{l}$$

$$\left(\frac{n}{l} - 1\right) \times 2 + 3$$

16-bit

$$\text{RCA: } \underline{\underline{32}}$$

$$\text{CLA-1 : } \left(\frac{16}{4} - 1\right) 2 + 3 = \underline{\underline{9}}$$

Cascade Style II : Higher level
 Generate and Propagate
 function

→ Ripple carry cascade

→ C_4, C_8, C_{12}, C_{16} : AM in parallel

$$C_4 = \frac{G_3 + P_3 G_{12} + P_3 P_2 G_{11} + P_3 P_2 P_1 G_0}{G_0'} + \frac{P_3 P_2 P_1 P_0 C_0}{P_0'}$$

$$G_0' = G_3 + P_3 G_{12} + P_3 P_2 G_{11} + P_3 P_2 P_1 G_0$$

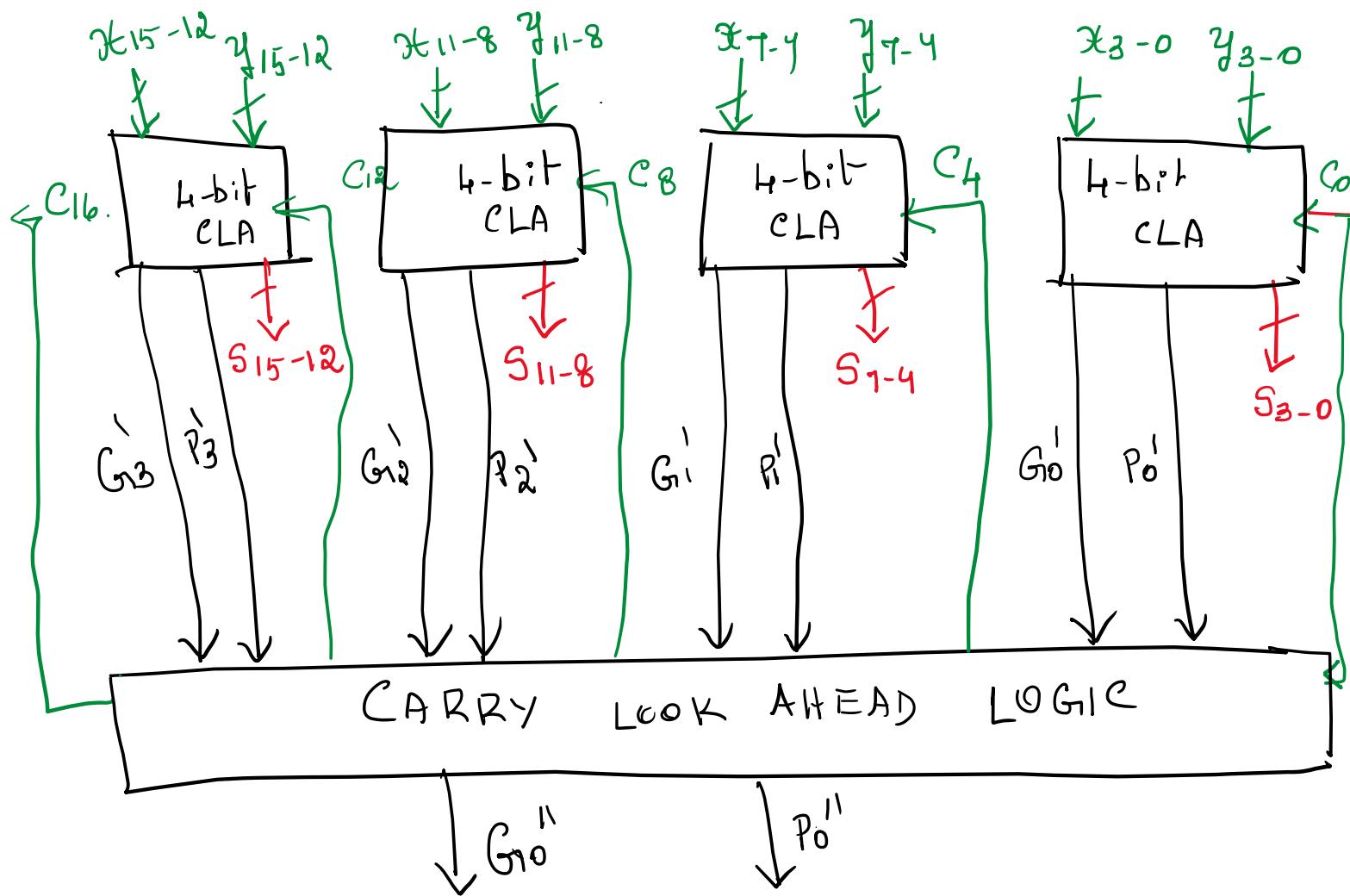
$$P_0' = P_3 P_2 P_1 P_0$$

$$C_4 = G_0' + P_0' C_0$$

P_i, G_i : First level propagate, generate functions
 - Bit stage i

Second lvl $P_k^{'}, G_k^{'}$: k , generates or propagates

$G_0^{'}, P_0^{'}$



Delay

$P_i^{'}, G_i^{'}$: 1 gate delay $\rightarrow \textcircled{1}$

$P_k^{'}, G_k^{'}$: 2 gate delay $\rightarrow \textcircled{2}$

Carry: $\frac{C_4, C_8, C_{12}, C_{16}}{① + ② + ③ = 5} \rightarrow 2$ gate delays $\rightarrow ③$

$\frac{C_{12}}{C_{13}, C_{14}, C_{15}} \rightarrow 2$ gate delays $\rightarrow ④$

$S_i \rightarrow 1$ gate delay $\rightarrow ⑤$

Total delay: $① + ② + ③ + ④ + ⑤ = 8$ tpd.

16-bit addition

RCA: 32

CLA - I : 10 tpd.

CLA - II : 8 tpd.

Issue: Additional Carry look ahead

logic.



Additional electronic
circuit