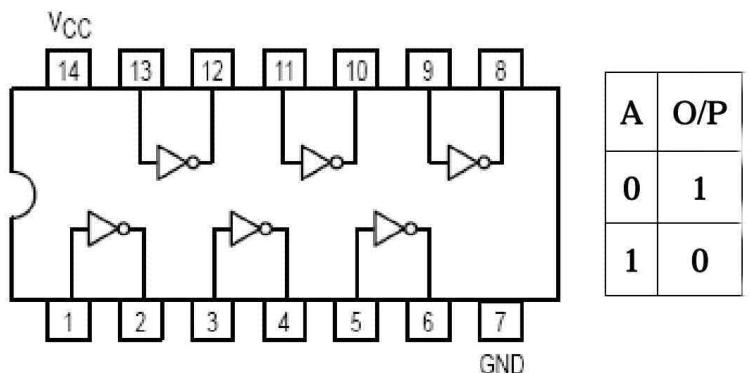


CONTENTS

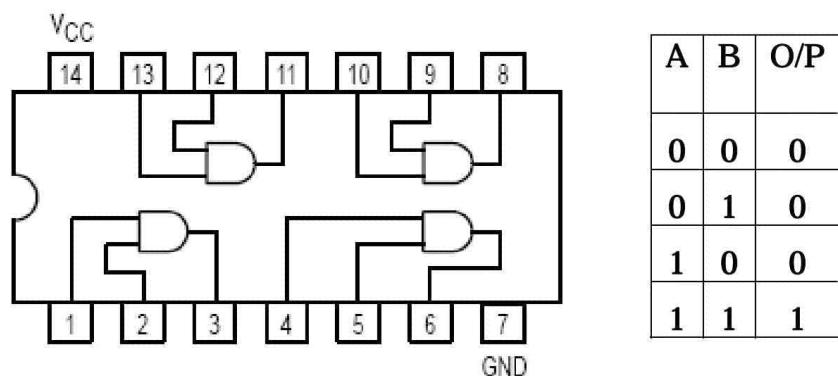
Experiment No

1. *Verification of Gates*
2. *Half/Full Adder/Subtractor*
3. *Parallel Adder/Subtractor*
4. *Excess-3 to BCD & Vice Versa*
5. *Binary-Grey & Grey-Binary Converter*
6. *MUX/DEMUX*
7. *MUX/DEMUX using only NAND Gates*
8. *Comparators*
9. *Encoder/Decoder*
10. *Flip-Flops*
11. *Counters*
12. *Shift Registers*
13. *Johnson/Ring Counters*
14. *Sequence Generator*

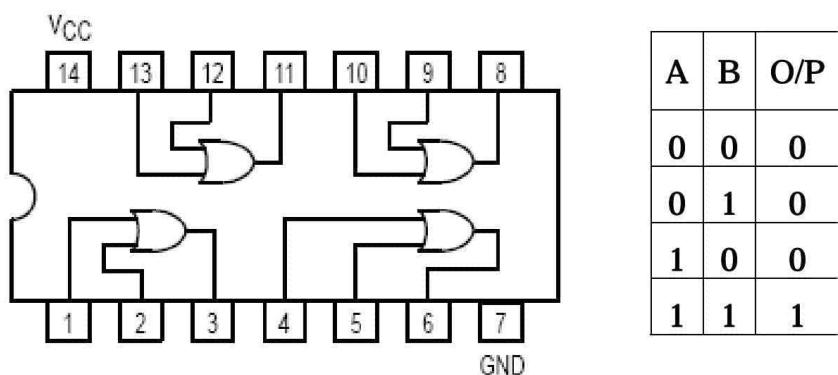
Inverter Gate (NOT Gate) → 7404LS



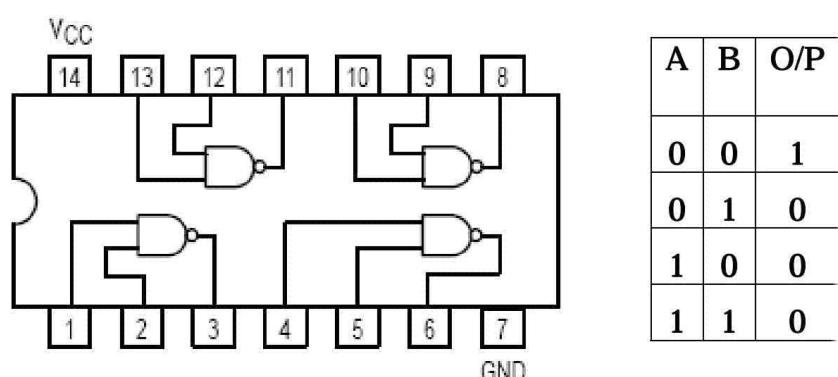
2-Input AND Gate → 7408LS



2-Input OR Gate → 7432LS



2-Input NAND Gate → 7400LS



VERIFICATION OF GATES

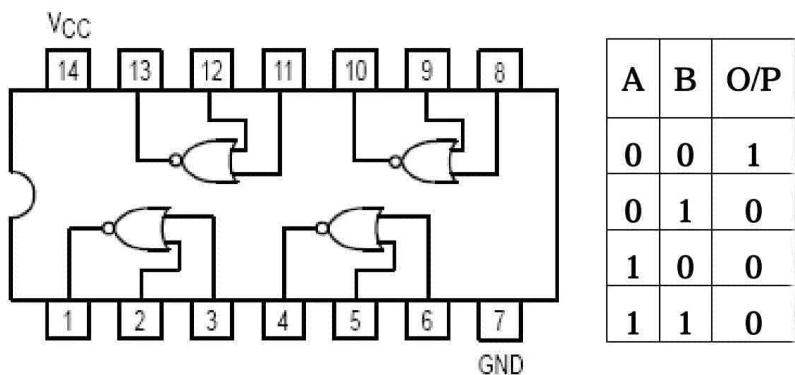
Aim: - To study and verify the truth table of logic gates

Apparatus Required: -

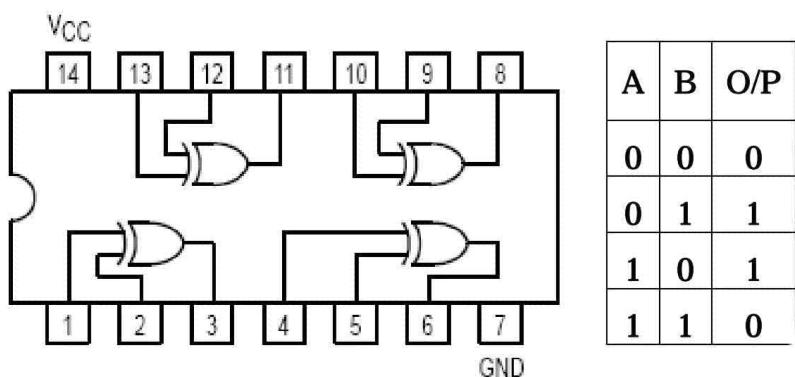
All the basic gates mention in the fig.

Procedure: -

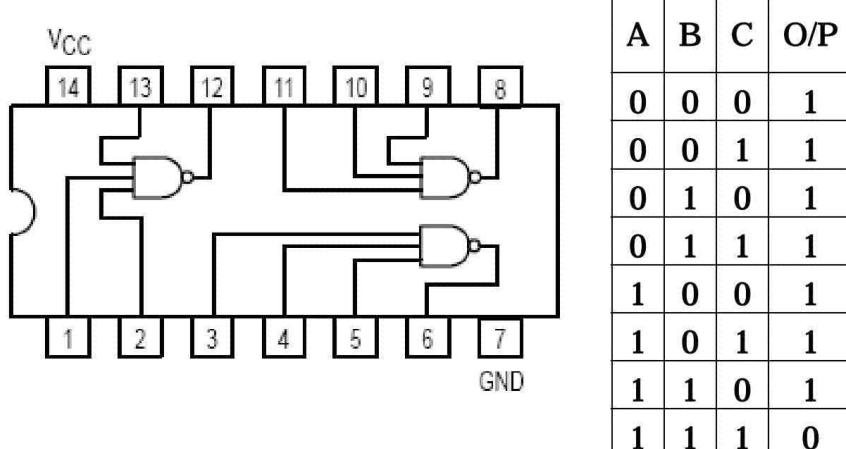
1. Place the IC on IC Trainer Kit.
2. Connect V_{CC} and ground to respective pins of IC Trainer Kit.
3. Connect the inputs to the input switches provided in the IC Trainer Kit.
4. Connect the outputs to the switches of O/P LEDs,
5. Apply various combinations of inputs according to the truth table and observe condition of LEDs.
6. Disconnect output from the LEDs and note down the corresponding multimeter voltage readings for various combinations of inputs.



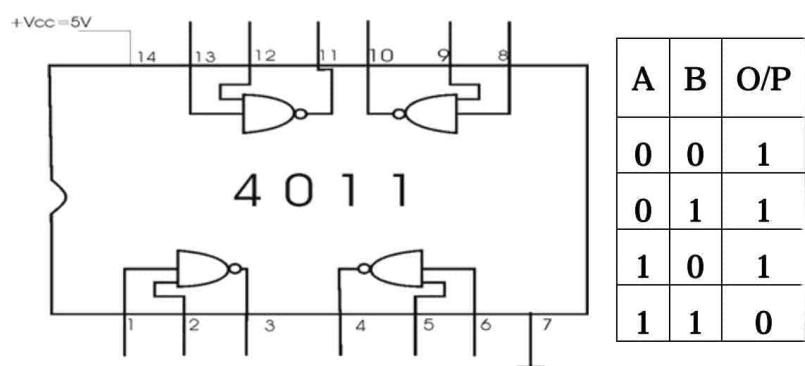
2-Input EX-OR Gate → 7486LS



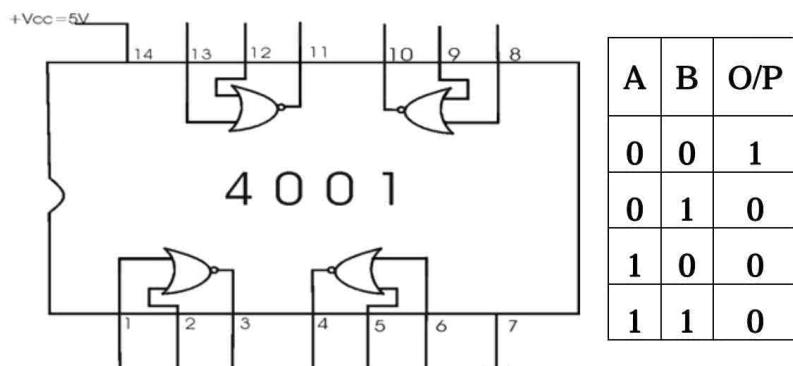
3-Input NAND Gate → 7410LS



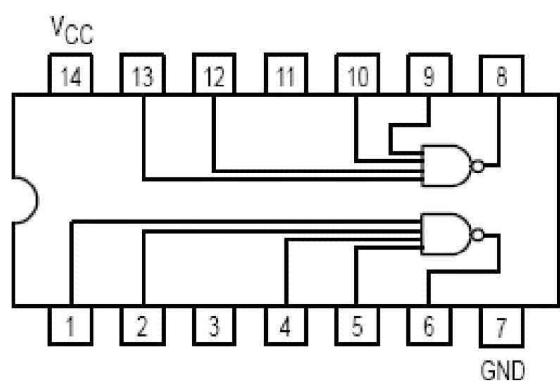
2-Input NAND Gate → CD4011



2-Input NOR Gate → CD4001

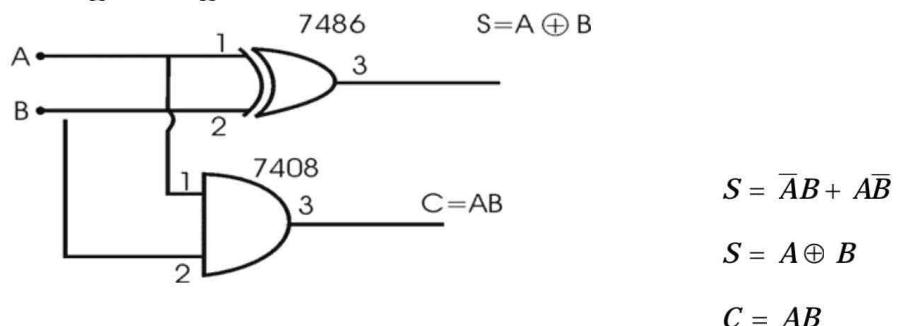


4-Input NAND Gate → 7420LS



A	B	C	D	O/P
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	1	0	1
1	1	1	1	0

Half Adder using basic gates:-

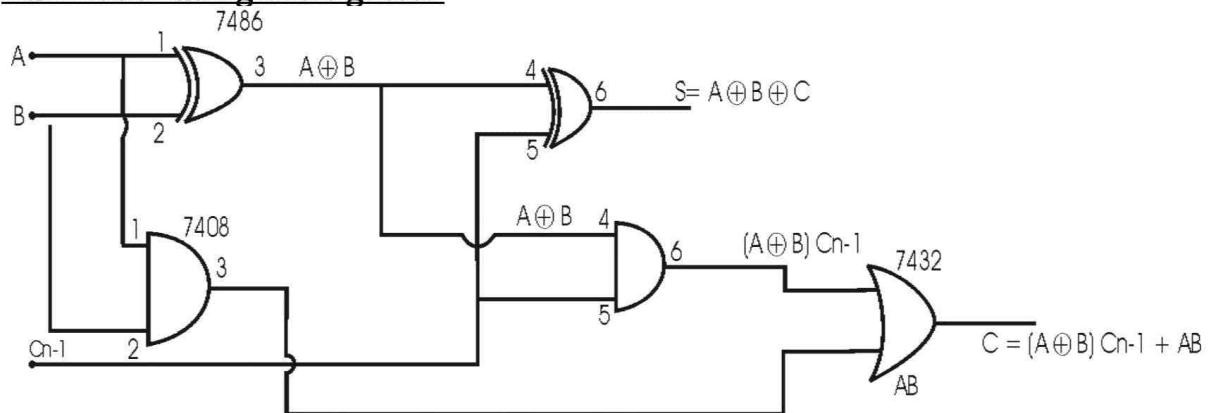


$$S = \overline{AB} + A\overline{B}$$

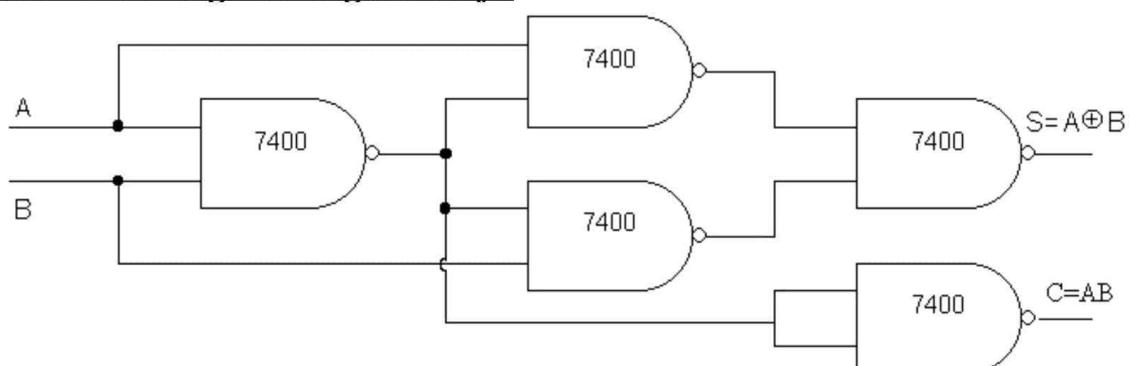
$$S = A \oplus B$$

$$C = AB$$

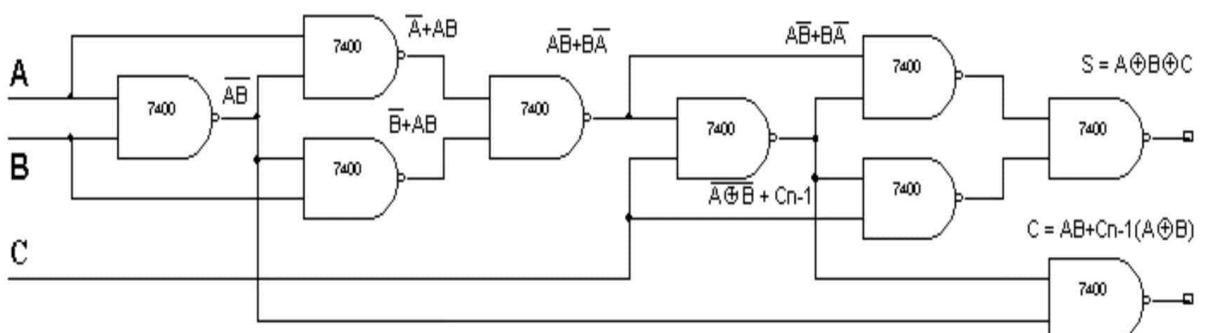
Full Adder using basic gates:-



Half Adder using NAND gates only:-



Full Adder using NAND gates only:-



HALF/FULL ADDER & HALF/FULL SUBTRACTOR

Aim: - To realize half/full adder and half/full subtractor.

- i. Using X-OR and basic gates
- ii. Using only nand gates.

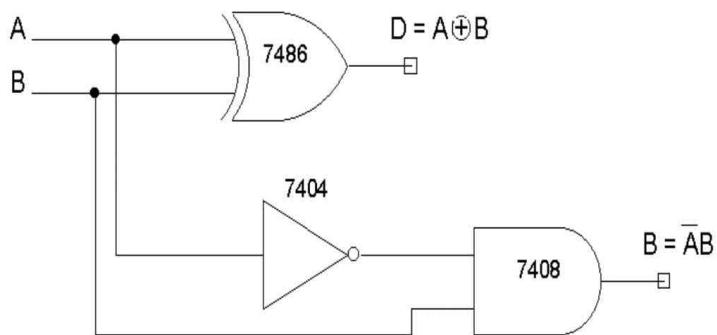
Apparatus Required: -

IC 7486, IC 7432, IC 7408, IC 7400, etc.

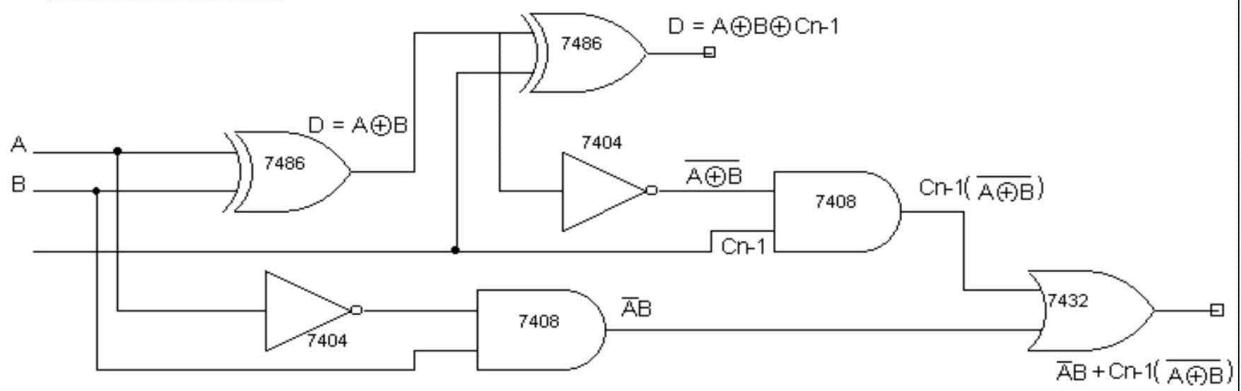
Procedure: -

1. Verify the gates.
2. Make the connections as per the circuit diagram.
3. Switch on V_{CC} and apply various combinations of input according to the truth table.
4. Note down the output readings for half/full adder and half/full subtractor sum/difference and the carry/borrow bit for different combinations of inputs.

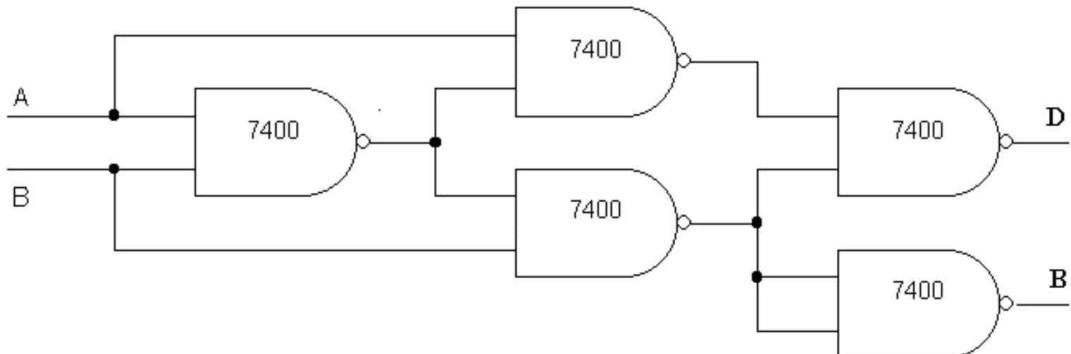
Using X – OR and Basic Gates (a) Half Subtractor



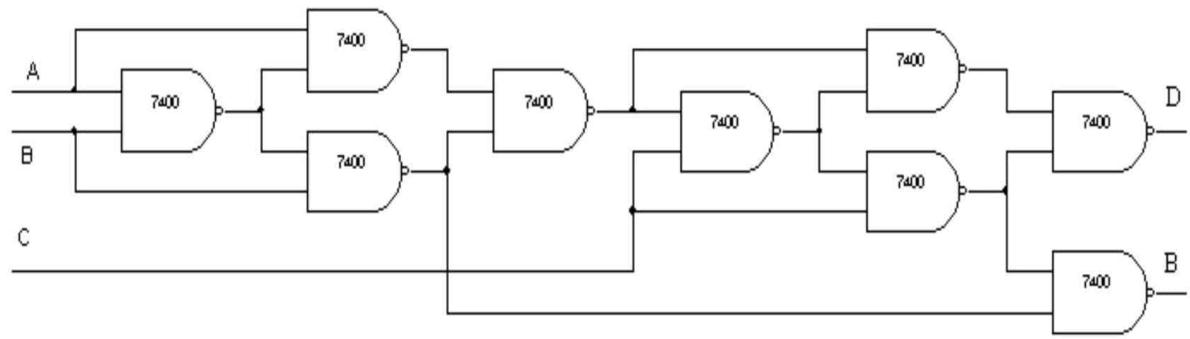
Full Subtractor



(ii) Using only NAND gates (a) Half subtractor



(b) Full Subtractor



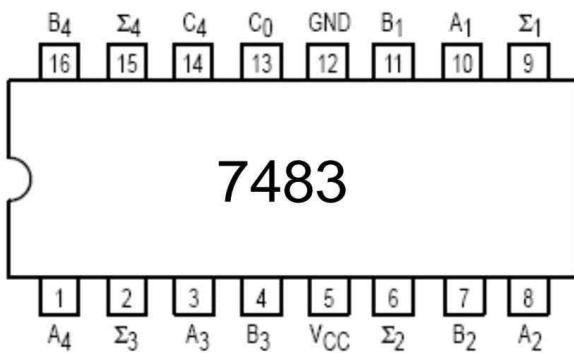
Half Adder			
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Half Subtractor			
A	B	D	B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

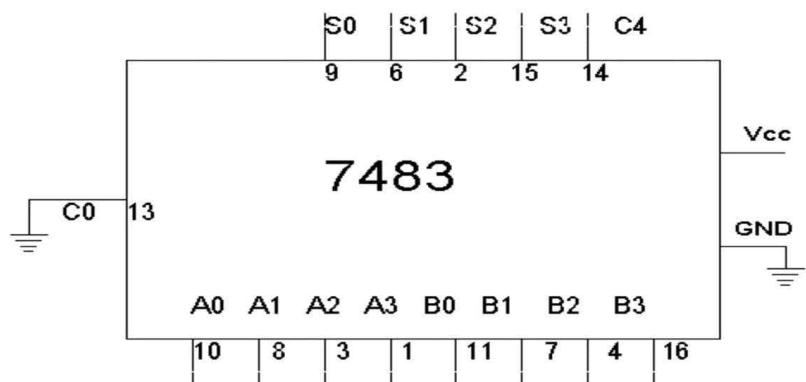
Full Adder				
A	B	Cn-1	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Full Subtractor				
A	B	Cn-1	D	B
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Pin Detail: -



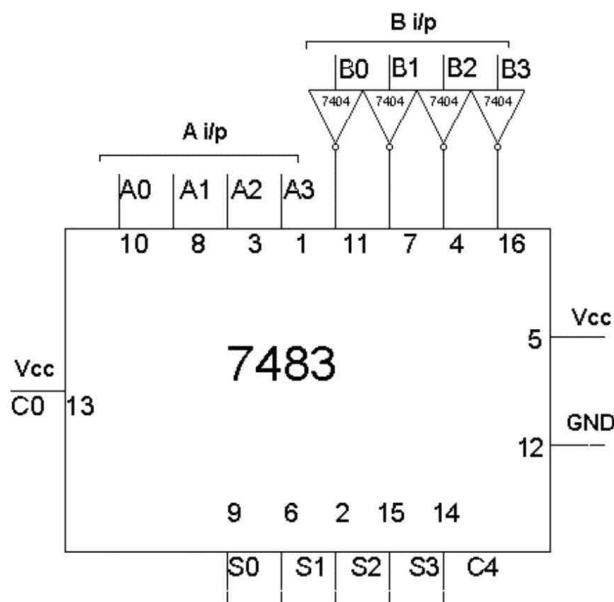
Adder: -



Truth Table: -

A ₃	A ₂	A ₁	A ₀	B ₃	B ₂	B ₁	B ₀	C ₄ (V)	S ₃ (V)	S ₂ (V)	S ₁ (V)	S ₀ (V)
0	0	0	1	0	0	1	0	0	0	0	1	1
0	1	0	1	1	0	1	1	1	1	0	0	0
1	0	1	0	1	0	1	0	1	0	1	0	0
1	1	1	1	1	1	1	1	1	1	1	1	0
0	1	1	1	0	0	1	1	0	1	0	1	0

Subtractor:-



PARALLEL ADDER AND SUBTRACTOR USING 7483

Aim: - To realize IC7483 as parallel adder / Subtractor.

Apparatus Required: -

IC 7483, IC 7404, etc.

Procedure: -

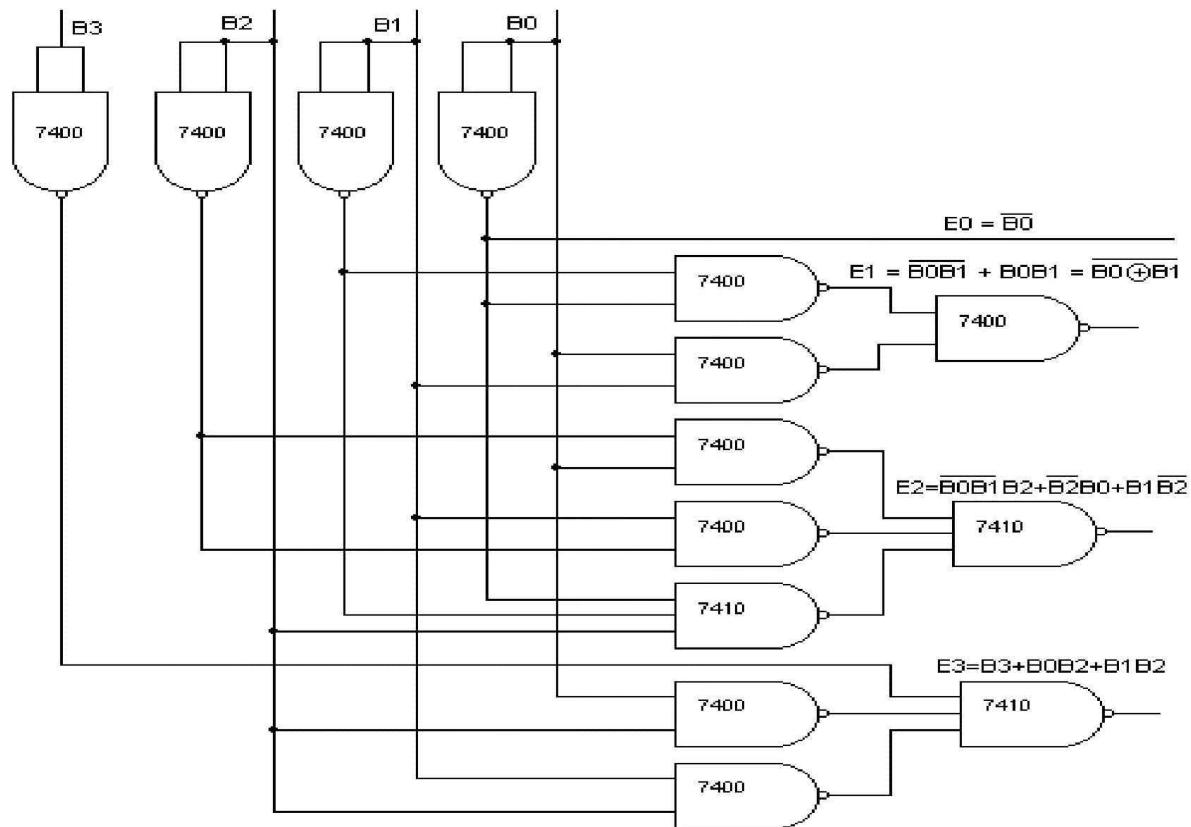
1. Apply the inputs to A0 to A3 and B0 to B3.
2. Connect C0 to the Ground.
3. Check the output sum on the S0 to S3 and also C4.
4. For subtraction connect C0 to Vcc, Apply the B input through NOT gate, which gives the complement of B.
5. The truth table of adder and Subtractor are noted down.

Truth Table for Subtractor

A3	A2	A1	A0	B3	B2	B1	B0	C4(V)	S3(V)	S2(V)	S1(V)	S0(V)
0	0	1	0	0	0	0	1	1	0	0	0	1
0	1	0	1	0	0	1	1	1	0	0	1	0
0	0	1	1	0	1	0	1	0	1	1	1	0

1	0	1	0	0	1	1	0	1	0	1	0	0	0
1	0	0	0	1	1	1	1	0	1	0	0	0	1

BCD To Excess-3



Truth Table For Code Conversion: -

Inputs				Outputs			
B3	B2	B1	B0	E3 (v)	E2 (v)	E1 (v)	E0 (v)
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0

BCD to Excess 3 AND Excess 3 to BCD

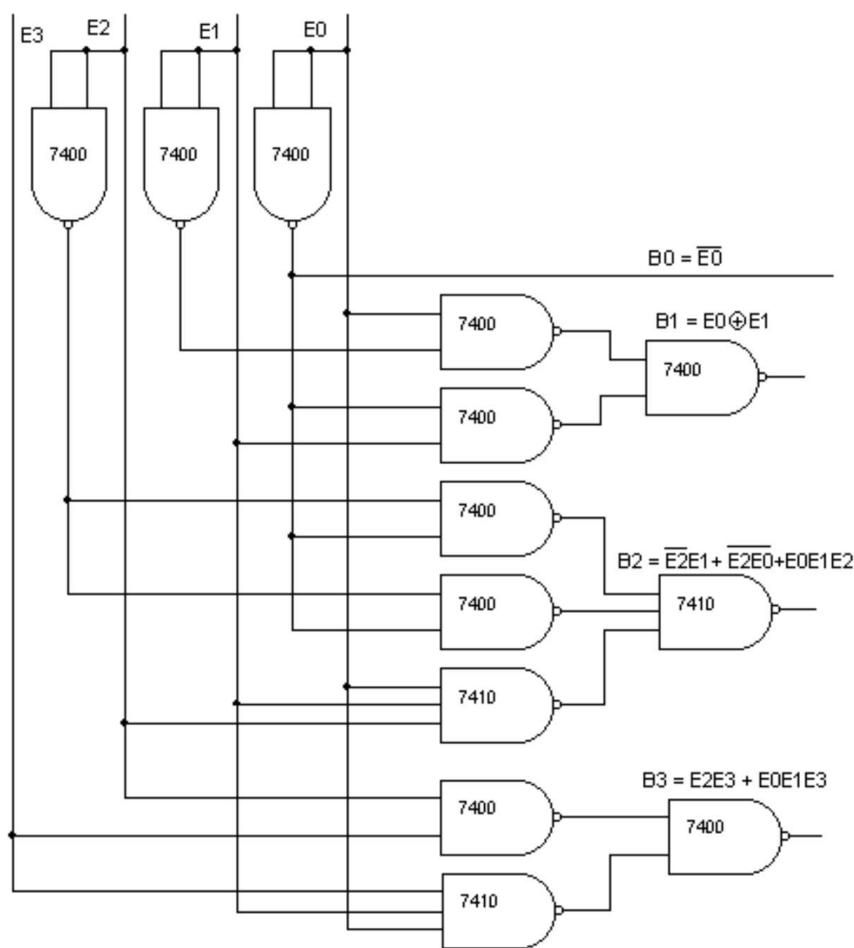
Aim: - To verify BCD to excess –3 code conversion using NAND gates. To study and verify the truth table of excess-3 to BCD code converter

Apparatus Required: -

IC 7400, IC 7404, etc.

Procedure: - (BCD Excess 3 and Vice Versa)

1. Make the connections as shown in the fig.
2. Pin [14] of all IC'S are connected to +5V and pin [7] to the ground.
3. The inputs are applied at E3, E2, E1, and E0 and the corresponding outputs at B3, B2, B1, and B0 are taken for excess – 3 to BCD.
4. B3, B2, B1, and B0 are the inputs and the corresponding outputs are E3, E2, E1 and E0 for BCD to excess – 3.
5. Repeat the same procedure for other combinations of inputs.
6. Truth table is written.

Excess-3 To BCD :-Truth Table For Code Conversion: -

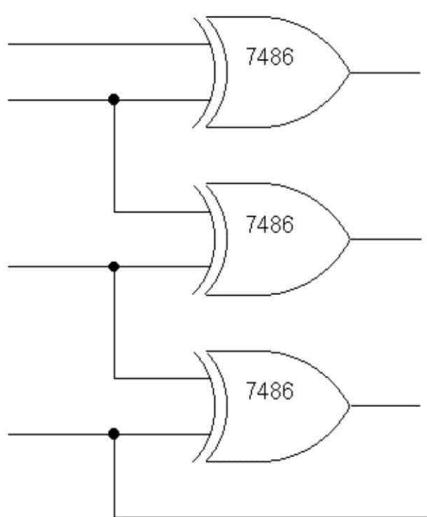
Inputs				Outputs			
E3	E2	E1	E0	B3 (v)	B2 (v)	B1 (v)	B0(v)
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	1
0	1	0	1	0	0	1	0
0	1	1	0	0	0	1	1
0	1	1	1	0	1	0	0
1	0	0	0	0	1	0	1
1	0	0	1	0	1	1	0
1	0	1	0	0	1	1	1
1	0	1	1	1	0	0	0
1	1	0	0	1	0	0	1

Exercise: -

1. Obtain the expression for E3, E2, E1 and E0
2. Obtain the expression for B3, B2, B1 and B0

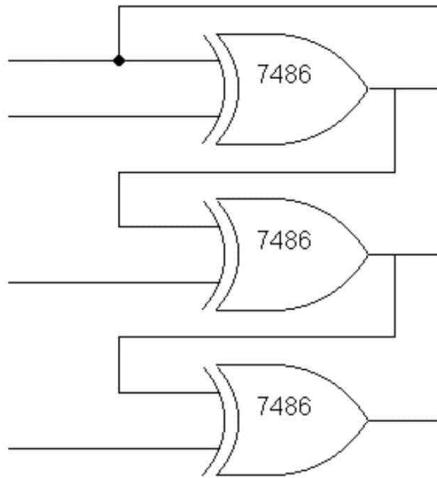
Circuit Diagram: -

Binary To Gray



Using EX-OR gates

Gray To Binary



Using EX-OR gates

Truth Table For Both: -

Inputs				Outputs			
B3	B2	B1	B0	G3 (V)	G2 (V)	G1 (V)	G0 (V)
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

BINARY TO GRAY AND GRAY TO BINARY CONVERSION

Aim: - To convert given binary numbers to gray codes.

Apparatus Required: -

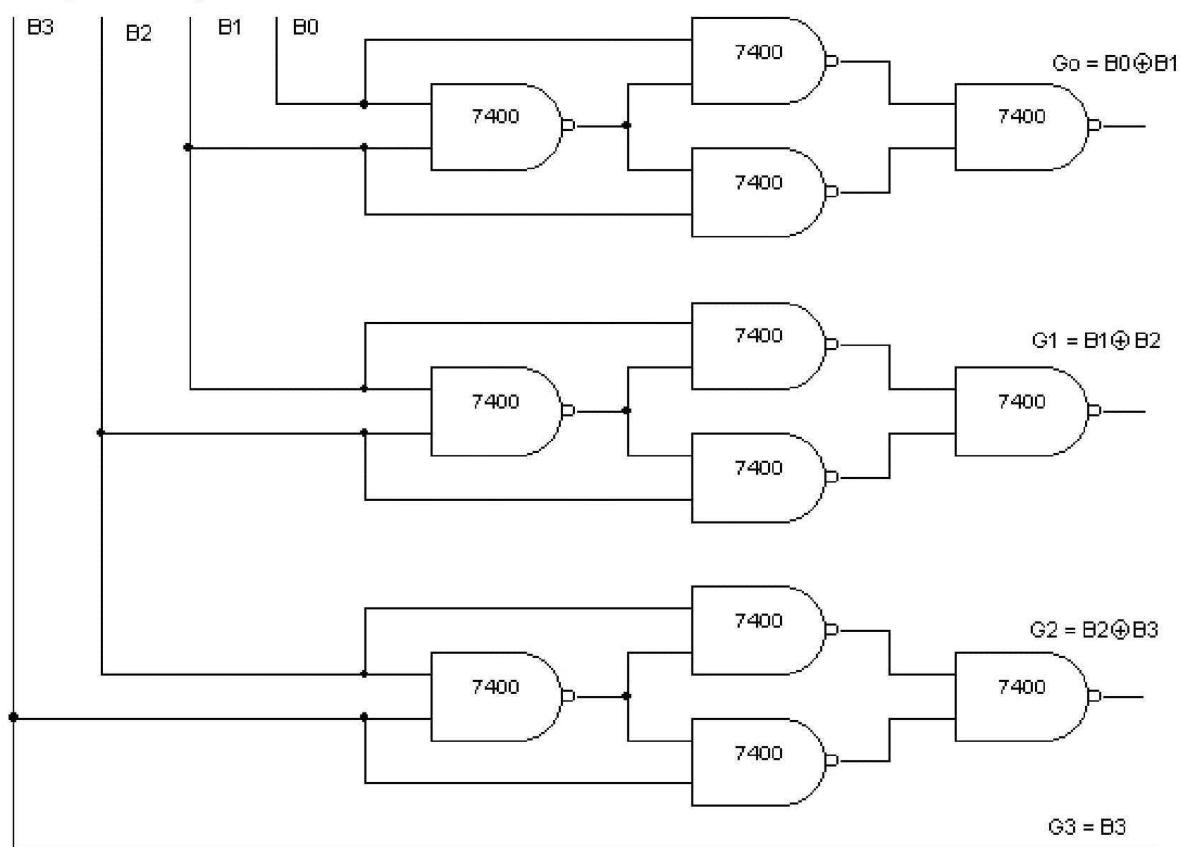
IC 7486, etc

Procedure: -

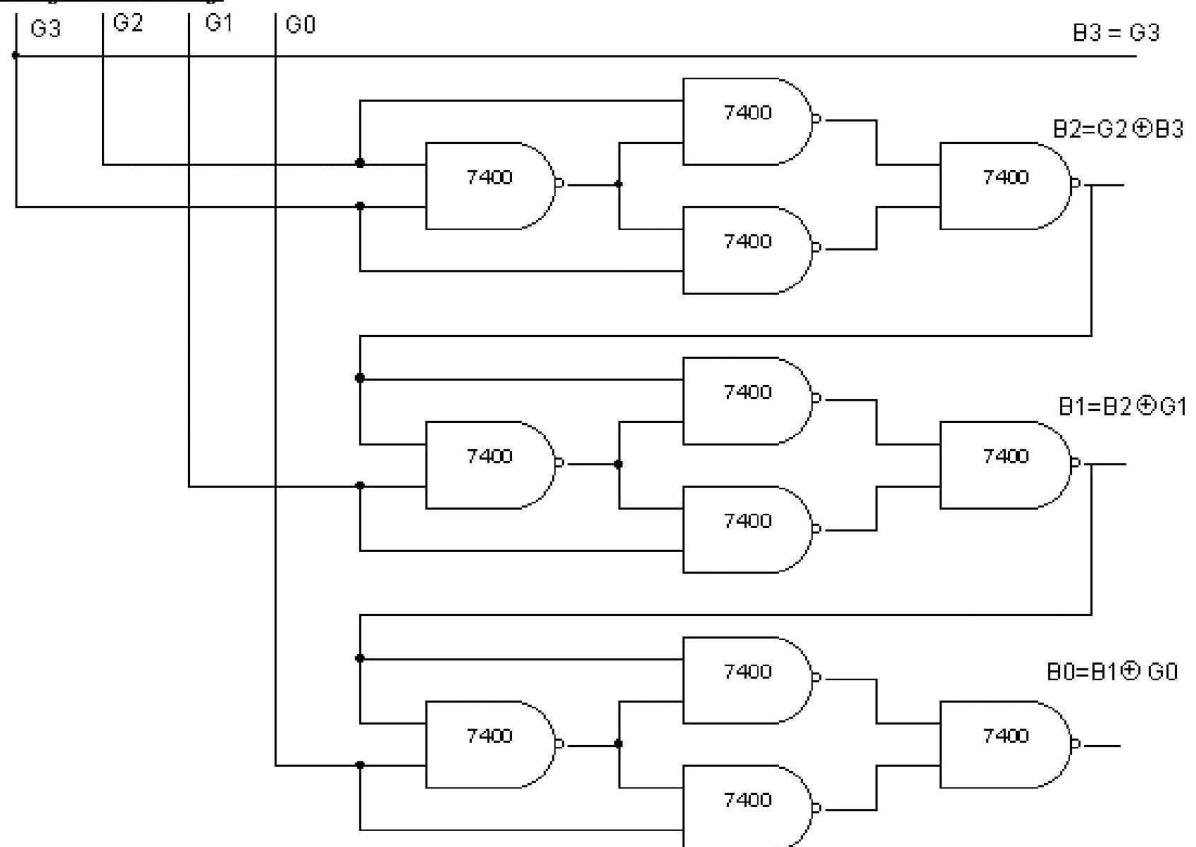
1. The circuit connections are made as shown in fig.
2. Pin (14) is connected to +Vcc and Pin (7) to ground.
3. In the case of binary to gray conversion, the inputs B0, B1, B2 and B3 are given at respective pins and outputs G0, G1, G2, G3 are taken for all the 16 combinations of the input.
4. In the case of gray to binary conversion, the inputs G0, G1, G2 and G3 are given at respective pins and outputs B0, B1, B2, and B3 are taken for all the 16 combinations of inputs.
5. The values of the outputs are tabulated.

Using Nand Gates Only: -

Binary To Gray



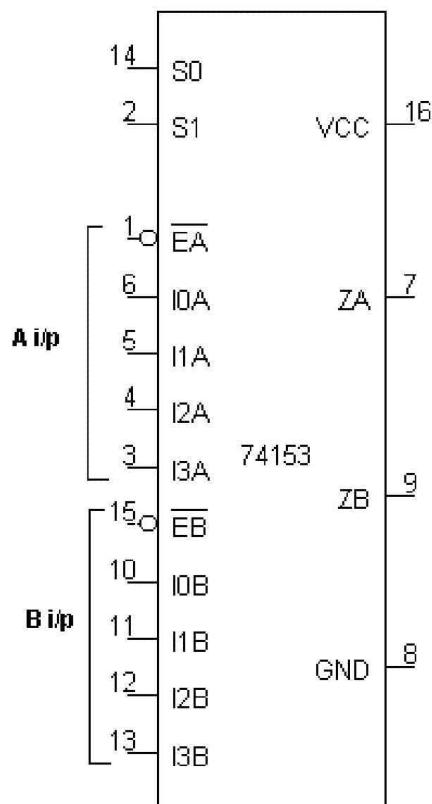
Gray To Binary



Truth Table For Both: -

Inputs				Outputs			
B3	B2	B1	B0	G3 (V)	G2 (V)	G1 (V)	G0 (V)
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

Pin Details: -



Truth Table: -

CHANNEL – A								CHANNEL – B							
INPUTS					SELECT LINES		O/P	INPUTS					SELECT LINES		O/P
Ēa	Ioa	I1a	I2a	I3a	S1	S2	Za(v)	Ēa	Iob	I1b	I2b	I3b	S1	S2	Za(v)
1	X	X	X	X	X	X	0	1	X	X	X	X	X	X	0
0	0	X	X	X	0	0	0	0	0	X	X	X	0	0	0
0	1	X	X	X	0	0	1	0	1	X	X	X	0	0	1
0	X	0	X	X	0	1	0	0	X	0	X	X	0	1	0
0	X	1	X	X	0	1	1	0	X	1	X	X	0	1	1
0	X	X	0	X	1	0	0	0	X	X	0	X	1	0	0
0	X	X	1	X	1	0	1	0	X	X	1	X	1	0	1
0	X	X	X	0	1	1	0	0	X	X	X	0	1	1	0
0	X	X	X	1	1	1	1	0	X	X	X	1	1	1	1

MUX/DEMUX USING 74153 & 74139

Aim: - To verify the truth table of multiplexer using 74153 & to verify a demultiplexer using 74139. To study the arithmetic circuits half-adder half Subtractor, full adder and full Subtractor using multiplexer.

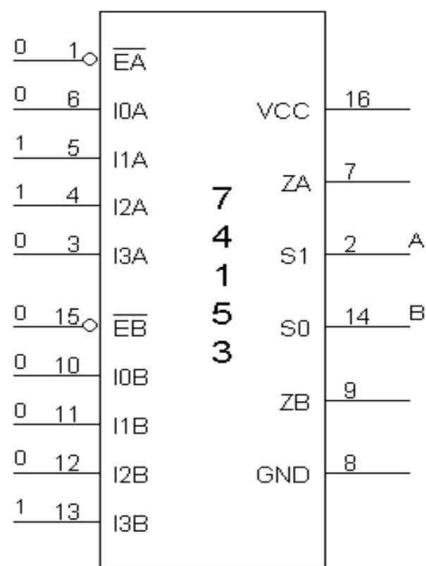
Apparatus Required: -

IC 74153, IC 74139, IC 7404, etc.

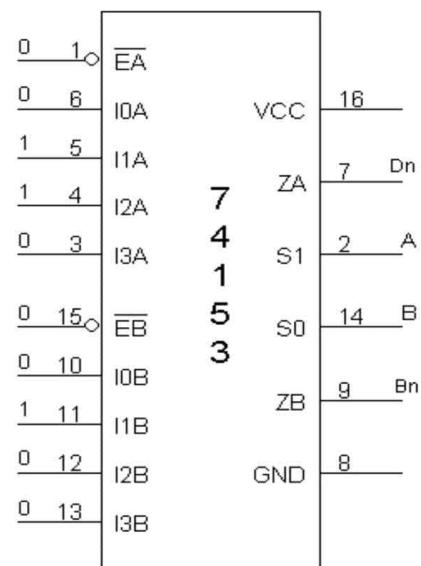
Procedure: - (IC 74153)

1. The Pin [16] is connected to + Vcc.
2. Pin [8] is connected to ground.
3. The inputs are applied either to 'A' input or 'B' input.
4. If MUX 'A' has to be initialized, Ea is made low and if MUX 'B' has to be initialized, Eb is made low.
5. Based on the selection lines one of the inputs will be selected at the output and thus the truth table is verified.
6. In case of half adder using MUX, sum and carry is obtained by applying a constant inputs at I_{0a} , I_{1a} , I_{2a} , I_{3a} and I_{0b} , I_{1b} , I_{2b} and I_{3b} and the corresponding values of select lines are changed as per table and the output is taken at Z_{0a} as sum and Z_{0b} as carry.
7. In this case, the channels A and B are kept at constant inputs according to the table and the inputs A and B are varied. Making Ea and Eb zero and the output is taken at Za, and Zb.
8. In full adder using MUX, the input is applied at C_{n-1} , A_n and B_n . According to the table corresponding outputs are taken at C_n and D_n .

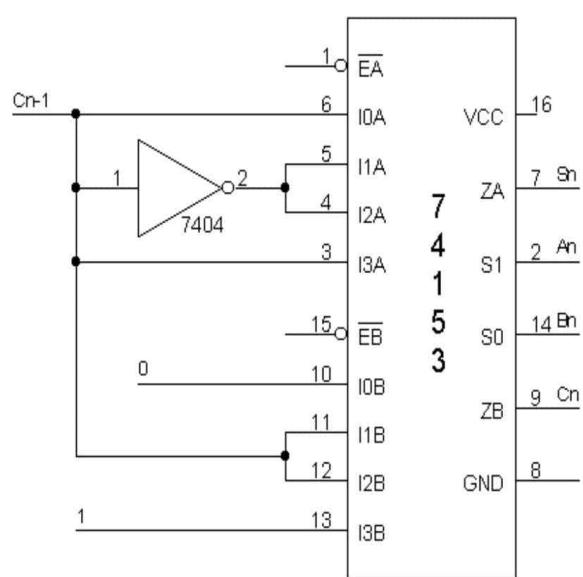
Half Adder Using 74153 -



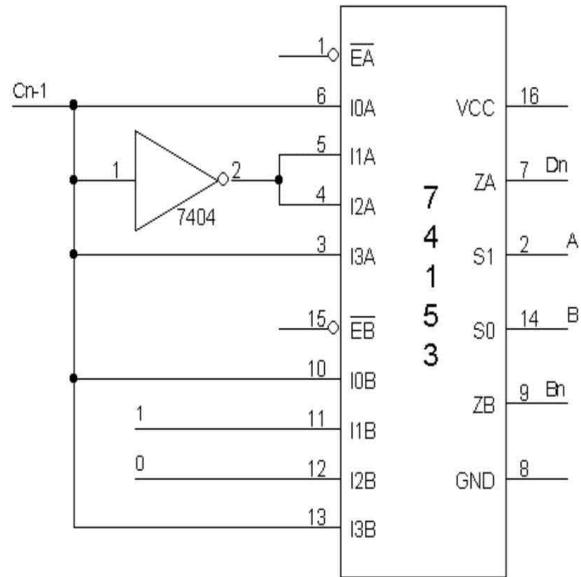
Half Subtractor:-



Full Adder Using 74153:-



Full Subtractor Using 74153:-



Truth Tables: - Same for both Subtractor and adder

Half adder/subtractor			
A	B	Sn/Dn (V)	Cn/Bn (V)
0	0		
0	1		
1	0		
1	1		

Full Adder/subtractro				
An	Bn	Cn-1	Sn/Dn (V)	Cn/Bn (V)
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Pin Details: -



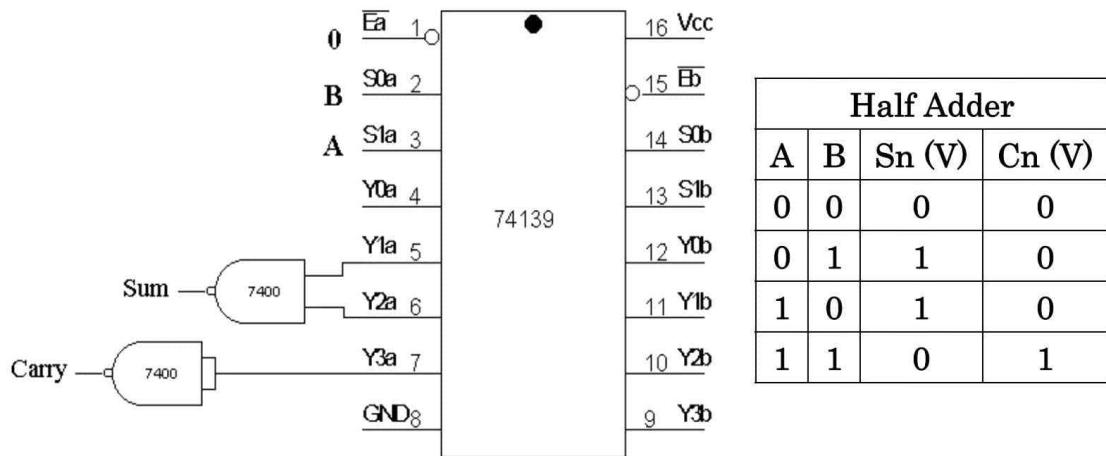
Truth Table For Demux: -

CHANNEL – A							CHANNEL – B						
Inputs			Outputs				Inputs			Outputs			
\bar{E}_a	S_{1a}	S_{0a}	Y_{0a}	Y_{1a}	Y_{2a}	Y_{3a}	\bar{E}_b	S_{1b}	S_{0b}	Y_{0b}	Y_{1b}	Y_{2b}	Y_{3b}
1	X	X	1	1	1	1	1	X	X	1	1	1	1
0	0	0	0	1	1	1	0	0	0	0	1	1	1
0	0	1	1	0	1	1	0	0	1	1	0	1	1
0	1	0	1	1	0	1	1	1	0	1	1	0	1
0	1	1	1	1	1	0	1	1	1	1	1	1	0

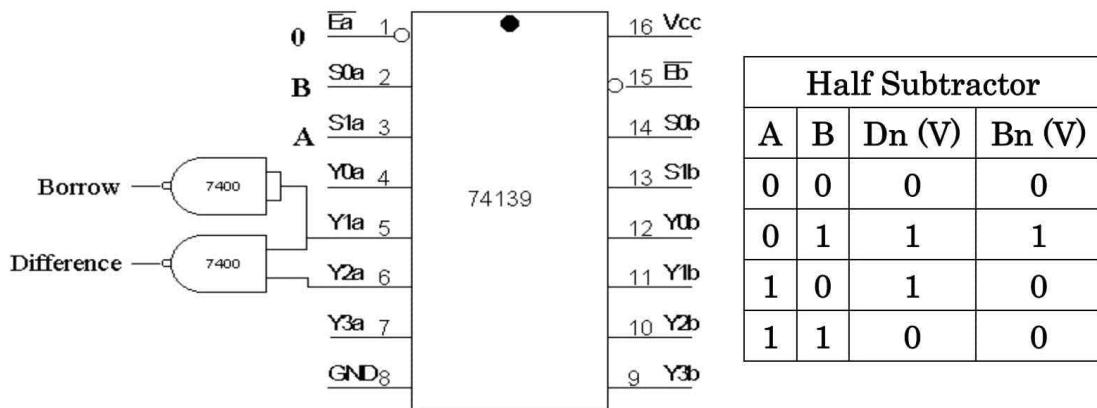
Procedure: - (IC 74139)

1. The inputs are applied to either 'a' input or 'b' input
2. The demux is activated by making Ea low and Eb low.
3. The truth table is verified.

Half adder



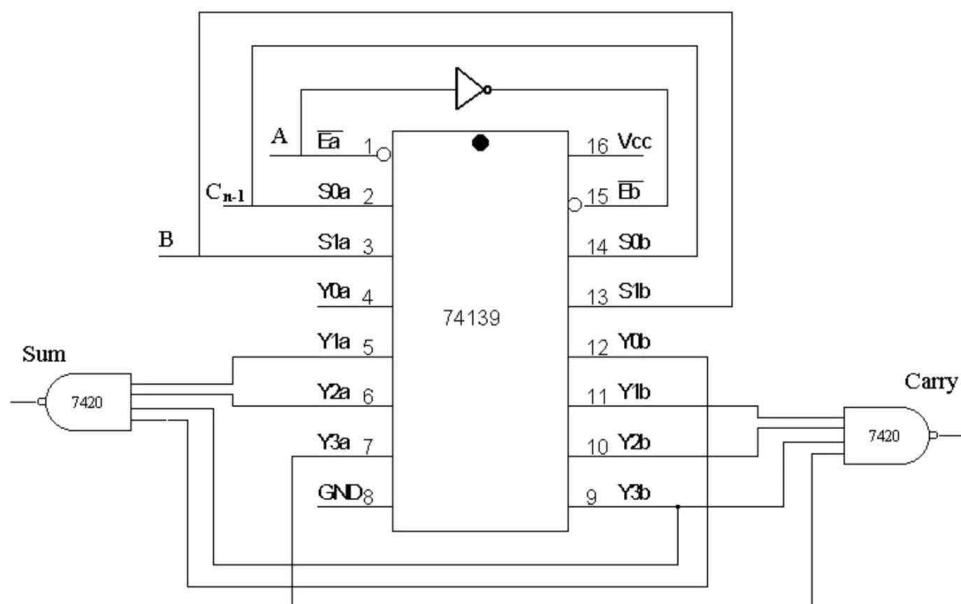
Half subtractor:-



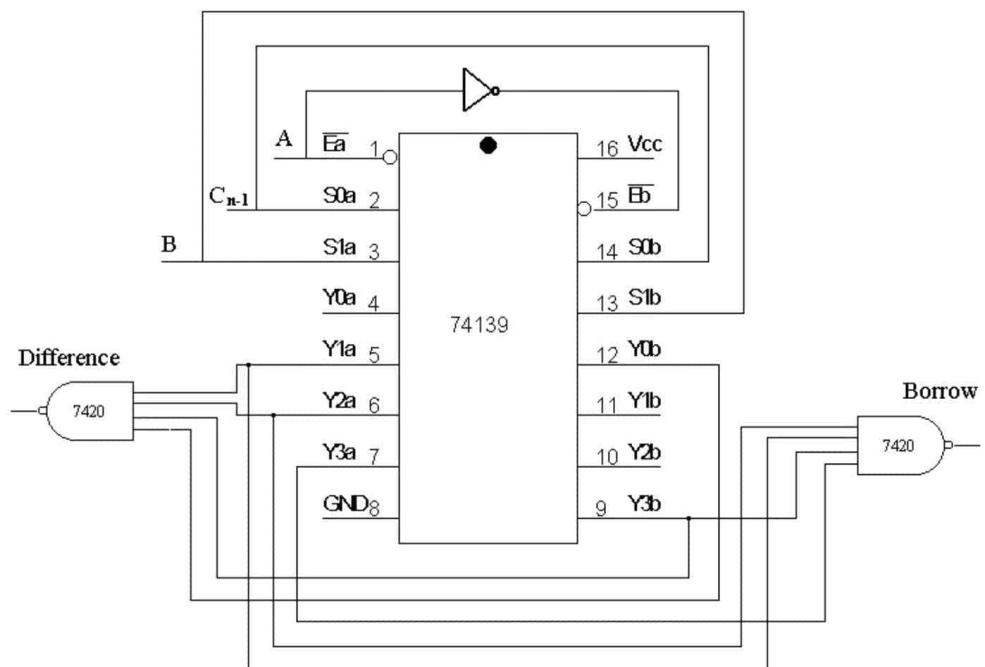
Exercise:-

- Repeat the experiment to verify Channel B.

Full Adder using IC 74139:-



Full subtractor using IC 74139:-

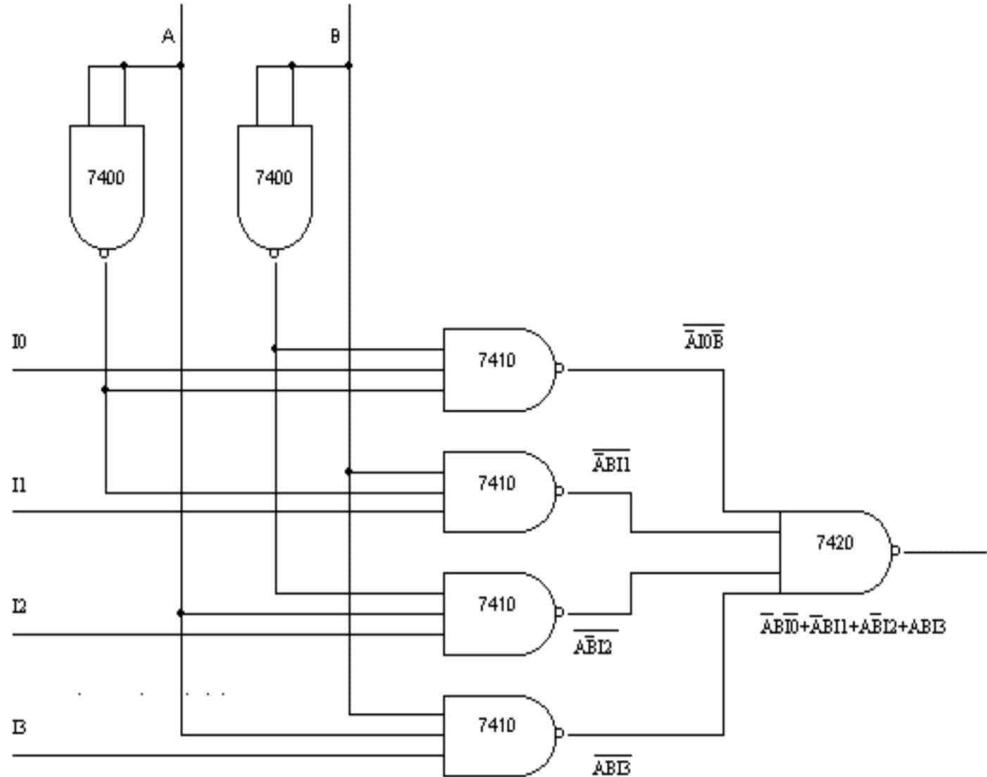


Truth Tables:-

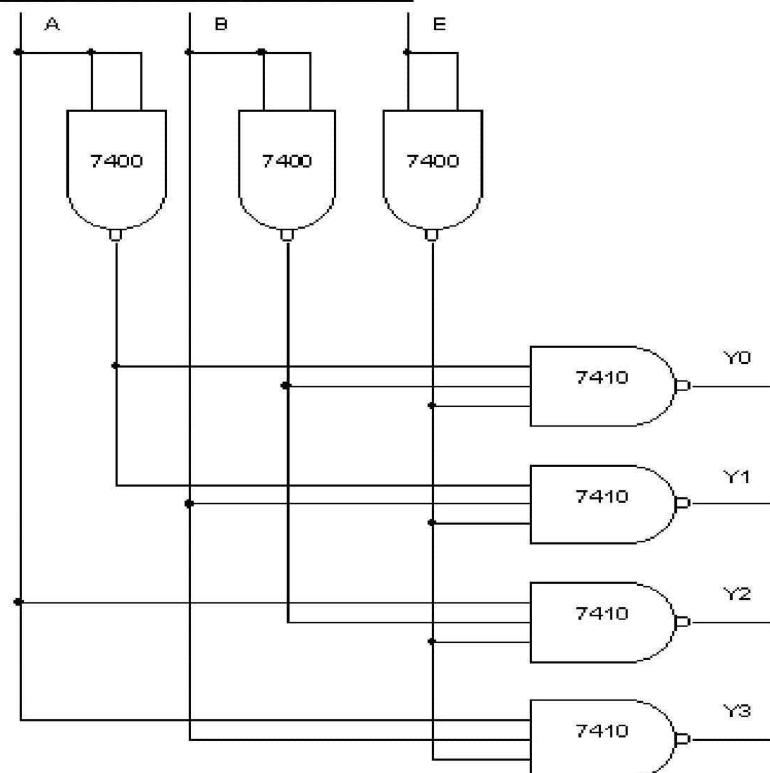
Full Adder				
An	Bn	Cn-1	Sn (V)	Cn (V)
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Full Subtractor				
An	Bn	Cn-1	Dn (V)	Bn (V)
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

MUX USING NAND GATES ONLY: -



DEMUX USING NAND GATES ONLY: -



MUX AND DEMUX USING NAND GATES

AIM: - To verify the truth table of MUX and DEMUX using NAND.

APPARATUS REQUIRED: -

IC 7400, IC 7410, IC 7420, etc.

PROCEDURE: -

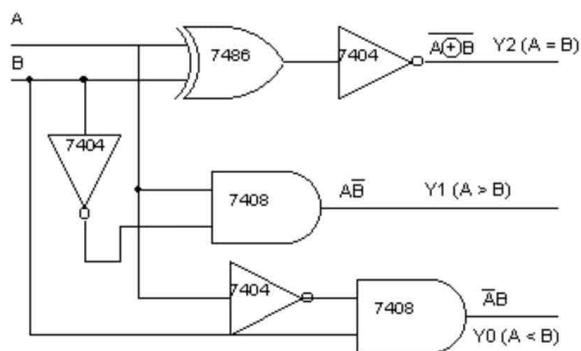
1. Connections are made as shown in the Circuit diagram.
2. Change the values of the inputs as per the truth table and note down the outputs readings using multimeter.

TRUTH TABLES: -

INPUT						OUPUT
A	B	I0	I1	I2	I3	Y (V)
0	0	0	X	X	X	0
0	0	1	X	X	X	1
0	1	X	0	X	X	0
0	1	X	1	X	X	1
1	0	X	X	0	X	0
1	0	X	X	1	X	1
1	1	X	X	X	0	0
1	1	X	X	X	1	1

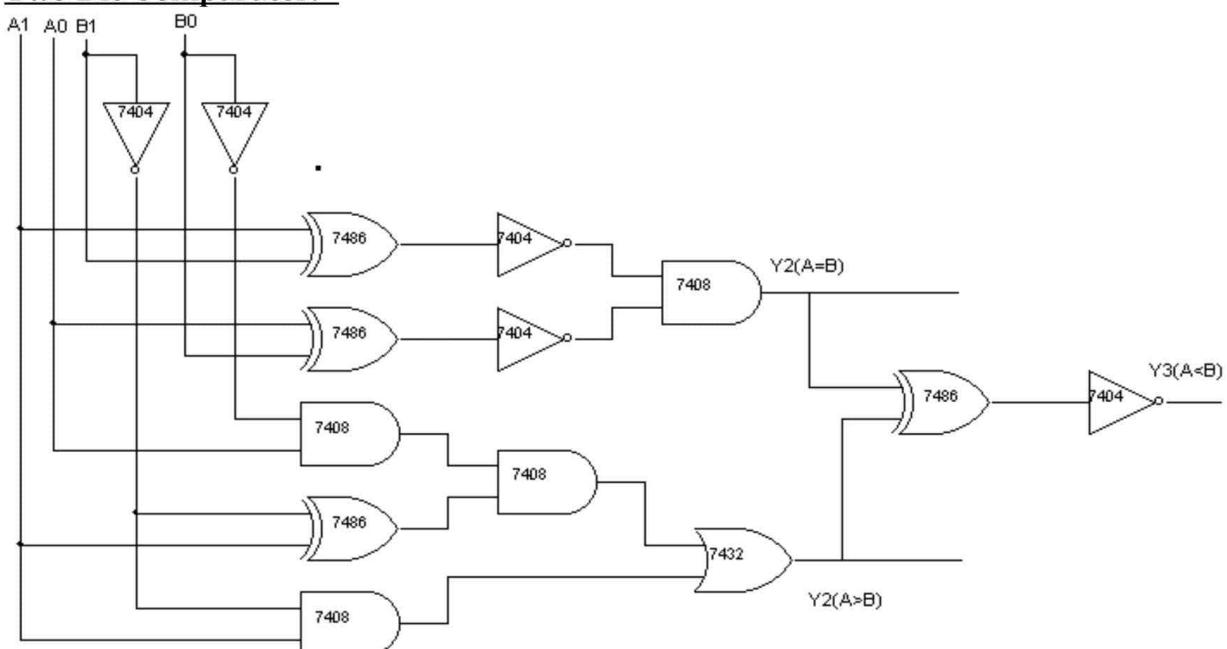
INPUT			OUPUT			
E	A	B	Y0 (V)	Y1 (V)	Y2 (V)	Y3 (V)
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

One Bit Comparator: -



A	B	Y_1 $(A > B)$	Y_2 $(A = B)$	Y_3 $(A < B)$
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

Two Bit Comparator: -



Two-Bit Comparator: -

A1	A0	B1	B0	$Y_1 (A > B)$	$Y_2 (A = B)$	$Y_3 (A < B)$
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

COMPARATORS

Aim: - To verify the truth table of one bit and two bit comparators using logic gates.

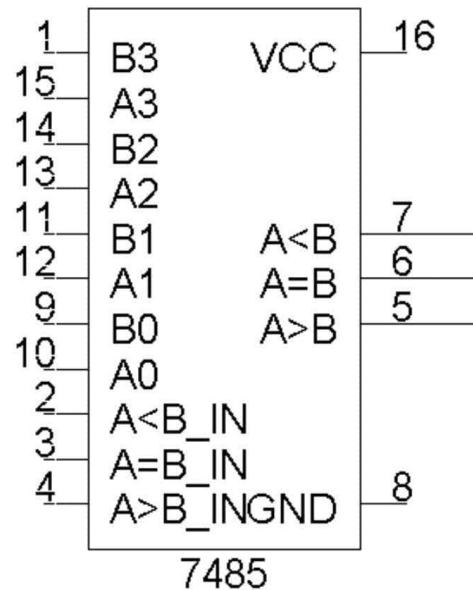
Apparatus Required: -

IC 7486, IC 7404, IC 7408, etc.

Procedure: -

1. Verify the gates.
2. Make the connections as per the circuit diagram.
3. Switch on Vcc.
4. Applying i/p and Check for the outputs.
5. The voltameter readings of outputs are taken and tabulated in tabular column.
6. The o/p are verified.

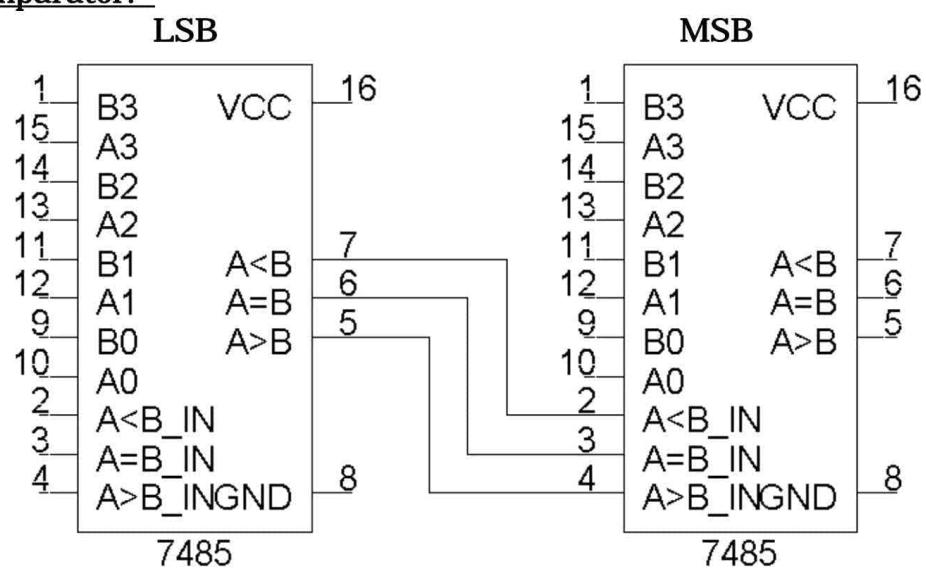
4-bit Comparator



Tabular Column For 8-Bit Comparator: -

$A_3 \ B_3$	$A_2 \ B_2$	$A_1 \ B_1$	$A_0 \ B_0$	$A > B$	$A = B$	$A < B$	$A > B$	$A = B$	$A < B$
$A_3 > B_3$	X	X	X	X	X	X			
$A_3 < B_3$	X	X	X	X	X	X			
$A_3 = B_3$	$A_2 > B_2$	X	X	X	X	X			
$A_3 = B_3$	$A_2 < B_2$	X	X	X	X	X			
$A_3 = B_3$	$A_2 = B_2$	$A_1 > B_1$	X	X	X	X			
$A_3 = B_3$	$A_2 = B_2$	$A_1 < B_1$	X	X	X	X			
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 > B_0$	X	X	X			
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 < B_0$	X	X	X			
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	1	0	0			
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	0	1	0			
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	0	0	1			

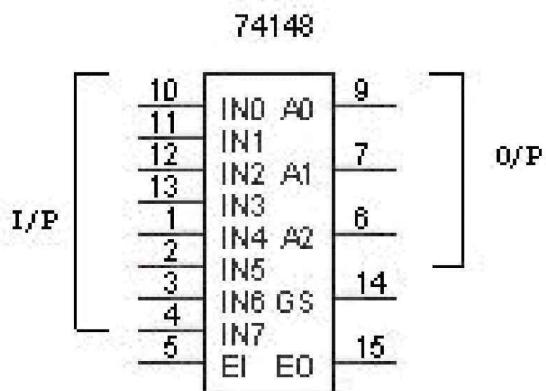
8-Bit Comparator: -



Exercise:-

- Write the truth table for 8-bit comparator and verify the same for the above circuit.

PIN DETAILS:-



TRUTH TABLE:-

E_n	A	B	C	D	E	F	G	H	$Q_2(V)$	$Q_1(V)$		$Q_0(V)$		$E_s(V)$		$E_o(V)$	
1	X	X	X	X	X	X	X	X	1			1		1		1	
0	0	1	1	1	1	1	1	1	1			1		0		1	
0	X	0	1	1	1	1	1	1	1			1		0		0	
0	0	X	0	1	1	1	1	1	1			0		1		0	
0	0	0	X	0	1	1	1	1	1			0		0		0	
0	0	0	0	X	0	1	1	1	0			1		1		0	
0	0	0	0	0	X	0	1	1	0			1		0		0	
0	0	0	0	0	0	X	0	1	0			0		1		0	
0	0	0	0	0	0	0	X	0	0			0		0		0	
0	1	1	1	1	1	1	1	1	1			1		1		1	

ENCODER & DECODER

AIM:-To convert a given octal input to the binary output and to study the LED display using 7447 7-segment decoder/ driver.

APPARATUS REQUIRED: -

IC 74148, IC 7447, 7-segment display, etc.

PROCEDURE: - (Encoder)

1. Connections are made as per circuit diagram.
2. The octal inputs are given at the corresponding pins.
3. The outputs are verified at the corresponding output pins.

PROCEDURE: - (Decoder)

1. Connections are made as per the circuit diagram.
2. Connect the pins of IC 7447 to the respective pins of the LED display board.
3. Give different combinations of the inputs and observe the decimal numbers displayed on the board.

RESULT: -

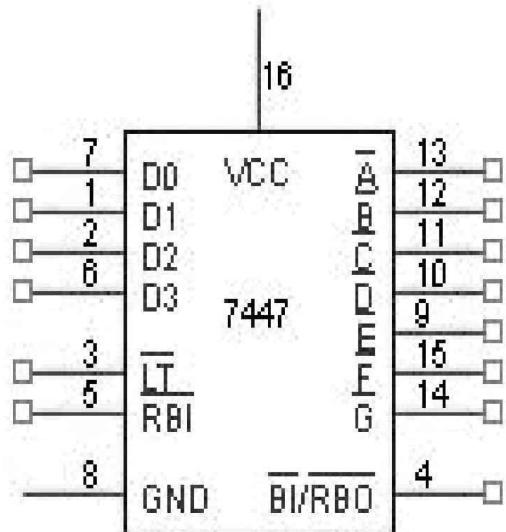
The given octal numbers are converted into binary numbers.

The given data is displayed using 7-segment LED decoder.

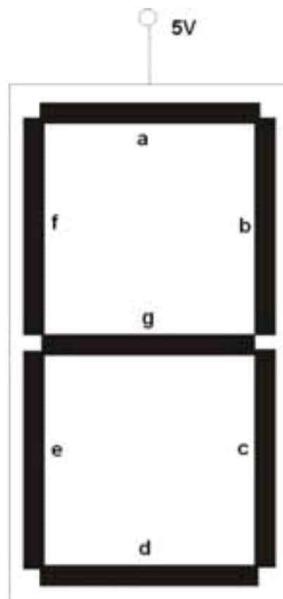
TABULAR COLUMN:-

Q4	Q3	Q2	Q1	O/P	Display	Glowing LEDs
0	0	0	0	0		a,b,c,d,e,f
0	0	0	1	1		b,c
0	0	1	0	2		a,b,d,e,g
0	0	1	1	3		a,b,c,d,g
0	1	0	0	4		b,c,f,g
0	1	0	1	5		a,c,d,f,g
0	1	1	0	6		a,c,d,e,f,g
0	1	1	1	7		a,b,c
1	0	0	0	8		a,b,c,d,e,f,g
1	0	0	1	9		a,b,c,d,f,g
1	0	1	0	10		d,e,g
1	0	1	1	11		c,d,g
1	1	0	0	12		c,d,e
1	1	0	1	13		a,g,d
1	1	1	0	14		d,e,f,g
1	1	1	1	15		blank

PIN DETAILS:-

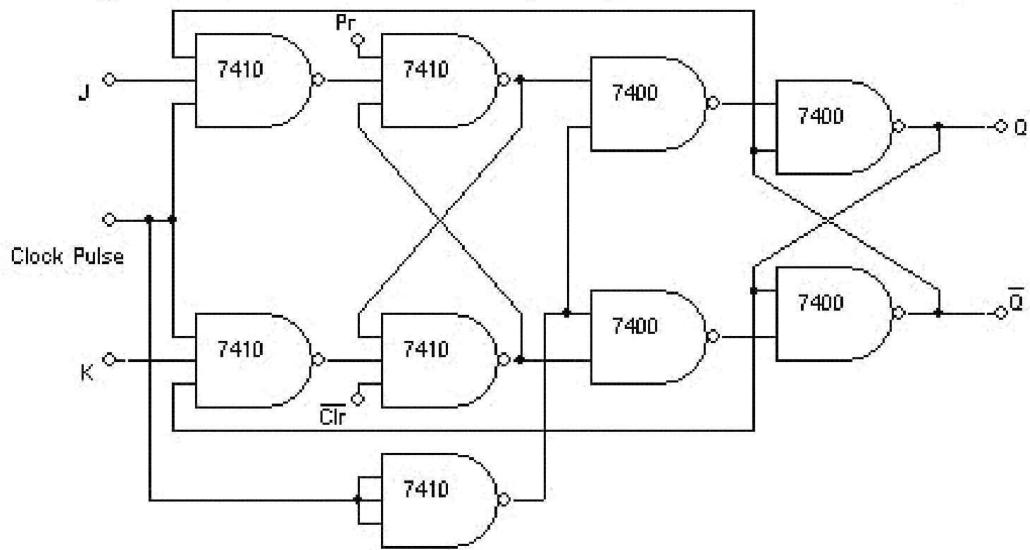


DISPLAY:-

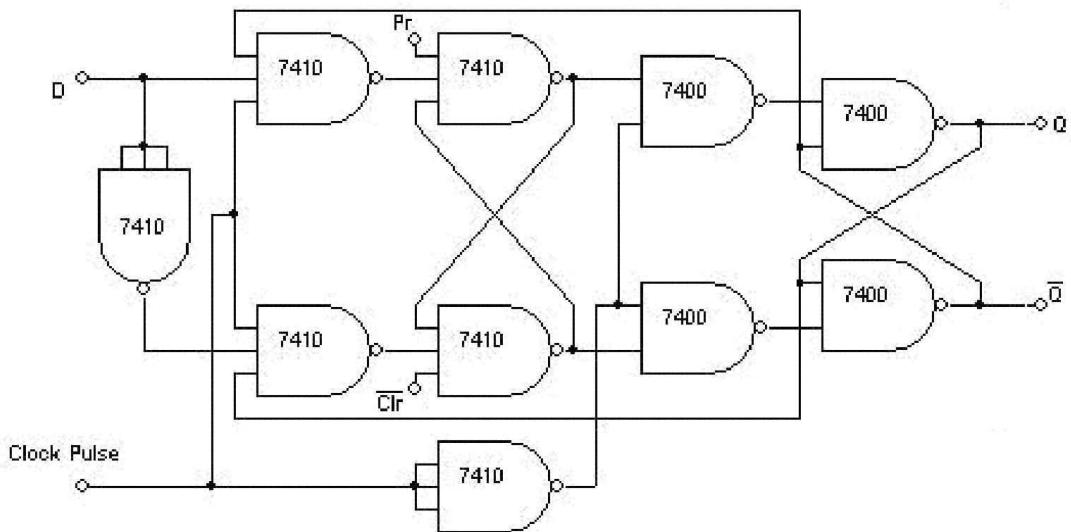


Conclusion:-

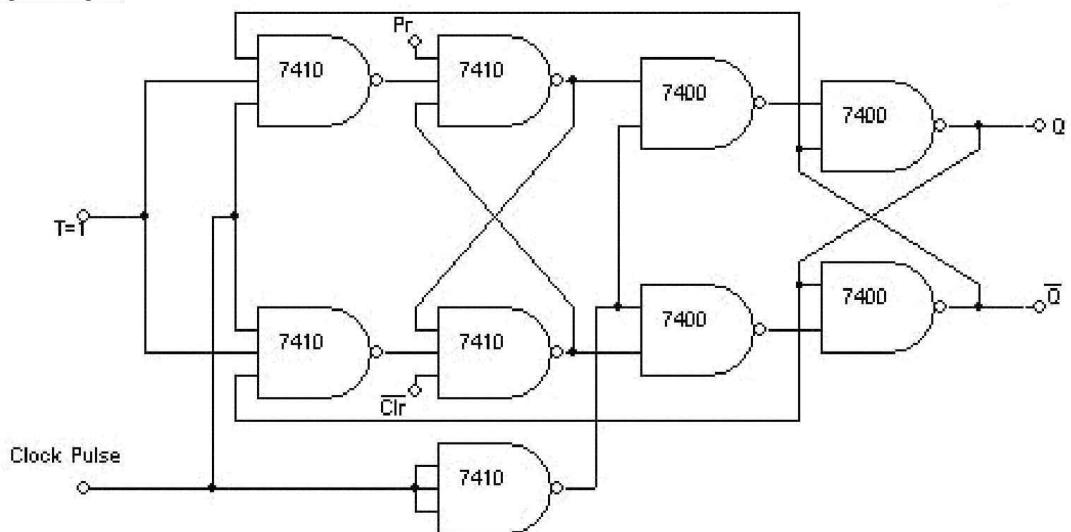
Circuit Diagram: - (Master Slave JK Flip-Flop)



D Flip-Flop:-



T Flip-Flop:-



FLIP-FLOP

Aim:- Truth table verification of Flip-Flops:

- (i) JK Master Slave
- (ii) D- Type
- (iii) T- Type.

Apparatus Required:-

IC 7410, IC 7400, etc.

Procedure:-

1. Connections are made as per circuit diagram.
2. The truth table is verified for various combinations of inputs.

Truth Table:- (Master Slave JK Flip-Flop)

Preset	Clear	J	K	Clock	Q_{n+1}	\bar{Q}_{n+1}	
0	1	X	X	X	1	0	Set
1	0	X	X	X	0	1	Reset
1	1	0	0	⊟	Q_n	\bar{Q}_n	No Change
1	1	0	1	⊟	0	1	Reset
1	1	1	0	⊟	1	0	Set
1	1	1	1	⊟	\bar{Q}_n	Q_n	Toggle

D Flip-Flop:-

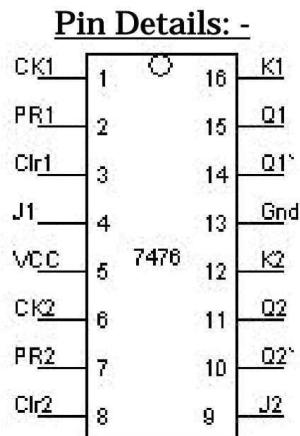
Preset	Clear	D	Clock	Q_{n+1}	\bar{Q}_{n+1}
1	1	0	⊟	0	1
1	1	1	⊟	1	0

T Flip-Flop:-

Preset	Clear	T	Clock	Q_{n+1}	\bar{Q}_{n+1}
1	1	0	⊟	Q_n	\bar{Q}_n
1	1	1	⊟	\bar{Q}_n	Q_n

Exercise:-

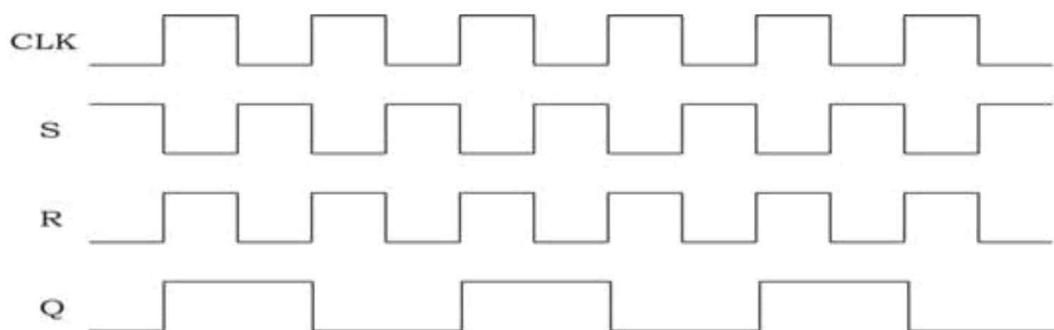
- Write the timing diagrams for all the above Flip-Flops



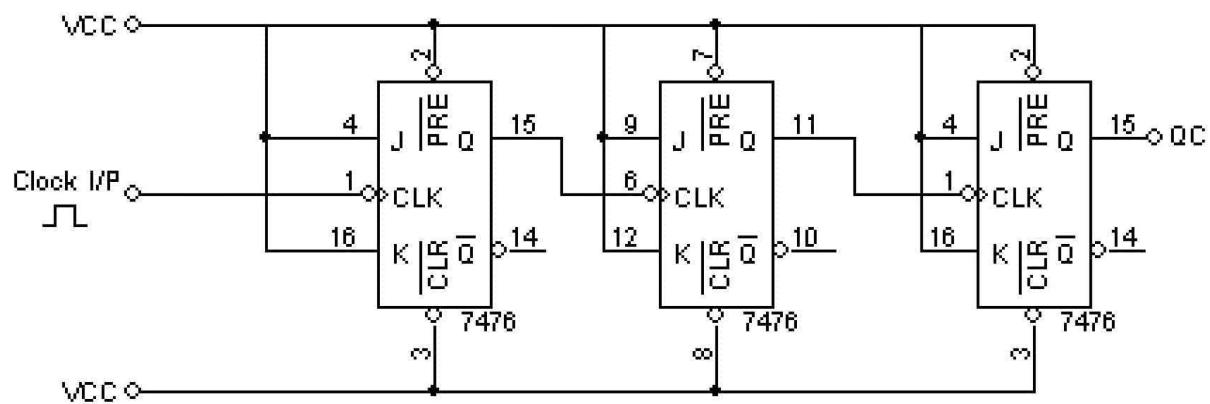
Truth Table:-

Clock	QC	QB	QA
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

Timing Diagram:-

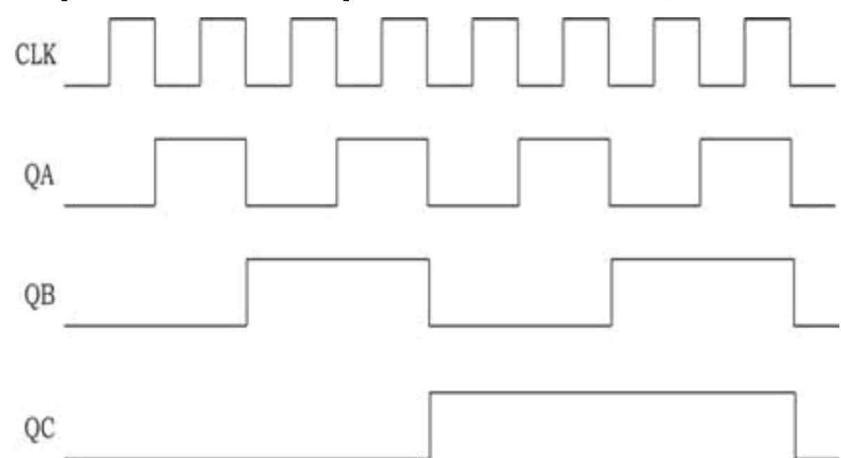


Circuit Diagram: - 3-Bit Asynchronous Up Counter



3-bit Asynchronous up counter

Clock	QC	QB	QA
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0



COUNTERS

Aim:- Realization of 3-bit counters as a sequential circuit and Mod-N counter design (7476, 7490, 74192, 74193).

Apparatus Required: -

IC 7408, IC 7476, IC 7490, IC 74192, IC 74193, IC 7400, IC 7416, IC 7432 etc.

Procedure: -

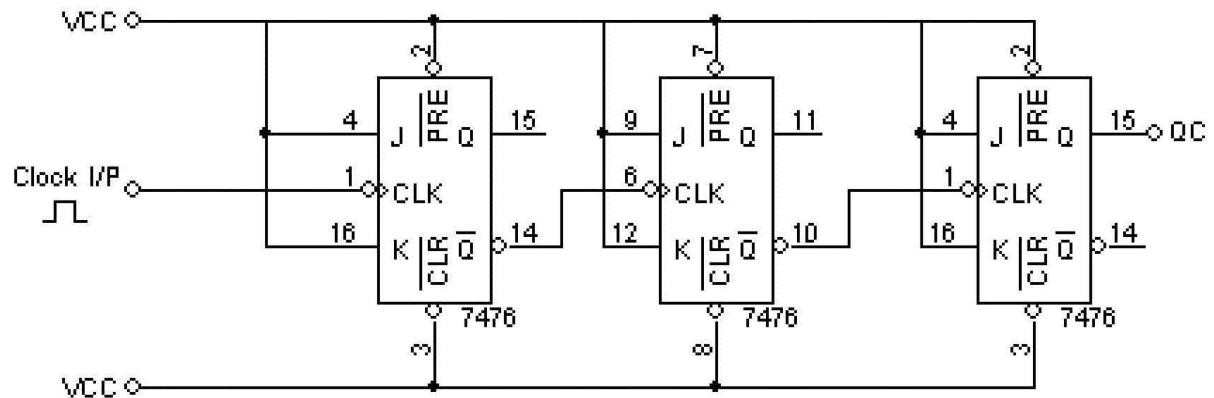
1. Connections are made as per circuit diagram.
2. Clock pulses are applied one by one at the clock I/P and the O/P is observed at QA, QB & QC for IC 7476.
3. Truth table is verified.

Procedure (IC 74192, IC 74193):-

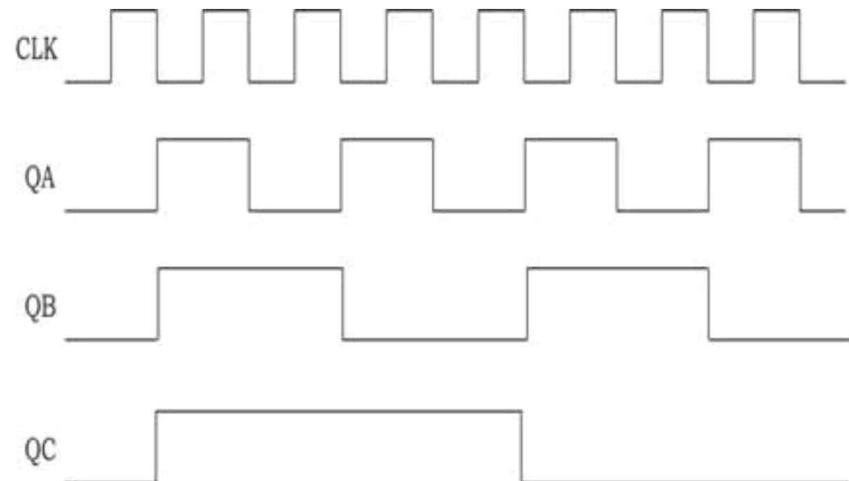
1. Connections are made as per the circuit diagram except the connection from output of NAND gate to the load input.
2. The data $(0011) = 3$ is made available at the data i/p's A, B, C & D respectively.
3. The load pin made low so that the data 0011 appears at QD, QC, QB & QA respectively.
4. Now connect the output of the NAND gate to the load input.
5. Clock pulses are applied to "count up" pin and the truth table is verified.
6. Now apply $(1100) = 12$ for 12 to 5 counter and remaining is same as for 3 to 8 counter.

7. The pin diagram of IC 74192 is same as that of 74193. 74192 can be configured to count between 0 and 9 in either direction. The starting value can be any number between 0 and 9.

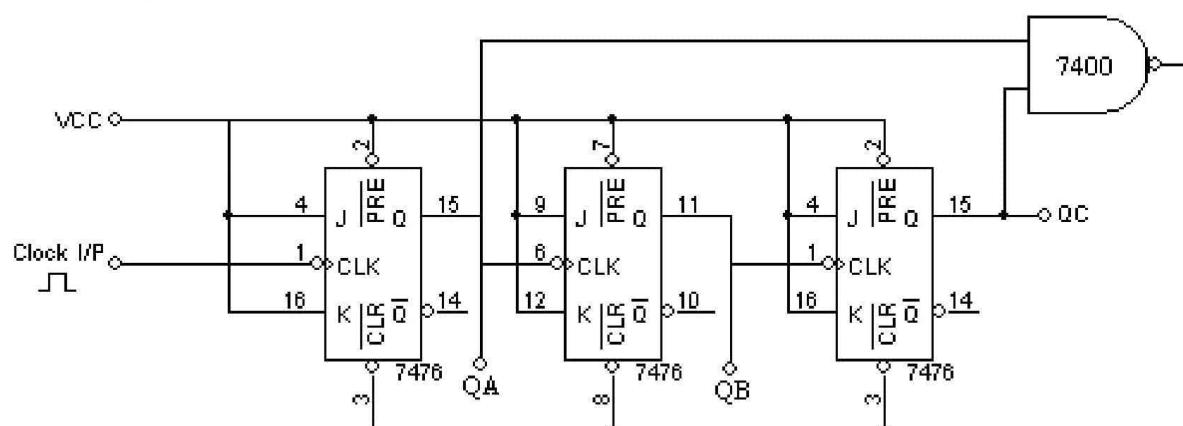
Circuit Diagram: - 3-Bit Asynchronous Down Counter



3-bit Asynchronous down counter			
Clock	QC	QB	QA
0	1	1	1
1	1	1	0
2	1	0	1
3	1	0	0
4	0	1	1
5	0	1	0
6	0	0	1
7	0	0	0
8	1	1	1
9	1	1	0

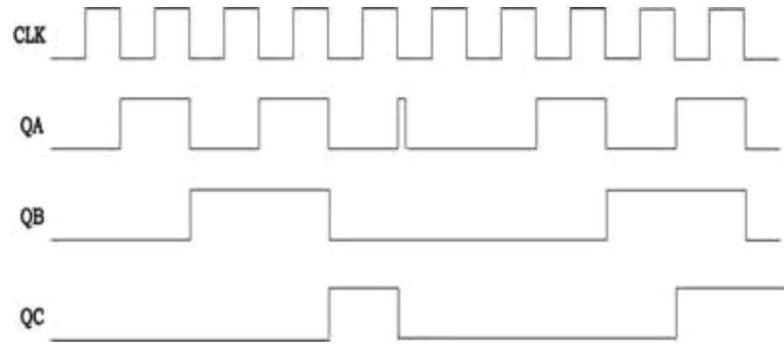


Mod 5 Asynchronous Counter:-

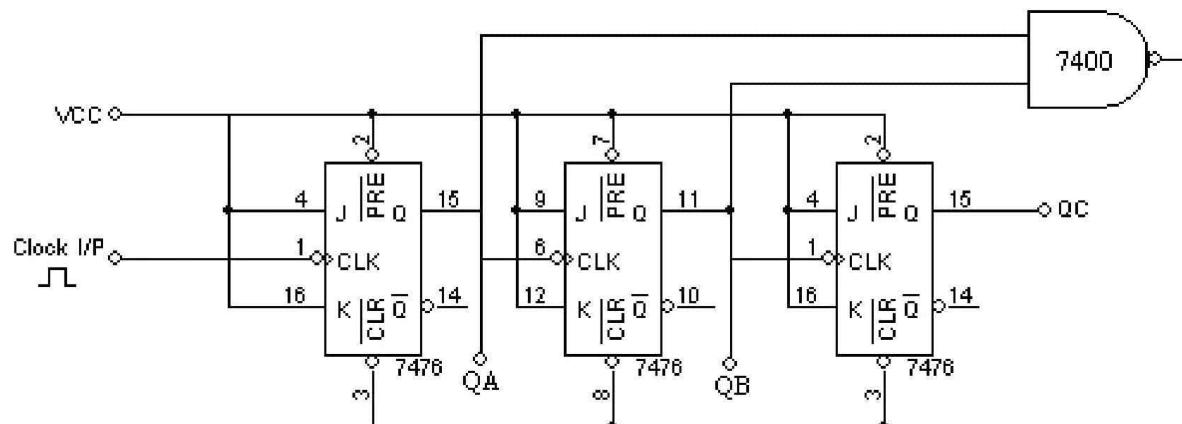


Mod 5 Asynchronous counter

Clock	QC	QB	QA
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	0	0	0

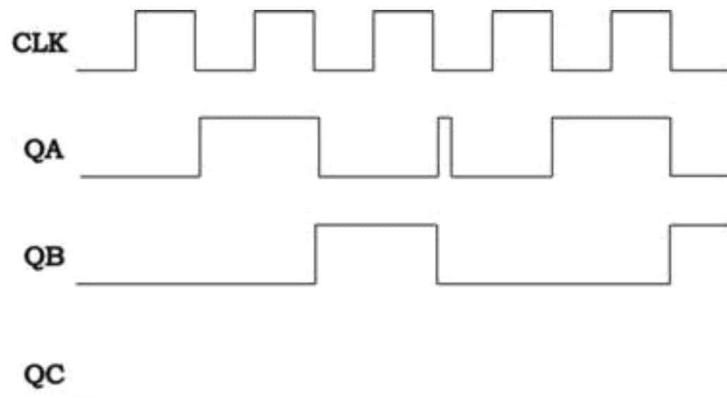


Mod 3 Asynchronous Counter:-

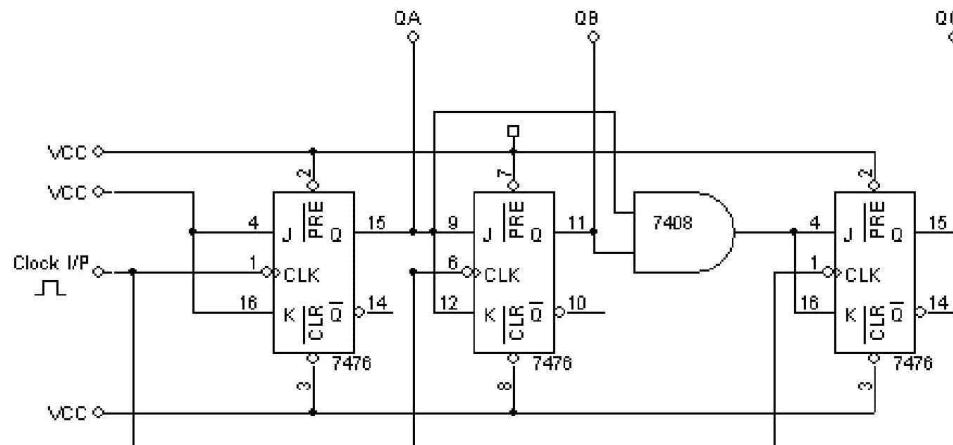


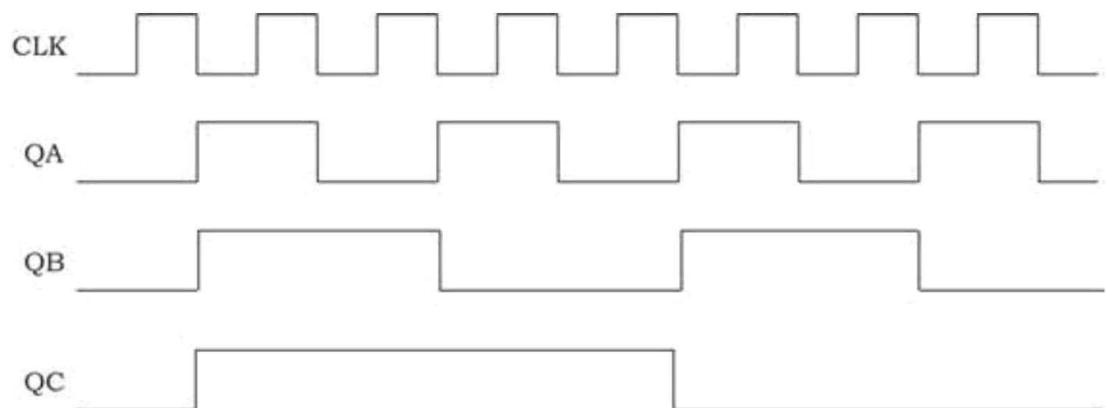
Mod 3 Asynchronous counter

Clock	QC	QB	QA
0	0	0	0
1	0	0	1
2	0	1	0
3	0	0	0
4	0	0	1
5	0	1	0

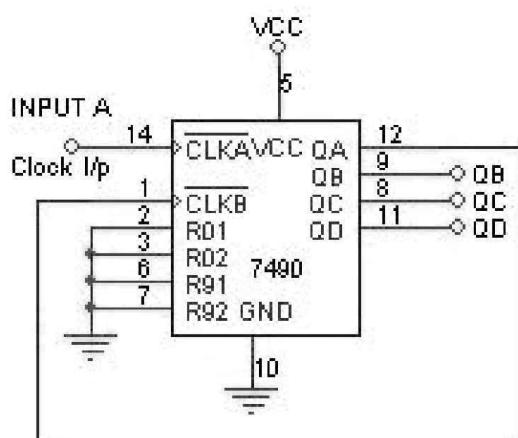


3-bit Synchronous Counter:-



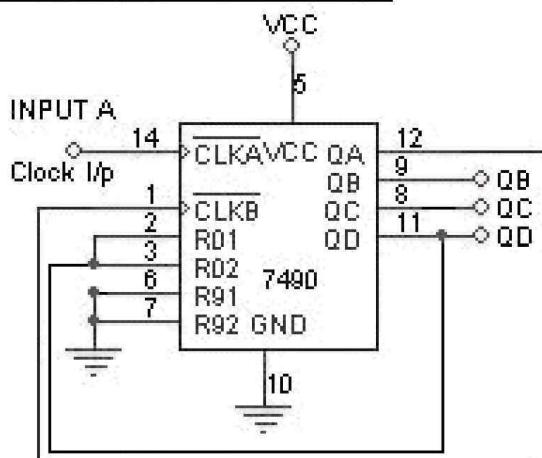


IC 7490 (Decade Counter):-



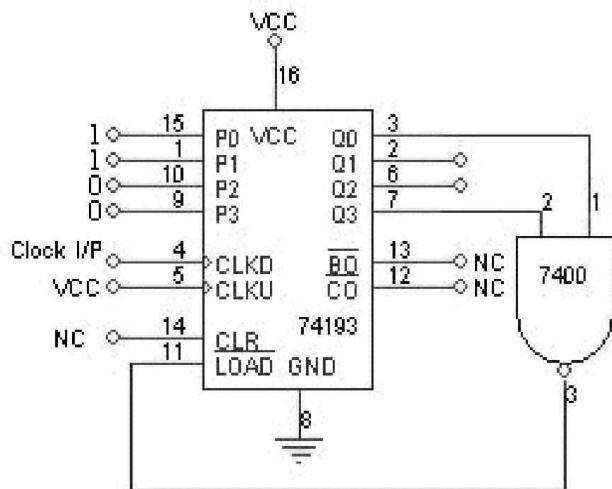
Clock	QD	QC	QB	QA
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	0	0	0	0

IC 7490 (MOD-8 Counter):-



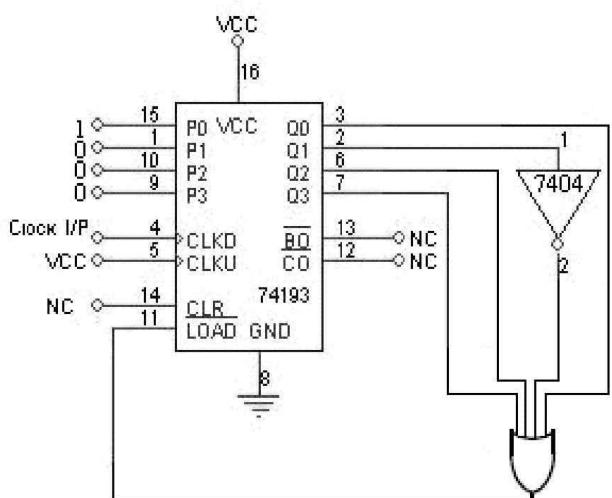
Clock	QD	QC	QB	QA
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	0	0	0	0
9	0	0	0	1

Circuit Diagram (IC 74193) To Count from 3 to 8:-



Clock	QD	QC	QB	QA	Count in Decimal
0	0	0	1	1	3
1	0	1	0	0	4
2	0	1	0	1	5
3	0	1	1	0	6
4	0	1	1	1	7
5	1	0	0	0	8
6	0	0	1	1	3
7	repeats				4

Circuit Diagram (IC 74193) To Count from 8 to 3:-

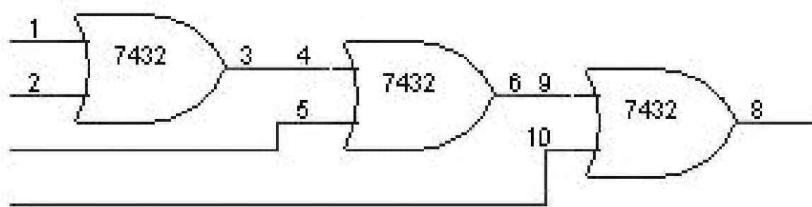


Clock	QD	QC	QB	QA	Count in Decimal
0	0	1	0	1	5
1	0	1	1	0	6
2	0	1	1	1	7
3	1	0	0	0	8
4	1	0	0	1	9
5	1	0	1	0	10
6	1	0	1	1	11
7	1	1	0	0	12
8	0	1	0	1	5
9	repeats				6

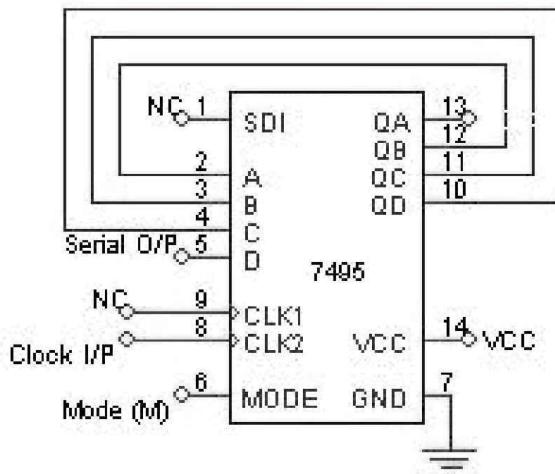
Function Table for 7490:-

Clock	R1	R2	S1	S2	QD	QC	QB	QA	
X	H	H	L	X	L	L	L	L	RESET
X	H	H	X	L	L	L	L	L	RESET
X	X	X	H	H	H	L	L	H	SET TO 9
<u>l</u>	X	L	X	L					COUNT
<u>l</u>	L	X	L	X					COUNT
<u>l</u>	L	X	X	L					COUNT
<u>l</u>	X	L	L	X					COUNT

4 I/P OR Gate can be realized as follows:-

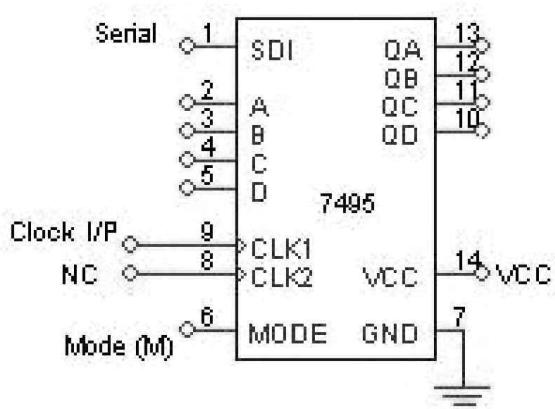


Circuit Diagram: - Shift Left



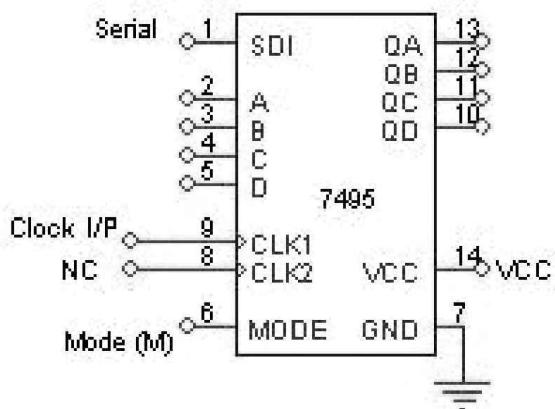
Clock	Serial i/p	QA	QB	QD	
1	1	X	X	X	1
2	0	X	X	1	0
3	1	X	1	0	1
4	1	1	0	1	1

SIPo (Right Shift):-



Clock	Serial i/p	QA	QB	QD	
1	0	0	X	X	X
2	1	1	0	X	X
3	1	1	1	0	X
4	1	1	1	1	0

SISO:-



Clock	Serial i/p	QA	QB	QD	
1	do=0	0	X	X	X
2	d1=1	1	0	X	X
3	d2=1	1	1	0	X
4	d3=1	1	1	1	0=do
5	X	X	1	1	1=d1
6	X	X	X	1	1=d2
7	X	X	X	X	1=d3

SEQUENCE GENERATOR

Aim:- Design of Sequence Generator.

Apparatus Required:-

IC 7495, IC 7486, etc.

Design:-

To generate a sequence of length S it is necessary to use at least N number of Flip-Flops, which satisfies the condition $S \leq 2^N - 1$.

The given sequence length $S = 15$.

Therefore $N = 4$.

Note: - There is no guarantee that the given sequence can be generated by 4 f/fs. If the sequence is not realizable by 4 f/fs then 5 f/fs must be used and so on.

Procedure:-

1. Connections are made as per the circuit diagram.
2. Clock pulses are applied one by one and truth table is verified.

Conclusion:-