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## NATIONAL INSTITUTE OF TECHNOLOGY GOA

Farmagudi, Ponda, Goa, 403401

Programme Name: B.Tech

End Semester Examinations, December-2022

Course Name: Computer Organization and Architecture

Course Code: CS202

Date: 07/12/2022

Time: 02:00 PM-05:00 PM

Duration: 3 Hours

Max. Marks: 100

### ANSWER ALL QUESTIONS

- 1.
- Draw a neat diagram of sequential circuit binary multiplier.
  - Using the approach followed in sequential circuit binary multiplier, multiply 26 (multiplicand) and 30 (multiplier). Here n=5.
- (5+5=10 marks)

- 2.
- Multiply -11 (multiplicand) by 27 (multiplier) using bit pair recoding of multiplier method
  - Divide 45 (dividend) with 15 (divisor) using non restoring division algorithm. Here the divisor is represented using 6 bits.
- (5+5=10 marks)

3. Using single-precision floating point representation

- Add 0.5 and 1.5
- Multiply 1.75 by 0.25

Note: The IEEE standard 754 representation must compulsorily be used for above operations.

(5+5=10 marks)

- 4.
- Improving the RAM of a computer typically improves performance because
    - Virtual memory increases
    - Larger RAMs are faster
    - Fewer page faults occur
    - Fewer segmentation faults occur

Choose the correct answer(s)

Justify the answer

- 8 MB  
CM
- Consider a system with 2 levels of cache. Access times of Level 1 cache, Level 2 cache and main memory are 1 ns, 10 ns, and 500 ns, respectively. The hit rates of Level 1 and Level 2 caches are 0.8 and 0.9, respectively. What is the average access time of the system ignoring the search time within the cache?
  - How many 32K X 1 RAM chips are needed to provide a memory capacity of 256 K bytes?
  - Consider a computer with a 4-way set-associative mapped cache of the following characteristics: a total of 1 MB of main memory, a word size of 1 byte, a block size of 128 words and a cache size of 8 KB. What are the number of bits in the TAG, SET and WORD fields?

(2+2+2+4 = 10 marks)

5. A byte-addressable computer has a small data cache capable of holding eight 32-bit words. Each cache block consists of one 32-bit word. When a given program is executed, the processor reads data from the following sequence of hex addresses:  
 ✓ 200, 204, 208, 20C, 2F4, 2F0, 200, 204, 218, 21C, 24C, 2F4  
 This pattern is repeated four times.
- Show the contents of the cache at the end of each reference if a direct-mapped cache is used. Compute the hit rate for this example. Assume that the cache is initially empty.
  - Repeat part (a) for an associative-mapped cache that uses the LRU (least recently used) replacement algorithm.
  - Repeat part (a) for a four-way set-associative cache.

(8+8+8=24 marks)

- 6.
- The total size of address space in a virtual memory system is limited by
    - The length of MAR
    - ✓ The available secondary storage
    - ✓ The available main memory
    - All of the above
- Choose the correct answer(s)  
 Justify your answer
- Which of the following is/are advantage of virtual memory?
    - Faster access to memory on an average
    - Processors can be given protected address space
    - ✓ Linkers can assign addresses independent of where the program will be loaded in physical memory
    - ✓ Programs larger than the physical memory size can be run

Choose the correct answer(s)

Justify your answer

- What is address translation process in the presence of virtual memory? How is it performed? Briefly explain

(2+2+2=6 marks)

- 7.
- What are the approaches to achieve required synchronization between processor and an I/O device?
  - A hardwired CPU uses 10 control signals S1 to S10 in various time steps T1 to T5 to implement 4 instructions I1 to I4 as shown below:

	T1	T2	T3	T4	T5
I1	S1,S3,S5	S2,S4,S6	S1,S7	S10	S3,S8
I2	S1,S3,S5	S8,S9,S10	S5,S6,S7	S6	S10
I3	S1,S3,S5	S7,S8,S10	S2,S6,S9	S10	S1,S3
I4	S1,S3,S5	S2,S6,S7	S5,S10	S6,S9	S10

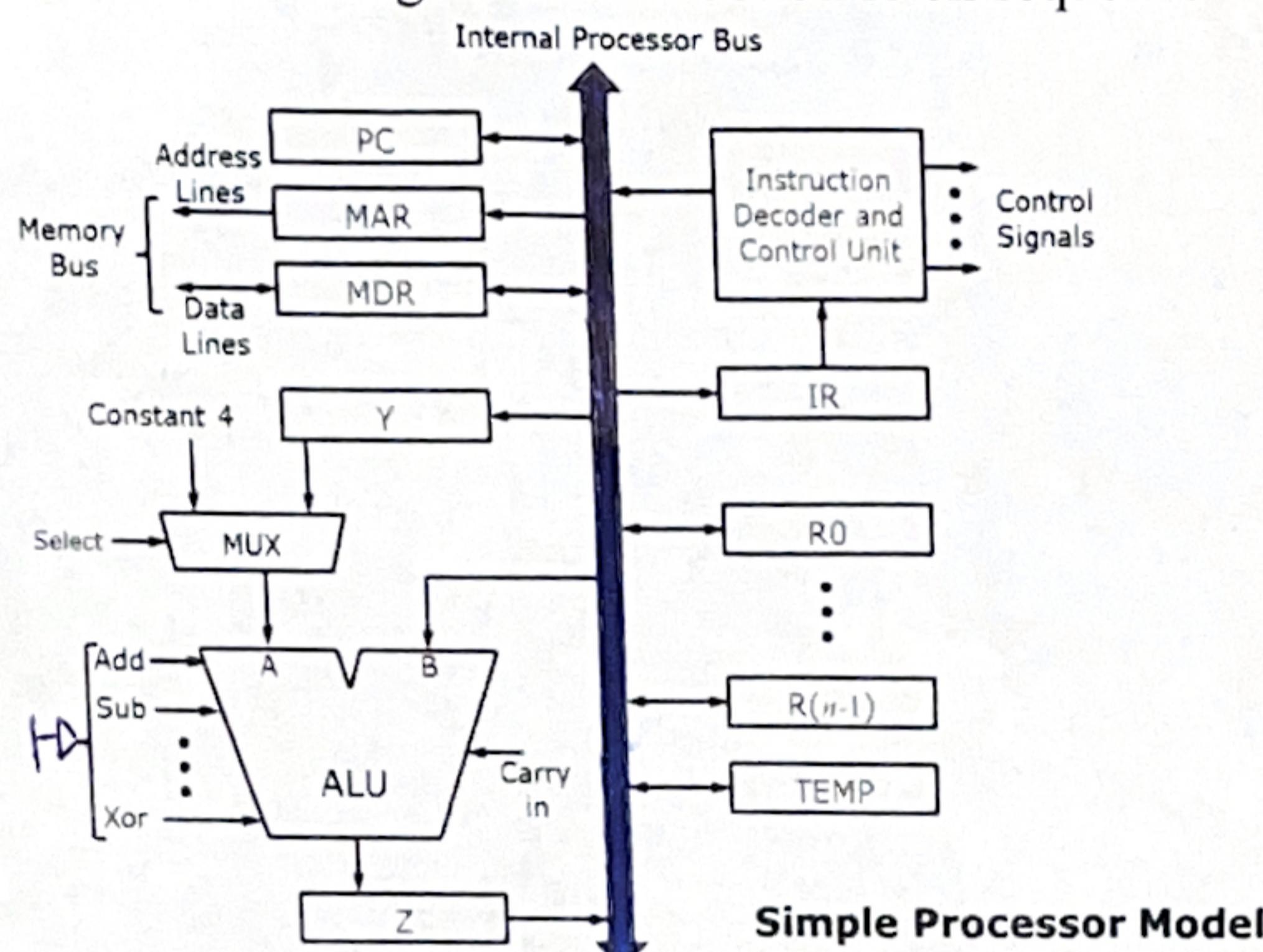
Derive an expression each to represent the circuit for generating every control signal.

(5+5=10 marks)

8. Assume that a processor has single internal bus as shown in the Figure below. Give the control sequences for the following

- Instruction fetch
- Execution of **MUL R3, [R1], R2** that corresponds to multiplying the content of memory location pointed to by R1 to the content of register R2 and storing the result of multiplication in R3
- Execution of **SUB R1, #NUM** that corresponds to subtracting the (immediate) number NUM to register R1.
- Execution of **JN LoopBegin** that corresponds to conditional jump on negative to LoopBegin

**Note** For b,c,d there is no need to give the instruction fetch sequence



(10 marks)

9.

- a. Draw a neat pipeline flow diagram for the following segment of code.

- I1 LOAD R0, N
- I2 LOAD R1, X
- I3 LOAD R2, Y
- I4 MUL R3, R1, R2
- I5 ADD R4, R2, R3
- I6 STORE Z, R4
- I7 FADD F0, F1, F2
- I8 FMUL F5, F6, F7

Assume that the program is running on a hardware that supports 5 stage pipeline (IF, ID, RD, EX, WB). The block containing instructions I1, I2 and I3 is not available in cache. Hence fetching (IF) step of I1 will take 3 cycles and I2 and I3 take 1 cycle. Similarly, the block containing I7 and I8 need to be mapped onto I-cache. Hence, fetching (IF) of I7 will take 2 cycles and I8 1 cycle. Assume that N, X and Y are the locations on L1 cache and Z is the location in main memory. The execution stage of LOAD in I1, I2 and STORE in I6 take 1 clock cycle and LOAD in I3 take 2 clock cycle. The execution stage of MUL and ADD instructions take 3 and 1 clock cycles respectively. The execution stage of FADD and FMUL to take 3 and 4 cycles respectively. Mention the total number of clock cycles needed.

- b. What are pipeline hazards? Explain

10 10

(6+4=10 marks)