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Paper Code	BCS-11

Roll No.									

B.Tech. 2nd Year

Odd Semester Examination 2016-2017

DIGITAL CIRCUITS AND LOGIC DESIGN

Time: 3 hrs **Max. Marks: 40**

Note: Attempt all questions. Each question carries equal marks.

Q.1 Attempt any three of the following Q.1(a) is compulsory.

(a) A packet with data 11000100 is transmitted over a network with even parity with single bit error correction. 4

I. Give expression to for finding out parity check bits.

II. Find out how many minimum parity check bits must be included in above data word for single bit error correction.

III. What will be final data word including parity check bits before transmission?

IV. Suppose data word received at receiver end is 001100010100. Find out error bit.

(b) Find the complement of $F = x + yz$. Show that $F.F' = 0$ and $F+F' = 1$. Convert F into canonical sum-of-product form. 3

(c) Determine the value of x if $(211)_x = (152)_8$. Convert binary number 110110101 to base x number system. 3

(d) What is weighted and non-weighted binary codes. Give atleast two example of each. Convert Gray code 10111011 to decimal number system. 3

Q.2 Attempt any three of the following Q.2(a) is compulsory.

(a) Simplify the following Boolean expression F together with don't care d using K-map. 4

$$F(A,B,C,D,E) = \sum(0,2,3,4,5,6,7,11,15,16,18,19,23,27,31)$$

$$d(A,B,C,D,E) = \sum(1,13,21.29)$$

(b) Design a combinational circuit with three input and six outputs. The output binary number should be the square of the input binary number. 3

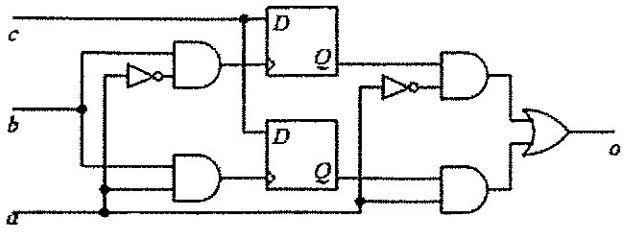
(c) Design an eight-bit adder using only four-bit adders. Each four-bit adder has two four-bit inputs and one five-bit output. Your eight-bit adder should have two eight-bit inputs and a one nine-bit output. 3

(d) Implement the following Boolean function using an 8 x 1 multiplexer. 3

$$F(A,B,C,D) = \sum(0,3,5,6,8,9,14,15)$$

Q.3 Attempt any three of the following Q.3(a) is compulsory.

(a) Consider the following circuit with two D flip-flops. 4



Say a user enters the sequence of inputs given in following table, one after the other. Label what the output of the circuit will settle into after each of the user's inputs.

a	*b*	*c*	*o*
1	1	1	?
0	1	1	?
0	0	1	?
0	0	0	?
0	1	0	?
0	0	0	?
1	0	0	?

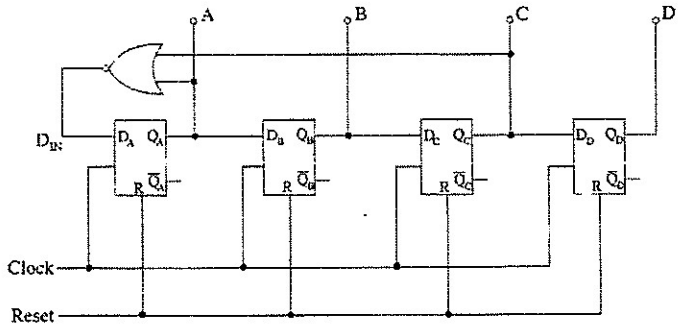
(b) Convert D flip flop to JK flip flop. Explain the conversion process in detail. 3

(c) Design a 4-bit binary synchronous counter with D flip flop. 3

(d) Construct a mod-9 asynchronous up-counter using T Flip-Flop. Give the number of T Flip-Flop required to construct the above counter. 3

Q.4 Attempt any three of the following Q.4(a) is compulsory.

(a) The following circuit diagram shows a Serial Input Parallel Output shift register with outputs A and C connected to a NOR gate. The output of the NOR gate is used to generate D_{IN}. 4



Initially the shift register is reset so that outputs A, B, C and D are logic 0. Complete the following table to give the state of the output after the given number of clock pulses have been applied.

Clock Pulse	Outputs A	B	C	D
0	0	0	0	0
1				
2				
3				
4				

pipelined processor.

b) Consider a four-stage floating point adder with a 2-ns delay per stage which equals the pipeline clock period.

I. Name the appropriate functions to be performed by UTE four stages.

II. Find the minimum number of periods required to add 100 floating-point numbers A1 + A1 + ...+ An using this pipeline adder, assuming that the output Z of stage S4 can be routed back to either of the two inputs X or Y of the pipeline with delays equal to a multiple of the clock period.

c) Consider the following reservation table for a four stage pipeline

	1	2	3	4	5	6
S1	X					X
S2		X		X		
S3			X			
S4				X	X	

I. Find the forbidden latencies and initial collision vector.

II. Draw the state transition diagram for scheduling the pipeline and determine the Minimum available latency

d) Discuss super scalar execution. Also compute the performance of m-issue superscalar machine.