ECS301

Roll No: | | | | | | | | | | |

B. Tech.
(SEM III) ODD SEMESTER
THEORY EXAMINATION 2013 - 2014

DIGITAL LOGIC DESIGN

Time: 3 Hrs. Max. Marks: 100

Note: Attempt all questions.

Q.1 Attempt any four parts of the following: 4 x 5 = 20

(a) What is difference between Boolean Function and Boolean algebra? Discuss with example.

(b) Perform the decimal addition in the 8421 code and by 9's complement method on 679.6 + 536.8

(c) Simplify the Boolean function and implement with NAND gate
$F(A,B,C,D)=\sum(1,3,10)+\sum_d(0,2,8,12)$

(d) Minimize the following switching function using the Quine-Mc Cluskey method
$f(x_1,x_2,x_3,x_4) = \sum_m(0,5,7,8,9,10,11,14,15)$

(e) Dicuss the difference between Error detection and Error correcting code.

(f) Discuss about Hamming code.

Q.2 Attempt any two parts of the following: 2 x 10 = 20

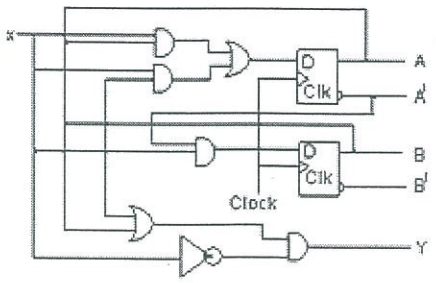
(a) Discuss the difference between decoder and demultiplexer. Explain three-to-eight-line decoder.

(b) What is multiplexer? Draw the circuit diagram of Quadruple 2-to-1-line multiplexer and discuss the working of it.

(c) Define Carry propagation phenomena. How can you rectify it with carry look ahead logic and draw the logic diagram of carry look ahead generator.

Q.3 Attempt any two parts of the following: 2 x 10 = 20

(a) Define state equation and state table. Draw the state diagram of following circuit diagram.



(b) What is Universal shift register? Draw the block diagram and circuit diagram of Four bit universal shift register.

(c) What is Binary Ripple counter? D raw the logic diagram of Four bit binary ripple counter.

Q.4 Attempt any two parts of the following: 2 x 10 = 20

(a) What is READ-ONLY MEMORY (ROM)? Give the detail of 32 X 8 ROM.

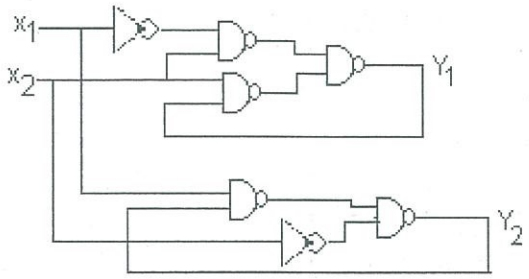
(b) Define Programmable logic device (PLDs). Explain the difference between PLA and PAL with example.

(c) What is Algorithmic state Machines (ASMs)? Discuss about ASMD chart with example.

Q.5 **Attempt any two parts of the following:** 2 x 10 = 20

(a) Explain RACE-FREE state assignment concept and Hazards with suitable example.

(b) Derive the transition table for the asynchronous sequential circuit shown in given below figure.



Determine the sequence of internal state Y_1 Y_2 for the following sequence of inputs X_1 X_2 : 00, 01, 11, 10.

(c) Draw the Block diagram of an asynchronous sequential circuit. Discuss the Analysis procedure using the concept of stability of asynchronous sequential circuits.