

Name Manush Shazim Faculty. Class Batch 3 Sem.

AIM: to verify the truth table of basic gats: AND, OR, NOR, NAND, Not also verify the truth table of

Ex=-or,-Nor, Jor(2,3,4 as an input)
(2,3,4 as an output)

Approxt us Required: - Tarainer Kit, power Supply and commecting lids

Theory: - There are three types of lagical gates
In which three are basic gates that
and Not, OR, AND gates and two universal
gates NOR, Nand two Special gates
Ex-OR, Ex-NOR the basic gates do basic
authomatic operations like Not gates does
inverse of Imput OR gates does addition of
Imput and AND gate does multiplication of
Imput there are forme foundamentals of
This gates.

A y= A an NOT gates

B = A+B An OR gates



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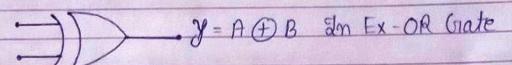
A- Y= A-B In AND gates

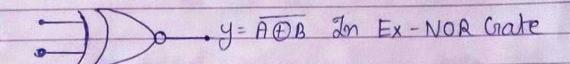
universal gates are in like:

A - Y = A+B In NOR gates

B - Y = A.B In NAND gates

Special gates





* Procedure:
ii Verification of truth table of 'AND' Grates

iii Verification of truth table of 'AND' Grates

iii Commect A and B input AND gates to logic

Imput 'O' & 'O' as Shown in the to totale

truth table of AND gate

(b) quater as the imstuments using off y

toggle switch provided on the front



Name Manush Sharma Faculty Class Batch & Sem (3) Because the output indicator. If It glosus the is that the output is in (1) and otherwise 'o' tion of input A and B as in the truth (4) table for AND gate de verification of truth table of 'OR' input '0' and '0' is thrown in the truth dable for OR Grate also. (2) Switch on the instrument using off on taggle provided on the front panel The output . If It glow the Indication is that output is " and otherwise's (4) Similarly verify the output for other combination of imput 'A' and 'B) 1 Connect A and B imput of Ex-OR gates to dogic imput 10' and 10' as for Ex-OR gates also comment output of Ex-OR gate to output indicates.



Experiment No.... Page No. 4 Name Month Sharma Faculty Class Batch & Sem (d) Similer on the interment using OFFION toggle reviter provided on the front panel.

3) The output indicater if it glow the indicator that output is 1' and if also not Similarly verify the output for other com-bination of A and B in truth table for Exor gate. (4) Verification of but table for NOR (a) connect A and B at NOR gate to logic input NOR gate to output indicator through ON the instrument using OFFION c) toggle

(c) The output if Andicator glow than output is '1' and 'o'

(D) verify the output for other of A and B (5) Voitication of NAND Crate. ii connecte A and B imput of NAND Gate to Jogic in putts '0' and '0' for NAND gate - Also connect output Indicator on the instrument. (ti) (iii) verify the output of other of A and B

	Modi Institute of Technology, KOTA Date Experiment No. 4 Page No. 5 Name Manish Sharma Faculty Class Batch 3.8.270
(0)	Vertification of NOT gate. Connect A imput of NOT gate to logic imput 'o' also gate connect output of NOT gate to output indicator
(b)	on the anstrument.
(c)	the output Indicator
	Similary verify the output of other imputs Result: Thus are verified the truth table of logic gate.



Modi Institute of Technology, KOTA
Date Page No. 2
Name Monish Shoomoraculty. Class Batch 3 Sem
Name.t.,(Chita.b.)
aim:- To verify the truth table of OR, AND NOR, EX-OR, EX-NOR utalized using NAN and NOR gates.
NAME - 10 VERLEY - NOR Utalized using NAM
JVOR, EX-OR, EX-NOR CAMERO
and took gaves.
Appratus Required: - trainer Kit, power Supply connecting lids.
commecting lids.
theory: for every Boolean expression the logic circuit can be shult
logic circuit can be shult
for every dogic current, can while a poolities
expression to Build algic circuit or gates is
used for multiplication Sign and NOT
is used for inverse, Herice they ding of
logic gares an dance that the property
of the of logic
logic circuit have the property of it
If the no logic gates for particular are
given other logic can be obtaine by
expression to Build Logic circuit of gates is used for multiplication. Sign and Not gate is used for inverse, Hence AND, OR and Not Logic gates all called busic beuilding of Logic circuit. Logic circuit have the property of it of the mo Logic gates for particular are given other Logic can be obtaine by of these gate NAND and NOR gates the basic block. Hence NAND and NOR are called universal beuilding block
gates the basic solock, nonce while one
NOR one caused graversal vertiling shock

of Jogic gates.

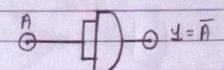
Riocedure: - Cverification of "nano", "AND" gates

NAND as AND gates.

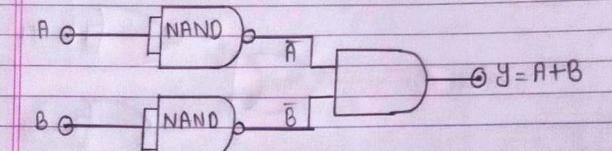


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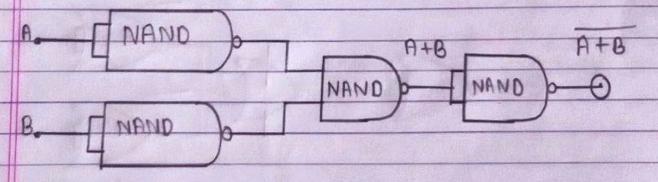
verification of "NAND" as "NOT" gate.



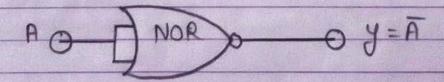
verification of "NAND" as "OR" gate

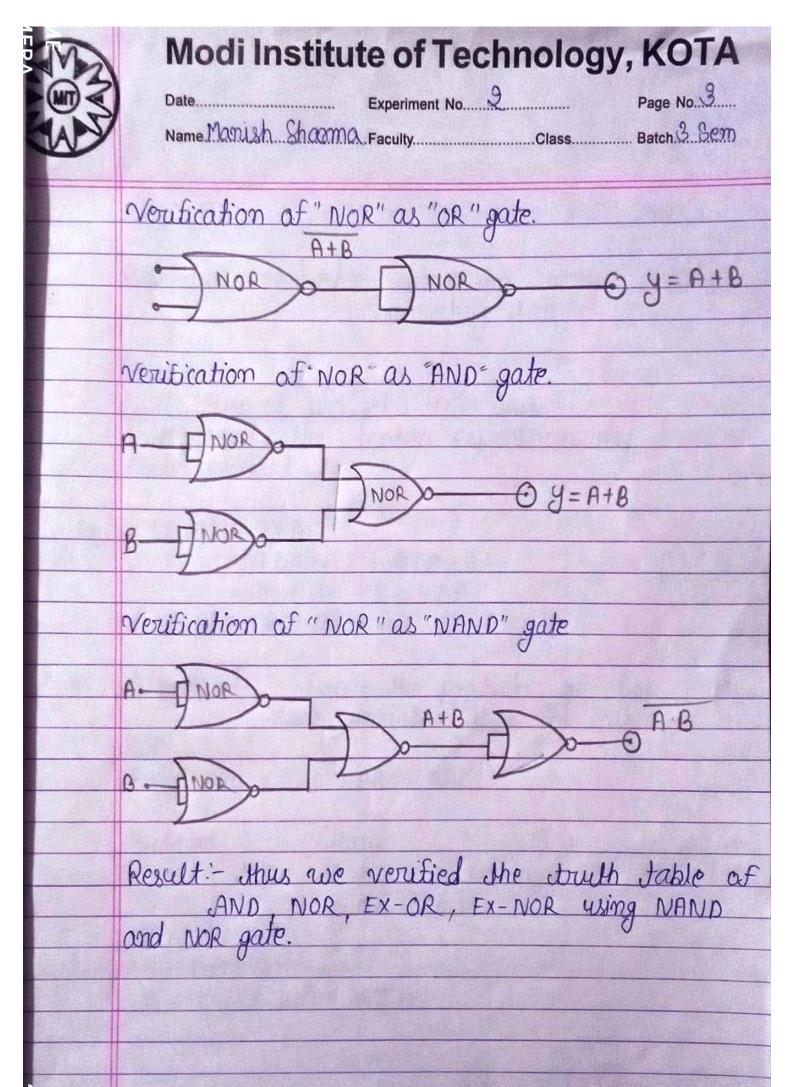


voiltication of "NAND" as NOR gate



Verification of NOR as NOT gate







Name Manual Shanno-Faculty Class Batch 3.8cm

Aim: - To an Sop and pos exp.

approatus required: - Trainer Kit, power supply connecting leds.

SOP [Sum of product] -> In this we orepresent the boaten expression by sum of each product

Eq $f(A,B) = A + \overline{B}$ $= A(B + \overline{B}) + \overline{B}(A + \overline{A})$ $= AB + A\overline{B} + \overline{B}A + \overline{B}\overline{A}$ $f(A,B) = AB + A\overline{B} + A\overline{B}$

Standard Sop: - the product of Sop that each variable then Sop called

Eg: ABC + ABC + ABC + ABC

Minterm: - Jean Sop produce

Jean that is logic I called as

of Sop or

Eq:-

Y= [f(A, B)] = m [12

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Date
Name Manish SharmPaculty
Pos (Product of Sum): - In this technique we
(MODICACIO)
by the product of each Sum form. Eq: y = (A+B+C). (A+B). (A+B+C)
Stondard POS: - The Sum item of pos that con-
- ta each varible then pos.
$\mathcal{J} = (A + \overline{B} + C) \cdot (\overline{A} + B + C) \cdot (A + B + \overline{C})$
Max Jerm: In the Pos thate Sum
Max Jerm: In the POS thate sum throw that value is dogical 'O' called
as max term
$\mathcal{Y} = (A+B) \cdot (\overline{A}+\overline{B})$
y= [(f (AB)]
Relization of pos: - (: $A\overline{A} = 0$) f(A,B) = (A+B)(B)
$\mathcal{F}(A,B) = (A+B)(B)$
$= (A+B)(B+A\bar{A})$
$= (A+B)(B+A)(B+\bar{A})$
$f(A,B) = (A+B)(\overline{A}+B)$
$y = (A+B)(\bar{A}+B)$
a 11. a 11. an applier and San and Pa
Result - & mus we nearly an sop was ro.
Result: 8 thus we realize an Sop and Po. exp by lisning of lagic gate.