Prelab 3

Tuesday, September 14, 2021 1:03 PM

#1 $F2(W,X,Y,Z) = (X' \cdot Y')' \cdot (W \cdot Z)'$

W	X	Y	Z	F(W,X,Y,Z)
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	$0 \cdot 1 = 0$
1	0	0	1	$0 \cdot 0 = 0$
1	0	1	0	$1 \cdot 1 = 1$
1	0	1	1	$1 \cdot 0 = 0$
1	1	0	0	$0 \cdot 1 = 0$
1	1	0	1	$0 \cdot 0 = 0$
1	1	1	0	$1 \cdot 1 = 1$
1	1	1	1	$1 \cdot 0 = 0$

2) $F1(W,X,Y,Z) = X \cdot Z' + W' \cdot X + W' \cdot Y + Y \cdot Z'$

$= ((X \cdot Z')' \cdot (W' \cdot X)' \cdot (W' \cdot Y)' \cdot (Y \cdot Z')')'$

3) $F2(W,X,Y,Z) = (X' \cdot Y')' \cdot (W \cdot Z)'$

$= (X + Y) \cdot (W' + Z')$

$= ((X + Y)' + (W' + Z')')'$

4) 74HC00 style 2 input NAND gate

74HC02 style 2 input NOR gate

74HC04 style inverters

74HC08 style 2 input AND gates (74LS08)

74HC10 style 3 input NAND gates (74LS10)