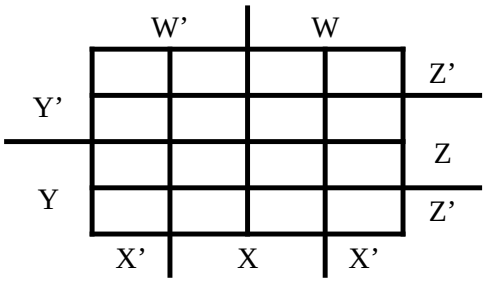
1) For a function F(W,X,Y,Z) that has the following truth table, fill in the equivalent Karnaugh map for it below, and use it to determine the minimal sum of products for F.

W	X	Y	Z	F(W,X,Y,Z)
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0



A) W'X' + Y'Z' + W'Y'Z'
B) XY + X'Z' + WXZ'
C) X'Z' + Y'Z' + WXY'
D) W'Y + W'X + XY'Z'
E) None of the above

2) If the function F(X,Y,Z) is represented by the **ON set** $\Sigma_{X,Y,Z}$ (2,3,4), the **complement** of this function is represented by the **OFF set**:

A) $\Pi_{X,Y,Z}$(0,1,5,6,7)
B) $\Pi_{X,Y,Z}$(2,3,4)
C) $\Pi_{X,Y,Z}$(1,7)
D) $\Pi_{X,Y,Z}$(2,3,5,6,7)
E) None of the above

3) If the function F(X,Y,Z) is represented by the **ON set** $\Sigma_{X,Y,Z}$ (0,1,2,3,5), the **complement** of this function is represented by the **ON set**:

A) $\Sigma_{X,Y,Z}$(0,1,2,3,5)
B) $\Sigma_{X,Y,Z}$(2,3,7)
C) $\Sigma_{X,Y,Z}$(0,6)
D) $\Sigma_{X,Y,Z}$(4,6,7)
E) None of the above

4) What device does the expression F(A,B,S) = A·S' + B·S implement?

A) 2-to-1 multiplexer
B) 2-to-1 encoder
C) 1-to-2 demultiplexer
D) 1-to-2 decoder
E) None of the above

5) Which of the following statements is NOT always true for all values of X?

A) X ⊕ 1 = X'
B) X ⊕ X' = 1
C) X' ⊕ 1 = X
D) X ⊕ X = 0
E) None of the above

For the two Karnaugh maps below, pick the minimal sum-of-products expressions for the ON set of F(W, X, Y, Z).

6)

	W'		W		
Y'	d	d	d	d	Z'
	0	d	0	0	
	d	d	1	d	Z
Y	0	1	0	0	Z'
	X'	X		X'	

A) W'·X + Y'·Z
B) Y·Z + Y'·Z'
C) W'·X + Y'·Z'
D) W'·X + Y·Z
E) None of the above

7)

	W'		W		
Y'	0	d	0	0	Z'
	1	d	d	d	
	d	0	0	1	Z
Y	d	0	d	1	Z'
	X'	X		X'	

A) W·X' + X'·Z
B) Y'·Z + Y'·Z'
C) W'·X + Y·Z
D) Y·X' + Y'·Z
E) None of the above

8) What kind of hazard exists for the circuit below?

A) Static-1 when X goes from high-to-low
B) Static-0 when X goes from high-to-low
C) Static-1 when X goes from low-to-high
D) Static-0 when X goes from low-to-high
E) None of the above.

	W'		W		
Y'	1	1	1	1	Z'
	1	0	1	0	
	1	0	0	0	Z
Y	0	0	0	0	Z'
	X'	X		X'	

9) For a circuit realized using a minimal sum of products from the Karnaugh map above, what kind of hazard exists?

A) A static-1 hazard when W=1,X=1,Y=0 and Z changes from low to high
B) A static-1 hazard when W=1,X=1,Y=0 and Z changes from high to low
C) A static-1 hazard when W=0,X=0,Y=0 and Z changes from low to high
D) A static-1 hazard when W=0,X=0,Y=0 and Z changes from high to low
E) None of the above

10) Given the expression

F' (X,Y,Z) = X'·Y·Z + X·Y·Z' + Y·Z

use DeMorgan's law to choose the expression that is the product-of-sums form of F.

A) (X'+Y+Z) · (X+Y+Z') · (Y+Z)
B) (X+Y'+Z') · (X'+Y'+Z) · (Y'+Z')
C) ((X'+Y+Z) · (X'+Y'+Z) · (Y'+Z'))'
D) ((X+Y'+Z') · (X'+Y'+Z) · (Y'+Z'))'
E) None of the above

11) What would be the cost of implementing the expression F(X,Y,Z) = X·Y + X' + Y'·Z + X·Z ? Assume that variables and their complements are provided to you. Gates with any number of inputs are allowed.

A) 11
B) 12
C) 13
D) 14
E) None of the above

12) The output of an n-input XOR function is __ if an odd number of inputs are __. Fill in the blanks.

A) 0, 0
B) 0, 1
C) 1, 0
D) 1, 1
E) None of the above

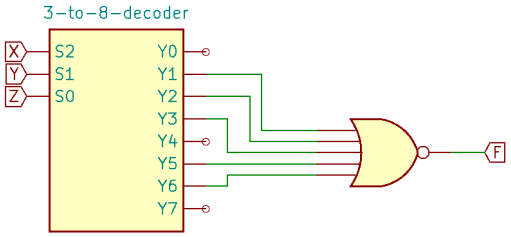
13) If you were given a multiplexer with 8 inputs and 3 select lines, how many output(s) would it have?

A) 1
B) 2
C) 4
D) 16
E) None of the above

14) If you were given an encoder with 16 inputs, how many output(s) would it have?

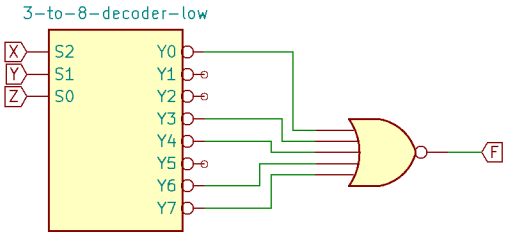
A) 1
B) 2
C) 4
D) 16
E) None of the above

15) What is the ON set for this circuit with a 3-to-8 decoder and a 5-input NOR gate?



A) $\Sigma_{X,Y,Z}(0,4,7)$
B) $\Sigma_{X,Y,Z}(1,2,5,6,7)$
C) $\Sigma_{X,Y,Z}(1,2,3)$
D) $\Sigma_{X,Y,Z}(1,4,5,6)$
E) None of the above

16) What is the OFF set for this circuit with a 3-to-8 decoder and a 5-input NOR gate?



A) $\Pi_{X,Y,Z}(0,3,4,6,7)$
B) $\Pi_{X,Y,Z}(0,3,4)$
C) $\Pi_{X,Y,Z}(1,2,5)$
D) $\Pi_{X,Y,Z}(1,5,6,7)$
E) None of the above

17) An XOR can also be described as:

A) A selective AND
B) A selective OR
C) A selective NOR
D) A selective NAND
E) None of the above

Two Verilog modules are instantiated in the top module as follows:

```
module mystic1 (a, b, c);
input [1:0] a;
input b;
output c;

assign c = a[b];

endmodule

module mystic2 (a, b, c);
input [7:0] a;
input [2:0] b;
output c;

assign c = b == 3'd7 ?  a[7] :
           b == 3'd6 ?  a[6] :
           b == 3'd5 ?  a[5] :
           b == 3'd4 ?  a[4] :
           b == 3'd3 ?  a[3] :
           b == 3'd2 ?  a[2] :
           b == 3'd1 ?  a[1] : a[0];

endmodule

module top
(hz100,reset,pb,
ss7,ss6,ss5,ss4,ss3,ss2,ss1,ss0,
left,right,
red, green,blue);

input hz100, reset;
input [20:0] pb;
output [7:0] ss7, ss6, ss5, ss4,
ss3, ss2, ss1, ss0, left, right;
output red, green, blue;

mystic1 m1 (pb[1:0], pb[2],
right[0]);
mystic2 m2 (pb[15:8], pb[3],
right[0]);

endmodule
```

18) What will be the value of c when a is 2 and b is 1 for the mystic1 module?

A) 0
B) 1
C) 2
D) Hi-Z
E) None of the above

19) What will be the value of c when a is 28 and b is 5 for the mystic2 module?

A) 0
B) 1
C) 2
D) Hi-Z
E) None of the above

20) Which function F(X,Y,Z) does the module below implement?

```
module func (X,Y,Z,F);
input X, Y, Z;
output F;

assign F = X? (~Y? ~Z : 0) : 0;

endmodule
```

A) F = X'·Y·Z'
B) F = X'·Y'·Z
C) F = X·Y'·Z'
D) F = X·Y·Z'
E) None of the above

21) Given three buses declared as follows:

```
wire [15:0] x, y, z;
```

what would be the length of
`{x[10:2],y[8:4],x[9:3]}` ?

A) 18
B) 20
C) 22
D) 24
E) None of the above

22) For the following Verilog module,

```
module decode(x,a);
input wire [2:0]a;
output wire [7:0]x;
wire [7:0] map [7:0];
assign map[0] = 8'hf1;
assign map[1] = 8'he2;
assign map[2] = 8'hd3;
assign map[3] = 8'hc4;
assign map[4] = 8'hb5;
assign map[5] = 8'ha6;
assign map[6] = 8'h97;
assign map[7] = 8'h88;
assign x = map[a];
endmodule
```

What is the value of x[3:0] when a == 3'b110 ?

A) 4'b0111
B) 4'b1000
C) 4'b0001
D) 4'b0010
E) None of the above

23) What will be the resulting value of `f` in the module below, assuming `a` = 4'b1000, `b` = 4'b1100, and `c` = 4'b0110 ?

```
module decode(a,b,c,f);
input [3:0] a,b,c;
output [1:0] f;

assign f = {a[3], b[1]} | {c[2], c[3]};

endmodule
```

A) 2'b00
B) 2'b01
C) 2'b10
D) 2'b11
E) None of the above

24) For the following Verilog module

```
module priority42(in,s);
    input wire [3:0] in;
    output wire [2:0] s;
    assign s = in[3] == 1 ? 3'b100 :
               in[2] == 1 ? 3'b101 :
               in[1] == 1 ? 3'b111 :
               in[0] == 1 ? 3'b110 :
               3'b000;
endmodule
```

What is the value of s when in == 4'b0101 ?

A) 3'b000
B) 3'b100
C) 3'b110
D) 3'b101
E) None of the above

25) For the following Verilog code, what is the value of f when x=1, y=0, z=0 in the `multi` module?

```
module mux8to1(in,s,out);
    input wire [7:0] in;
    input wire [2:0] s;
    output wire out;
    assign out = (s== 3'b111) ? in[7] :
                 (s== 3'b110) ? in[6] :
                 (s== 3'b101) ? in[5] :
                 (s== 3'b100) ? in[4] :
                 (s== 3'b011) ? in[3] :
                 (s== 3'b010) ? in[2] :
                 (s== 3'b001) ? in[1] :
                                in[0];
endmodule

module multi(x,y,z,f);
  input x,y,z;
  output [2:0]f;
  mux8to1 u2(8'b10010101,{x,y,z},f[2]);
  mux8to1 u1(8'b01010011,{x,y,z},f[1]);
  mux8to1 u0(8'b01100101,{x,y,z},f[0]);
endmodule
```

A) 3'b100
B) 3'b110
C) 3'b001
D) 3'b000
E) None of the above

Observe the ssdec module below and answer questions 26-27 regarding this module:

```
module ssdec (in, enable, out);
  input [3:0] in;
  input enable;
  output [7:0] out;

  wire [7:0] SEG7 [15:0];
  assign SEG7[15] = 8'b01110001;
  assign SEG7[14] = 8'b01111001;
  assign SEG7[13] = 8'b01011110;
  assign SEG7[12] = 8'b00111001;
  assign SEG7[11] = 8'b01111100;
  assign SEG7[10] = 8'b01110111;
  assign SEG7[9]  = 8'b01101111;
  assign SEG7[8]  = 8'b01111111;
  assign SEG7[7]  = 8'b00000111;
  assign SEG7[6]  = 8'b01111101;
  assign SEG7[5]  = 8'b01101101;
  assign SEG7[4]  = 8'b01100110;
  assign SEG7[3]  = 8'b01001111;
  assign SEG7[2]  = 8'b01011011;
  assign SEG7[1]  = 8'b00000110;
  assign SEG7[0]  = 8'b00111111;

  assign out = enable ? SEG7[in] : 0;
endmodule
```

26) What will be the value of out when in[3] is 1, in[2] is 0, in[1] is 0, in[0] is 1 and enable is 1?

A) 8'b00000000
B) 8'b01101101
C) 8'b01101111
D) 8'b00111111
E) None of the above

27) If out is connected to a seven-segment display ss0 as shown:

```
/* Let ss0[0] be segment A, ss0[1] be
segment B, ss0[2] be segment C, etc. */
assign ss0 = out;
```

which segments would be on for in[3] = 0, in[2] = 1, in[1] = 1 and in[0] = 0?

A) A, C, D, F, G
B) A, B, C, D, F
C) B, C, D, E, F, G
D) A, C, D, G
E) None of the above

28) Which of these, if inserted into a syntactically correct Verilog design, will cause a syntax error? Assume all variable names are already declared as wires/buses.

A) `assign right = pb;`
B) `assign pb = right;`
C) `input [2:0] w;`
D) `inv (.a (pb[0]), .o (pb[1]));`
E) None of the above

29) Which of the following Verilog dataflow expressions is equivalent to the given structural Verilog design? Assume all variables and ports are defined.

```
/* format: nand inst (output, input,
                      input);    */
nand u1 (N1, X, ~Y);
nand u2 (F, N1, Z);
```

A) (X + Z') · (Y' + Z')
B) (X + Y') · (X' + Z)
C) (Y' + Z') · (X + Y')
D) (Y + Z) · (Y' + Z')
E) None of the above

30) Which of the following structural designs is equivalent to the given Verilog dataflow expression? Assume all wires are defined.

```
assign f = (a && b) || (b && ~c);
```

A)
```
nor u1 (a1, ~a, ~b);
nor u2 (a2, ~b, c);
or u3 (a1, a2, f);
```

B)
```
nor u1 (a1, a, ~b);
nor u2 (a2, b, ~c);
or u3 (a1, a2, f);
```

C)
```
nor u1 (a1, a, b);
nor u2 (a2, b, c);
or u3 (a1, ~a2, f);
```

D)
```
nor u1 (a1, a, b);
nor u2 (a2, b, ~c);
or u3 (~a1, a2, f);
```

E) None of the above