Prelab13

Monday, November 29, 2021 12:49 PM

The instruction types are arranged as follows:

opcode	Description
0 - 2	Immediate 8-bit operand
3	Two-Register Arithmetic/Logical
c	Load or store

Immediate Instructions (format rNNX)

opcode	Mnemonic	Description
0	LDBI Rr,#NN	Rr = NN
1	ADDI Rr,#NN	Rr = (Rr) + NN
2	SUBI Rr,#NN	Rr = (Rr) - NN

Two-Register Arithmetic/Logical Instructions (format rfsX)

opcode	function	Mnemonic	Description
3	0	CMP Rr,Rs	(Rr) - (Rs) // just set flags
3	1	NEG Rr,Rs	Rr = -(Rs)
3	2	ADD Rr,Rs	Rr = (Rr) + (Rs)
3	3	ADC Rr,Rs	Rr = (Rr) + (Rs) + C
3	4	SUB Rr,Rs	Rr = (Rr) - (Rs)
3	5	SBC Rr,Rs	Rr = (Rr) - (Rs) + C
3	6	MUL Rr,Rs	Rr = (Rr) * (Rs)
3	7	DIVS Rr,Rs	Rr = (Rr) / (Rs) // signed
3	8	DIVU Rr,Rs	Rr = (Rr) / (Rs) // unsigned
3	9	TST Rr,Rs	(Rr) & (Rs) // just set flags
3	a	NOT Rr,Rs	Rr = ~(Rs)
3	b	OR Rr,Rs	Rr = (Rr) | (Rs)
3	c	AND Rr,Rs	Rr = (Rr) & (Rs)
3	d	BIC Rr,Rs	Rr = (Rr) & ~ (Rs)
3	e	XOR Rr,Rs	Rr = (Rr) ^ (Rs)
3	f	CPY Rr,Rs	Rr = (Rs)

For each 16-bit (4 hexadecimal digit) instruction decode it into a representative mnemonic and description.

Instruction	Mnemonic	Description
3f70	LDBI R3,#0xF7	R3 = 0x000000F7
a2b3	ADD R10,R11	R10 = (R10) + (R11)
d2f0	LDBI Rd,#0x2f	Rd = 0x0000002f
24c3	SUB R2,R12	R2 = (R2) − (R12)
9353	ADC R9,R5	R9 = (R9)+(R5) + C
2c63	AND R2,R6	R2 = (R2) & (R6)
1102	SUBI R1,#0x10	R1 = (R1) − 0x00000010
4b23	OR R4,R2	R4 = (R4) | (R2)
5d33	BIC R5,R3	R5 = (R5) &~(R3)
0fb3	CPY R0,R11	R0 = (R11)
32d3	ADD R3,R13	R3 = (R3) + (R13)
65c1	SBC R6,R12	R6 = (R6) − (R12) + C
7ac3	NOT R7,R12	R7 = ~(R12)
6533	SBC R6,R3	R6 = (R6) − (R3) + C
4e23	XOR R4,R2	R4 = (R4) ^ (R2)
2da3	BIC R2,R10	R2 = (R2) & ~(R10)
5073	CMP R5,R7	(R5) − (R7)