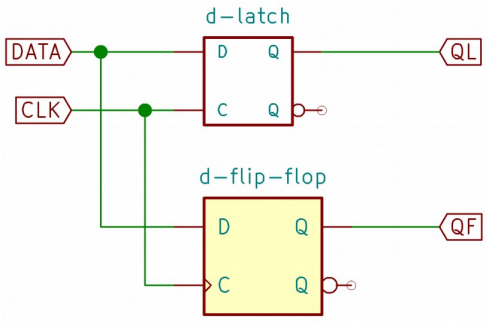
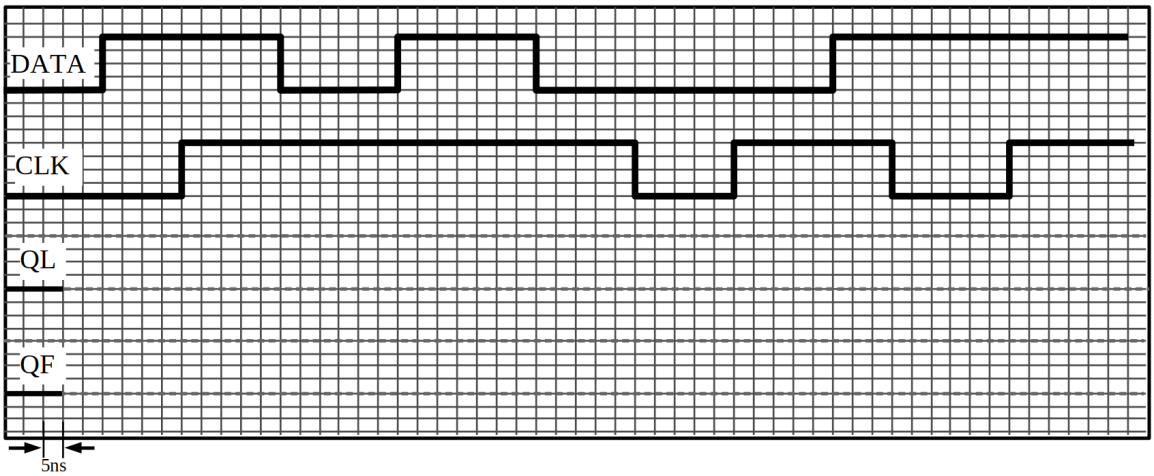
Use the following circuit consisting of a latch and a D flip-flop for the next two questions. Assume that, for each device in question, $t_{pHL(C\rightarrow Q)}$ = 15 ns, $t_{pLH(C\rightarrow Q)}$ = 20 ns, $t_{pHL(D\rightarrow Q)}$ = 5 ns, and $t_{pLH(D\text{->}Q)}$ = 10 ns. (Not all parameters are relevant to all devices.) Assume that all setup and hold requirements are met. The initial states of QL and QF are 0.



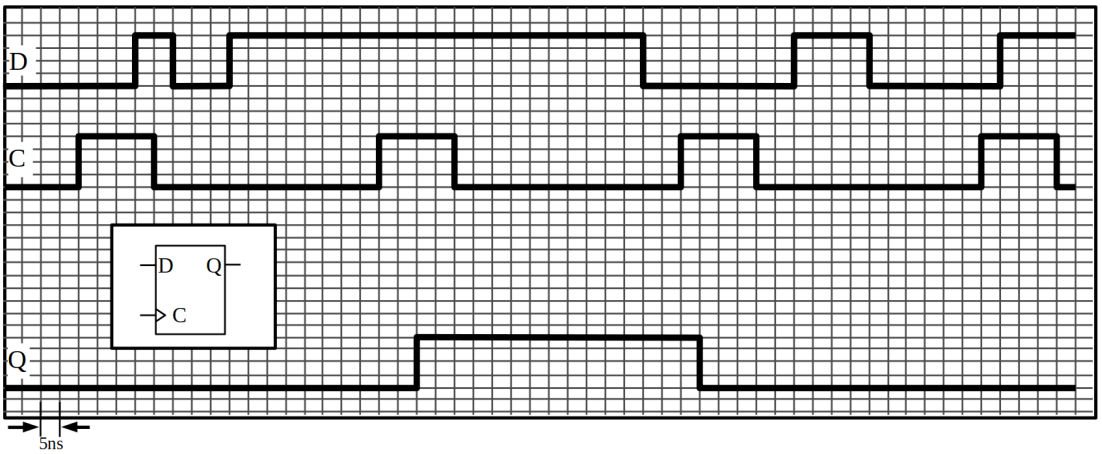
1) On the timing diagram below, draw the expected signal for QL.
2) On the same diagram below, draw the expected signal for QF.



3) What happens when a D flip-flop becomes metastable?

4) Describe three circumstances that could cause metastability with a D flip-flop.

Use the diagram below for the following questions about the use of a D flip-flop.



5) What edge of the clock is the flip-flop “triggered” on?

6) What is $t_{pHL(C \rightarrow Q)}$? (in nanoseconds)

7) What is $t_{pLH(C \rightarrow Q)}$? (in nanoseconds)

8) What is the nominal setup time? (in nanoseconds)

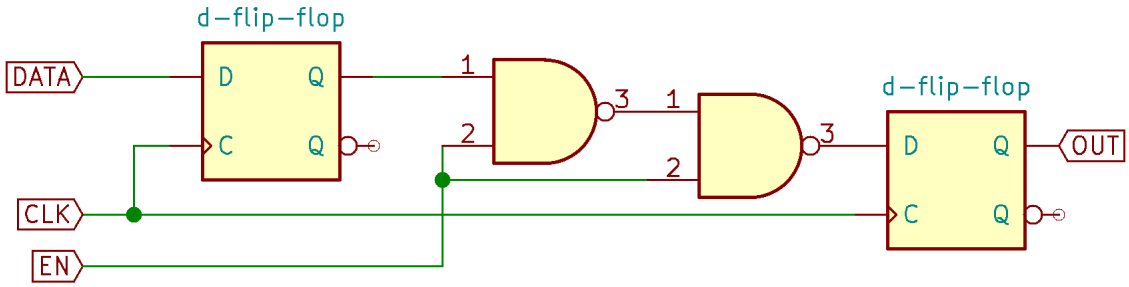
9) What is the nominal hold time? (in nanoseconds)

10) What is the clock period? (in nanoseconds)

11) What is the clock’s pulse width? (in nanoseconds)

12) What is the clock’s duty cycle?

13) For the figure below,



assume that $t_{pHL(C \rightarrow Q)}$ and $t_{pLH(C \rightarrow Q)}$ for the flip-flops are both 10 ns. The setup time (t_S) for the flip-flops is 10 ns. The hold time (t_H) for the flip-flops is 0 ns. The propagation delays (t_{pHL} and t_{pLH}) for each NAND gates is 5 ns. If the clock is a periodic square wave, what is the minimum period that will avoid the second flip-flop exhibiting metastability?

14) For the following Verilog statements,

```
always @ (posedge clock, posedge reset) begin
      if (reset == 1) begin
            x <= 0;
            y <= 0;
      end
      else if (a == 1'b1) begin
            x <= y;
            y <= z;
      end
      else begin
            x <= 1;
      end
end
```

cross out all **begin** and **end** statements that are not necessary.

15) For the following Verilog statements,

```
reg x,y;
wire z;
...
always @ (posedge clock) begin
      x = y;
      y = z;
end
```

how many state elements are needed to realize this specification in hardware, and are they flip-flops or latches?

16) For the following Verilog statements,

```
reg x;
wire a,b,c;
...
always @ (a,b,c) begin
      if (a == 1) begin
            x = b;
      end
      else begin
            x = c;
      end
end
```

how many state elements are needed to realize this specification in hardware, and are they flip-flops or latches?

17) For the following Verilog statements,

```
reg x;
wire a,b,c;
…
always @ (*) begin
      if (a == 1)
            x = b;
end
```

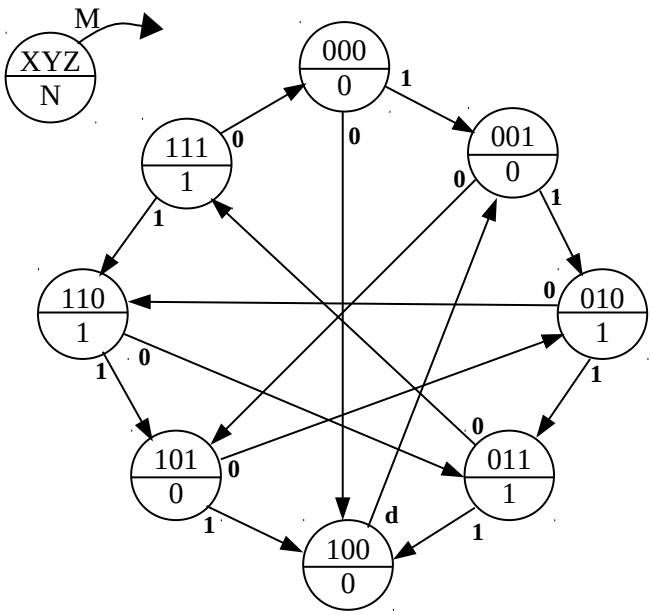
how many state elements are needed to realize this specification in hardware, and are they flip-flops or latches?

18) For the following Verilog statements,

```
reg x;
wire a,b;
…
always @ (*) begin
      if (b == 0)
            x = 1'b0;
      else
            x = a;
end
```

what kind of circuit will be produced to realize this specification in hardware? (i.e., what is the relationship between **x**, **a**, and **b**?

19) Given the following state-transition diagram, complete the present state / present output/ next state table, and use it for the rest of the questions on this page.



X	Y	Z	M	N	X*	Y*	Z*
0	0	0	0				
0	0	0	1				
0	0	1	0				
0	0	1	1				
0	1	0	0				
0	1	0	1				
0	1	1	0				
0	1	1	1				
1	0	0	0				
1	0	0	1				
1	0	1	0				
1	0	1	1				
1	1	0	0				
1	1	0	1				
1	1	1	0				
1	1	1	1				

20) The start state is 000. If M is always 0, what repeating output pattern is produced on N?

21) The start state is 000. If M is always 1, what repeating output pattern is produced on N?

22) For the following Moore machine, whose start state is 000. Choose next state values such that the Z bit follows the pattern: **0 0 0 1 1 0 0 0 0 1 1 0 …**
Note that there are many arrangements of next state values that will produce the correct pattern for the Z bit, and many others that will not. You do not need to make an optimal choice. Any next state combination that produces the correct pattern for Z is as good as any of the others.

X	Y	Z	X*	Y*	Z*
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

23) For the following Verilog code, meant to run on the FPGA development system, complete the counter equations to implement a 4-bit synchronous up-counter.

```
reg [3:0] Q;
assign left[0] = Q[3];
always @ (posedge hz100, posedge reset) begin
      if (reset == 1)         begin  Q <= 4'b0000;  end
      else if (Q == 4'b1001)  begin  Q <= 4'b0000;  end
      else                    begin  Q <= next_Q;   end
else

always @ (Q) begin
      next_Q[0] =


      next_Q[1] =


      next_Q[2] =


      next_Q[3] =
end
```

24) For the previous question, at what frequency does the LED on left[0] flash? (You should assume that the hz100 wire is a 100 Hz square wave.)

25) Complete the Verilog always block body to implement a circular shift register that outputs one element of the repeating sequence 0 0 0 0 1 1 1 on the left[0] output each time it sees the rising edge of pb[0] and resets the sequence to the beginning on the rising edge of pb[1].

```
module top(hz100, left, pb);
        input hz100;
        output [7:0] left;
        input [20:0] pb;

        reg [6:0] shift;

        assign left[0] = shift[6];

        // Write your always block in the space below...




endmodule
```