

# Lab6

Saturday, February 26, 2022 1:38 PM

## Prelab6

### Pre-lab Assignment 6

Due: Fri, 04 Mar 2022 11:30:00 (approximately 5 days from the time this page was loaded)  
[30 points possible] [100 penalties possible] [0 penalties graded so far]

For this lab experiment, you will use C to configure the digital-to-analog converter (DAC), the analog-to-digital converter (ADC), set up timers, and invoke interrupt service routines (ISRs). DMA will be used to copy a memory array to the 7-segment outputs on GPIOB. DMA will also be used to copy ADC values to memory.

#### Academic Integrity Statement [0 ... -100 points]

By typing my name, below, I hereby certify that the work on this prelab is my own and that I have not copied the work of any other student (past or present) while completing it. I understand that if I fail to honor this agreement, I will receive a score of zero for the lab, a one letter drop in my final course grade, and be subject to possible disciplinary action.

Save

#### (1) DAC configuration interface [6 points]

For the DAC subsystem, name the registers that are used to perform the operations described.

a) What register is used to enable the RCC clock to the DAC?

RCC\_APB1ENR

b) In the register you just named, which bit is used to enable the RCC clock?

29

c) Into which register should you write a 12-bit left-aligned value to be converted only by the channel 1 DAC?

DAC\_DHR12L1

d) Which register is used to configure the *type* of *trigger* used to start the digital-to-analog conversion?

DAC\_SWTRIGR

e) If channel 2 of the DAC is configured for software trigger, which register must be written to to cause channel 2 to start a conversion?

DAC\_SR

f) In the register you just named, which bit is used to trigger channel 2?

29

Save

#### (2) ADC configuration interface [4 points]

For the ADC subsystem, name the registers that are used to perform the operations described.

a) What register is used to enable the RCC clock to the ADC?

RCC\_APB2ENR

b) In the register you just named, which bit is used to enable the RCC clock?

1

c) Which register is read to check for the end-of-conversion status?

ADC\_ISR

d) In the register you just named, which bit indicates the end-of-conversion status?

2

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#### (3) [1 point]

When the STM32's analog-to-digital converter is operating in **12-bit** mode, how many distinct quantization levels can it resolve?

12

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#### (4) [1 point]

How many cycles of the high-speed internal clock does the STM32's analog-to-digital converter take to make a sample-and-hold and conversion to a 10-bit result?

12

Save

#### (5) [1 point]

How long (in nanoseconds) does the STM32's analog-to-digital converter take to sample, hold, and convert to a 12-bit result when using the high-speed internal clock?

100 ns

1000000 conversions / second

$\frac{1}{1000000} < 0.000001$

Save

#### (6) [1 point]

What external pin can ADC\_IN8 be connected to?

PA8

Save

#### (7) [1 point]

Suppose the ADC is supplied with reference voltages  $V_{SSA}=0V$  and  $V_{DDA}=3.100 V$ . When operating in 12-bit mode, what is the smallest change in the input voltage that the STM32's ADC can resolve? (In other words, what change in the input voltage will produce a 1-bit change to the least significant bit of the converted value?)

0.00075683594 V

$\frac{3.1}{2^{12}} = 0.00075683594$

Save

#### (8) ADC Values [5 points]

Given an STM32 ADC operating in 12-bit right-aligned mode with reference voltages  $V_{SSA}=0V$  and  $V_{DDA}=3.0000 V$ , determine the converted hexadecimal values for the following input voltages. Your instructor feels very strongly that you should use the formula  $\lfloor 4096 \times V_{sample}/V_{DDA} \rfloor$ , and he's prepared to explain why if you have the patience to listen to it. For the sake of this exercise, if you're off by one binary bit too high or too low, it is acceptable. In any case, that difference is still smaller than the noise present in the ADC.

0.06306152 V 0x056 86.01

0.72955322 V 0x3E4 996.083

0.97650146 V 0x535 1333.75

2.18121893 V 0x1A2 2978.09

3.09235174 V 0x07C 4222.09

Save

#### (9) DAC Values [5 points]

Given an STM32 DAC operating in 12-bit **left-aligned** mode with reference voltages  $V_{SSA}=0V$  and  $V_{DDA}=3.1000 V$ , determine the output voltages produced for the following hexadecimal values written to the DAC\_DHR12L1. Remember that a 12-bit left-aligned value can be interpreted as a 16-bit value where the most significant bit represents  $1/2 \times V_{DDA}$ , the next most significant bit represents  $1/4 \times V_{DDA}$ , and so on. If you want to use a direct conversion multiplier, your instructor feels very strongly that you should use the formula  $\lfloor 12\text{bitvalue}/4096 \times V_{DDA} \rfloor$ , and he's prepared to explain why if you have the patience to listen to it. Express your answer in Volts with as much precision as you can.

0x0950 0.011735 V  $149/4096 \times 3.1 = 0.011735$

0x3630 0.068281 V  $867/4096 \times 3.1 = 0.068281$

0x42B0 0.084032 V  $1067/4096 \times 3.1 = 0.084032$

0x7E70 0.159321 V  $2023/4096 \times 3.1 = 0.159321$

0xC480 0.247606 V  $3144/4096 \times 3.1 = 0.247606$

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#### (10) DMA Configuration [5 points]

The following questions pertain to DMA channel configuration for DMA controller 1 of the STM32F091 microcontroller. See table 32 in the Family Reference Manual for information on request mapping.

a) Assuming all of the CxS fields of the DMA\_CSELRL are their default value of 0000, which DMA channel is triggered by an update event on TIM3?

3

b) If you wanted a DMA channel to always copy each datum from the CMAR address to the CPAR address, should the DIR bit be set or clear (zero) in the CCR register for the channel?

Set

c) If you wanted to set a DMA channel peripheral address target to the ODR of GPIOC, what value would you put in the CPAR? (Express your answer as an 8-digit hexadecimal value.)

ODR effect: 0x14

0x48001414

Save

d) Which DMA channel is triggered by the ADC?

channel 1

e) To what 32-bit value should a DMA channel's CCR register be set to configure the following features:

- Disable memory-to-memory mode.

- Medium priority.

- Memory datum size: 16-bit

- Peripheral datum size: 32-bit

- Memory address increment mode on.

- Peripheral address increment mode off.

- Circular mode on.

- Transfer direction from memory to peripheral.

- Transfer error interrupt disabled.

- Half-transfer interrupt disabled.

- Transfer complete interrupt enabled.

- Enable the DMA channel.

Express the answer as an 8-digit hexadecimal number.

0x000016B3

Save