bus

File: bus.kicad_sch

power

File: power.kicad_sch

buffers

File: buffers.kicad_sch

fpanel

File: fpanel.kicad_sch

65816CPU

File: 65816CPU.kicad_sch

GALS

File: GALS.kicad_sch

bus sharing

File: bussharing.kicad_sch

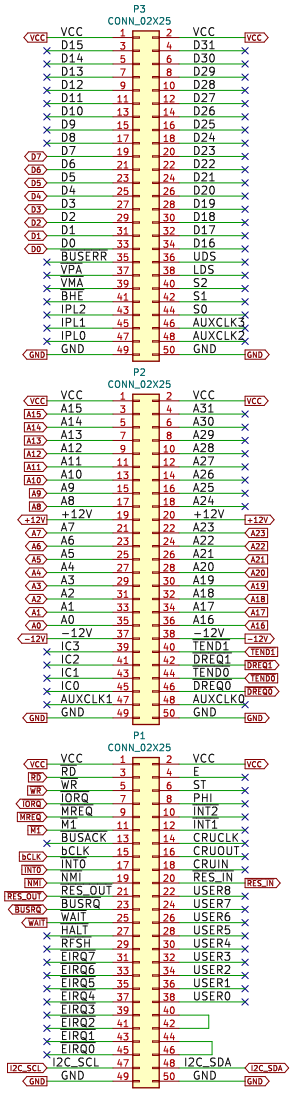
mapper

File: mapper.kicad_sch

Sheet: /
File: processor.65816.kicad_sch

Title: Duodyne 65816 CPU board

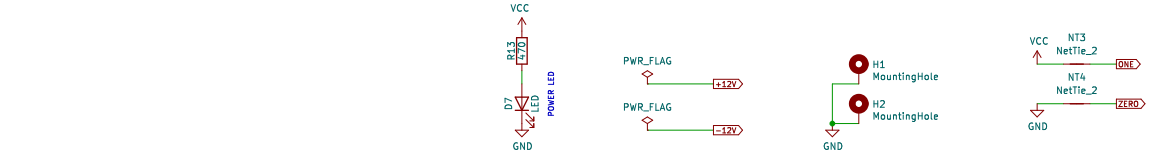
Size: B	Date: 2023-12-17	**Rev: V1.00**
KiCad E.D.A. kicad (6.0.11)		Id: 1/9



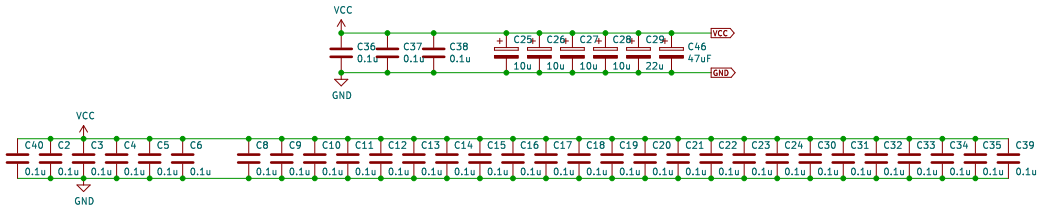
Sheet: /bus/
File: bus.kicad_sch

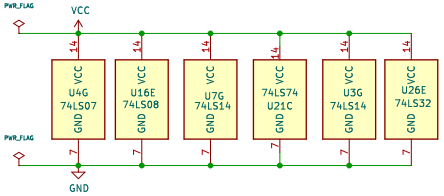
Title: Duodyne 65816 CPU board

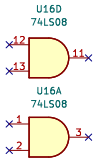
Size: B	Date: 2023-12-17	**Rev: V1.00**
KiCad E.D.A. kicad (6.0.11)		Id: 2/9

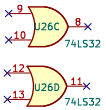


SPARE GATES

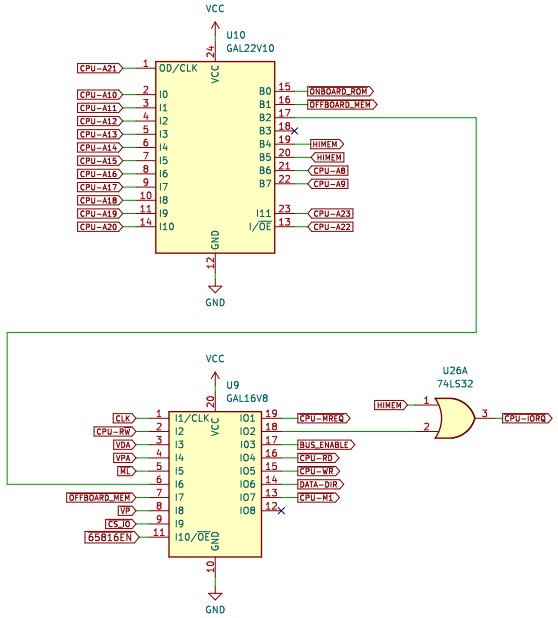




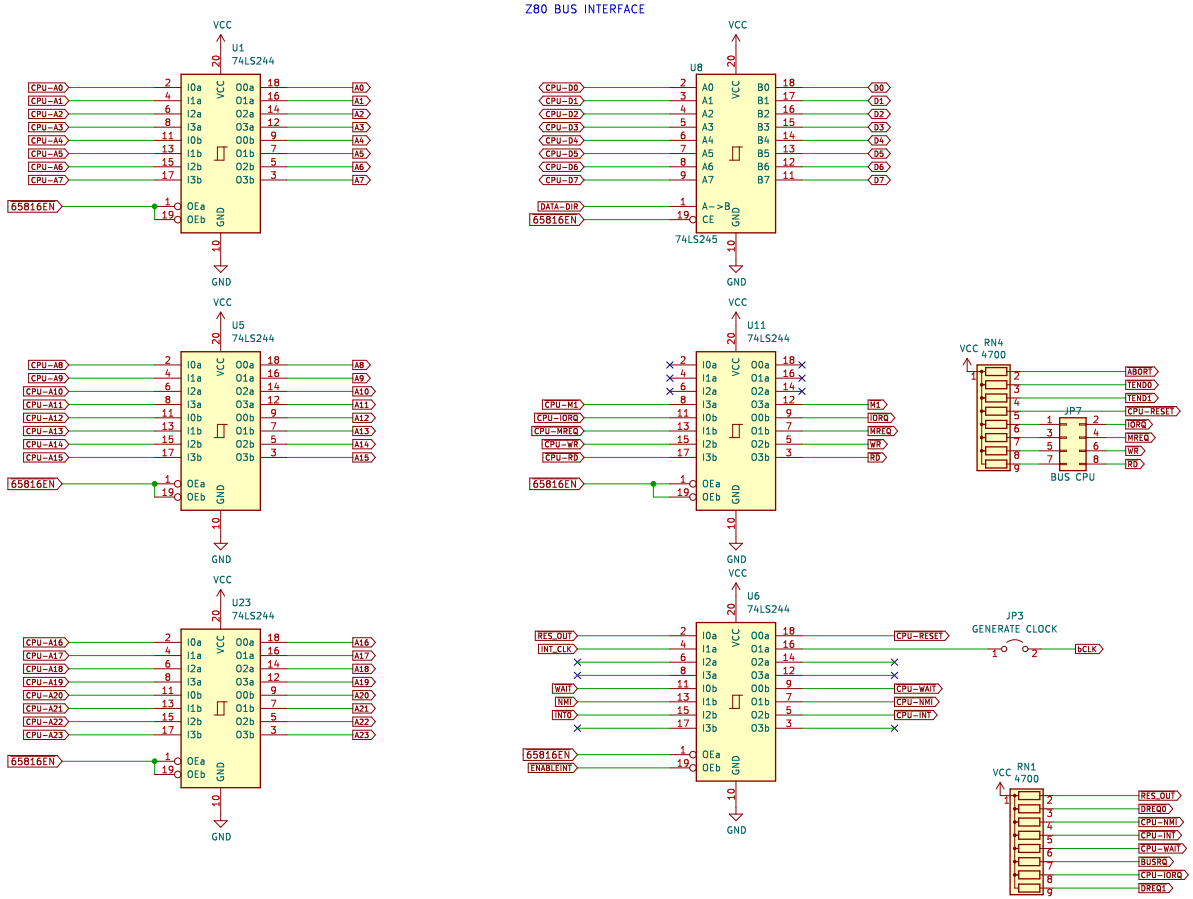




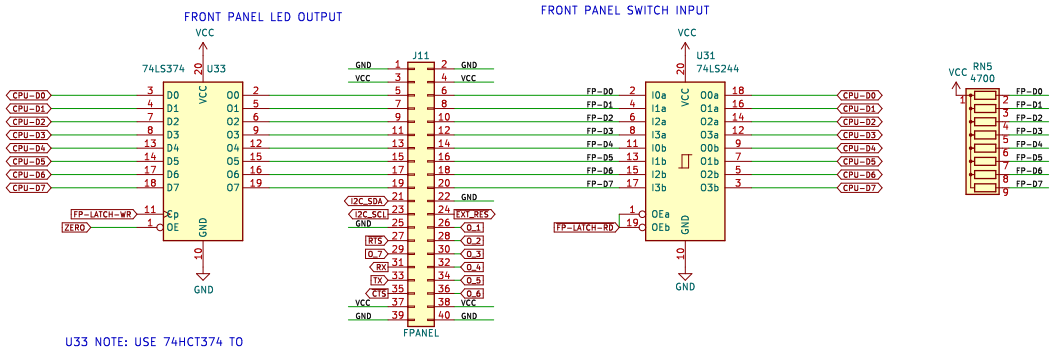
Sheet: /power/	
File: power.kicad_sch	
Title: Duodyne 65816 CPU board	
Size: B	Date: 2023-12-17
KiCad E.D.A. kicad (6.0.11)	Id: 4/9



Sheet: /GALS/	
File: GALS.kicad_sch	
Title: Duodyne 65816 CPU board	
Size: B	Date: 2023-12-17
KiCad E.D.A. kicad (6.0.11)	**Rev: V1.00**
	Id: 5/9



Sheet: /buffers/	
File: buffers.kicad_sch	
Title: Duodyne 65816 CPU board	
Size: B	Date: 2023-12-17
KiCad E.D.A. kicad (6.0.11)	Rev: V1.00
	Id: 6/9



U33 NOTE: USE 74HCT374 TO SOURCE OR SINK ADEQUATE CURRENT TO DRIVE LEDS ON FRONT PANEL

J11 NOTE:

PINS 5, 7, 9, 11, 13, 15, 17, 19 ARE FOR LED STATUS FOR ROMWBW FRONT PANEL INDICATOR

PINS 6, 8, 10, 12, 14, 16, 18, 20 ARE FOR SWITCH INPUTS FOR ROMWBW FRONT PANEL

PINS 21, 23 ARE FOR I2C CONNECTION (SDA & SCL)

PINS 25, 27, 29, 31, 33, AND 35 ARE FOR TTL SERIAL CONNECTOR TO UART

PINS 29, 37 ARE FOR SERIAL VCC POWER ENABLE

PINS 22, 24 ARE FOR EXTERNAL RESET SWITCH

PINS 26, 28 ARE FOR IM2 CIRCUIT ENABLE

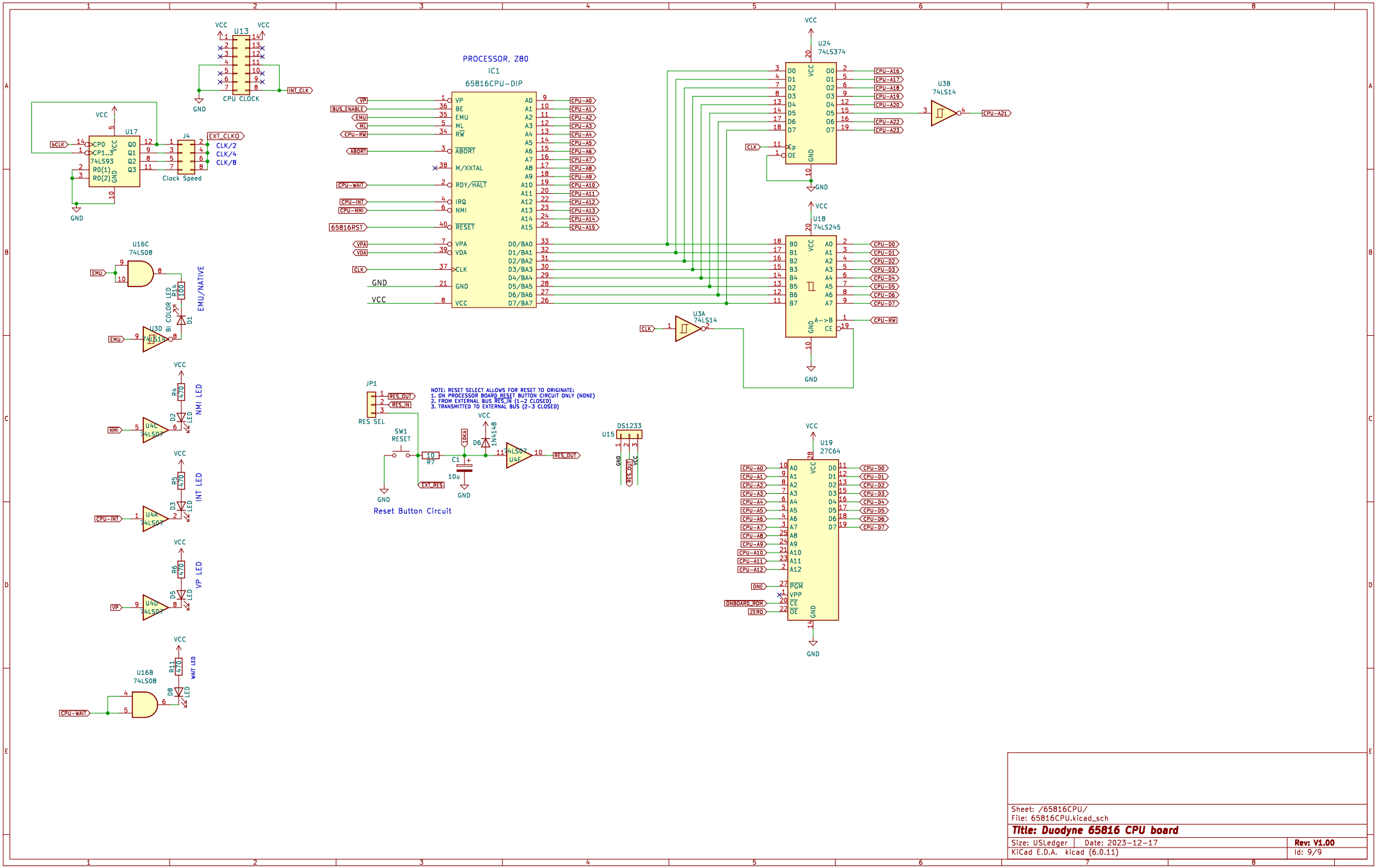
PINS 30, 32 ARE FOR INTERRUPT 0 ENABLE

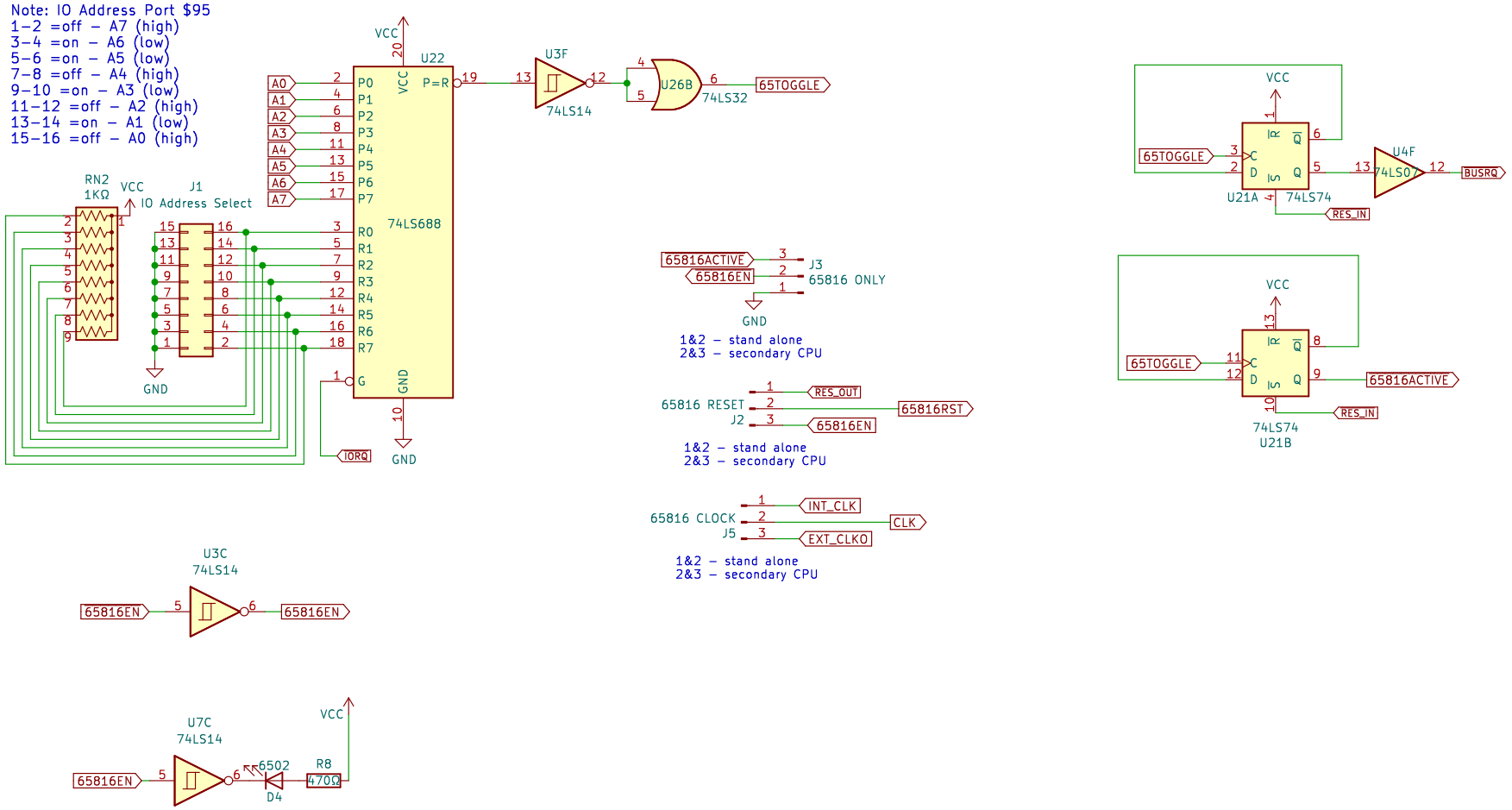
PINS 34, 36 ARE FOR WAIT STATE CIRCUIT ENABLE

Sheet: /fpanel/
File: fpanel.kicad_sch

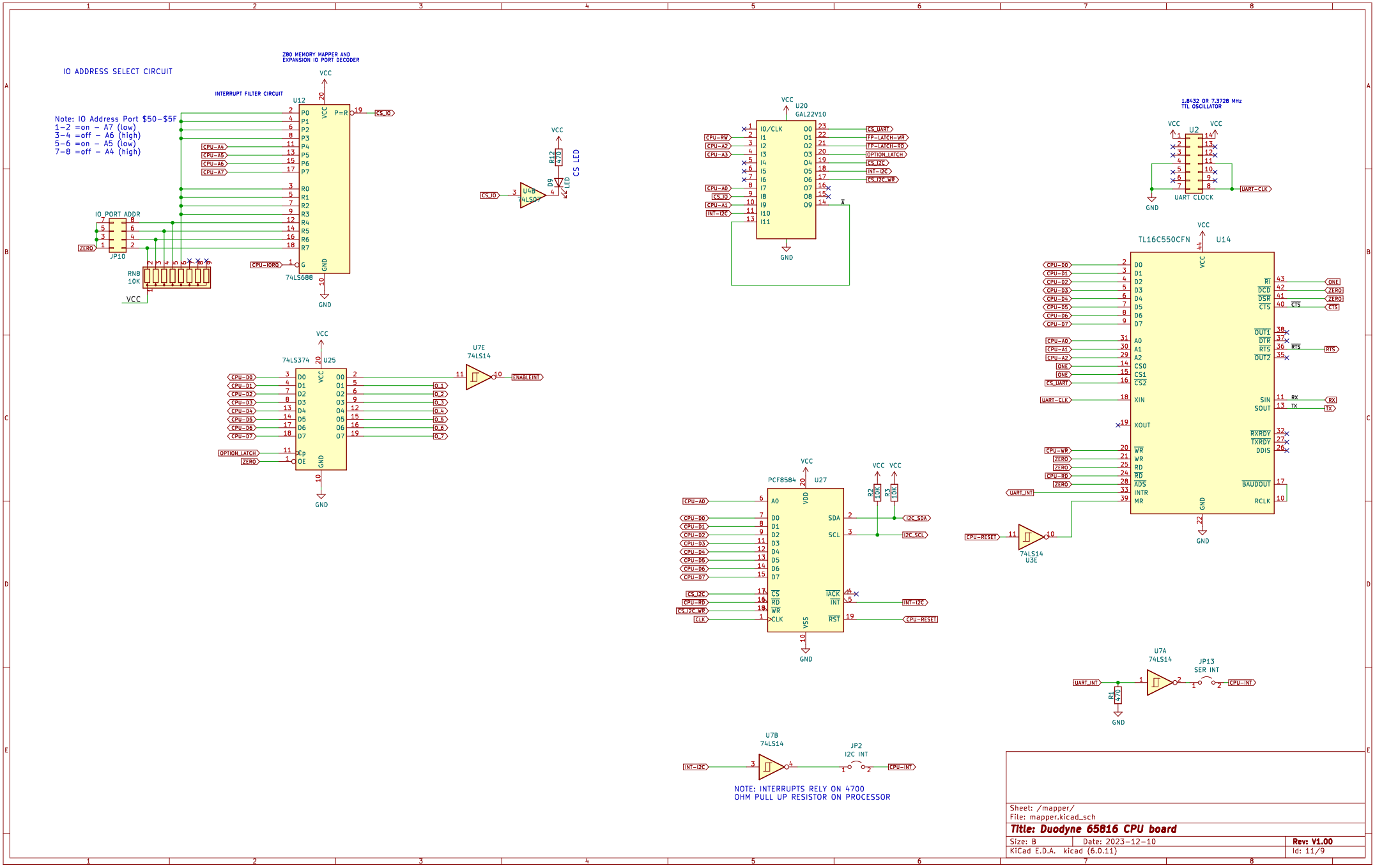
Title: Duodyne 65816 CPU board

Size: B	Date: 2023-12-17	**Rev: V1.00**
KiCad E.D.A. kicad (6.0.11)		Id: 8/9


PROCESSOR, Z80
IC1
65816CPU-DIP
U13
CPU CLOCK
U17
74LS93
J4
Clock Speed
EXT_CLKO
CLK/2
CLK/4
CLK/8
U16C
74LS08
EMU/NATIVE
U3D
74LS14
NMI LED
U4C
74LS07
INT LED
U4A
74LS07
VP LED
U4D
74LS07
U16B
74LS08
WAIT LED
U24
74LS374
U3B
74LS14
U18
74LS245
U3A
74LS14
U19
27C64
JP1
RES SEL
SW1
RESET
Reset Button Circuit
NOTE: RESET SELECT ALLOWS FOR RESET TO ORIGINATE:
1. ON PROCESSOR BOARD RESET BUTTON CIRCUIT ONLY (NONE)
2. FROM EXTERNAL BUS RES_IN (1-2 CLOSED)
3. TRANSMITTED TO EXTERNAL BUS (2-3 CLOSED)
DS1233
U15
Sheet: /65816CPU/
File: 65816CPU.kicad_sch
Title: Duodyne 65816 CPU board
Size: USLedger
Date: 2023-12-17
Rev: V1.00
KiCad E.D.A. kicad (6.0.11)
Id: 9/9



Sheet: /bus sharing/		
File: bussharing.kicad_sch		
Title: Duodyne 65816 CPU board		
Size: A4	Date: 2023-12-17	**Rev: V1.00**
KiCad E.D.A. kicad (6.0.11)		Id: 9/9


IO ADDRESS SELECT CIRCUIT
Z80 MEMORY MAPPER AND EXPANSION IO PORT DECODER
INTERRUPT FILTER CIRCUIT
Note: IO Address Port $50-$5F
1-2 =on - A7 (low)
3-4 =off - A6 (high)
5-6 =on - A5 (low)
7-8 =off - A4 (high)
U12
74LS688
IO_PORT_ADDR
JP10
RN8
10K
VCC
GND
CS_IO
CPU-A4
CPU-A5
CPU-A6
CPU-A7
CPU-IORQ
U4B
74LS07
R12
470
D9
LED
CS LED
U20
GAL22V10
CPU-RW
CPU-A2
CPU-A3
CPU-A0
CPU-A1
INT-I2C
CS_UART
FP-LATCH-WR
FP-LATCH-RD
OPTION_LATCH
CS_I2C
CS_I2C_WR
1.8432 OR 7.3728 MHz
TTL OSCILLATOR
U2
UART CLOCK
UART-CLK
TL16C550CFN
U14
CPU-D0
CPU-D1
CPU-D2
CPU-D3
CPU-D4
CPU-D5
CPU-D6
CPU-D7
ONE
ZERO
CTS
RTS
RX
TX
XIN
XOUT
CPU-WR
CPU-RD
UART_INT
CPU-RESET
74LS14
U3E
74LS374
U25
U7E
74LS14
ENABLEINT
OPTION_LATCH
PCF8584
U27
R2
10K
R3
10K
I2C_SDA
I2C_SCL
CPU-RD
CS_I2C_WR
CLK
INT-I2C
CPU-RESET
U7A
74LS14
JP13
SER INT
R1
470
U7B
74LS14
JP2
I2C INT
NOTE: INTERRUPTS RELY ON 4700
OHM PULL UP RESISTOR ON PROCESSOR
Sheet: /mapper/
File: mapper.kicad_sch
Title: Duodyne 65816 CPU board
Size: B
Date: 2023-12-10
Rev: V1.00
KiCad E.D.A. kicad (6.0.11)
Id: 11/9