Column1					Column42	Colu <mark>Column6</mark>					Column92	Colu						Column15
P1/J1	ODD		P1/J1	EVEN		P2/J2	ODD		P2/J2	EVEN			P3/J3	ODD		P3/J3	EVEN	
PIN	SIGNAL	DIRECTION	PIN	SIGNAL	DIRECTION	PIN	SIGNAL	DIRECTION	PIN	SIGNAL	DIRECTION		PIN	SIGNAL	DIRECTION	PIN	SIGNAL	DIRECTION
1	VCC		2	VCC			1 VCC		2	VCC			1	VCC			2 VCC	
	~RD	0		Е	0		3 A15	0		A31	0			D15	1/0		4 D31	I/O
	~WR	0		ST	0		A14	0		A30	0			D14	1/0		6 D30	I/O
	~IORQ	0		PHI	0		7 A13	0		A29	0			D13	1/0		8 D29	I/O
	~MREQ	0		~INT2	l*		9 A12	0		A28	0			D12	I/O		0 D28	I/O
	~M1	0		~INT1	l*		1 A11	0		A27	0			D11	I/O		2 D27	I/O
	~BUSACK	0		CRUCLK	0		3 A10	0		A26	0			D10	1/0		4 D26	1/0
	CLK	0		CROUT	0		A9	0		A25	0			D9	1/0		6 D25	1/0
	~INTO	l*		CRUIN	1		7 A8	0		A24	0			D8	I/O		8 D24	1/0
	~NMI	l*		~RES_IN	l*		9 +12V			+12V				D7	I/O		0 D23	I/O
	~RES_OUT	I/O*		USER8	I/O		1 A7	0		A23	0			D6	1/0		2 D22	1/0
	~BUSRQ	l*		USER7	I/O		3 A6	0		A22	0			D5	1/0		4 D21	1/0
	~WAIT	l*		USER6	I/O		5 A5	0		A21	0			D4	1/0		6 D20	1/0
	~HALT	0		USER5	I/O		7 A4	0	_	A20	0			D3	1/0		8 D19	1/0
	~RFSH	0		USER4	I/O		9 A3	0		A19	0			D2	1/0		0 D18	1/0
	~EIRQ7	I		USER3	I/O		1 A2	0		A18	0			D1	I/O		2 D17	1/0
	~EIRQ6	1		USER2	I/O		3 A1	0		A17	0			D0	1/0		4 D16	I/O
	~EIRQ5	1		USER1	I/O		A0	0		A16	0			~BUSERR	<u> </u>		6 UDS	0
	~EIRQ4	1		USER0	I/O		7 -12V			-12V				~VPA	<u> </u>		8 LDS	0
	~EIRQ3	I		~BAI	ı		IC3	1		~TEND1	0			~VMA	0		0 S2	0
	~EIRQ2	1		~BAO	0		1 IC2	1		~DREQ1	l*			~BHE	0		2 S1	0
	~EIRQ1	I		~IEI	I		IC1	1		~TEND0	0			IPL2	I/O		4 S0	0
	~EIRQ0	I		~IEO	0		5 ICO	I	_	~DREQ0	I*			IPL1	I/O		6 AUXCLK3	1/0
	I2C_RX	I		I2C_TX	0		7 AUXCLK1	I/O		AUXCLK0	I/O			IPL0	I/O		8 AUXCLK2	I/O
49	GND		50	GND		4:	9 GND		50	GND			49	GND		5	0 GND	
	LEGEND																	

TMS9900

Z80 Z180 MC68000 i8088/8086

DIRECTION IS FROM PROCESSORS PERSPECTIVE RELATIVE TO BUS

\* EXPECTED OPEN COLLECTOR OUTPUTS, MULTI-ACCESS