bus

File: bus.kicad_sch

power

File: power.kicad_sch

buffers

File: buffers.kicad_sch

fpanel

File: fpanel.kicad_sch

6809CPU

File: 6809CPU.kicad_sch

GALS

File: GALS.kicad_sch

bus sharing

File: bussharing.kicad_sch

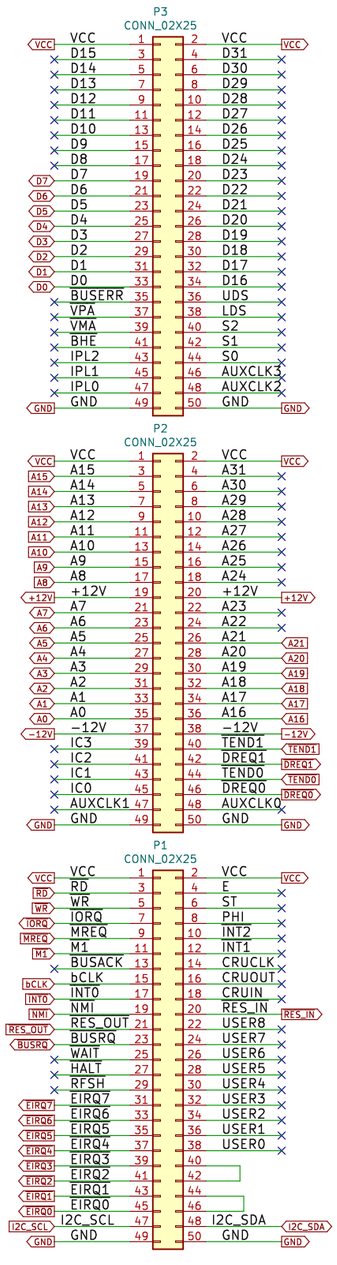
mapper

File: mapper.kicad_sch

Sheet: /
File: processor.6809.kicad_sch

Title: Duodyne 6809 CPU board

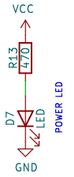
Size: B	Date: 2023-12-29	**Rev: V1.00**
KiCad E.D.A. eeschema (6.0.11)		Id: 1/9

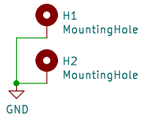


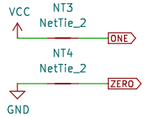
Sheet: /bus/
File: bus.kicad_sch

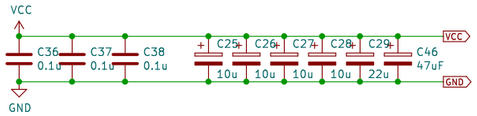
Title: Duodyne 6809 CPU board

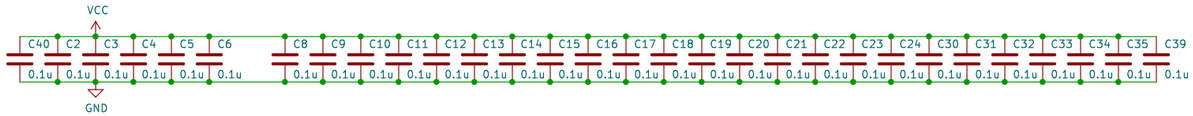
Size: B	Date: 2023-12-29	**Rev: V1.00**
KiCad E.D.A. eeschema (6.0.11)		Id: 2/9

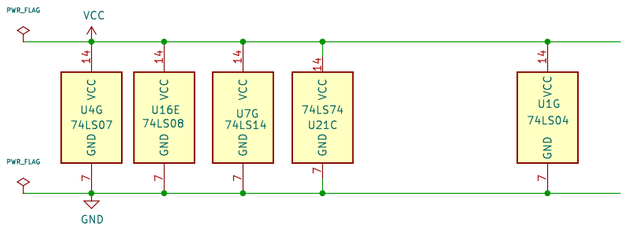




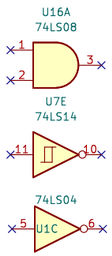








SPARE GATES



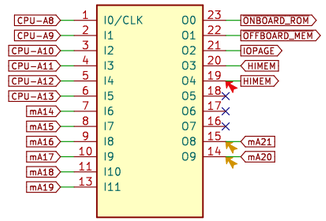
Sheet: /power/		
File: power.kicad_sch		
Title: Duodyne 6809 CPU board		
Size: B	Date: 2023-12-29	**Rev: V1.00**
KiCad E.D.A. eeschema (6.0.11)		Id: 4/9

IO Address Port $50-$5F

$50 Front Panel (RW)
$51
$52 PAGER (WR)
$53
$54
$55
$56-$57 I2C(RW)
$58-$5F UART (RW)

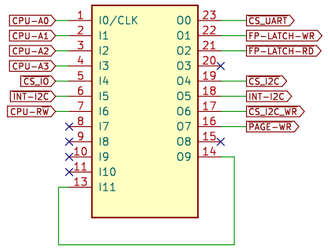
ADDRESS DECODER

U9
GAL22V10

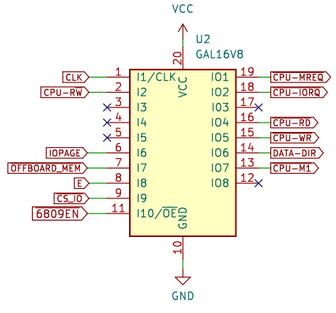


IO DECODER

U3
GAL22V10

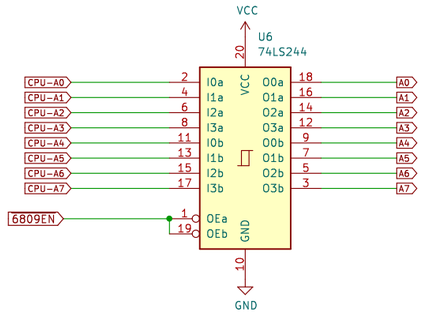


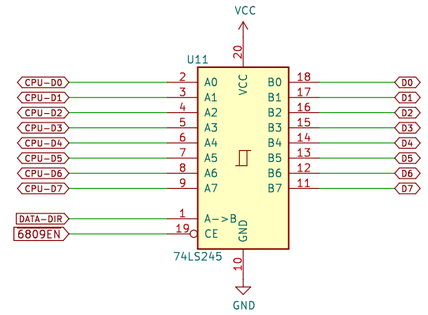
BUS SIGNALS

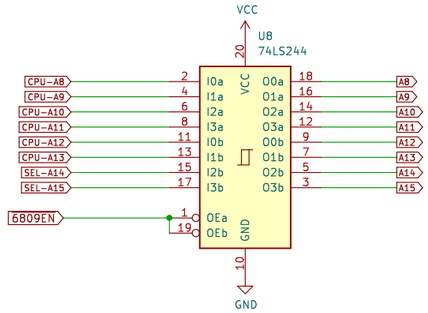


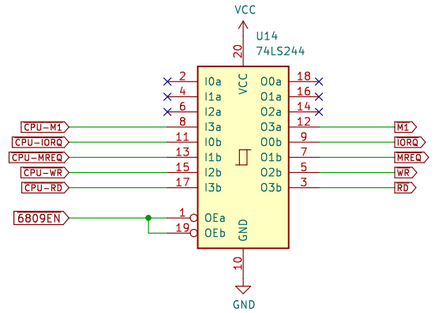
Sheet: /GALS/		
File: GALS.kicad_sch		
Title: Duodyne 6809 CPU board		
Size: B	Date: 2023-12-29	**Rev: V1.00**
KiCad E.D.A. eeschema (6.0.11)		Id: 5/9

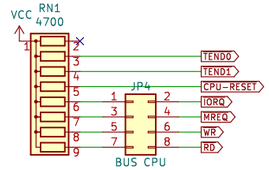
Z80 BUS INTERFACE

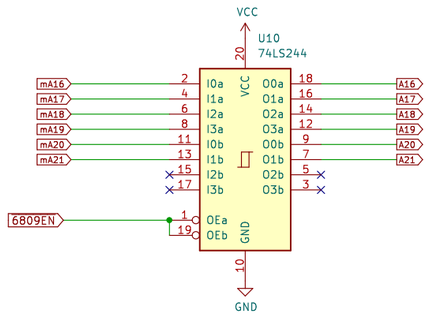


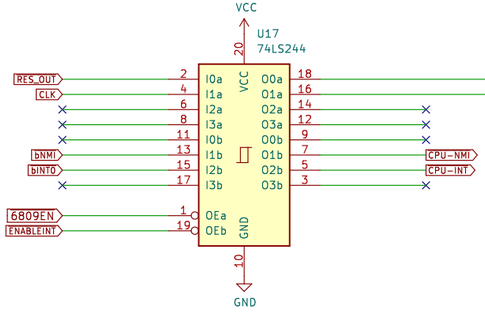


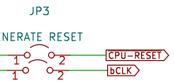


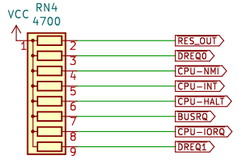


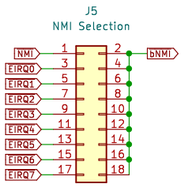


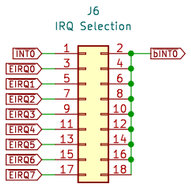




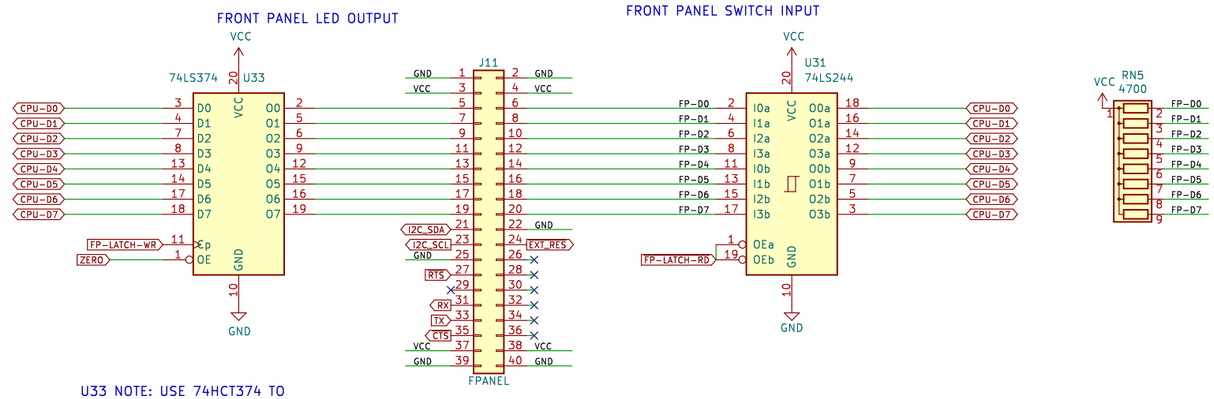








Sheet: /buffers/		
File: buffers.kicad_sch		
Title: Duodyne 6809 CPU board		
Size: B	Date: 2023-12-29	**Rev: V1.00**
KiCad E.D.A. eeschema (6.0.11)		Id: 6/9



U33 NOTE: USE 74HCT374 TO SOURCE OR SINK ADEQUATE CURRENT TO DRIVE LEDS ON FRONT PANEL

J11 NOTE:

PINS 5, 7, 9, 11, 13, 15, 17, 19 ARE FOR LED STATUS FOR ROMWBW FRONT PANEL INDICATOR

PINS 6, 8, 10, 12, 14, 16, 18, 20 ARE FOR SWITCH INPUTS FOR ROMWBW FRONT PANEL

PINS 21, 23 ARE FOR I2C CONNECTION (SDA & SCL)

PINS 25, 27, 29, 31, 33, AND 35 ARE FOR TTL SERIAL CONNECTOR TO UART

PINS 29, 37 ARE FOR SERIAL VCC POWER ENABLE

PINS 22, 24 ARE FOR EXTERNAL RESET SWITCH

PINS 26, 28 ARE FOR IM2 CIRCUIT ENABLE

PINS 30, 32 ARE FOR INTERRUPT 0 ENABLE

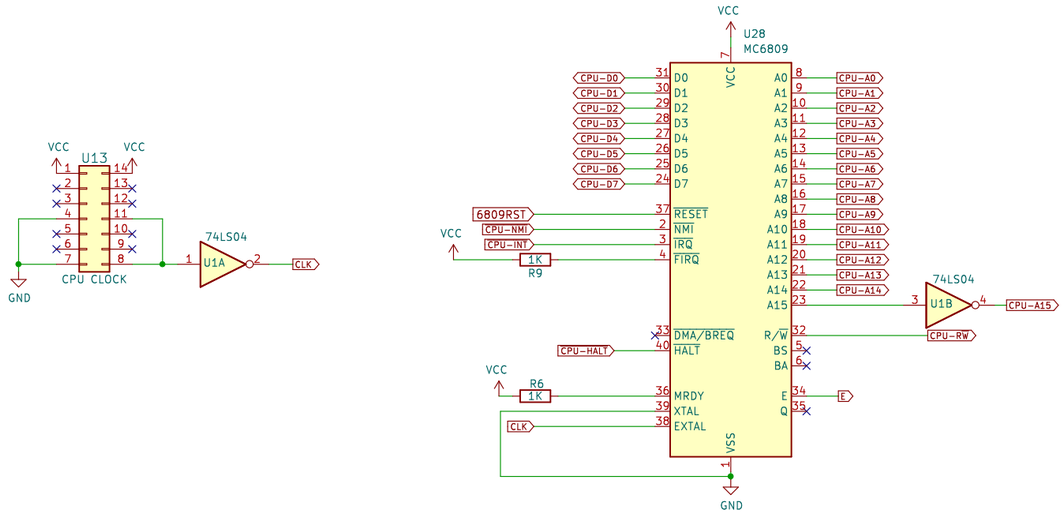
PINS 34, 36 ARE FOR WAIT STATE CIRCUIT ENABLE

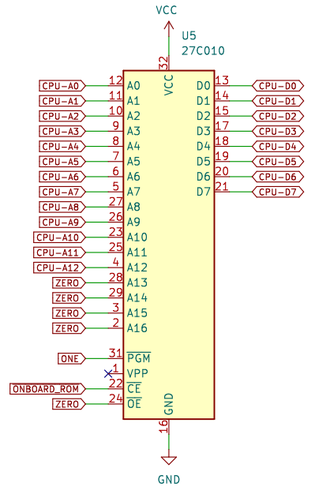
Sheet: /fpanel/
File: fpanel.kicad_sch

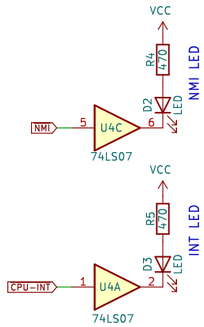
Title: Duodyne 6809 CPU board

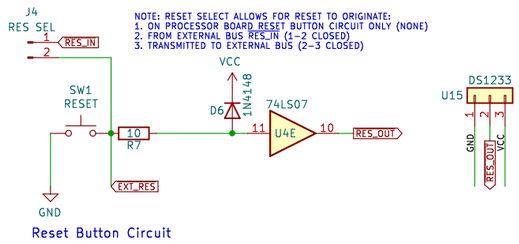
Size: B	Date: 2023-12-29	**Rev: V1.00**
KiCad E.D.A. eeschema (6.0.11)		Id: 8/9

PROCESSOR, 6809







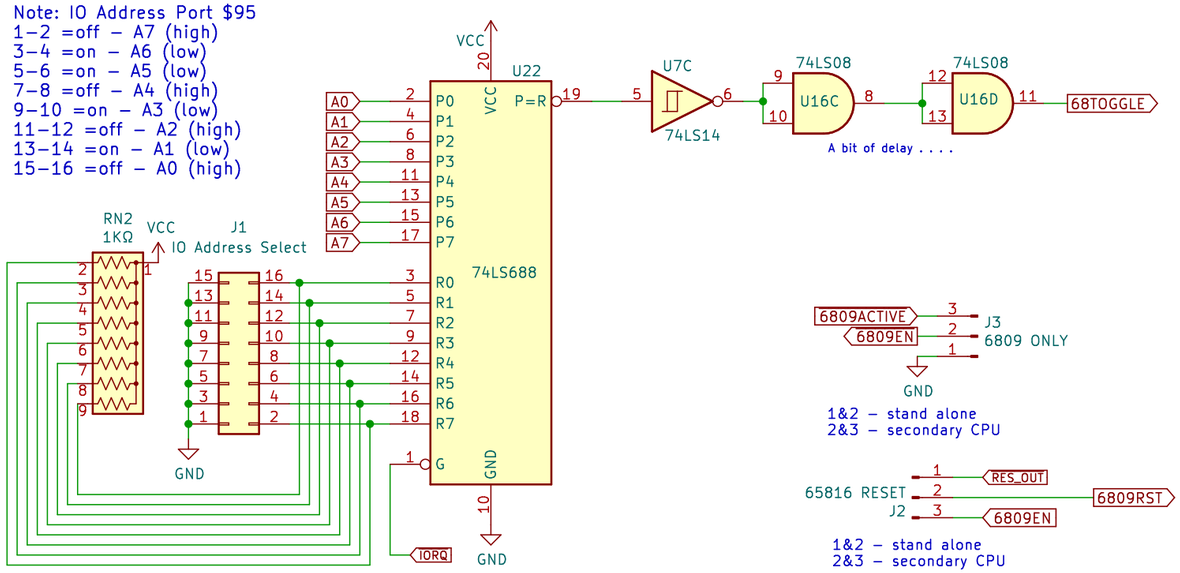


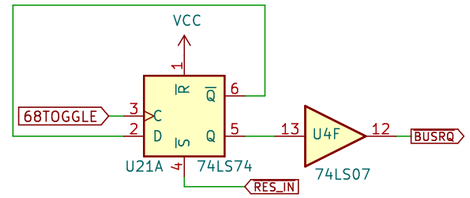
NOTE: RESET SELECT ALLOWS FOR RESET TO ORIGINATE:
1. ON PROCESSOR BOARD RESET BUTTON CIRCUIT ONLY (NONE)
2. FROM EXTERNAL BUS RES_IN (1-2 CLOSED)
3. TRANSMITTED TO EXTERNAL BUS (2-3 CLOSED)

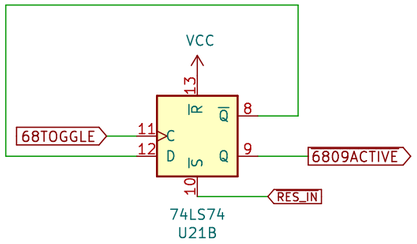
Reset Button Circuit

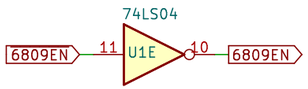
Sheet: /6809CPU/	
File: 6809CPU.kicad_sch	
Title: Duodyne 6809 CPU board	
Size: USLedger | Date: 2023-12-29	**Rev: V1.00**
KiCad E.D.A. eeschema (6.0.11)	Id: 9/9

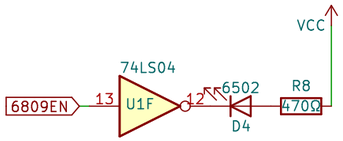
Note: IO Address Port $95
1–2 =off – A7 (high)
3–4 =on – A6 (low)
5–6 =on – A5 (low)
7–8 =off – A4 (high)
9–10 =on – A3 (low)
11–12 =off – A2 (high)
13–14 =on – A1 (low)
15–16 =off – A0 (high)











Sheet: /bus sharing/		
File: bussharing.kicad_sch		
Title: Duodyne 6809 CPU board		
Size: A4	Date: 2023–12–29	**Rev: V1.00**
KiCad E.D.A. eeschema (6.0.11)		Id: 9/9

IO ADDRESS SELECT CIRCUIT

MEMORY MAPPER AND
EXPANSION IO PORT DECODER

INTERRUPT FILTER CIRCUIT

Note: IO Address Port $50-$5F
1-2 =on - A7 (low)
3-4 =off - A6 (high)
5-6 =on - A5 (low)
7-8 =off - A4 (high)

U12 74LS688
P=R
CPU-A4 CPU-A5 CPU-A6 CPU-A7
CPU-IORQ
CS_IO
VCC GND

IO_PORT ADDR
JP10
ZERO
RN8 10K
VCC

U4B 74LS07
CS_IO
R12 470
D9 LED
CS LED

U7B 74LS14
INT-I2C
R10 470
GND

U7A 74LS14
UART_INT
R1 470
GND

J7 I2C IRQ Selection
INT0 EIRQ0 EIRQ1 EIRQ2 EIRQ3 EIRQ4 EIRQ5 EIRQ6 EIRQ7

J8 UART IRQ Selection
INT0 EIRQ0 EIRQ1 EIRQ2 EIRQ3 EIRQ4 EIRQ5 EIRQ6 EIRQ7

1.8432 OR 7.3728 MHz
TTL OSCILLATOR
U18 UART CLOCK
UART_CLK
GND

U20 TL16C550CFN
CPU-D0 CPU-D1 CPU-D2 CPU-D3 CPU-D4 CPU-D5 CPU-D6 CPU-D7
CPU-A0 CPU-A1 CPU-A2
ONE ONE
CS_UART
UART-CLK
CPU-WR ZERO ZERO CPU-RD ZERO
UART_INT
RI DCD DSR CTS
OUT1 DTR RTS OUT2
RTS CTS
ENABLEINT RTS PAGE-EN
SIN SOUT
RX TX
RXRDY TXRDY DDIS
BAUDOUT RCLK
VCC GND

U1D 74LS04
RES_OUT

MEMORY PAGING SRAMS

74LS670 U24
CPU-D0 CPU-D1 CPU-D2 CPU-D3
CPU-A0 CPU-A1
PAGE-WR
CPU-A14 CPU-A15
PAGE-EN
mA14 mA15 mA16 mA17
VCC GND

74LS670 U29
CPU-D4 CPU-D5 CPU-D6 CPU-D7
CPU-A0 CPU-A1
PAGE-WR
CPU-A14 CPU-A15
PAGE-EN
mA18 mA19 mA20 mA21
VCC GND

U19 74LS157
mA14 CPU-A14 mA15 CPU-A15
PAGE-EN
SEL-A14 SEL-A15
VCC GND

UPPER ADDRESS LINES
PULL-DOWN RESISTORS
RN3 470
mA14 mA15 mA16 mA17 mA18 mA19 mA20 mA21
GND

PCF8584 U27
CPU-A0 CPU-D0 CPU-D1 CPU-D2 CPU-D3 CPU-D4 CPU-D5 CPU-D6 CPU-D7
CS_I2C CPU-RD CS_I2C_WR CLK
SDA SCL
IACK INT RST
I2C_SDA I2C_SCL INT-I2C RES_OUT
R2 10K R3 10K
VCC GND

Sheet: /mapper/	
File: mapper.kicad_sch	
Title: Duodyne 6809 CPU board	
Size: B	Date: 2023-12-29
KiCad E.D.A. eeschema (6.0.11)	Id: 11/9

Rev: V1.00