

12345678

bus

power

buffers

fpanel

Z80CPU

File: bus.kicad_sch
DMA

File: power.kicad_sch
GALS

File: buffers.kicad_sch
IM2

File: fpanel.kicad_sch
waitstate

File: Z80CPU.kicad_sch
mapper

File: DMA.kicad_sch

File: GALS.kicad_sch

File: IM2.kicad_sch

File: waitstate.kicad_sch

File: mapper.kicad_sch

Sheet: /
File: processor.Z80.kicad_sch

Title:

Size: B

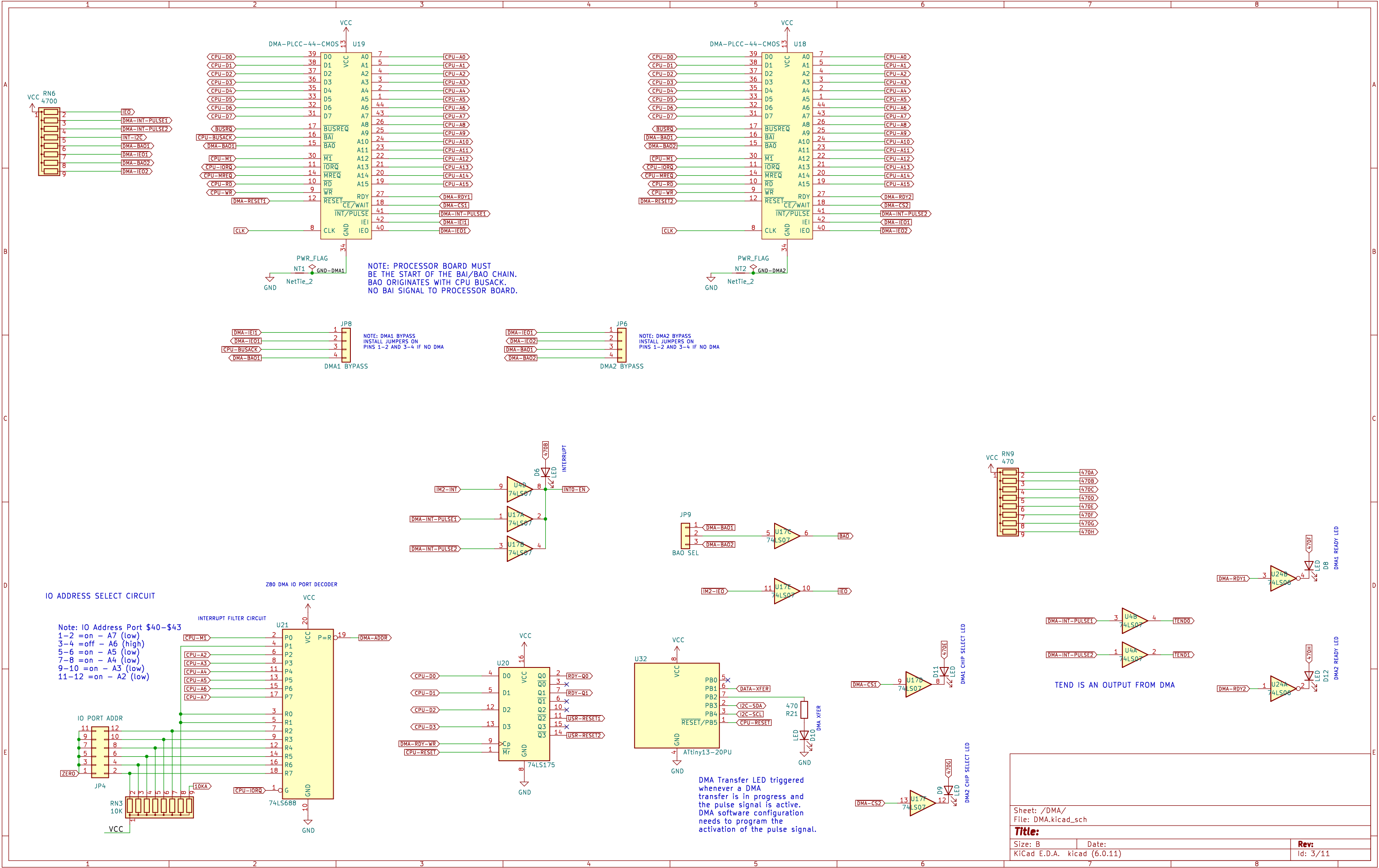
Date:

Rev:

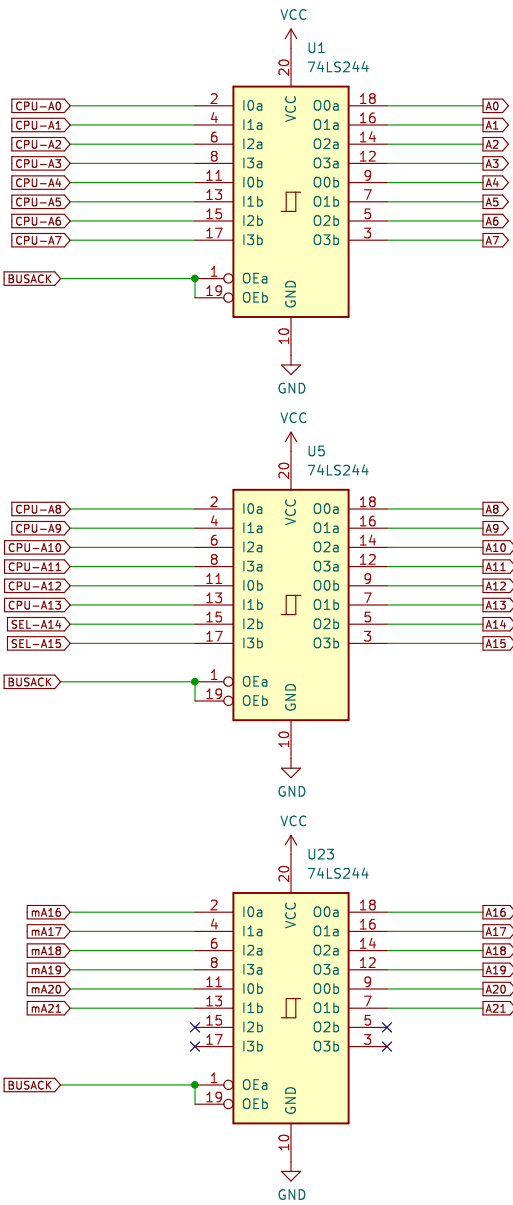
KiCad E.D.A. kicad (6.0.11)

Id: 1/11

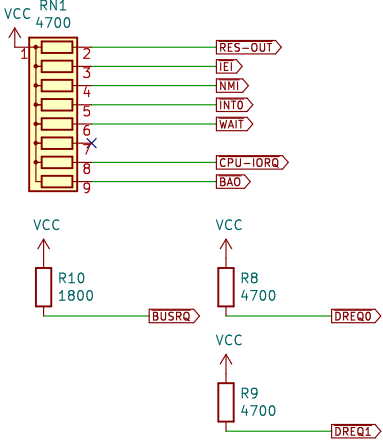
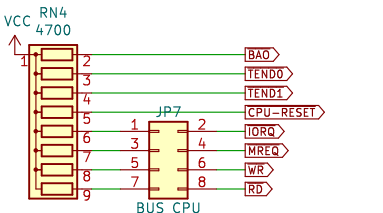
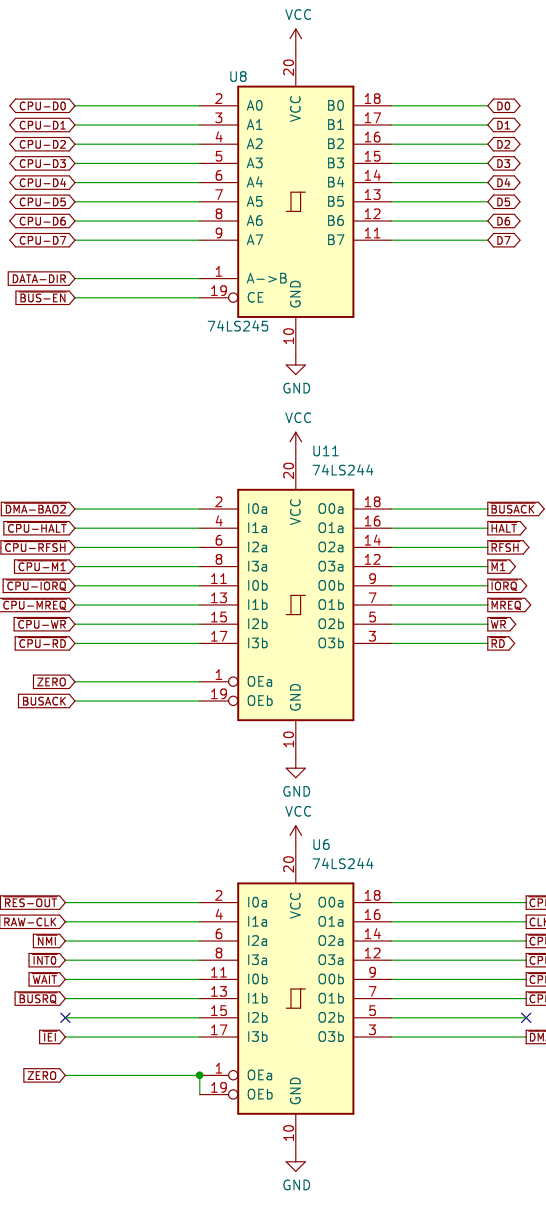


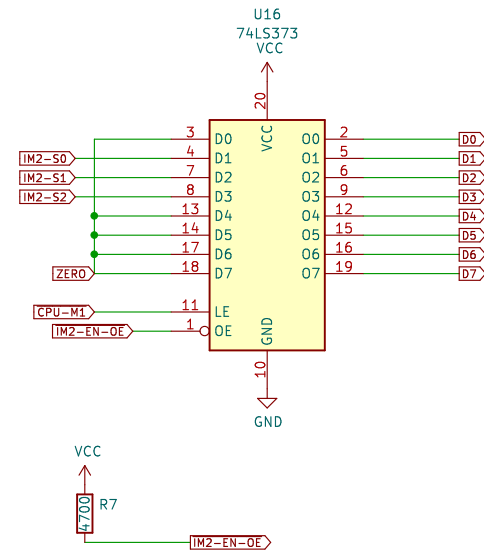
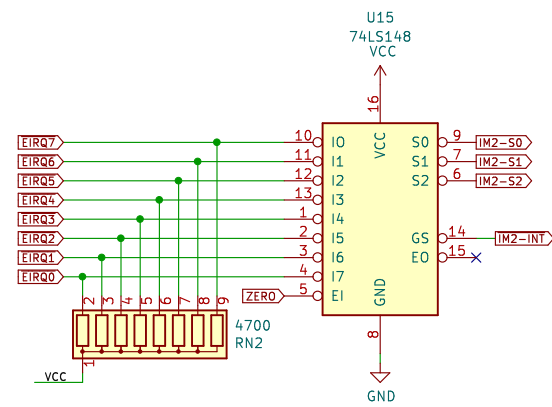


Id: 4/11



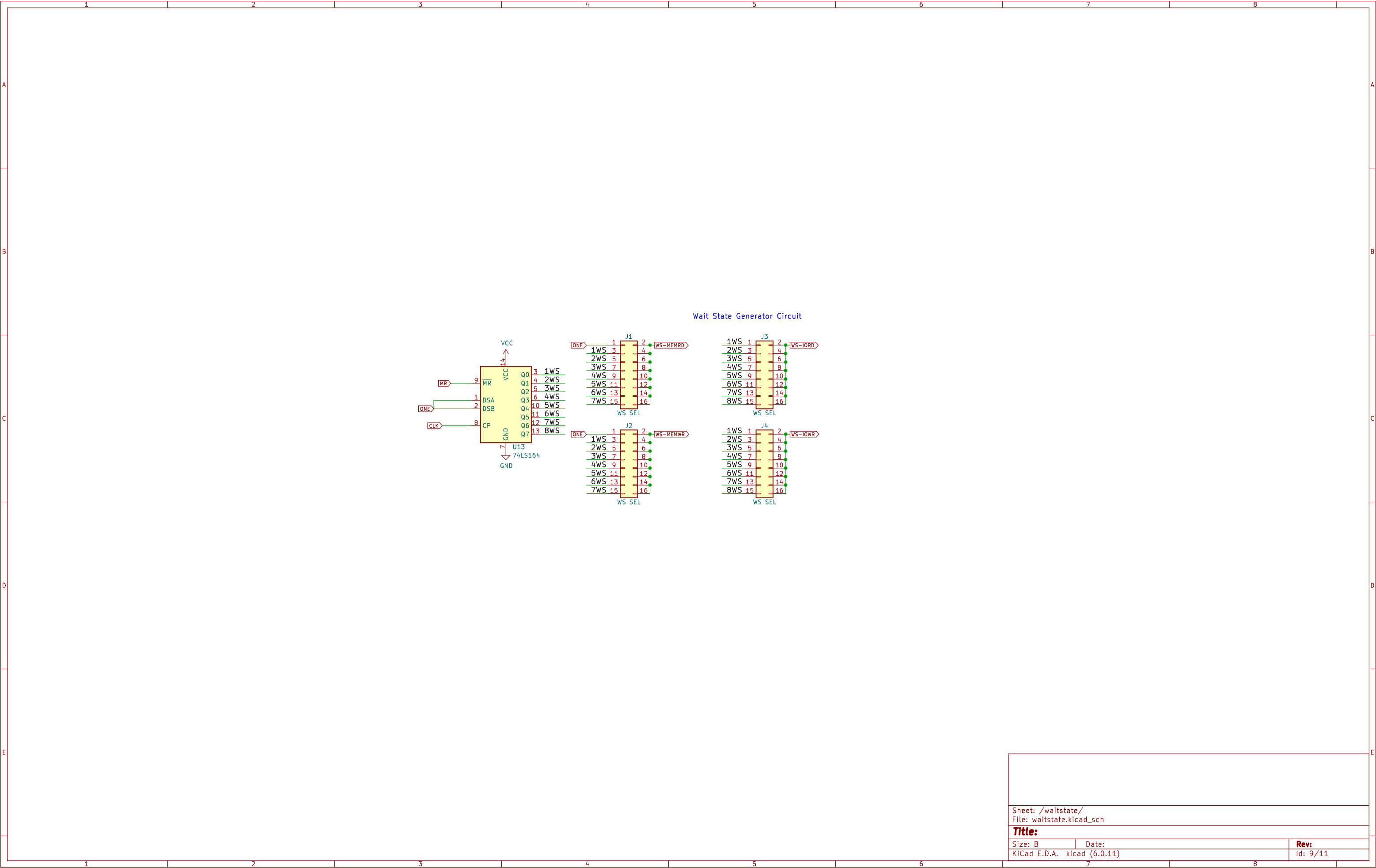
Z80 BUS INTERFACE







PINS 34, 36 ARE FOR WAIT STATE CIRCUIT ENABLE





Tri-state address, data, & control bus during DMA

