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power

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buffers

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fpanel

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Z80CPU

File: Z80CPU.kicad_sch

DMA

File: DMA.kicad_sch

GALS

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IM2

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waitstate

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mapper

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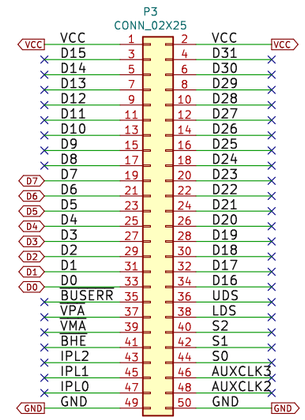

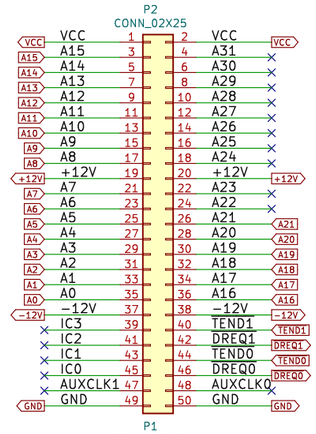

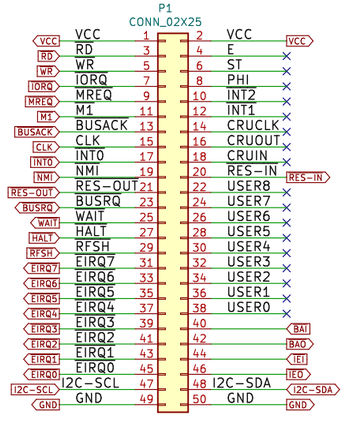

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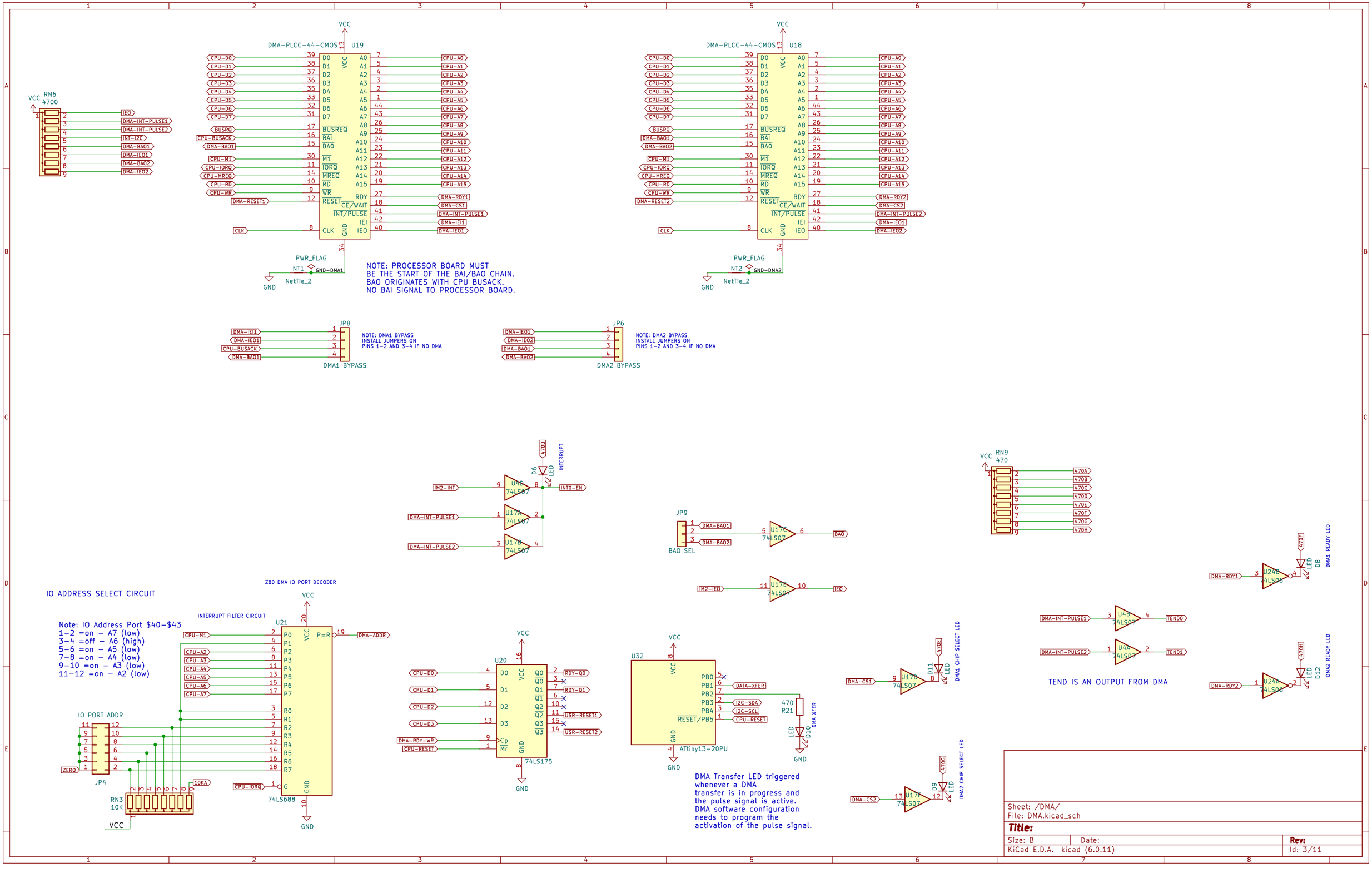

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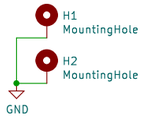
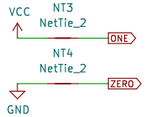
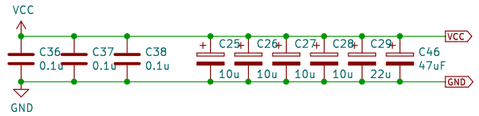
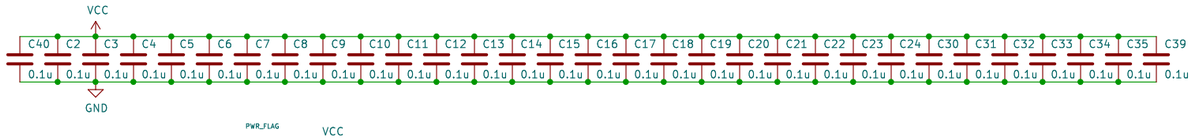
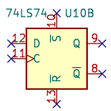


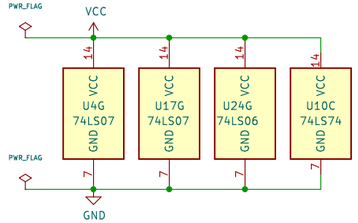






SPARE GATES





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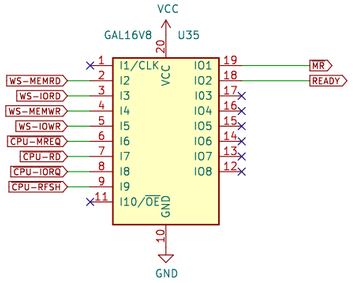
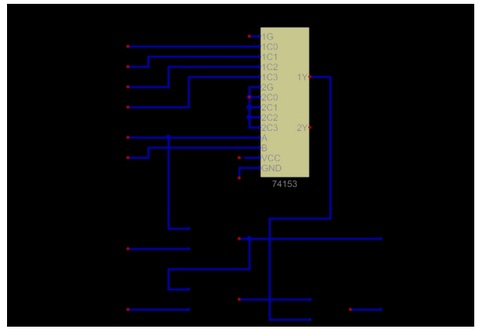
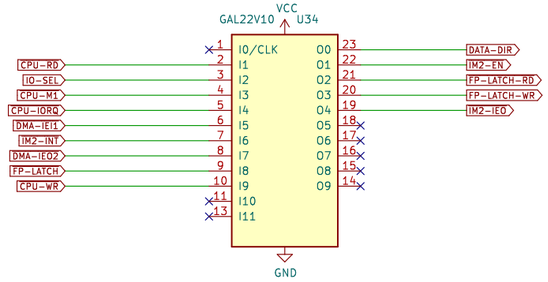
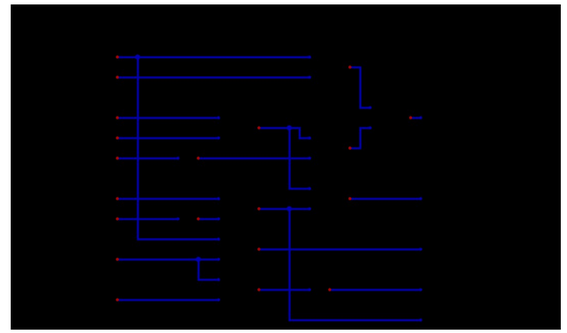
CPU WS GAL16V8

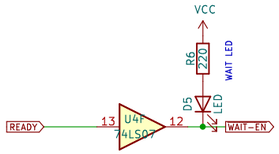




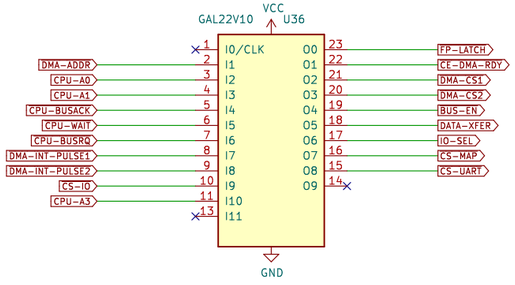
CPU DATA DIR GAL22V10

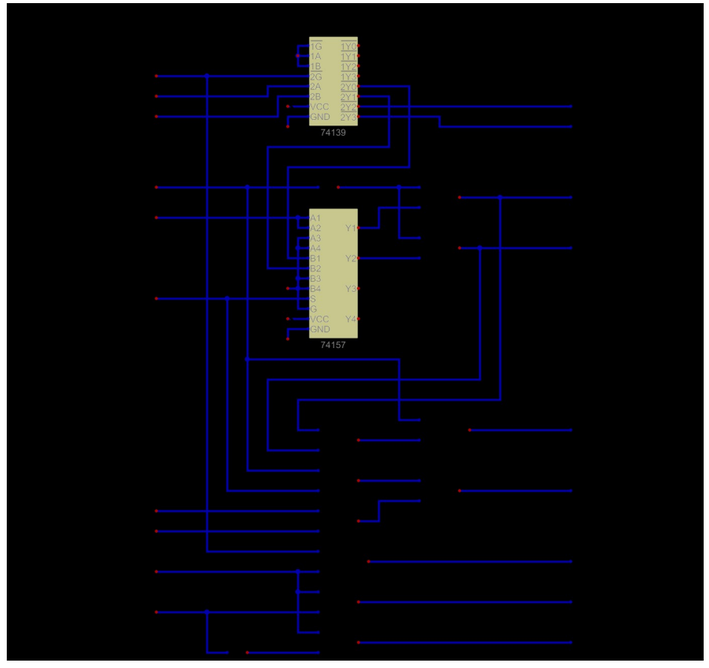






DMA CS V2 GAL22V10





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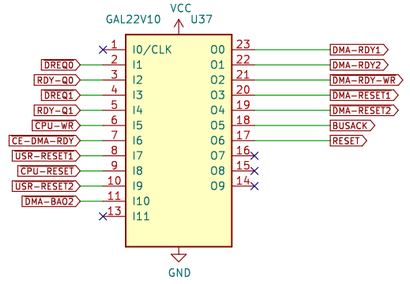

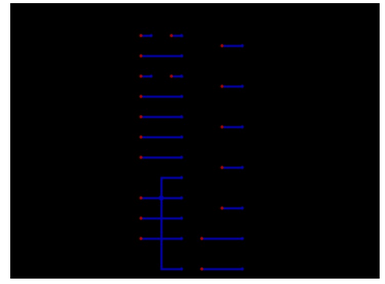

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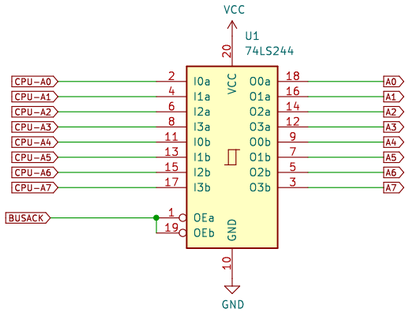
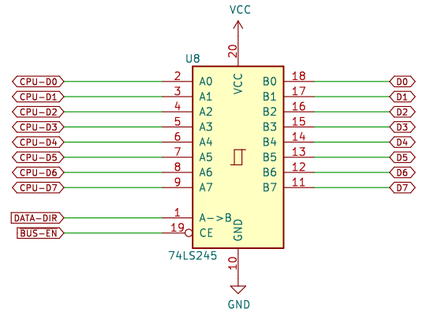
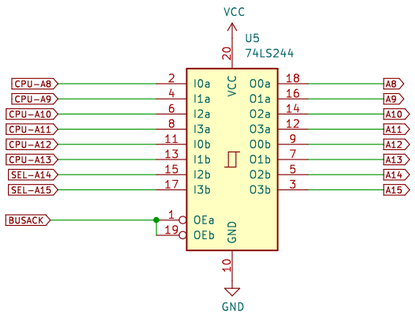
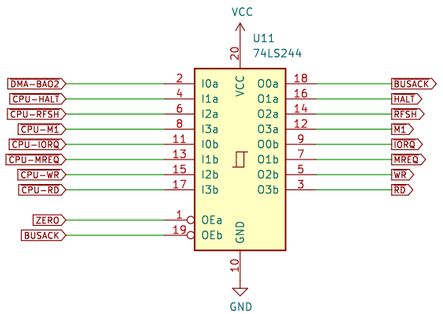
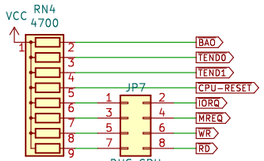
Z80 BUS INTERFACE

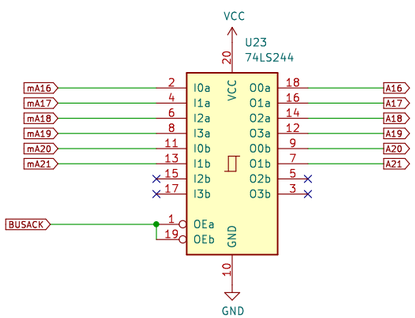


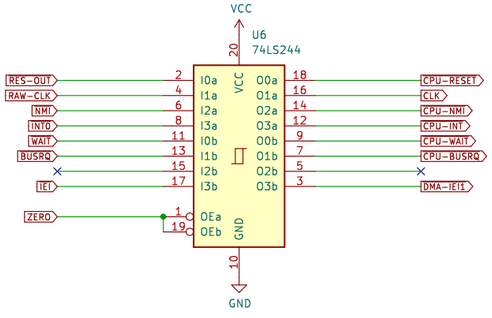


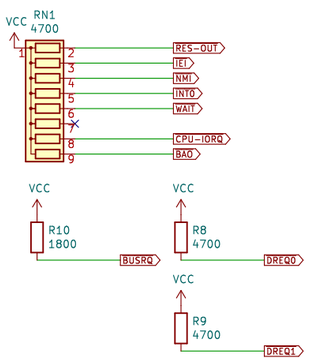












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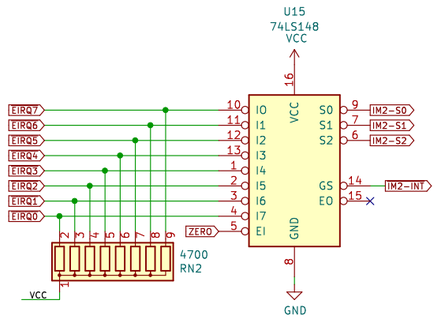
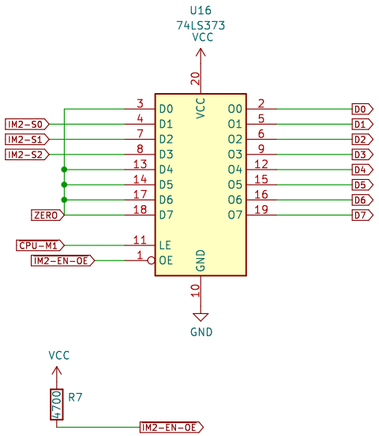
Interrupt Mode 2 (IM2) Circuit





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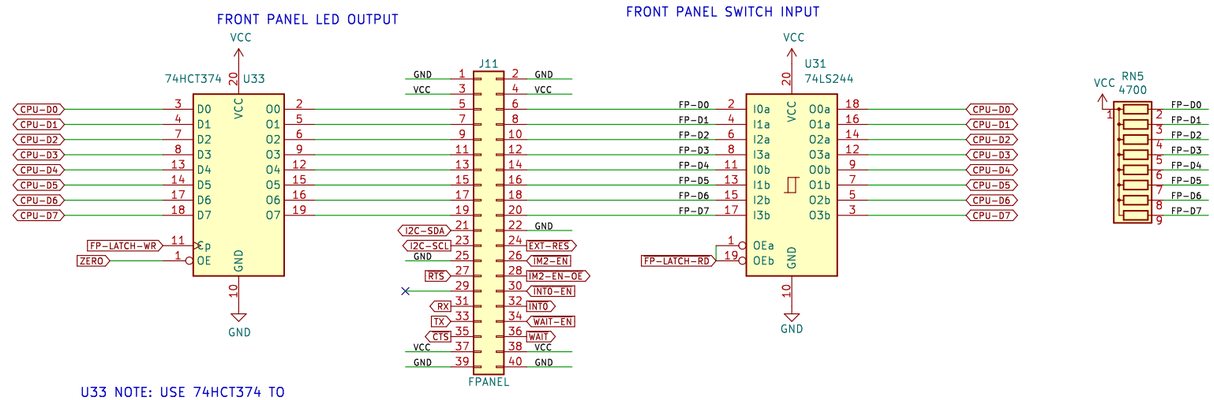

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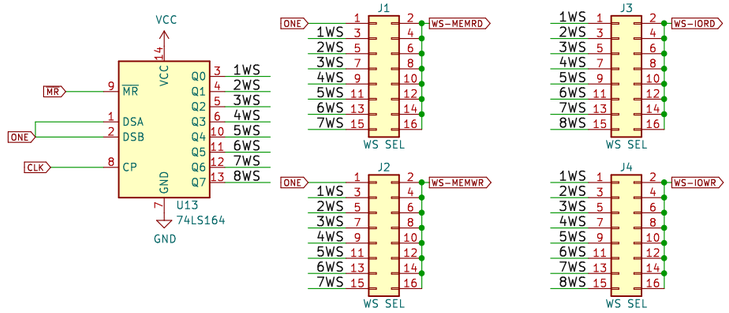
Wait State Generator Circuit



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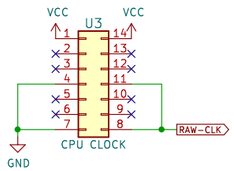
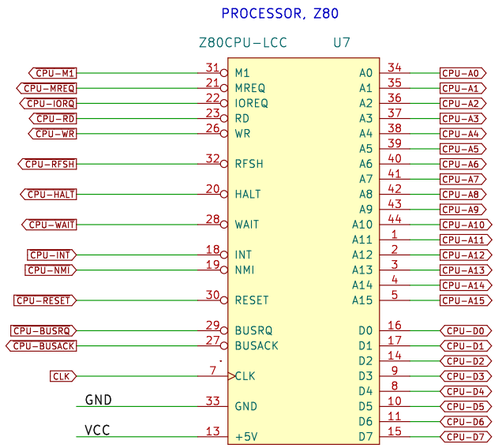
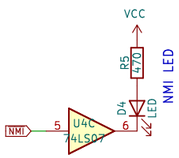
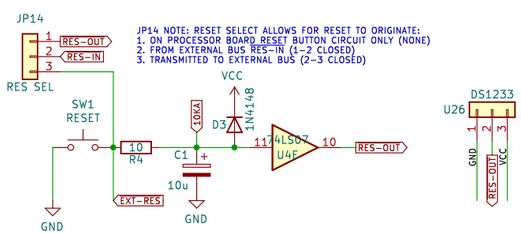




Tri-state address, data, & control bus during DMA





Reset Button Circuit

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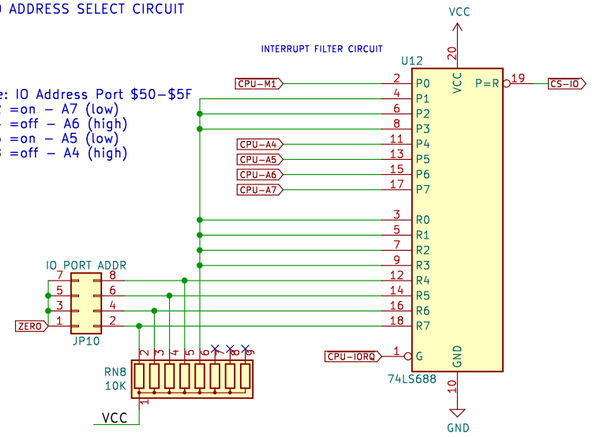
IO ADDRESS SELECT CIRCUIT

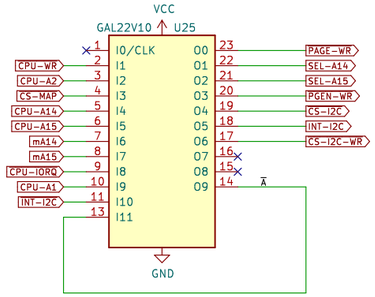
Z80 MEMORY MAPPER AND
EXPANSION IO PORT DECODER

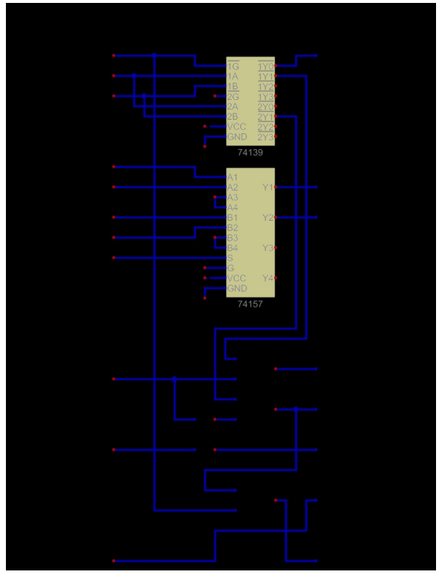
INTERRUPT FILTER CIRCUIT

Note: IO Address Port $50-$5F
1-2 =on - A7 (low)
3-4 =off - A6 (high)
5-6 =on - A5 (low)
7-8 =off - A4 (high)

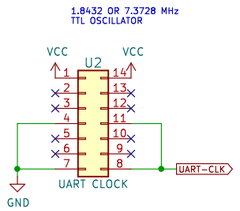


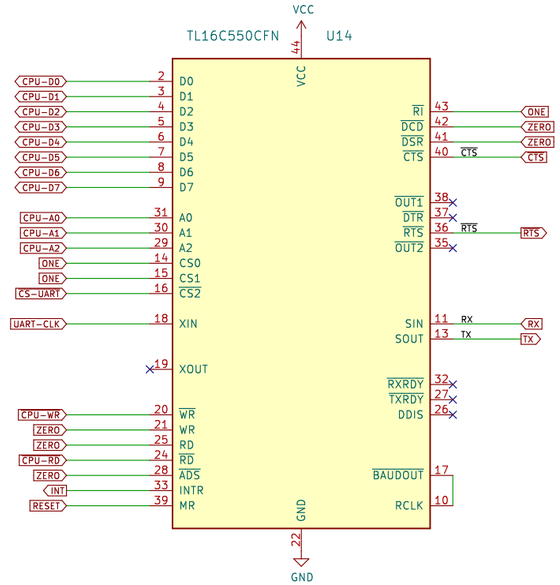
CPU MAPPER V2 GAL22V10



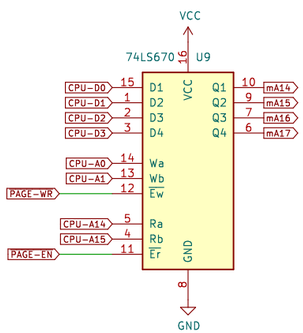


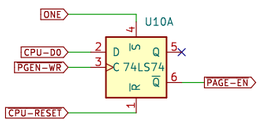
1.8432 OR 7.3728 MHz TTL OSCILLATOR

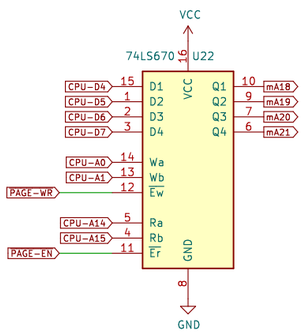




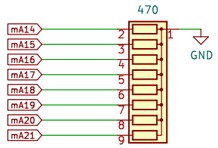
MEMORY PAGING SRAMS

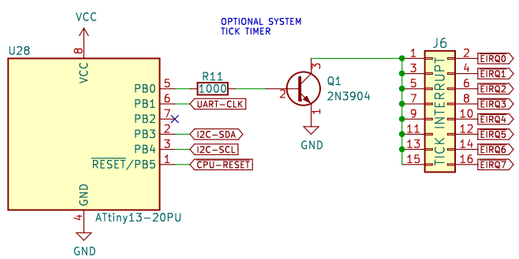


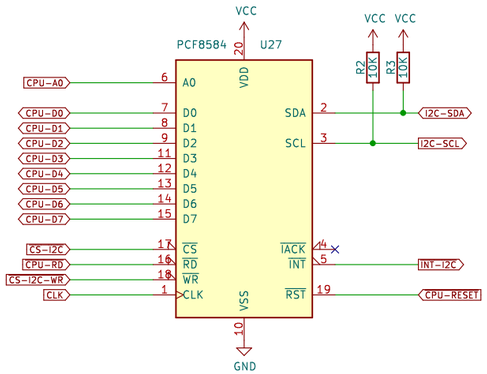


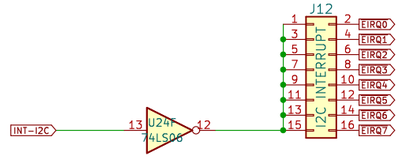


UPPER ADDRESS LINES PULL-DOWN RESISTORS

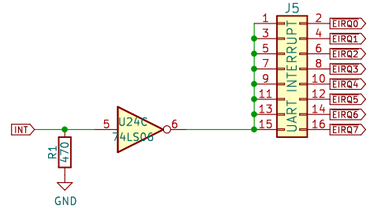








NOTE: INTERRUPTS RELY ON 4700
OHM PULL UP RESISTOR ON PROCESSOR



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