bus

File: bus.kicad_sch

power

File: power.kicad_sch

buffers

File: buffers.kicad_sch

fpanel

File: fpanel.kicad_sch

Z80CPU

File: Z80CPU.kicad_sch

DMA

File: DMA.kicad_sch

GALS

File: GALS.kicad_sch

IM2

File: IM2.kicad_sch

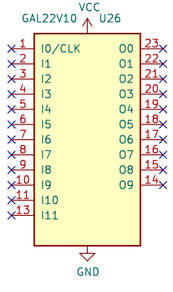
waitstate

File: waitstate.kicad_sch

mapper

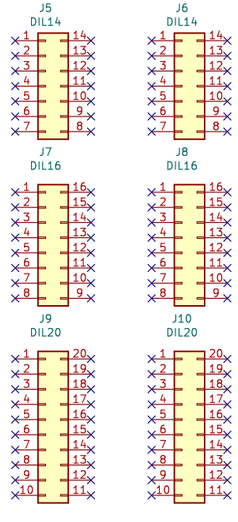
File: mapper.kicad_sch

SPARE GAL FOR DEBUGGING



THROUGH HOLES FOR PATCH WIRE ROUTING ACROSS SIDES

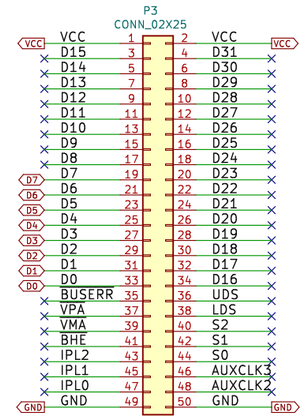
SPARE SOCKETS FOR DEBUGGING

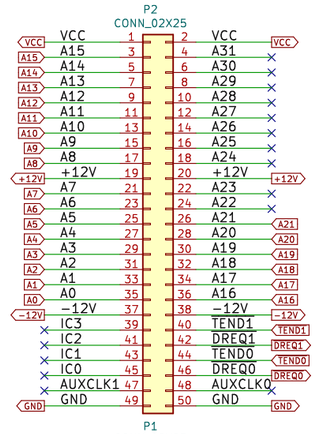


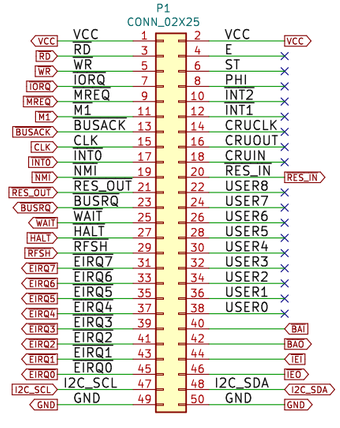
Sheet: /
File: processor.Z80.kicad_sch

Title:

Size: B	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.11)		Id: 1/11



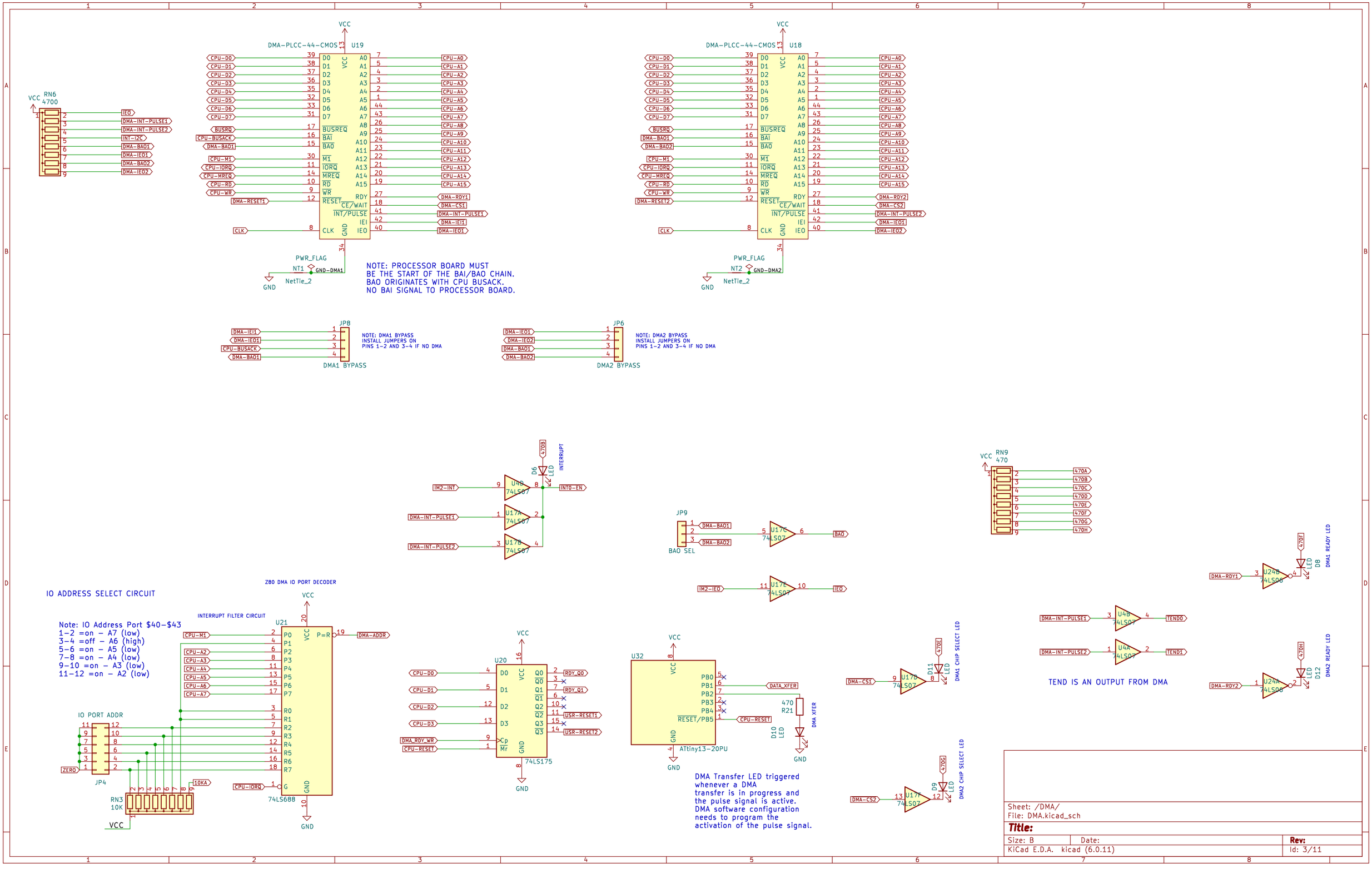




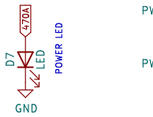
Sheet: /bus/
File: bus.kicad_sch

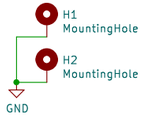
Title:

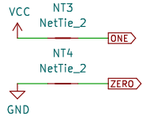
Size: B | Date: | **Rev:**
KiCad E.D.A. kicad (6.0.11) | Id: 2/11

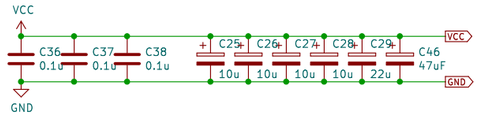


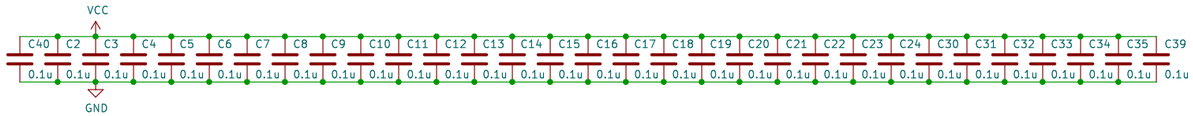
Sheet: /DMA/		
File: DMA.kicad_sch		
Title:		
Size: B	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.11)		Id: 3/11



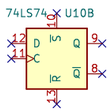


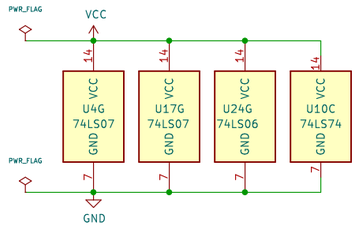






SPARE GATES



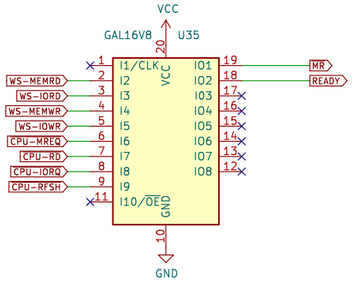


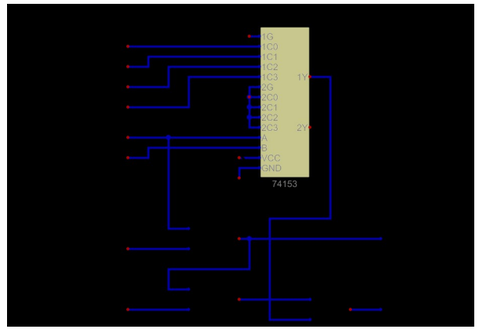
Sheet: /power/
File: power.kicad_sch

Title:

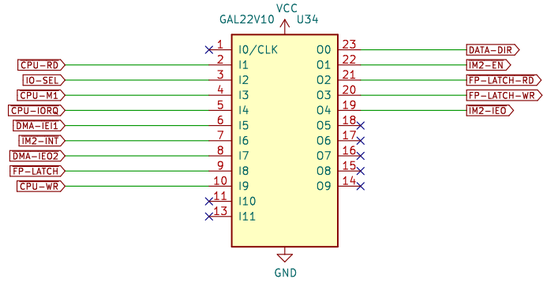
Size: B	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.11)		Id: 4/11

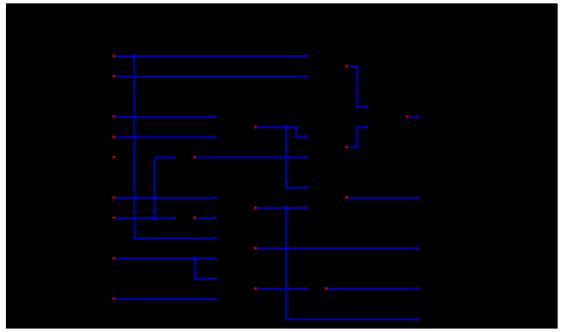
CPU WS GAL16V8

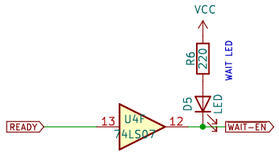




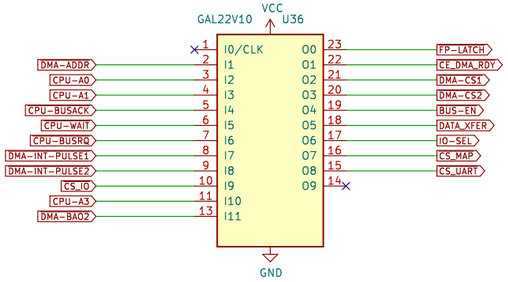
CPU DATA DIR V3 GAL22V10

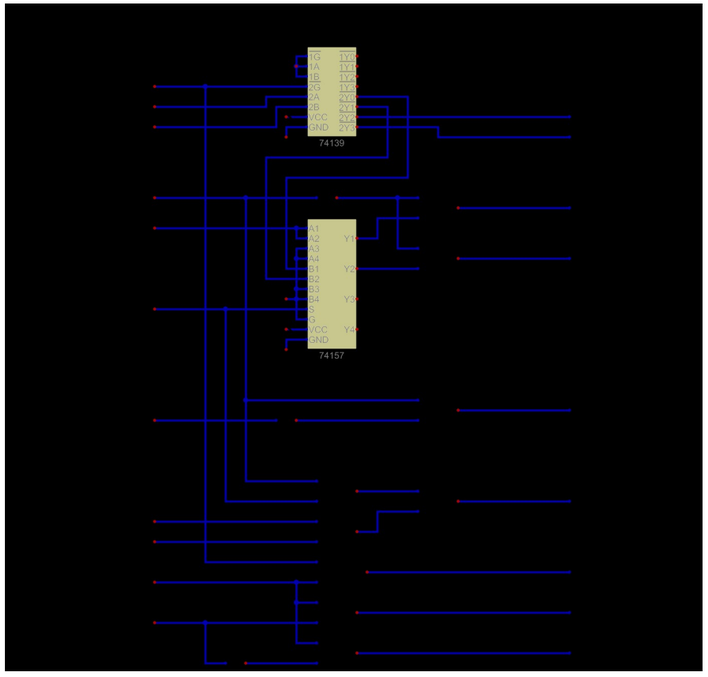




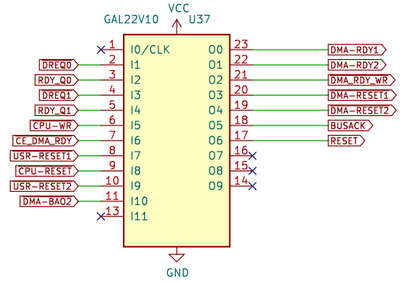


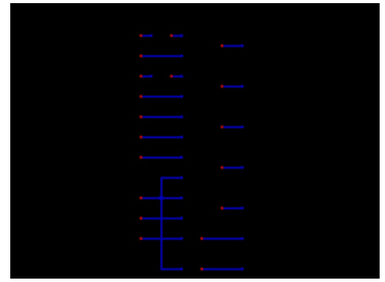
DMA CS V3 GAL22V10





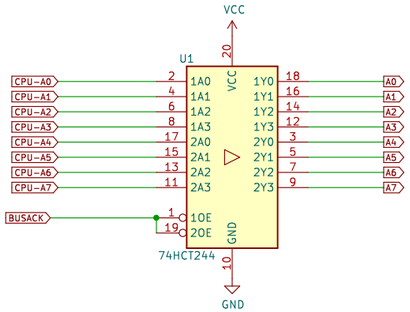
DMA RDY GAL22V10

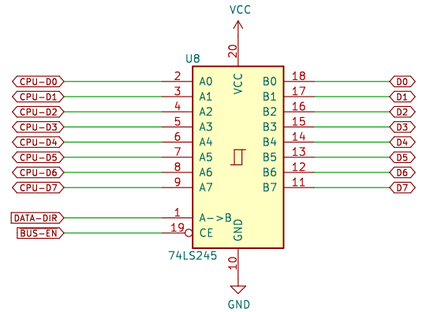


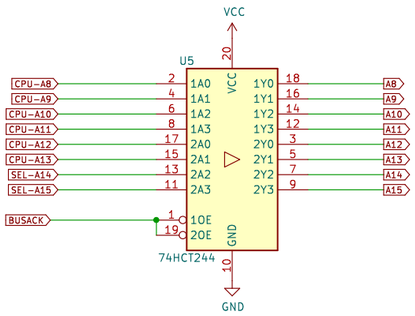


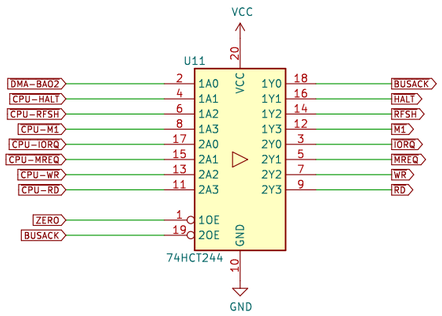
Sheet: /GALS/ File: GALS.kicad_sch		
Title:		
Size: B	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.11)		Id: 5/11

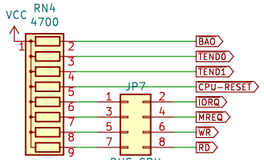
Z80 BUS INTERFACE

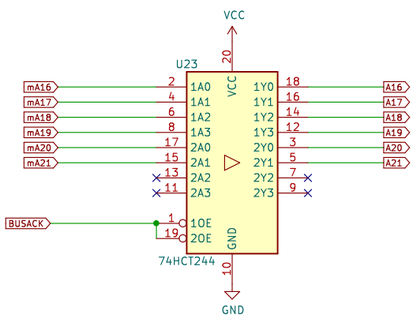


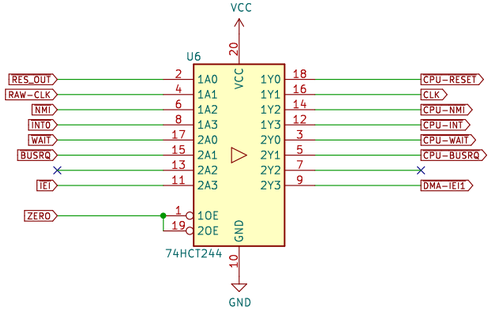


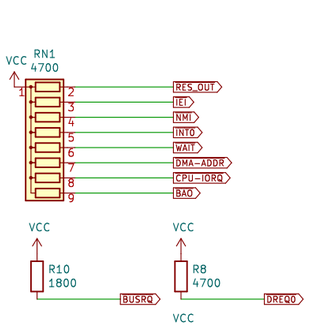










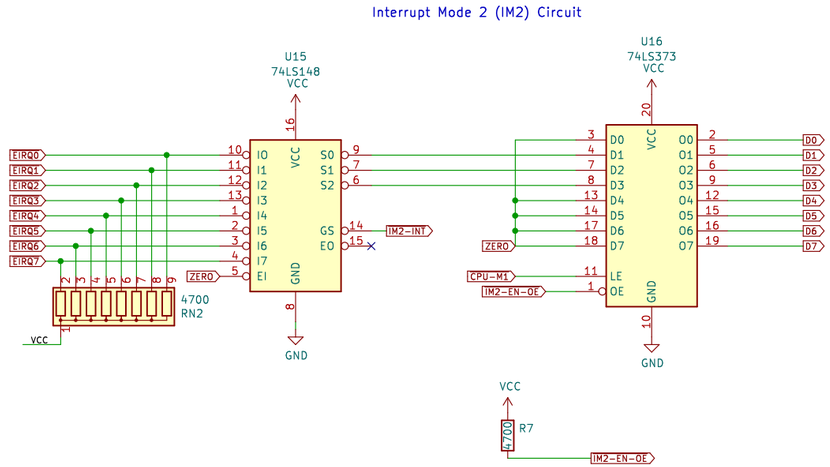


Sheet: /buffers/
File: buffers.kicad_sch

Title:

Size: B	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.11)		Id: 6/11

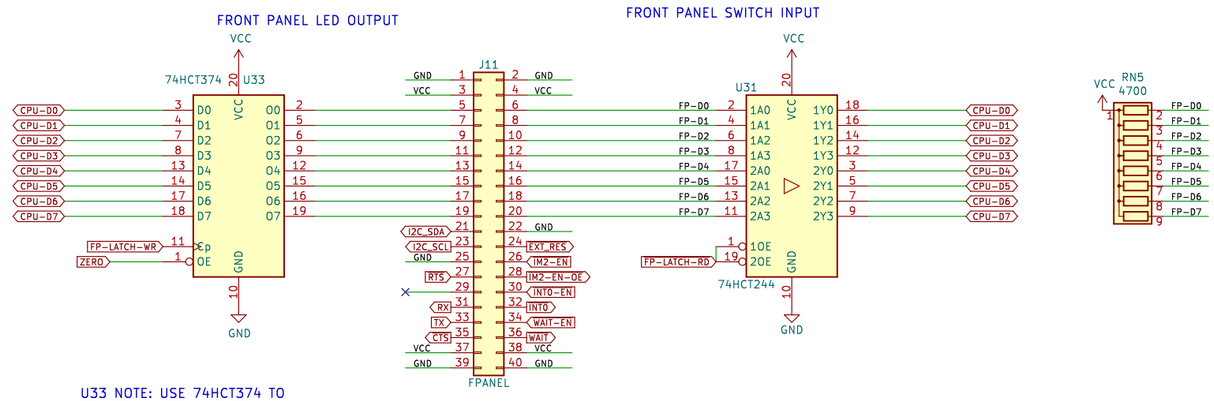
Interrupt Mode 2 (IM2) Circuit



Sheet: /IM2/
File: IM2.kicad_sch

Title:

Size: B	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.11)		Id: 7/11



U33 NOTE: USE 74HCT374 TO SOURCE OR SINK ADEQUATE CURRENT TO DRIVE LEDS ON FRONT PANEL

J11 NOTE:

PINS 5, 7, 9, 11, 13, 15, 17, 19 ARE FOR LED STATUS FOR ROMWBW FRONT PANEL INDICATOR

PINS 6, 8, 10, 12, 14, 16, 18, 20 ARE FOR SWITCH INPUTS FOR ROMWBW FRONT PANEL

PINS 21, 23 ARE FOR I2C CONNECTION (SDA & SCL)

PINS 25, 27, 29, 31, 33, AND 35 ARE FOR TTL SERIAL CONNECTOR TO UART

PINS 29, 37 ARE FOR SERIAL VCC POWER ENABLE

PINS 22, 24 ARE FOR EXTERNAL RESET SWITCH

PINS 26, 28 ARE FOR IM2 CIRCUIT ENABLE

PINS 30, 32 ARE FOR INTERRUPT 0 ENABLE

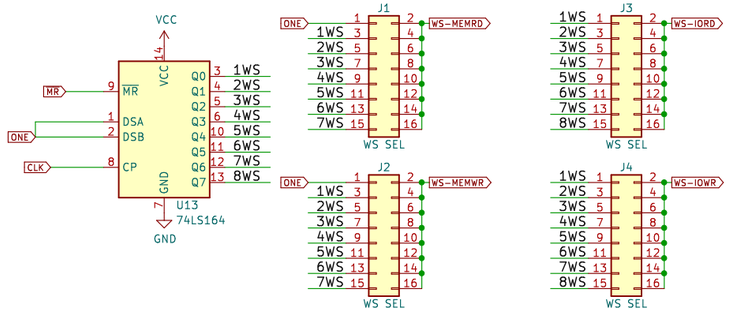
PINS 34, 36 ARE FOR WAIT STATE CIRCUIT ENABLE

Sheet: /fpanel/
File: fpanel.kicad_sch

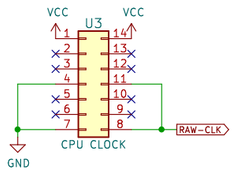
Title:

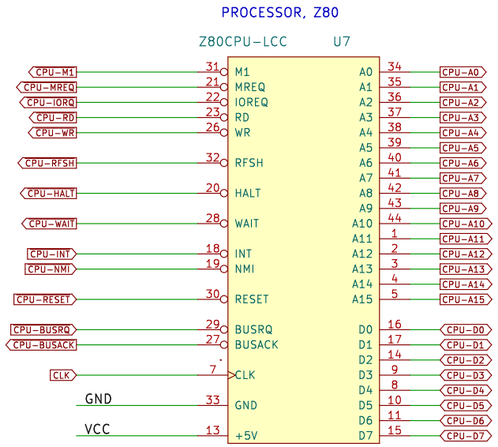
Size: B	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.11)		Id: 8/11

Wait State Generator Circuit

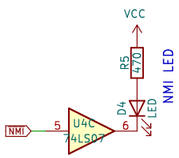


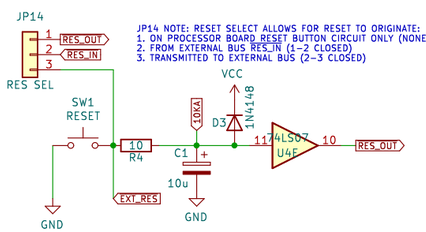
Sheet: /waitstate/		
File: waitstate.kicad_sch		
Title:		
Size: B	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.11)		Id: 9/11





Tri-state address, data, & control bus during DMA





Reset Button Circuit

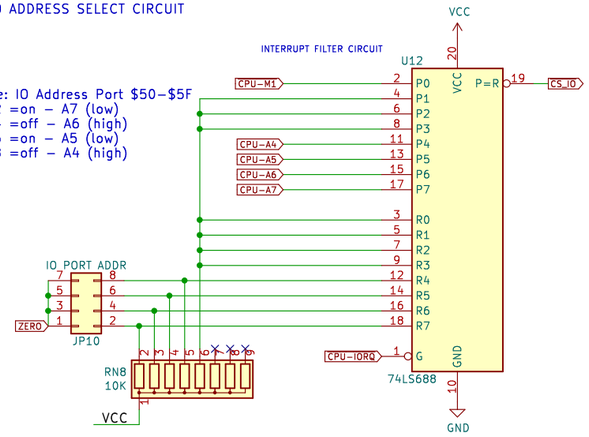
Sheet: /Z80CPU/	
File: Z80CPU.kicad_sch	
Title:	
Size: B	Date:
KiCad E.D.A. kicad (6.0.11)	Id: 10/11

Z80 MEMORY MAPPER AND
EXPANSION IO PORT DECODER

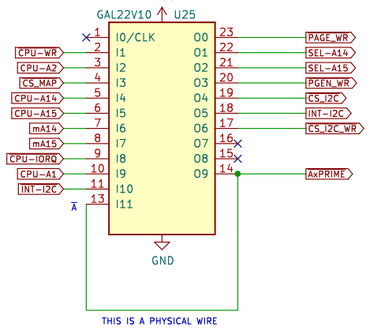
IO ADDRESS SELECT CIRCUIT

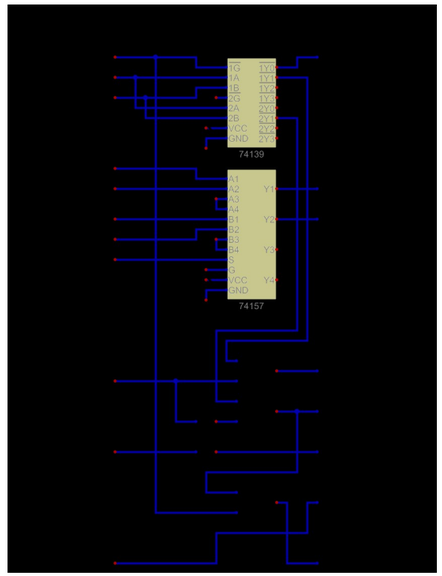
INTERRUPT FILTER CIRCUIT

Note: IO Address Port $50-$5F
1-2 =on - A7 (low)
3-4 =off - A6 (high)
5-6 =on - A5 (low)
7-8 =off - A4 (high)

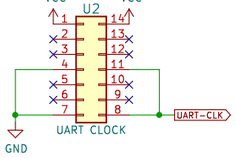


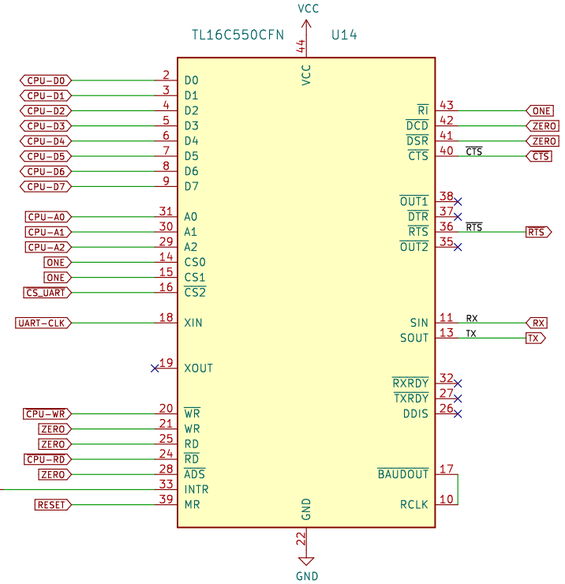
CPU MAPPER V3 GAL22V10



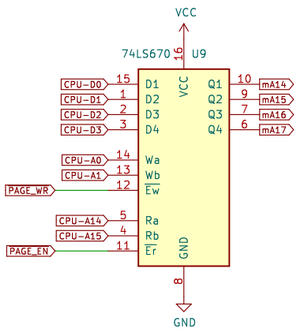


1.8432 OR 7.3728 MHz
TTL OSCILLATOR

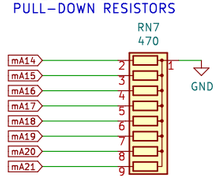


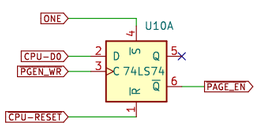


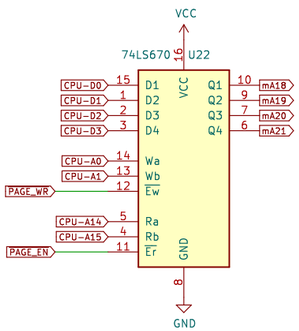
MEMORY PAGING SRAMS

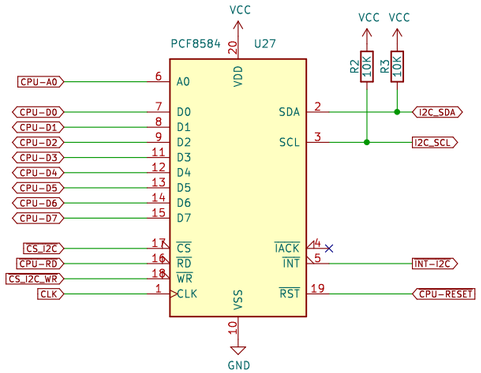


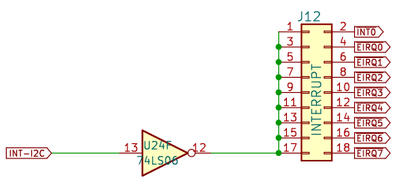
UPPER ADDRESS LINES
PULL-DOWN RESISTORS



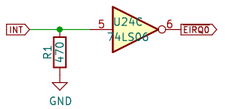








NOTE: INTERRUPTS RELY ON 4700
OHM PULL UP RESISTOR ON PROCESSOR



Sheet: /mapper/
File: mapper.kicad_sch

Title:

Size: B | Date: | **Rev:**
KiCad E.D.A. kicad (6.0.11) | Id: 11/11