bus

File: bus.kicad_sch

PPIDE

File: PPIDE.kicad_sch

GAL

File: GAL.kicad_sch

IO

File: IO.kicad_sch

power

File: power.kicad_sch

FDC

File: FDC.kicad_sch

buffers

File: buffers.kicad_sch

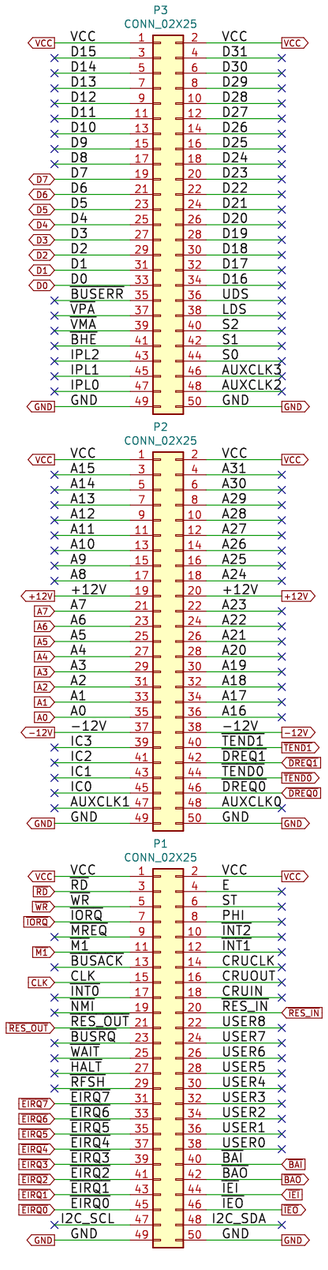
WIZNET

File: WIZNET.kicad_sch

Sheet: /
File: input-output.Disk.kicad_sch

Title:

Size: B	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.11)		Id: 1/9



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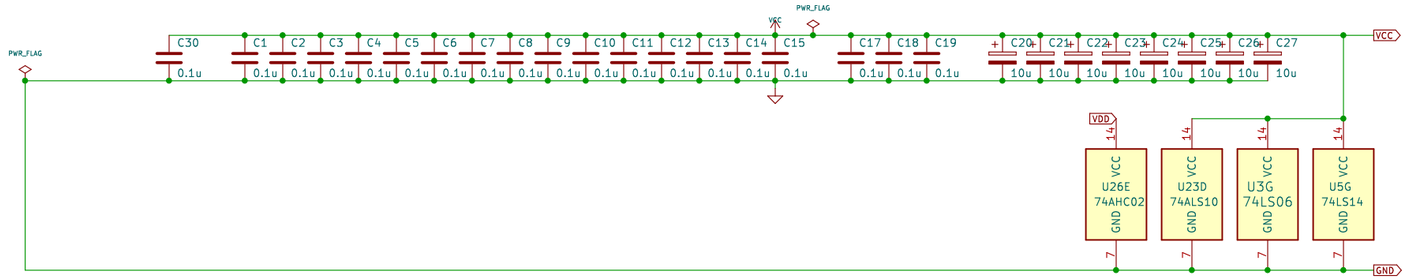
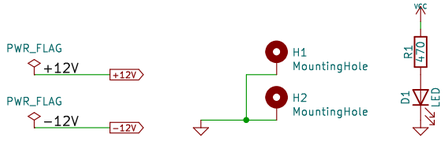
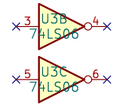
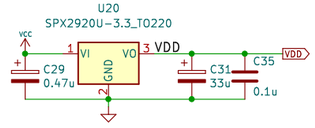
Size: B	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.11)		Id: 2/9





Spare Components

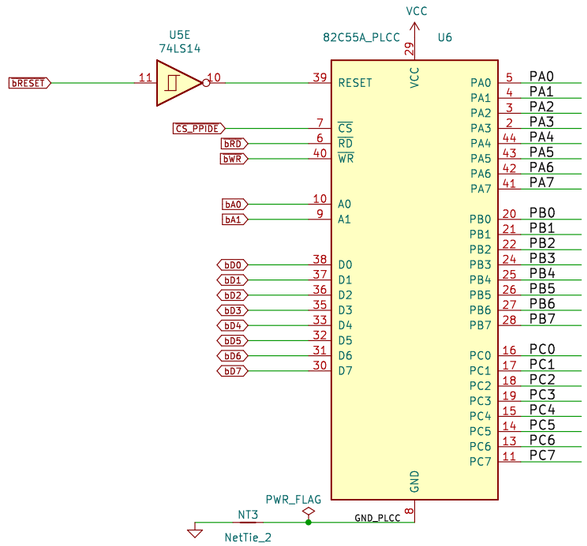


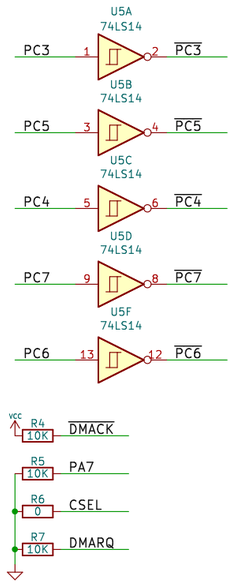


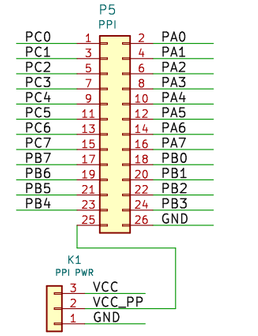
SPX2920U OR LM3940
EQUIVALENT VOLTAGE
REGULATOR OR USE
POLOLU 3.3V STEP
DOWN CONVERTER

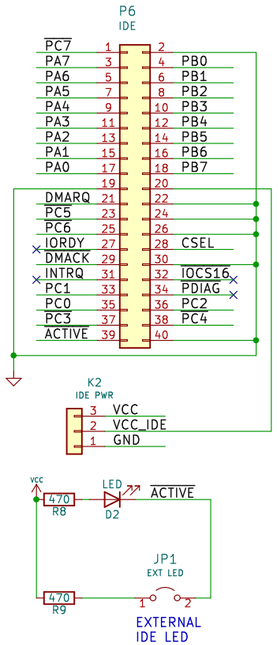
https://www.pololu.com/product/2122

Sheet: /power/		
File: power.kicad_sch		
Title:		
Size: B	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.11)		Id: 3/9









Sheet: /PPIDE/
File: PPIDE.kicad_sch

Title:

Size: B	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.11)		Id: 4/9

FLOPPY DRIVE INTERFACE

IO Ports
x0 read Main Status Register
x1 read/write Data In/Out
x2 read/write Terminal Count
x3 read/write User Reset FDC
x4 <none>
x5 write Load Control Register
x6 read DMA Acknowledge/write Load Operations Register
x7 read DMA Acknowledge and Terminal Count

U7 16 MHz
U9 9.6 MHz

NOTE: U12 OPTIONAL
SECONDARY CLOCK
FOR 150/300 KBPS
DRIVES. USE P5 1-2
CLOSED TO ENABLE;
DEFAULT IS 2-3 CLOSED

P7
FDC CLK
GND
16MHZ-CLK

U8
WD37C65BJM/WD
PLCC

FDC-RESET
FDC-TC
bRD
bWR
MSR-DATA
FDC-DACK
LDOR
LDCR
bD0 bD1 bD2 bD3 bD4 bD5 bD6 bD7
bA0
PCVAL
ZERO
INT_FDC
FDC_DMA
HS WE WD DIRC STEP DS1 DS2 MO1 MO2 HDL RWC RDD DCHG WP TR00 IDX

R10 4700
R12 4700
R13 4700
R11 4700

PWR_FLAG
NT4 GND_PLCC
NetTie_2

IBM floppy connector
A: = DS1 (no twist)
B: = DS2 (twist)

P10
FLOPPY

RP1 1000
RDD DCHG WP TR00 IDX PCVAL

NOTE: REPLACE RP1 WITH 150 OHM
9 PIN SIP RESISTOR PACK FOR
LEGACY FLOPPY DRIVES; 1000 OHM
FOR 3.5" IBM PC 1.44MB COMPATIBLE

EXTERNAL DMA INTERFACE

PULSE
P8
TEND SEL
TEND0 TEND1

U3A 74LS08
P9
DREQ SEL
DREQ0 DREQ1
RDY

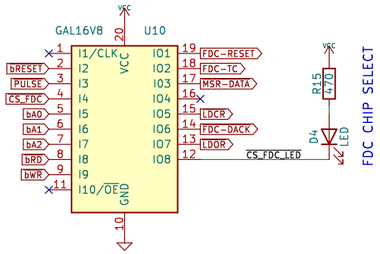
J7
FDC INTERRUPT
EIRQ0 EIRQ1 EIRQ2 EIRQ3 EIRQ4 EIRQ5 EIRQ6 EIRQ7

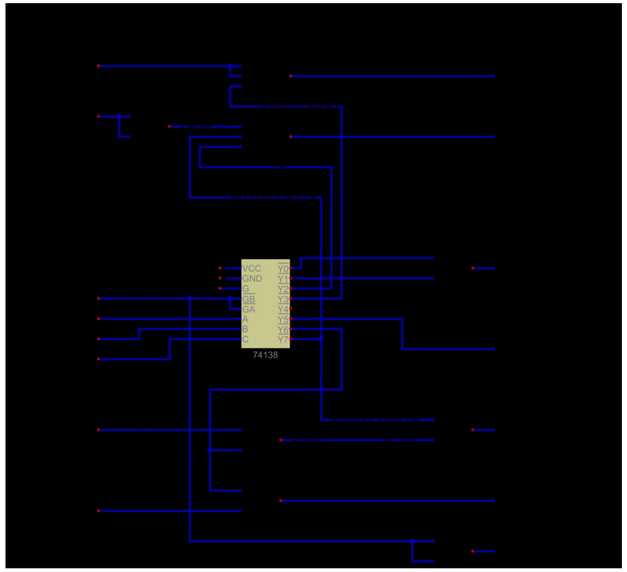
U3F 74LS08

NOTE: RELIES ON 4700 OHM PULL UP
RESISTOR ON Z80 PROCESSOR BOARD

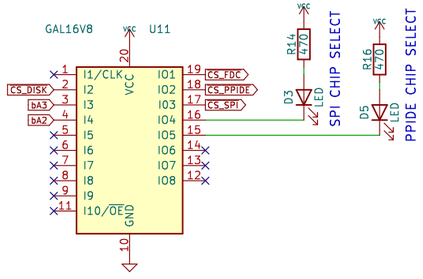
Sheet: /FDC/
File: FDC.kicad_sch
Title:
Size: B Date: Rev:
KiCad E.D.A. kicad (6.0.11) Id: 5/9

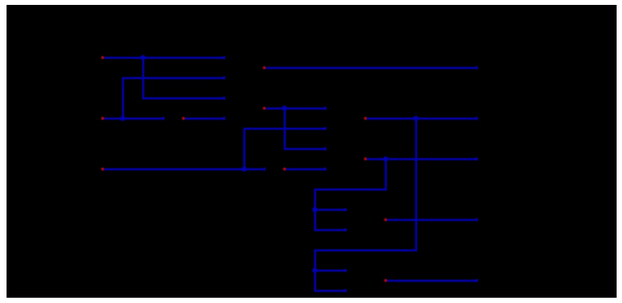
FDC DMA GAL16V8





DISK CS GAL16V8



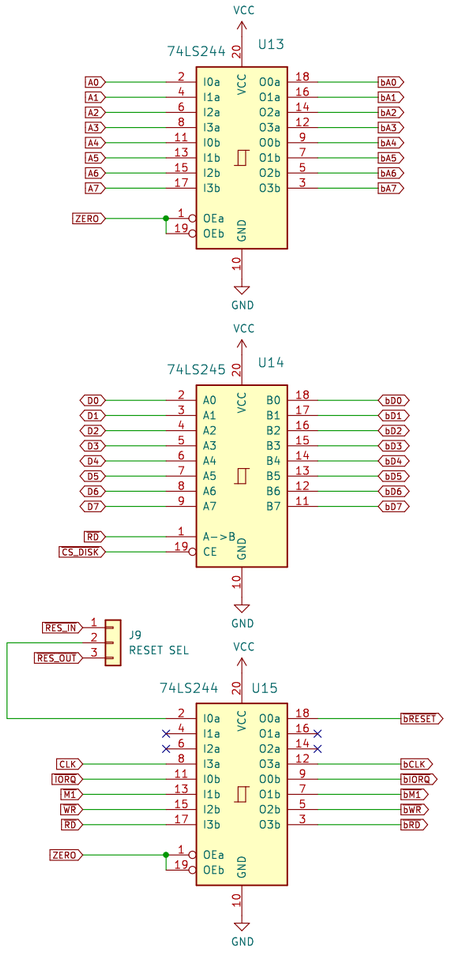


Sheet: /GAL/
File: GAL.kicad_sch

Title:

Size: B	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.11)		Id: 6/9

Z80 BUS INTERFACE



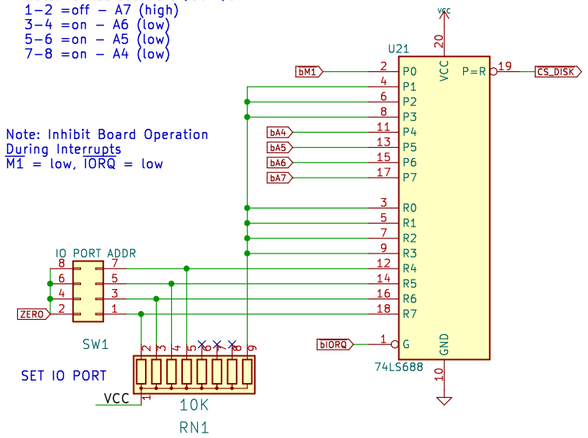
Note: Buffers and Transceivers
respond to IO and MEM cycles

Sheet: /buffers/		
File: buffers.kicad_sch		
Title:		
Size: B	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.11)		Id: 7/9

IO SELECTION CIRCUIT
FDC, PPIDE, SPI-SD

Note: IO Address Port $80-$8F
1-2 =off - A7 (high)
3-4 =on - A6 (low)
5-6 =on - A5 (low)
7-8 =on - A4 (low)

Note: Inhibit Board Operation
During Interrupts
M1 = low, IORQ = low



Sheet: /IO/		
File: IO.kicad_sch		
Title:		
Size: B	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.11)		Id: 9/9

SPI CIRCUIT BASED ON MT011 RC2014
https://github.com/markt4311/MT011

U25
74LS163

U28
74LS595

U29
74LS165

U26D
74AHC02

U23C
74ALS10

U23B
74ALS10

U26A
74AHC02

U26B
74AHC02

U23A
74ALS10

U26C
74AHC02

U31
WIZ850IO

JP2
ENET INT

C32
0.1u

U24
74LS138

U27
74HCT175

D8
1N4148

D9
1N4148

D10
1N4148

D11
1N4148

U30
25LCxxx

JP3
MISO

J12
SD_Card

Amphenol Product Number
101-00313-68-02 or Equivalent

U3D
74LS06

U3E
74LS06

J13
ENET INTERRUPT

NOTE: RELIES ON 4700 OHM PULL UP
RESISTOR ON Z80 PROCESSOR BOARD

Sheet: /WIZNET/
File: WIZNET.kicad_sch

Title:

Size: B | Date: | **Rev:**
KiCad E.D.A. kicad (6.0.11) | Id: 11/9