bus

File: bus.kicad_sch

PPIDE

File: PPIDE.kicad_sch

GAL

File: GAL.kicad_sch

IO

File: IO.kicad_sch

power

File: power.kicad_sch

FDC

File: FDC.kicad_sch

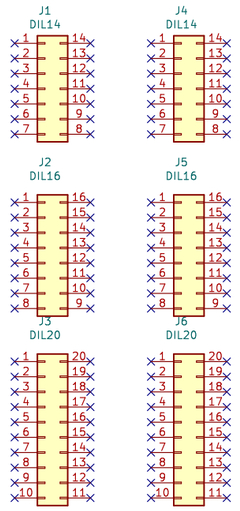
buffers

File: buffers.kicad_sch

SPI

File: SPI.kicad_sch

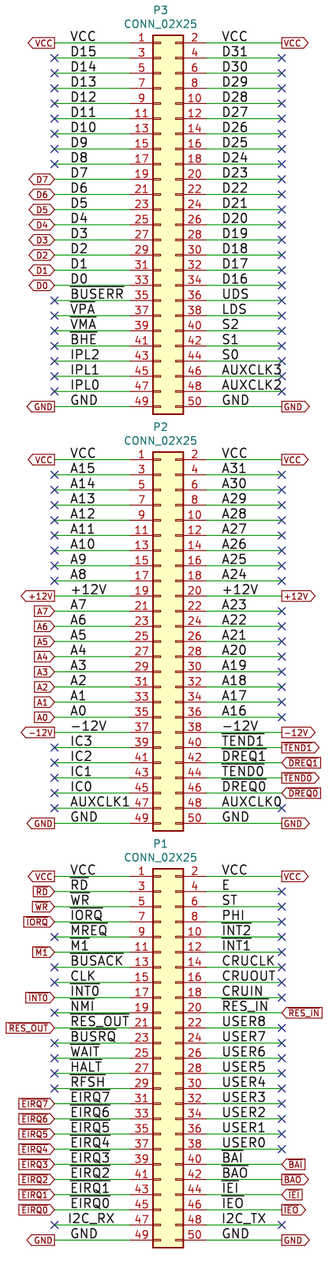
SPARE SOCKETS FOR DEBUGGING



Sheet: /
File: input-output.Disk.kicad_sch

Title:

Size: B	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.11)		Id: 1/9



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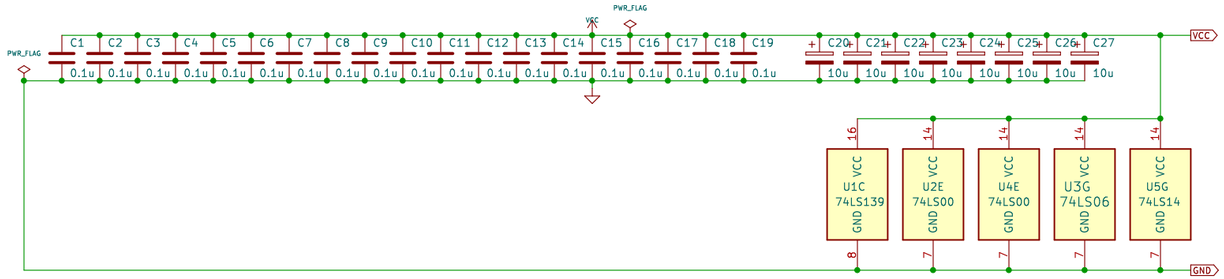
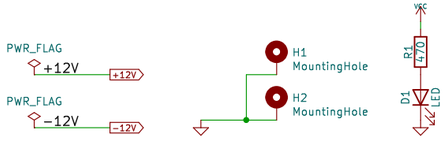
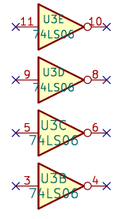
Size: B	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.11)		Id: 2/9





Spare Components



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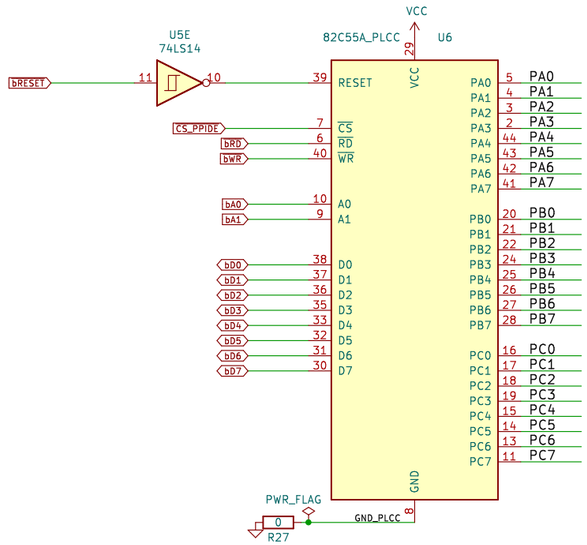
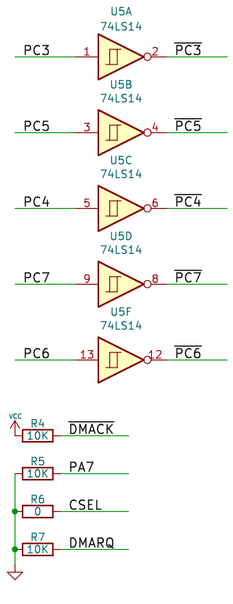
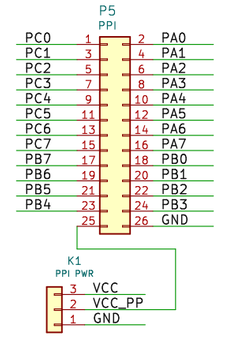
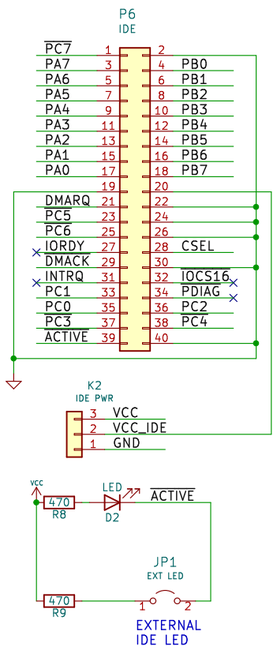
Size: B	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.11)		Id: 3/9









Sheet: /PPIDE/
File: PPIDE.kicad_sch

Title:

Size: B | Date: | **Rev:**

KiCad E.D.A. kicad (6.0.11) | Id: 4/9

FLOPPY DRIVE INTERFACE

IO Ports
x0 read Main Status Register
x1 read/write Data In/Out
x2 read/write Terminal Count
x3 read/write User Reset FDC
x4 <none>
x5 write Load Control Register
x6 read DMA Acknowledge/write Load Operations Register
x7 read DMA Acknowledge and Terminal Count

U7 16 MHz

U9 9.6 MHz

NOTE: U12 OPTIONAL
SECONDARY CLOCK
FOR 150/300 KBPS
DRIVES. USE P5 1-2
CLOSED TO ENABLE;
DEFAULT IS 2-3 CLOSED

P7
FDC CLK
GND

16MHZ-CLK

U8
WD37C65BJM/WD
PLCC

FDC-RESET
FDC-TC
bRD
bWR
MSR-DATA
FDC-DACK
LDOR
LDCR
bD0 bD1 bD2 bD3 bD4 bD5 bD6 bD7
bA0
PCVAL
ZERO

INT_FDC
FDC_DMA

R10 4700
R12 4700

PWR_FLAG
R28 0
GND_PLCC

IBM floppy connector
A: = DS1 (no twist)
B: = DS2 (twist)

P10
FLOPPY

RWC key IDX MO1 DS2 DS1 MO2 DIRC STEP WD WE TR00 WP RDD HS DCHG

RP1 1000
RDD DCHG WP TR00 IDX PCVAL

NOTE: REPLACE RP1 WITH 150 OHM
9 PIN SIP RESISTOR PACK FOR
LEGACY FLOPPY DRIVES; 1000 OHM
FOR 3.5" IBM PC 1.44MB COMPATIBLE

EXTERNAL DMA INTERFACE

PULSE
R13 4700
P8
TEND SEL
TEND0 TEND1

FDC_DMA
U3A 74LS08
R11 4700
RDY
P9
DREQ SEL
DREQ0 DREQ1

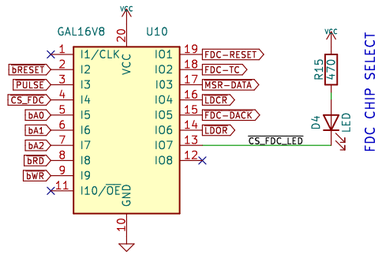
J7
INTERRUPT
INT0 EIRQ0 EIRQ1 EIRQ2 EIRQ3 EIRQ4 EIRQ5 EIRQ6 EIRQ7

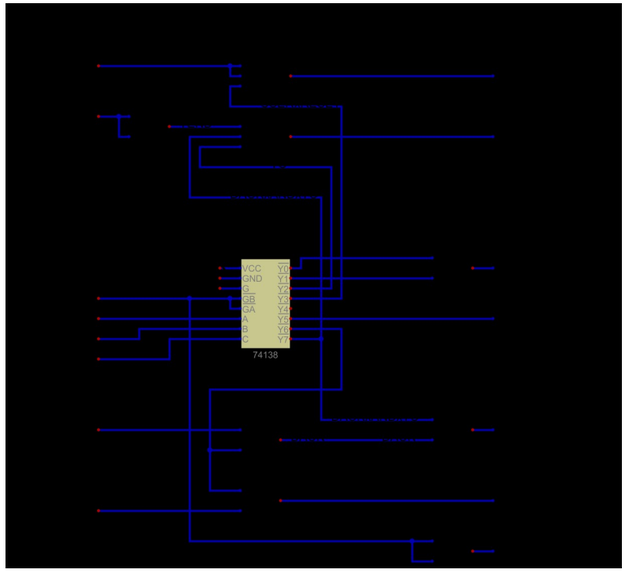
INT_FDC
U3F 74LS08

NOTE: RELIES ON 4700 OHM PULL UP
RESISTOR ON Z80 PROCESSOR BOARD

Sheet: /FDC/
File: FDC.kicad_sch
Title:
Size: B Date: Rev:
KiCad E.D.A. kicad (6.0.11) Id: 5/9

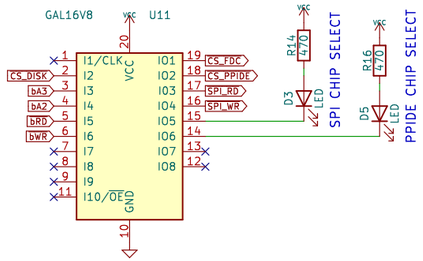
FDC DMA GAL16V8

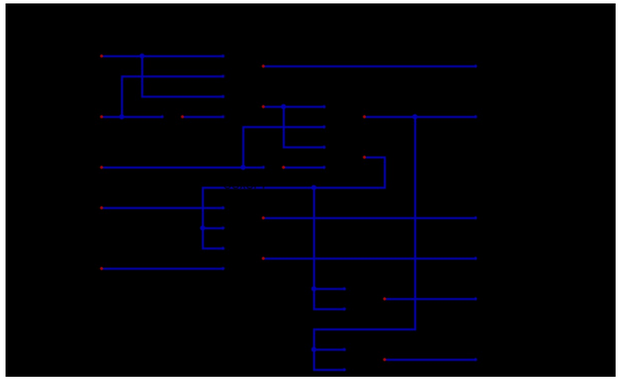




SPARE GAL FOR DEBUGGING

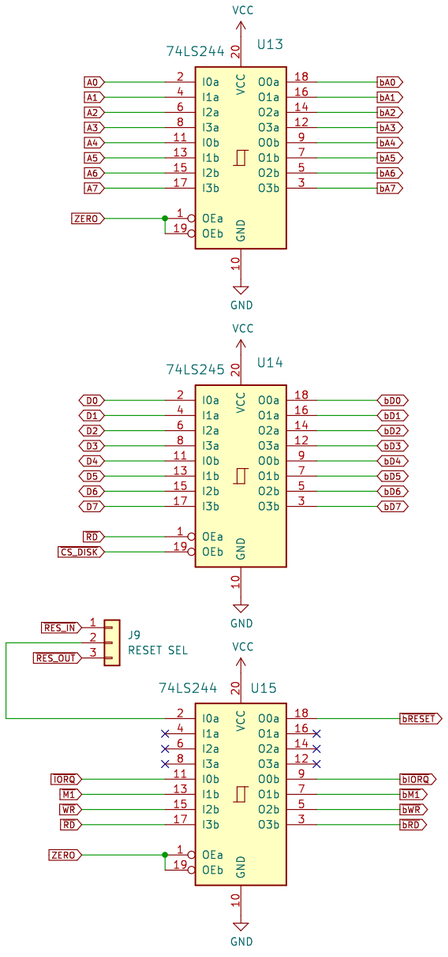
SPI CHIP SELECT / PPIDE CHIP SELECT





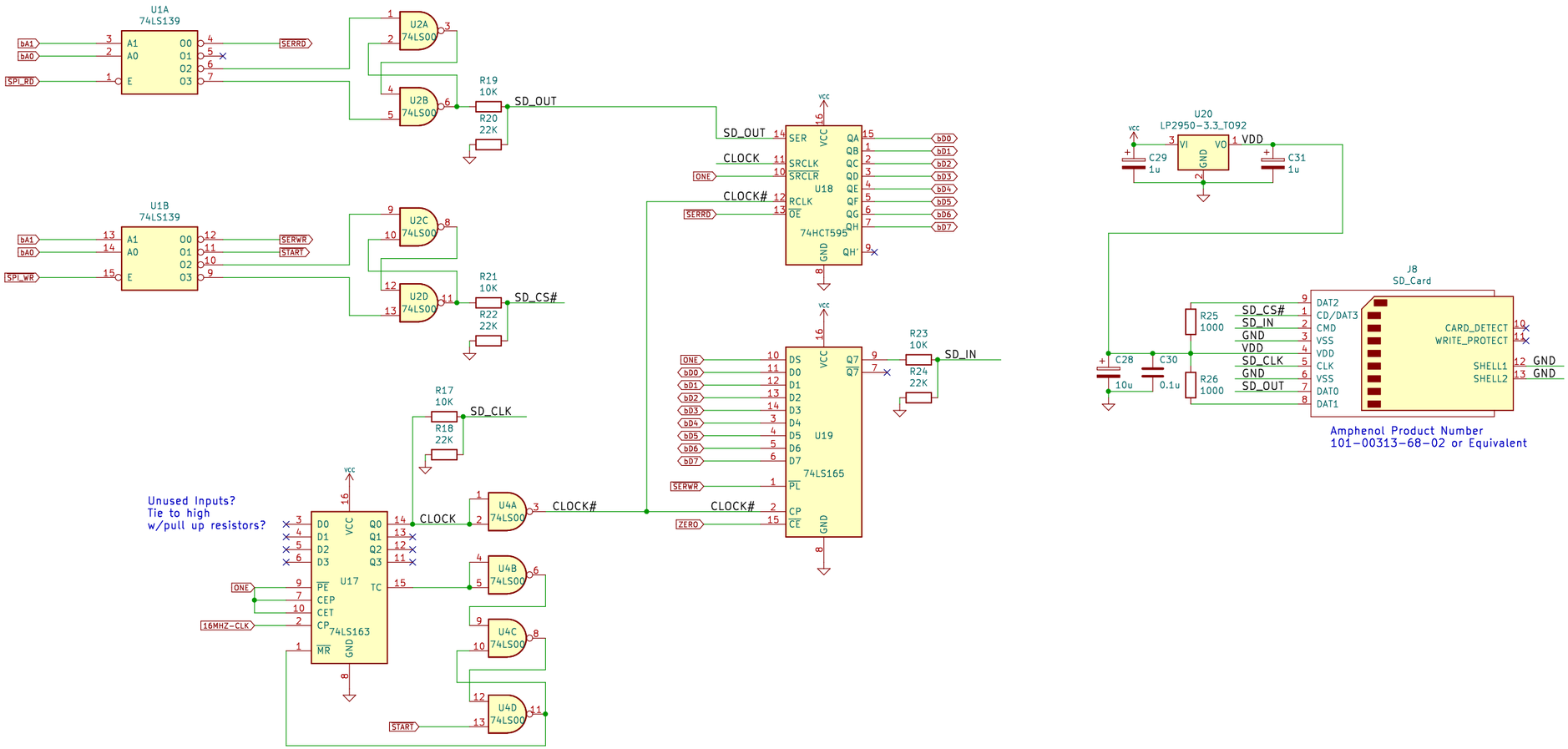
Sheet: /GAL/		
File: GAL.kicad_sch		
Title:		
Size: B	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.11)		Id: 6/9

Z80 BUS INTERFACE

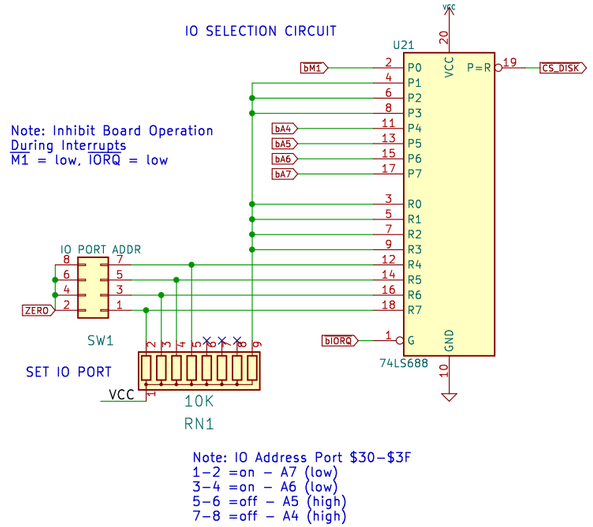


Note: Buffers and Transceivers
respond to IO and MEM cycles

Sheet: /buffers/		
File: buffers.kicad_sch		
Title:		
Size: B	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.11)		Id: 7/9



Sheet: /SPI/	
File: SPI.kicad_sch	
Title:	
Size: B	Date:
KiCad E.D.A. kicad (6.0.11)	Id: 8/9



Note: IO Address Port $30-$3F
1-2 =on - A7 (low)
3-4 =on - A6 (low)
5-6 =off - A5 (high)
7-8 =off - A4 (high)

Sheet: /IO/		
File: IO.kicad_sch		
Title:		
Size: B	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.11)		Id: 9/9