bus

File: bus.kicad_sch

VDC

File: VDC.kicad_sch

GAL

File: GAL.kicad_sch

IO

File: IO.kicad_sch

power

File: power.kicad_sch

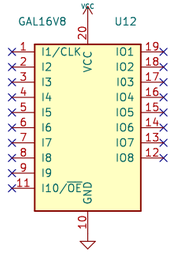
ENET

File: ENET.kicad_sch

buffers

File: buffers.kicad_sch

SPARE GAL FOR DEBUGGING

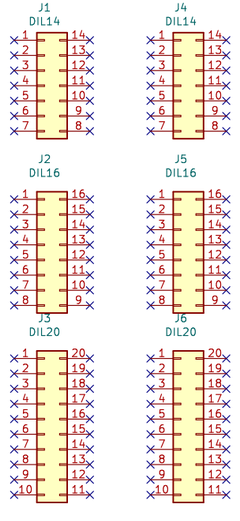


THROUGH HOLES FOR PATCH WIRE ROUTING ACROSS SIDES

H3
MountingHole

H4
MountingHole

SPARE SOCKETS FOR DEBUGGING



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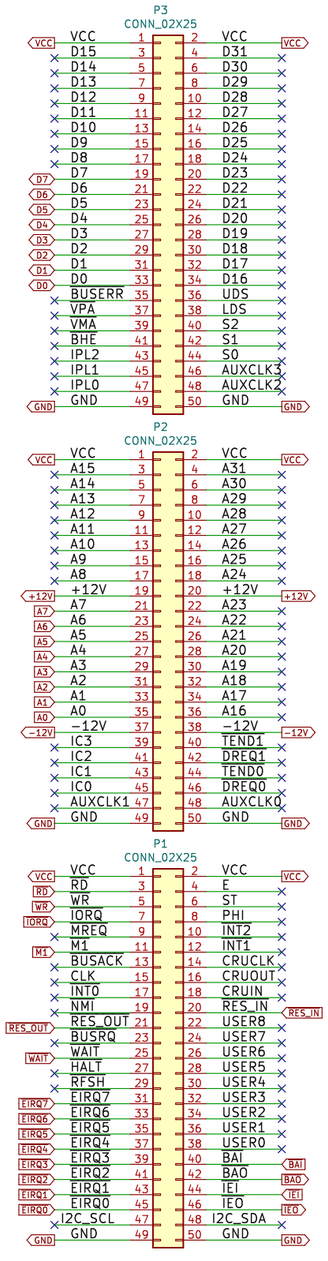
File: input-output.VDCENET.kicad_sch

Title:

Size: B	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.11)		Id: 1/8



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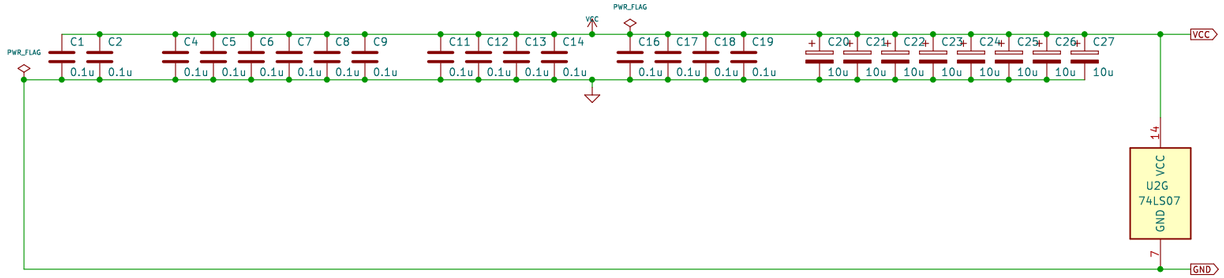
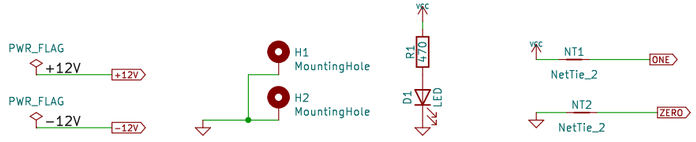
Title:		
Size: B	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.11)		Id: 2/8



Spare Components



Sheet: /power/		
File: power.kicad_sch		
Title:		
Size: B	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.11)		Id: 3/8

NOTE: MOS tech data on 8568 is wrong
and Commodore C128D schematic is
right. Pin 22 is INIT, not RESET#.
Pin 23 is RESET#, not INIT.

COLOR VDU

8568 U7

DD0 DD1 DD2 DD3 DD4 DD5 DD6 DD7

bD0 bD1 bD2 bD3 bD4 bD5 bD6 bD7

CS_VDC bA0 CS_VDC RD

INTR# LP2#

4700 R3

bRESET

DA0 DA1 DA2 DA3 DA4 DA5 DA6 DA7

CAS# RAS# DR-W CCLK ZERO ZERO CV R G B I VSYN HSYN CSYNC DCLK#

C43 0.22u

C44 0.22u

C45 0.22u

U8 41464

U16 41464

ZERO DR-W RAS# CAS#

DRAM chips must be 64Kx4
4464 or 41464

U5 DOT CLK

L1 INDUCTOR

C42 10p

DCLK#

NOTE: Caution, this interface uses much lower dot clock than
nearly all VGA monitors can sync with. Only a few monitors
support low frequency sync (Vizio VA19L HDTV10T & Acer V193HD)

U6 74LS138

MUST BE 74LS OR 74ALS SINCE
ONLY PULL-DOWN IS DESIRED

FIX_BROWN

74LS244 OR 74ACT244
FROM 8568

IOUT ROUT GOUT BOUT

390 R4 390 R5 390 R6 820 R8 820 R10 820 R12 820 R17

VGA-RED VGA-GREEN VGA-BLUE

I CV CSYNC

U2B U2C U2D 74LS07

R7 120 R11 120 R9 100 R13 330 R18 47 R19 82

Q1 2N3904

FB1 Ferrite_Bead_Small

MONOCHROME CVBS

Composite Video Circuit

P6 RGBI TTL

GND GND ROUT GOUT BOUT IOUT CVBS VSYNOUT LP2#

HSYNOUT CSYNOUT K3 RGBI CSYN

P26 connects to DE-9 female CGA
connector with ribbon cable crimp
Connect Pins 1, 2, 3, 5, 6, 7, 8, 9
Composite Video Output on Pin 4
Light Pen Input on Pin 10

P7

VGA-RED VGA-BLUE GND GND VCC GND GND GND GND VGA-CSYNC VGA-HSYNC VGA-GREEN VGA-VSYNC VGA-CSYNC

PIN13 K2

ANALOG RGB

NOTE: P7 FOR VGA
HD15F OPTION

INTR# U2A 74LS07

VDC Interrupt Circuit

J7 EIRQ0 EIRQ1 EIRQ2 EIRQ3 EIRQ4 EIRQ5 EIRQ6 EIRQ7

VDC INTERRUPT

R20 470 D2 LED VDC-LED

U9 74LS244

I B G R HSYN VSYN CSYNC ZERO ZERO ZERO

IOUT BOUT GOUT ROUT HSYNOUT VSYNOUT CSYNOUT

HSYNOUT VSYNOUT

Vertical and Horizontal Sync Circuit

P5 SYNC SELECTORS

SYNC POLARITY

VGA-HSYNC VGA-VSYNC

TO VGA CONNECTOR
(PLUS GROUNDS)

CSYNOUT

Composite Sync Circuit

CSYNC K1

VCC

10K R2 1000 R15 AV 180 R14 120 R16 YS AUDIO

JP2 AUD GND GND

J10 RGB

VGA-RED VGA-GREEN VGA-BLUE CVBS

J11 Composite

GND

Sheet: /VDC/
File: VDC.kicad_sch

Title:

Size: B | Date:

KiCad E.D.A. kicad (6.0.11)

Rev:

Id: 4/8

INTERNAL DECODE TO IO BASE 0300H

C54 0.1u GND

C55 0.1u GND

VCC

U18 RTL8019AS

6	VCC	58	TPIN-
17	VCC	59	TPIN+
47	VCC	46	TPOUT-
57	VCC	45	TPOUT+
70	VCC	65	JP = ONE
89	VCC	64	AUI = ZERO
14	GND	60	LEDBNC
28	GND	61	LED0
44	GND	62	LED1
52	GND	63	LED2
83	GND	4	INT0 = ENET_INT0
86	GND	3	INT1
		2	INT2
		1	INT3
		100	INT4
		99	INT5
		98	INT6
		97	INT7
		51	X2
		50	X1
		76	EECS
		77	EEDO
		78	EEDI
		79	EESK
		32	SMEMWB = ONE
		31	SMEMRB
		35	IOCHRDY
		29	*IORB = bRD
		30	*IOWB = bWR
		33	RSTDRV = bRESET
		34	*AEN = CS_ENET
		96	IOCS16B
		5	A0 = bA0
		7	A1 = bA1
		8	A2 = bA2
		9	A3 = bA3
		10	A4 = bA4
		11	A5
		12	A6
		13	A7 = ZERO
		15	A8
		16	A9 = ONE
		18	A10
		19	A11
		20	A12
		21	A13
		22	A14
		23	A15
		24	A16
		25	A17
		26	A18
		27	A19 = ZERO
		36	D0 = bD0
		37	D1 = bD1
		38	D2 = bD2
		39	D3 = bD3
		40	D4 = bD4
		41	D5 = bD5
		42	D6 = bD6
		43	D7 = bD7
		95	D8
		94	D9
		93	D10
		92	D11
		91	D12
		90	D13
		88	D14
		87	D15

NOTE: 1%

R24 200

P8 HR911105A

6	RD-	LED_GREEN_P	9
3	RD+	LED_GREEN_M	10
2	TD-	LED_YELLOW_P	12
1	TD+	LED_YELLOW_M	11
4	P4	NC	7
5	P5	Shell	SH
GND		Shell	SH

R26 1000 VCC

R27 1000

C58 0.01u

C59 0.01u

FB2 Ferrite_Bead_Small

SH GND

D6 LED

R25 1000 VCC

R21 470 VCC

D3 LED ENET_LED

JP1 WAIT EN

WAIT 1 2

U2F 74LS07 12 13

NOTE: WAIT# RELIES ON
4700 PULL UP RESISTOR
ON PROCESSOR BOARD

R22 27K

X1 20MHz

R23 1M

C56 10p

C57 10p

U19 93CxxC

1	CS	SCLK	2
6	ORG	DI	3
5	GND	DO	4
8	VCC		

NOTE: USE AT93C46C
64X16 BIT

U2E 74LS07 11 10

ENET_INT0

J8 ENET INTERRUPT

1		2	EIRQ0
3		4	EIRQ1
5		6	EIRQ2
7		8	EIRQ3
9		10	EIRQ4
11		12	EIRQ5
13		14	EIRQ6
15		16	EIRQ7

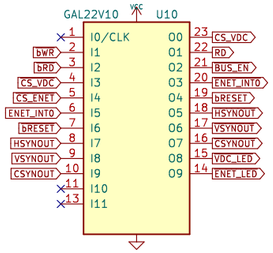
NOTE: INT0 RELIES ON
4700 PULL UP RESISTOR
ON PROCESSOR BOARD

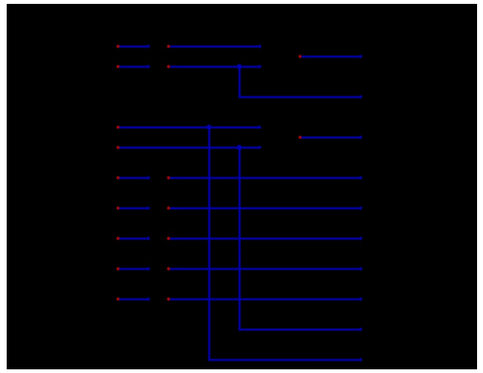
Sheet: /ENET/
File: ENET.kicad_sch

Title:

Size: B | Date: | **Rev:**
KiCad E.D.A. kicad (6.0.11) | Id: 5/8

VDCENET CS GAL22V10



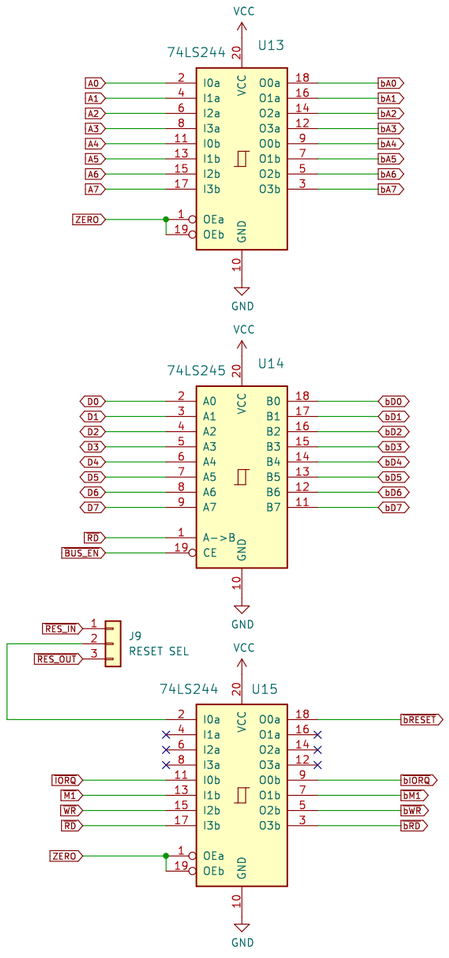


Sheet: /GAL/
File: GAL.kicad_sch

Title:

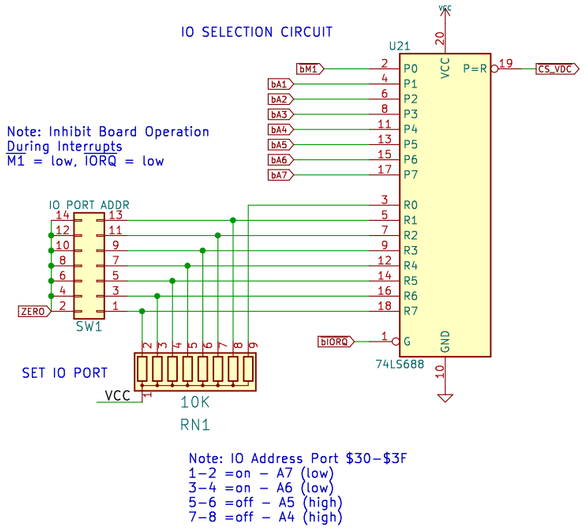
Size: B	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.11)		Id: 6/8

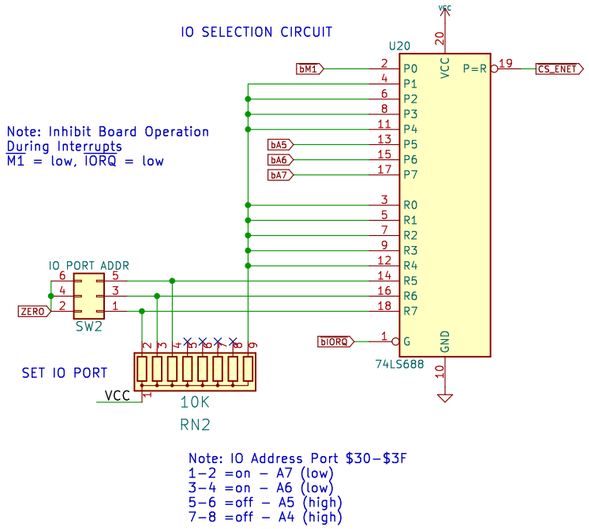
Z80 BUS INTERFACE



Note: Buffers and Transceivers
respond to IO and MEM cycles

Sheet: /buffers/		
File: buffers.kicad_sch		
Title:		
Size: B	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.11)		Id: 7/8





Sheet: /IO/		
File: IO.kicad_sch		
Title:		
Size: B	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.11)		Id: 9/8