bus

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power

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buffers

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fpanel

File: fpanel.kicad_sch

Z80CPU

File: Z80CPU.kicad_sch

DMA

File: DMA.kicad_sch

GALS

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IM2

File: IM2.kicad_sch

waitstate

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mapper

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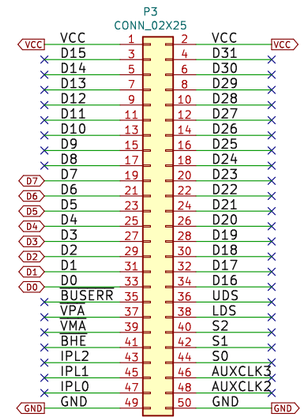

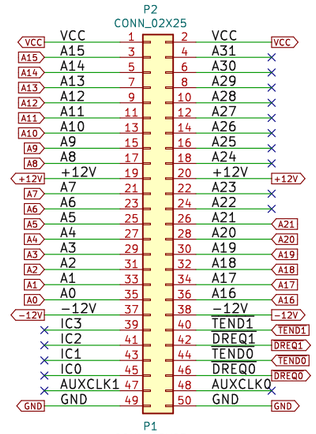

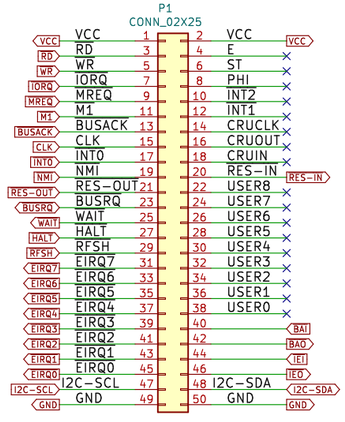

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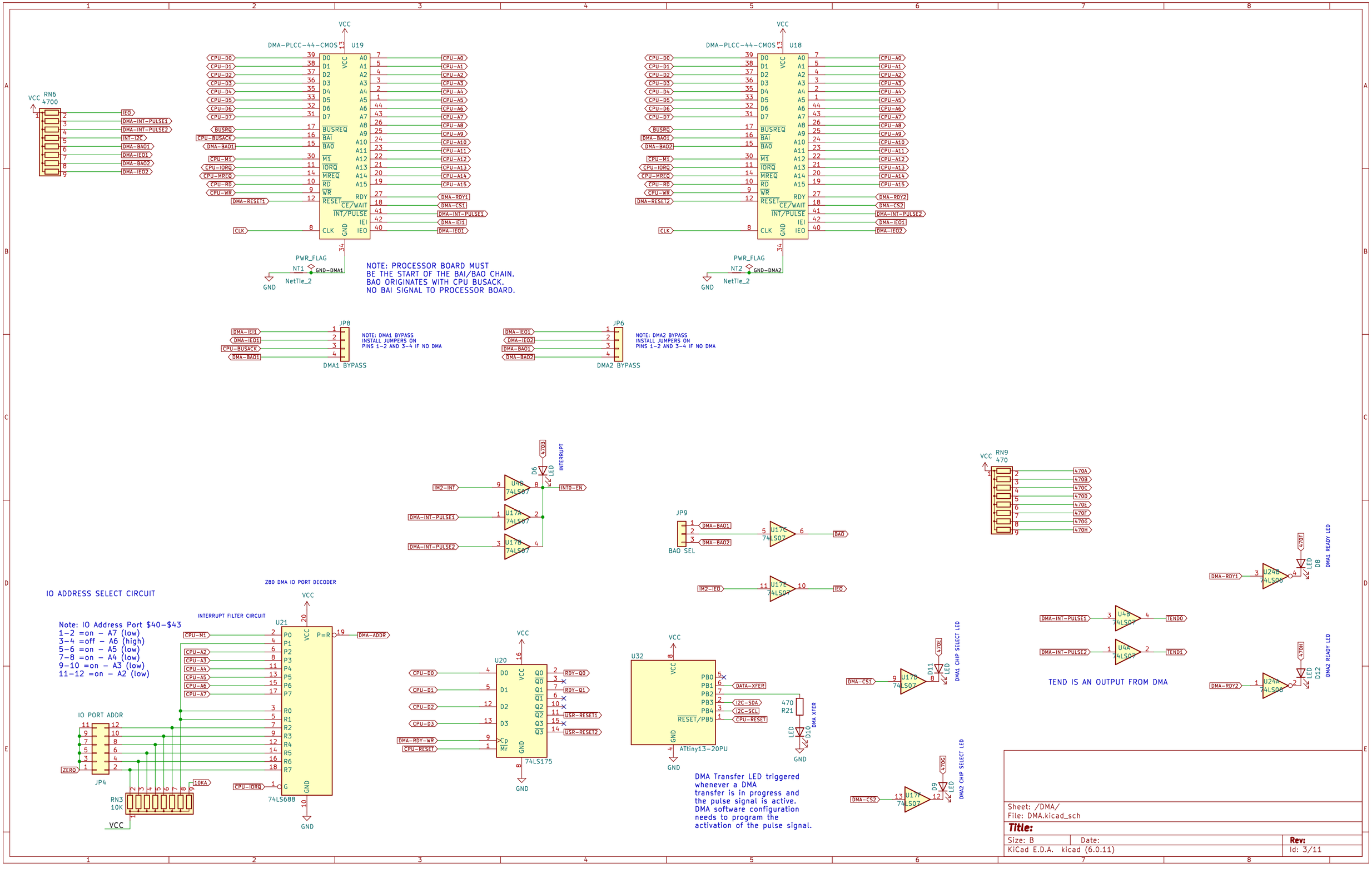

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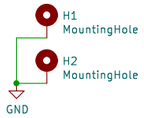
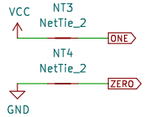
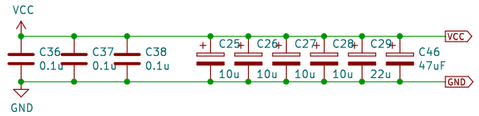
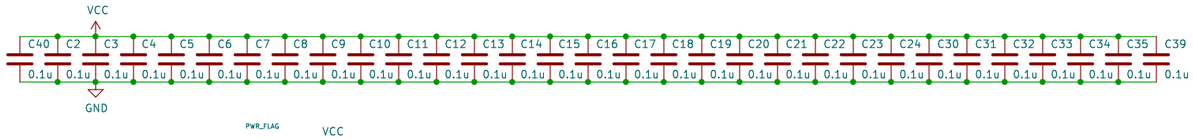
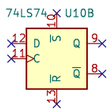


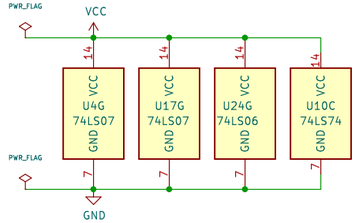






SPARE GATES





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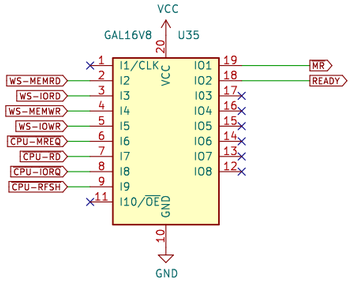
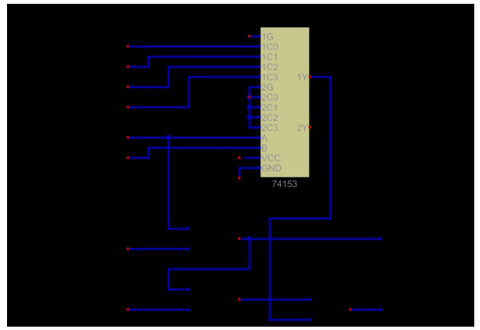
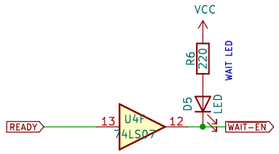
KiCad E.D.A. kicad (6.0.11)		Id: 4/11

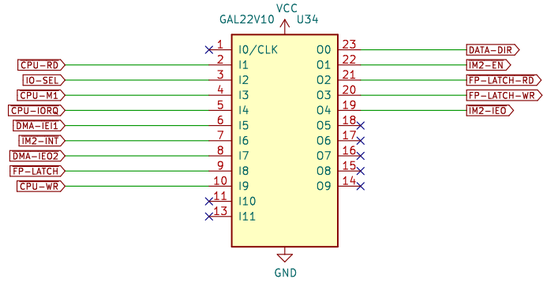
CPU WS GAL16V8

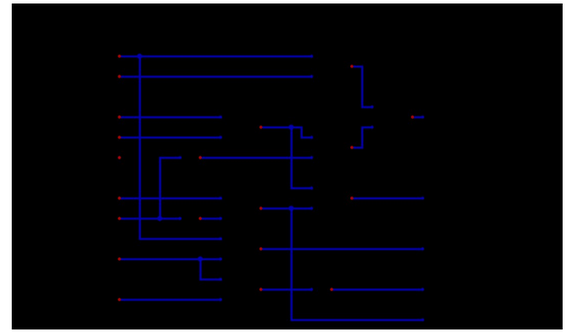




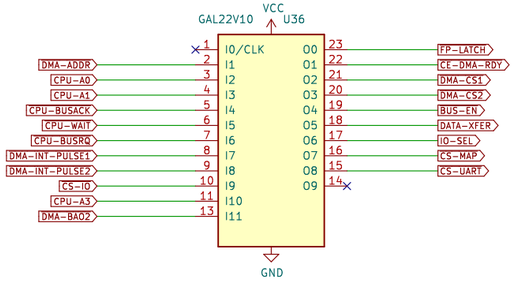


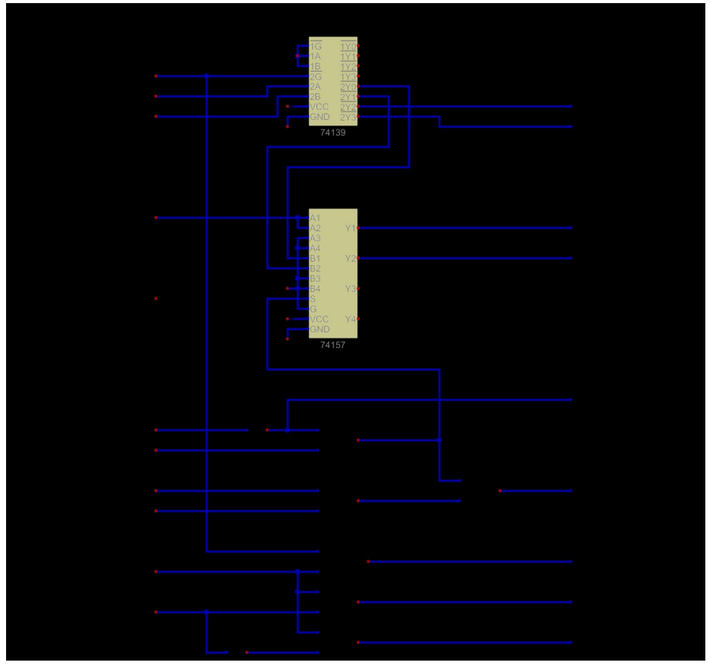
CPU DATA DIR V3 GAL22V10



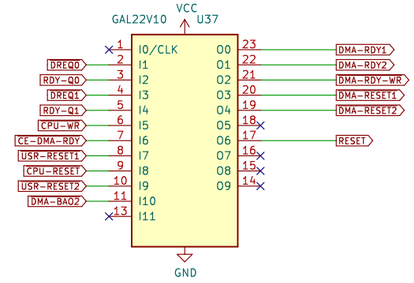


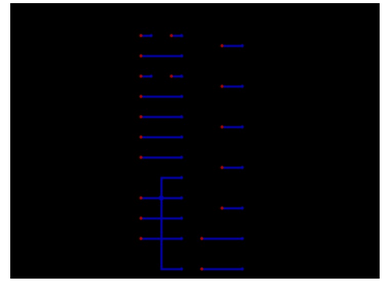
DMA CS V4 GAL22V10





DMA RDY GAL22V10





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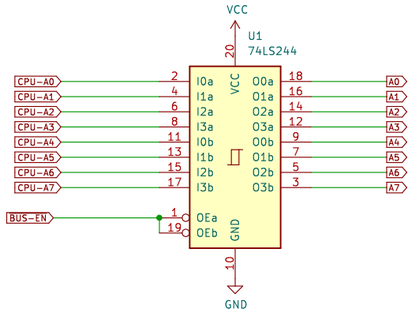
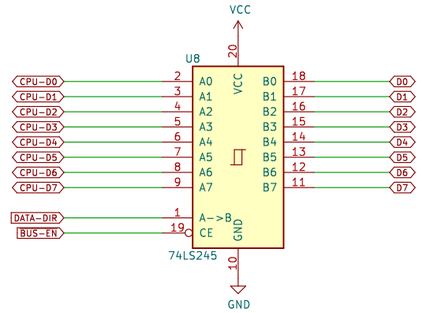
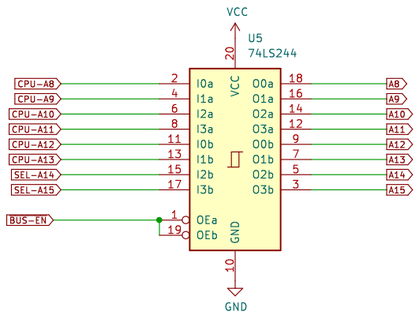
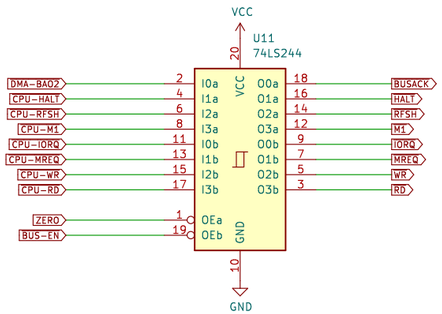
KiCad E.D.A. kicad (6.0.11)		Id: 5/11

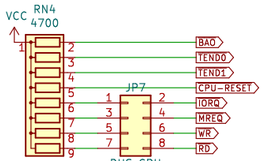
Z80 BUS INTERFACE

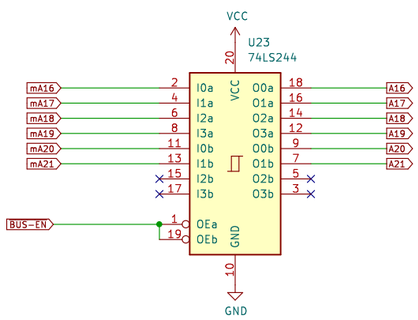


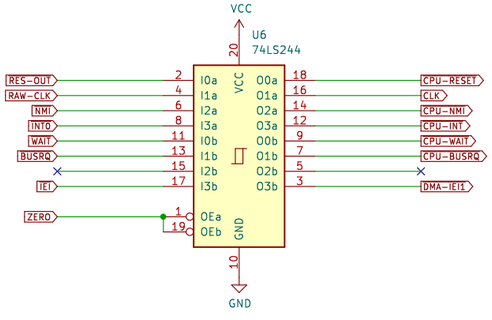


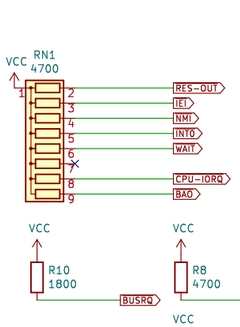


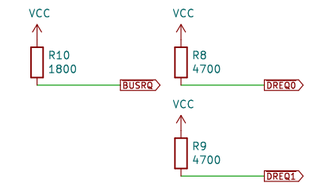












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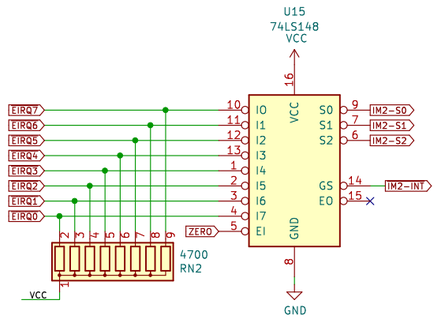
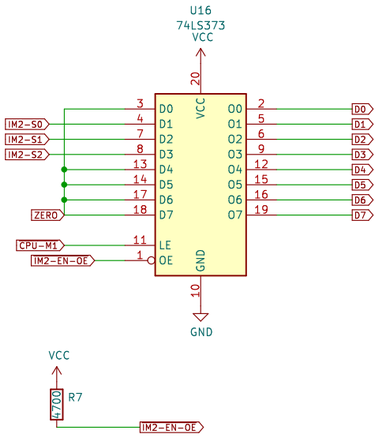
KiCad E.D.A. kicad (6.0.11) | Id: 6/11

Interrupt Mode 2 (IM2) Circuit





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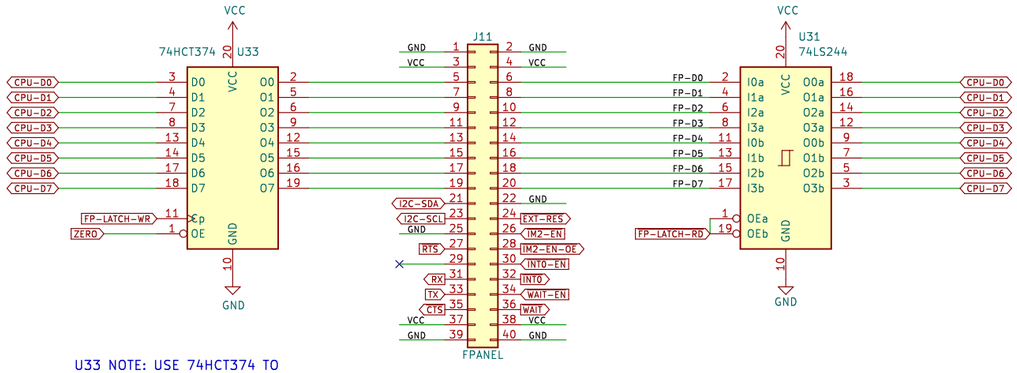
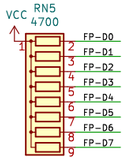
FRONT PANEL LED OUTPUT



U33 NOTE: USE 74HCT374 TO SOURCE OR SINK ADEQUATE CURRENT TO DRIVE LEDS ON FRONT PANEL

FRONT PANEL SWITCH INPUT



J11 NOTE:

PINS 5, 7, 9, 11, 13, 15, 17, 19 ARE FOR LED STATUS FOR ROMWBW FRONT PANEL INDICATOR

PINS 6, 8, 10, 12, 14, 16, 18, 20 ARE FOR SWITCH INPUTS FOR ROMWBW FRONT PANEL

PINS 21, 23 ARE FOR I2C CONNECTION (SDA & SCL)

PINS 25, 27, 29, 31, 33, AND 35 ARE FOR TTL SERIAL CONNECTOR TO UART

PINS 29, 37 ARE FOR SERIAL VCC POWER ENABLE

PINS 22, 24 ARE FOR EXTERNAL RESET SWITCH

PINS 26, 28 ARE FOR IM2 CIRCUIT ENABLE

PINS 30, 32 ARE FOR INTERRUPT 0 ENABLE

PINS 34, 36 ARE FOR WAIT STATE CIRCUIT ENABLE

Sheet: /fpanel/
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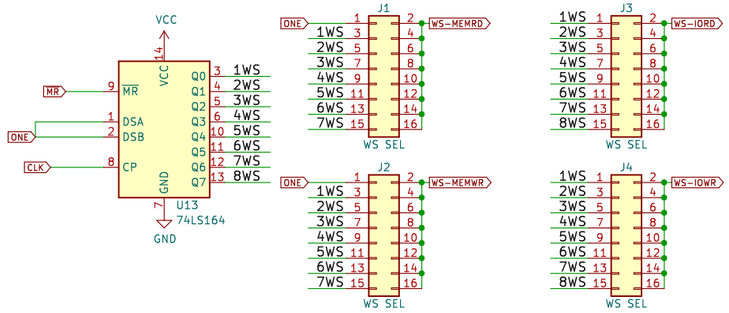
Size: B	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.11)		Id: 8/11

Wait State Generator Circuit



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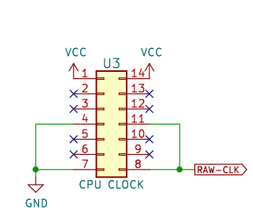
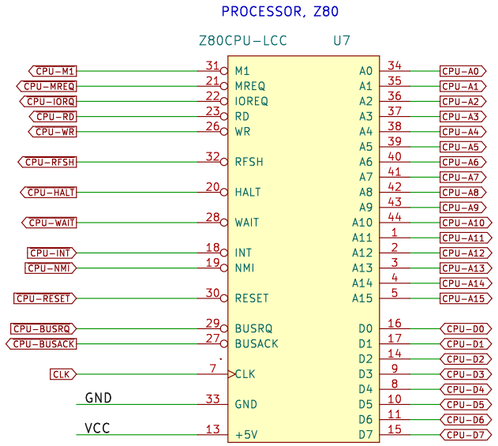
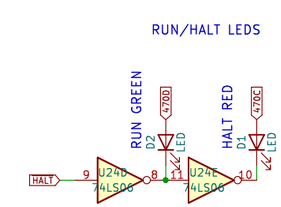
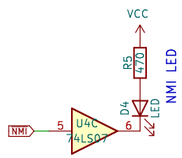
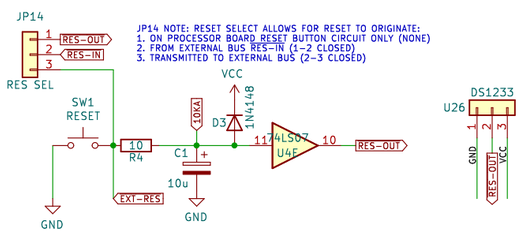






Tri-state address, data, & control bus during DMA





Reset Button Circuit

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Size: B	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.11)		Id: 10/11

CPU MAPPER V3 GAL22V10

IO ADDRESS SELECT CIRCUIT

Z80 MEMORY MAPPER AND
EXPANSION IO PORT DECODER

INTERRUPT FILTER CIRCUIT

Note: IO Address Port $50-$5F
1-2 =on - A7 (low)
3-4 =off - A6 (high)
5-6 =on - A5 (low)
7-8 =off - A4 (high)

IO_PORT ADDR

JP10

RN8
10K

U12
74LS688

MEMORY PAGING SRAMS

74LS670 U9

74LS670 U22

U10A
74LS74

UPPER ADDRESS LINES
PULL-DOWN RESISTORS

RN7
470

U28
ATtiny13-20PU

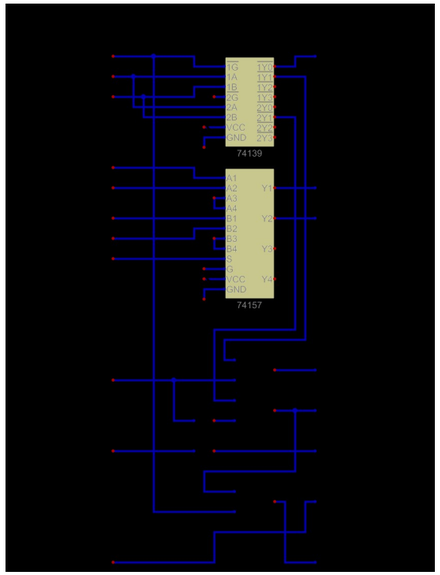
OPTIONAL SYSTEM
TICK TIMER

R11
1000

Q1
2N3904

J6
TICK INTERRUPT

U25
GAL22V10



PCF8584 U27

R2
10K

R3
10K

1.8432 OR 7.3728 MHz
TTL OSCILLATOR

U2
UART CLOCK

TL16C550CFN U14

J12
I2C INTERRUPT

U24F
74LS08

NOTE: INTERRUPTS RELY ON 4700
OHM PULL UP RESISTOR ON PROCESSOR

J5
UART INTERRUPT

U24E
74LS08

R1
4700

Sheet: /mapper/	
File: mapper.kicad_sch	
Title:	
Size: B	Date:
KiCad E.D.A. kicad (6.0.11)	**Rev:** Id: 11/11