bus

File: bus.kicad_sch

power

File: power.kicad_sch

buffers

File: buffers.kicad_sch

TMS9995CPU

File: TMS9995CPU.kicad_sch

GALS

File: GALS.kicad_sch

bus sharing

File: bussharing.kicad_sch

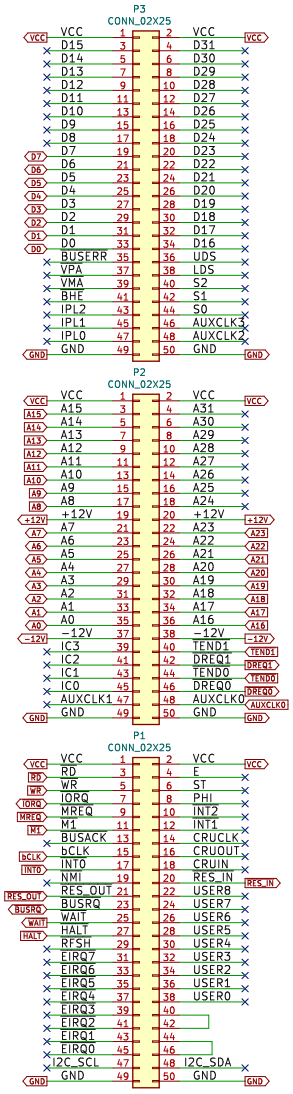
IO

File: io.kicad_sch

Sheet: /
File: processor.tms9995.kicad_sch

Title: Duodyne TMS9995 CPU board

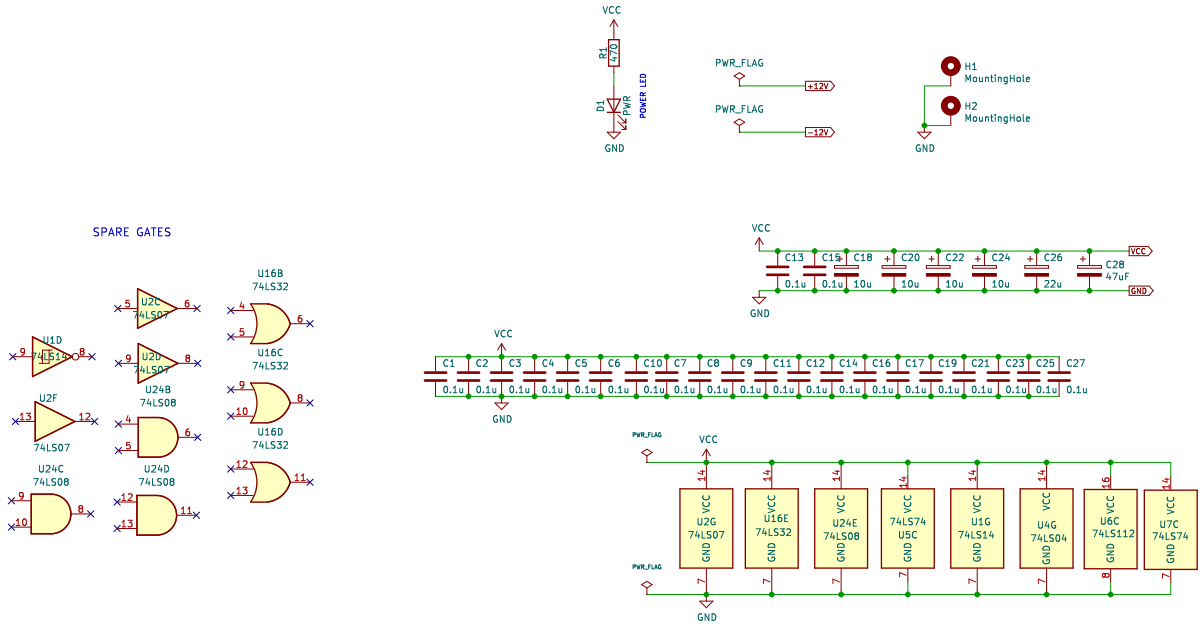
Size: B	Date: 2023-12-16	**Rev: V1.0**
KiCad E.D.A. kicad (6.0.11)		Id: 1/8



Sheet: /bus/
File: bus.kicad_sch

Title: Duodyne TMS9995 CPU board

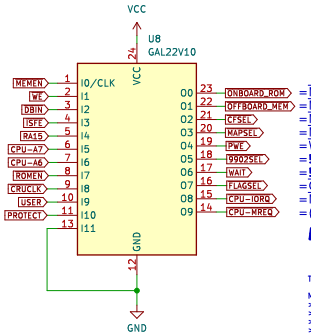
Size: B	Date: 2023-12-16	**Rev: V1.0**
KiCad E.D.A. kicad (6.0.11)		Id: 2/8



Sheet: /power/
File: power.kicad_sch

Title: Duodyne TMS9995 CPU board

Size: B	Date: 2023-12-16	**Rev: V1.0**
KiCad E.D.A. kicad (6.0.11)		Id: 4/8



=MEMEN+ROMEN+RA15
=MEMEN+(!ROMEN*!RA15*WE) + (!ISFE * RA15)
=MEMEN+ISFE+!RA15+CPU-A7+CPU-A6+USER
=MEMEN+ISFE+!RA15+CPU-A7+!CPU-A6+USER
=WE+(PROTECT*USER)
=!MEMEN+ISFE+RA15+CPU-A7+CPU-A6+USER
=!ROMSEL+!CFSEL
=CRUCLK+ISFE+RA15+CPU-A7+!CPU-A6
=MEMEN+ISFE+!CFSEL+!MAPSEL+!9902SEL+USER+!RA15
=(!ISFE * RA15)+OFFBOARD_MEM

Equation ('+' is 'OR', '*' is 'AND')

The memory map is shown in the table below.

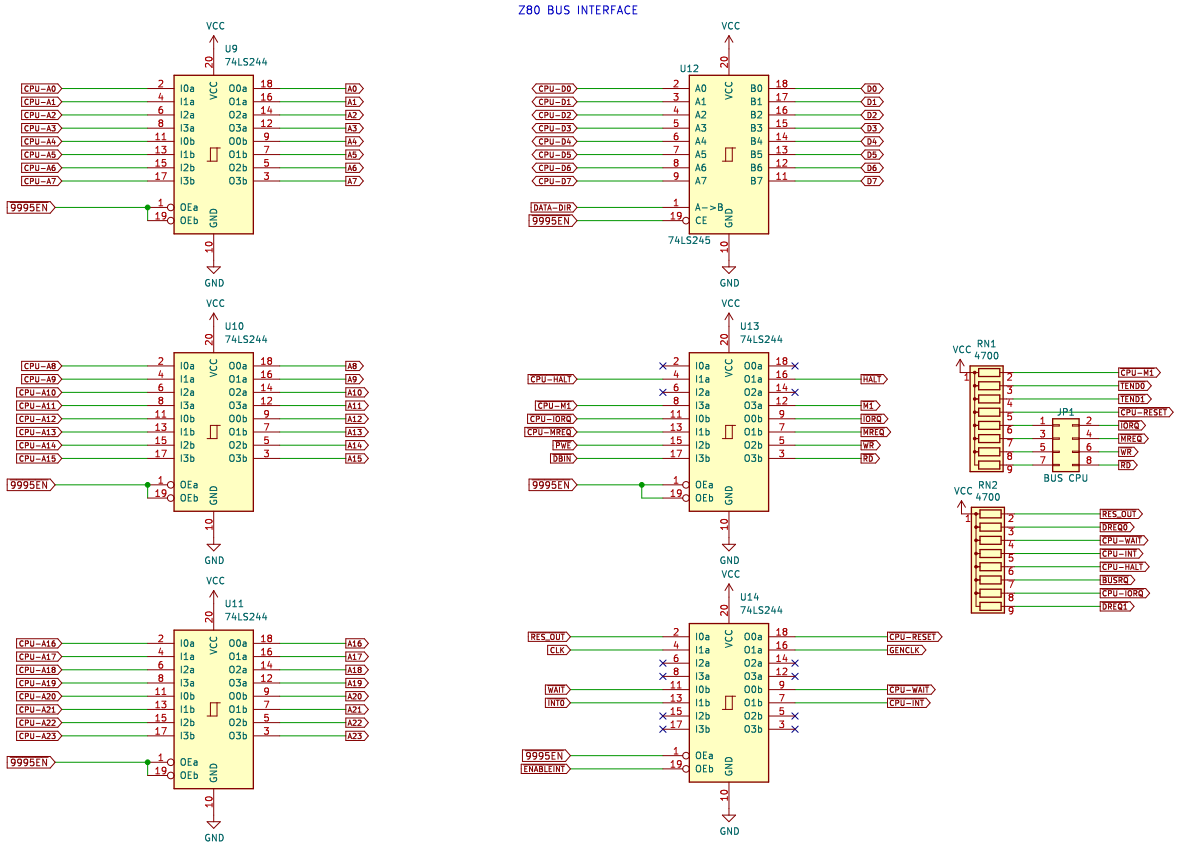
Memory Address	Mapped To
>0000 – >7FFF	ROM when enabled, otherwise RAM
>8000 – >EFFF	RAM
>F000 – >F0FB	TMS 9995 Internal RAM
>F0FC – >F0FF	RAM
>FE00 – >FE3F	CF card ATA registers (FIX INCOMPLETE DECODING WITH NEXT REVISION)
>FE40 – >FE7F	Memory mapper registers 0–15 (>FE40 – >FE4F, repeats at >FE50 etc. . . FIX INCOMPLETE DECODING WITH NEXT REVISION)
>FE80 – >FEBF	Offboard IO (ports $80–$FF)
>FFF0 – >FFF9	RAM
>FFFA – >FFFF	TMS 9995 Internal RAM

CRU Address	Mapped To
>0000 – >003F	TMS 9902 registers
>0040 – >007F	Control signal latch (further details here)
	(Plus processor internal CRU bits)

Sheet: /GALS/
File: GALS.kicad_sch

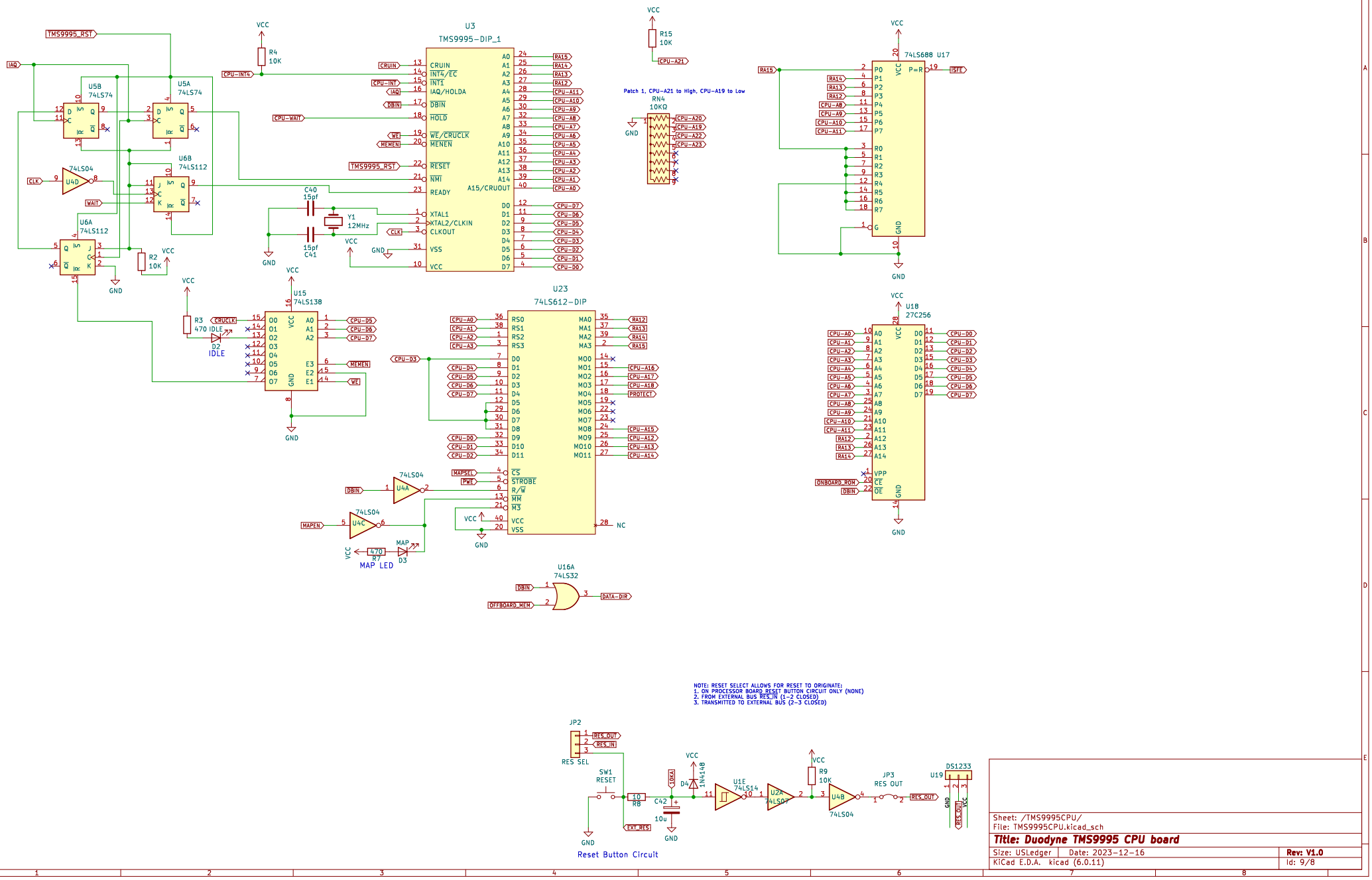
Title: Duodyne TMS9995 CPU board

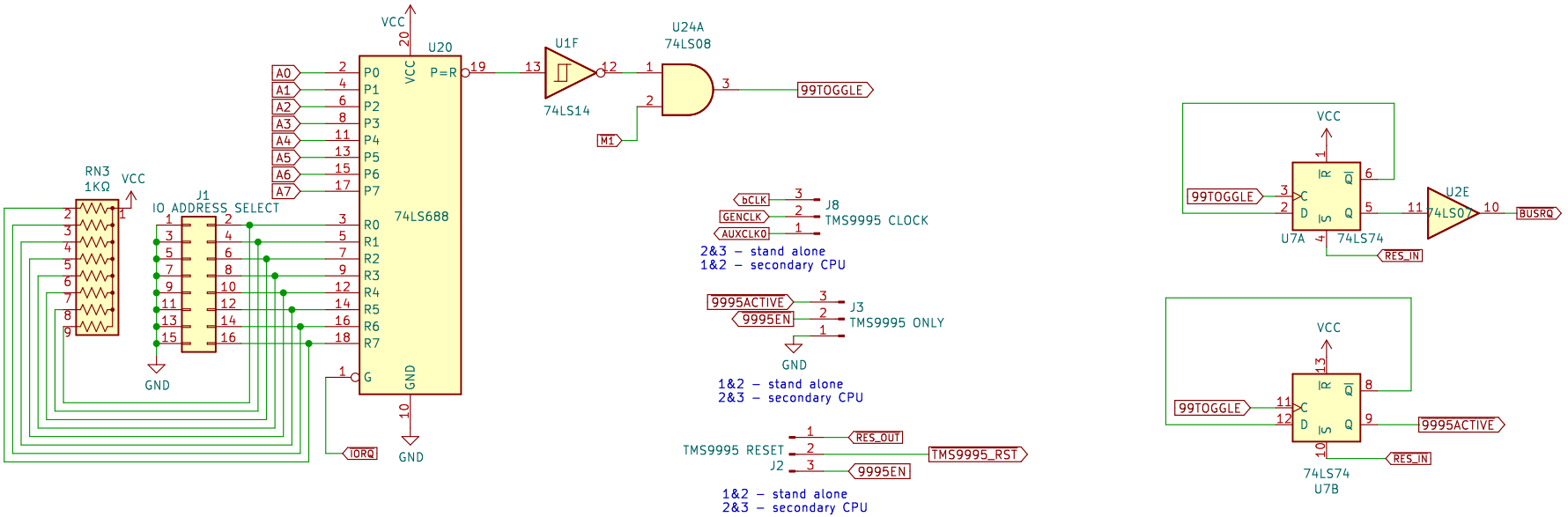
Size: B	Date: 2023-12-16	**Rev: V1.0**
KiCad E.D.A. kicad (6.0.11)		Id: 5/8



Sheet: /buffers/	
File: buffers.kicad_sch	
Title: Duodyne TMS9995 CPU board	
Size: B	Date: 2023-12-16
KiCad E.D.A. kicad (6.0.11)	Id: 6/8

Rev: V1.0

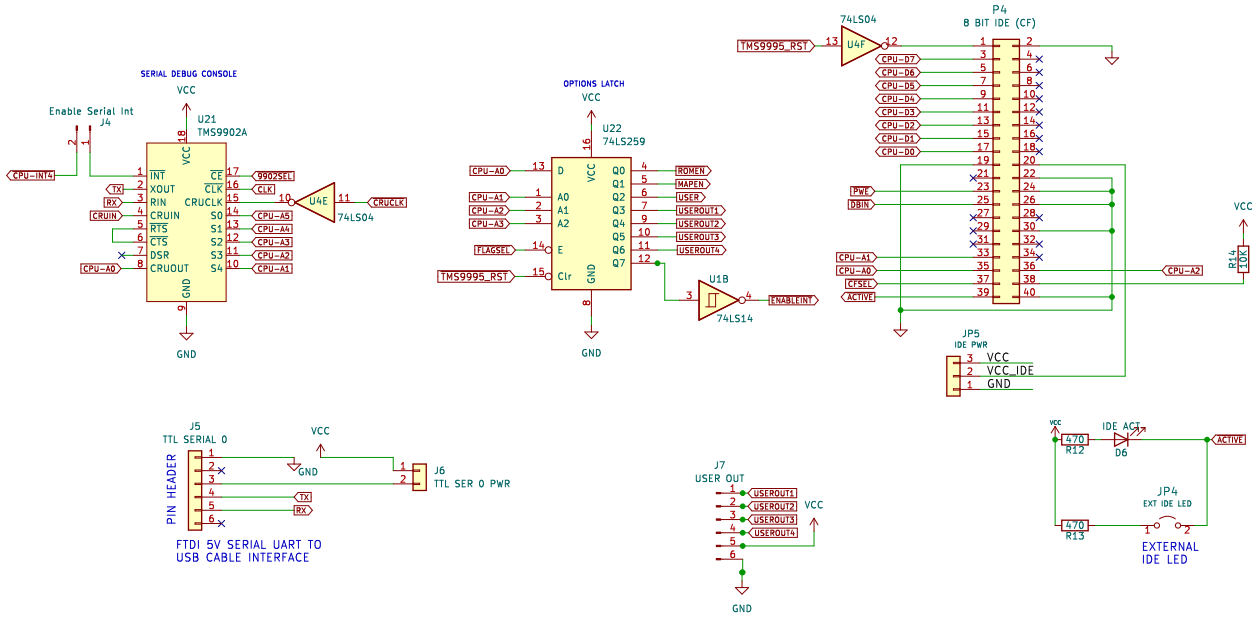

TMS9995_RST
IAQ
U5B
74LS74
U5A
74LS74
U6B
74LS112
U6A
74LS112
74LS04
U4D
CLK
WAIT
R2
10K
R4
10K
U3
TMS9995-DIP_1
CRUIN
INT4/EC
INT1
IAQ/HOLDA
DBIN
HOLD
WE/CRUCLK
MEMEN
RESET
NMI
READY
XTAL1
XTAL2/CLKIN
CLKOUT
VSS
VCC
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15/CRUOUT
D0
D1
D2
D3
D4
D5
D6
D7
CPU-INT4
CPU-INT
CPU-WAIT
C40
15pf
Y1
12MHz
C41
15pf
R15
10K
CPU-A21
Patch 1, CPU-A21 to High, CPU-A19 to Low
RN4
10KΩ
CPU-A20
CPU-A19
CPU-A22
CPU-A23
74LS688 U17
P=R
ISFE
U15
74LS138
R3
470
IDLE
D2
IDLE
CRUCLK
MEMEN
WE
U23
74LS612-DIP
RS0
RS1
RS2
RS3
MA0
MA1
MA2
MA3
MO0
MO1
MO2
MO3
MO4
MO5
MO6
MO7
MO8
MO9
MO10
MO11
CS
STROBE
R/W
MM
M3
NC
MAPSEL
PWT
MAPEN
74LS04
U4A
U4C
R7
470
MAP
D3
MAP LED
U18
27C256
VPP
CE
OE
ONBOARD_ROM
U16A
74LS32
OFFBOARD_MEM
DATA-DIR
NOTE: RESET SELECT ALLOWS FOR RESET TO ORIGINATE:
1. ON PROCESSOR BOARD RESET BUTTON CIRCUIT ONLY (NONE)
2. FROM EXTERNAL BUS RES_IN (1-2 CLOSED)
3. TRANSMITTED TO EXTERNAL BUS (2-3 CLOSED)
JP2
RES SEL
RES_OUT
RES_IN
SW1
RESET
R8
10
C42
10u
EXT_RES
D4
1N4148
U1E
74LS14
U2A
74LS02
U4B
74LS04
R9
10K
JP3
RES OUT
U19
DS1233
GND
RES_OUT
VCC
Reset Button Circuit
Sheet: /TMS9995CPU/
File: TMS9995CPU.kicad_sch
Title: Duodyne TMS9995 CPU board
Size: USLedger
Date: 2023-12-16
Rev: V1.0
KiCad E.D.A. kicad (6.0.11)
Id: 9/8



Sheet: /bus sharing/
File: bussharing.kicad_sch

Title: Duodyne TMS9995 CPU board

Size: A4	Date: 2023-12-16	**Rev: V1.0**
KiCad E.D.A. kicad (6.0.11)		Id: 9/8



Sheet: /IO/	
File: io.kicad_sch	
Title: Duodyne TMS9995 CPU board	
Size: B	Date: 2023-12-16
KiCad E.D.A. kicad (6.0.11)	Id: 11/8
	Rev: V1.0