bus

File: bus.kicad_sch

power

File: power.kicad_sch

buffers

File: buffers.kicad_sch

fpanel

File: fpanel.kicad_sch

Z80CPU

File: Z80CPU.kicad_sch

DMA

File: DMA.kicad_sch

GALS

File: GALS.kicad_sch

IM2

File: IM2.kicad_sch

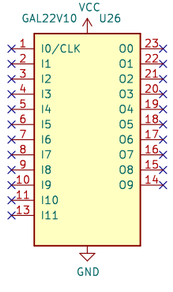
waitstate

File: waitstate.kicad_sch

mapper

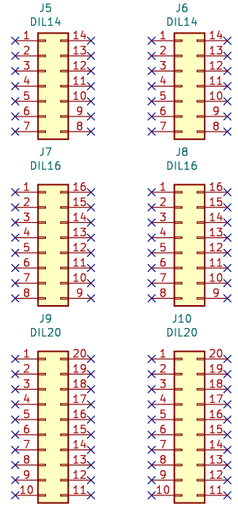
File: mapper.kicad_sch

SPARE GAL FOR DEBUGGING



THROUGH HOLES FOR PATCH WIRE ROUTING ACROSS SIDES

SPARE SOCKETS FOR DEBUGGING



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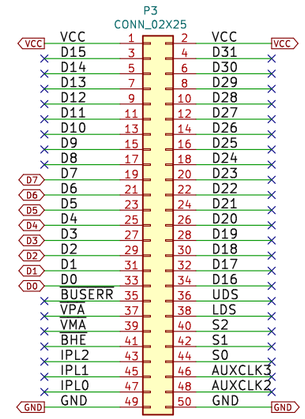
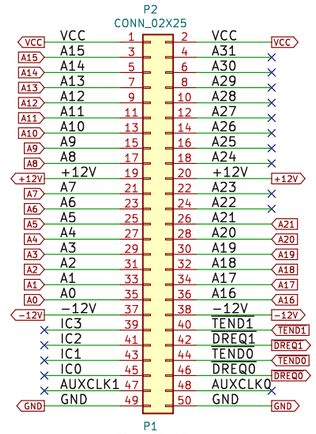
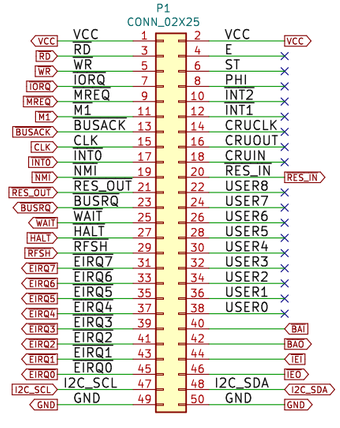
Size: B	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.11)		Id: 1/11







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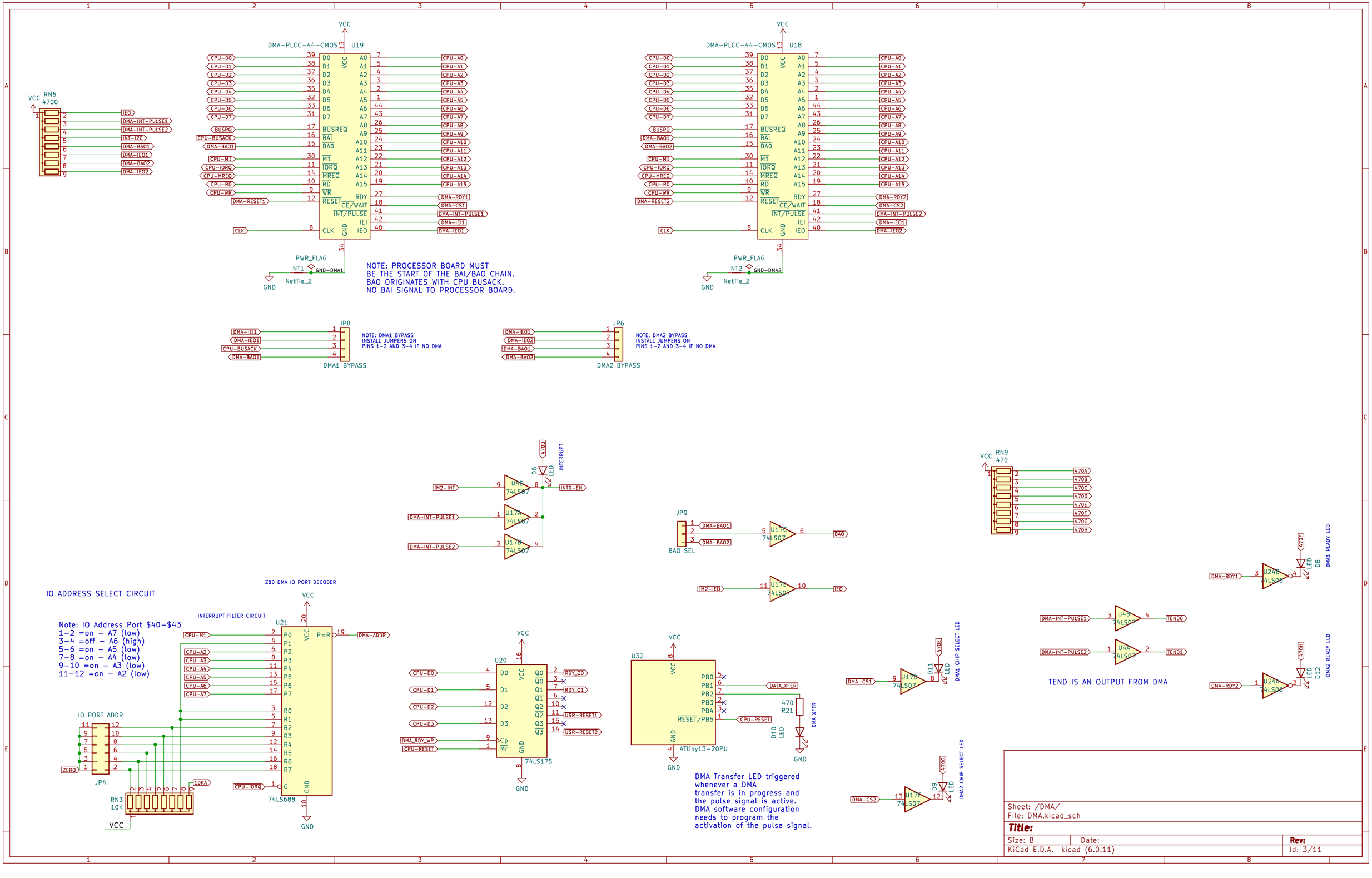
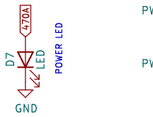
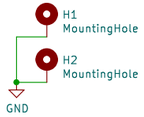
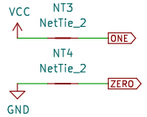
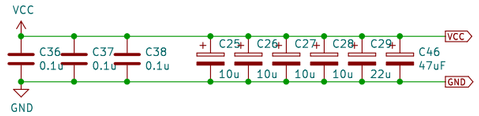
KiCad E.D.A. kicad (6.0.11) | Id: 2/11

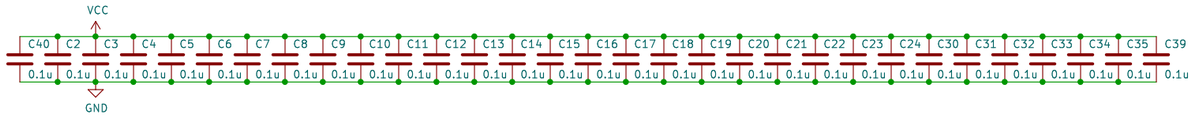

DMA-PLCC-44-CMOS
U19
U18
VCC
GND
CPU-D0
CPU-D1
CPU-D2
CPU-D3
CPU-D4
CPU-D5
CPU-D6
CPU-D7
CPU-A0
CPU-A1
CPU-A2
CPU-A3
CPU-A4
CPU-A5
CPU-A6
CPU-A7
CPU-A8
CPU-A9
CPU-A10
CPU-A11
CPU-A12
CPU-A13
CPU-A14
CPU-A15
BUSRQ
CPU-BUSACK
DMA-BAO1
DMA-BAO2
CPU-M1
CPU-IORQ
CPU-MREQ
CPU-RD
CPU-WR
DMA-RESET1
DMA-RESET2
CLK
DMA-RDY1
DMA-RDY2
DMA-CS1
DMA-CS2
DMA-INT-PULSE1
DMA-INT-PULSE2
DMA-IEI1
DMA-IEI2
DMA-IEO1
DMA-IEO2
RN6
4700
INT-I2C
PWR_FLAG
GND-DMA1
GND-DMA2
NetTie_2
NOTE: PROCESSOR BOARD MUST
BE THE START OF THE BAI/BAO CHAIN.
BAO ORIGINATES WITH CPU BUSACK.
NO BAI SIGNAL TO PROCESSOR BOARD.
JP8
DMA1 BYPASS
NOTE: DMA1 BYPASS
INSTALL JUMPERS ON
PINS 1-2 AND 3-4 IF NO DMA
JP6
DMA2 BYPASS
NOTE: DMA2 BYPASS
INSTALL JUMPERS ON
PINS 1-2 AND 3-4 IF NO DMA
IO ADDRESS SELECT CIRCUIT
Z80 DMA IO PORT DECODER
INTERRUPT FILTER CIRCUIT
Note: IO Address Port $40-$43
1-2 =on - A7 (low)
3-4 =off - A6 (high)
5-6 =on - A5 (low)
7-8 =on - A4 (low)
9-10 =on - A3 (low)
11-12 =on - A2 (low)
IO PORT ADDR
JP4
ZERO
10KA
RN3
10K
U21
74LS688
P=R
DMA-ADDR
U20
74LS175
RDY_Q0
RDY_Q1
USR-RESET1
USR-RESET2
DMA_RDY_WR
CPU-RESET
U32
ATtiny13-20PU
DATA_XFER
DMA XFER
R21
470
D10
LED
DMA Transfer LED triggered
whenever a DMA
transfer is in progress and
the pulse signal is active.
DMA software configuration
needs to program the
activation of the pulse signal.
U48
74LS07
U17A
U17B
U17C
U17D
U17E
U17F
INTERRUPT
INT0-EN
IM2-INT
IM2-IEO
IEO
BAO
BAO SEL
JP9
D6
D8
D9
D11
D12
DMA1 READY LED
DMA2 READY LED
DMA1 CHIP SELECT LED
DMA2 CHIP SELECT LED
RN9
470
TEND0
TEND1
TEND IS AN OUTPUT FROM DMA
Sheet: /DMA/
File: DMA.kicad_sch
Title:
Size: B
Date:
Rev:
KiCad E.D.A. kicad (6.0.11)
Id: 3/11



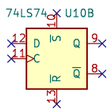


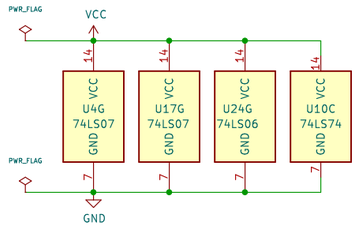






SPARE GATES





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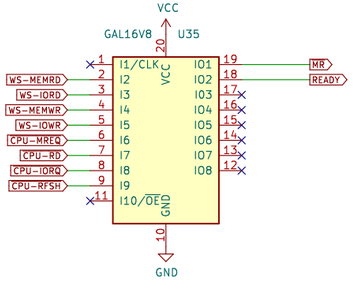
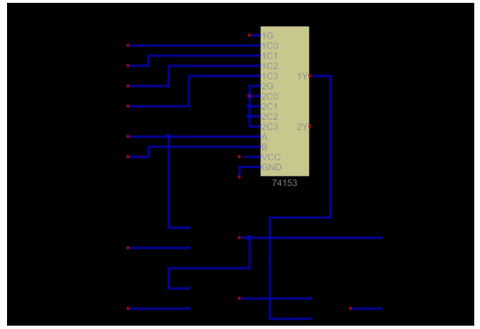
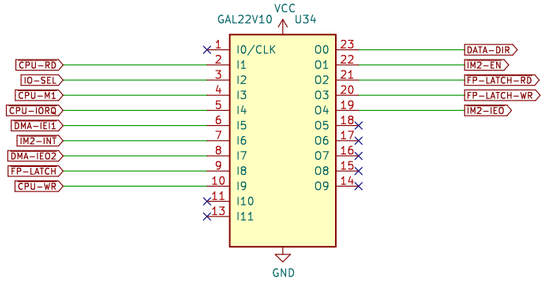
Size: B	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.11)		Id: 4/11

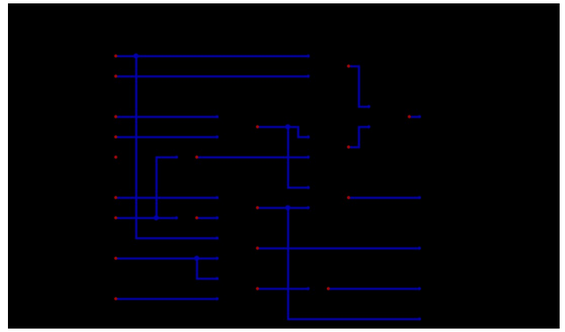
CPU WS GAL16V8

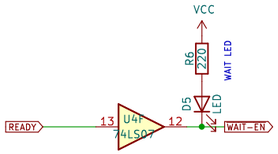




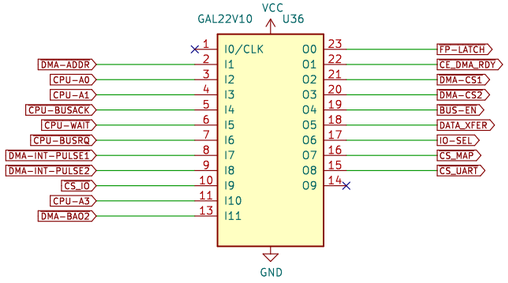
CPU DATA DIR V3 GAL22V10

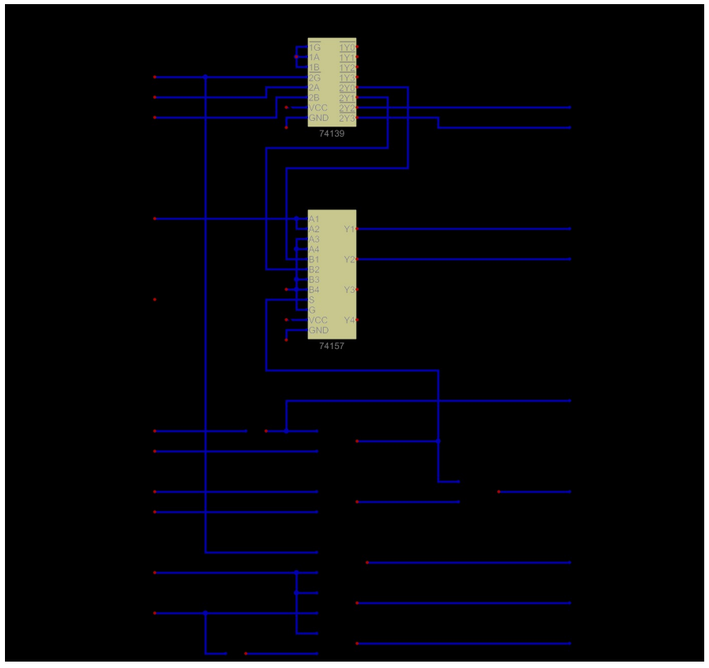




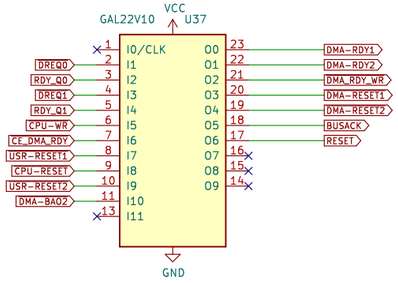


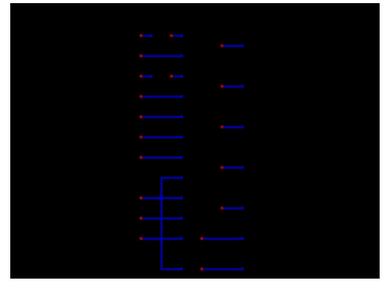
DMA CS V4 GAL22V10





DMA RDY GAL22V10





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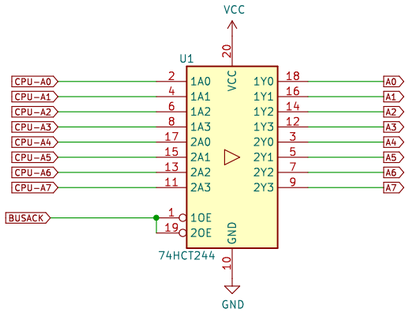
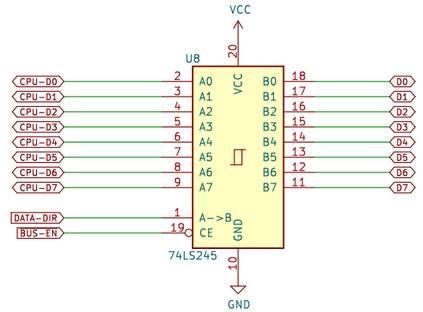
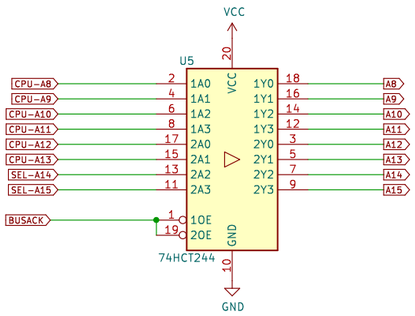
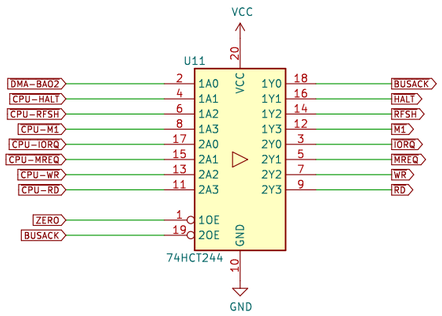
Size: B	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.11)		Id: 5/11

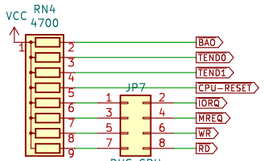
Z80 BUS INTERFACE

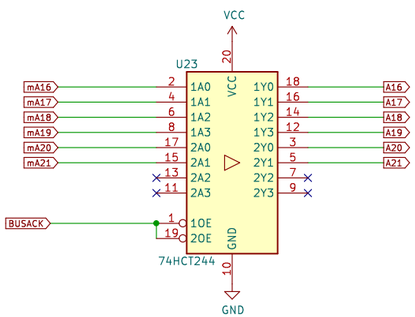


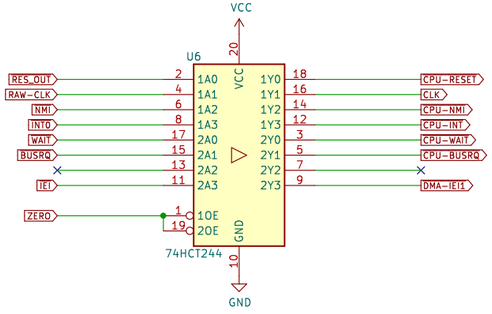


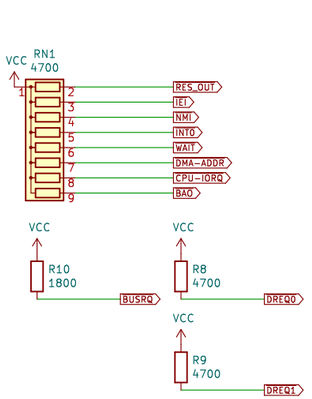












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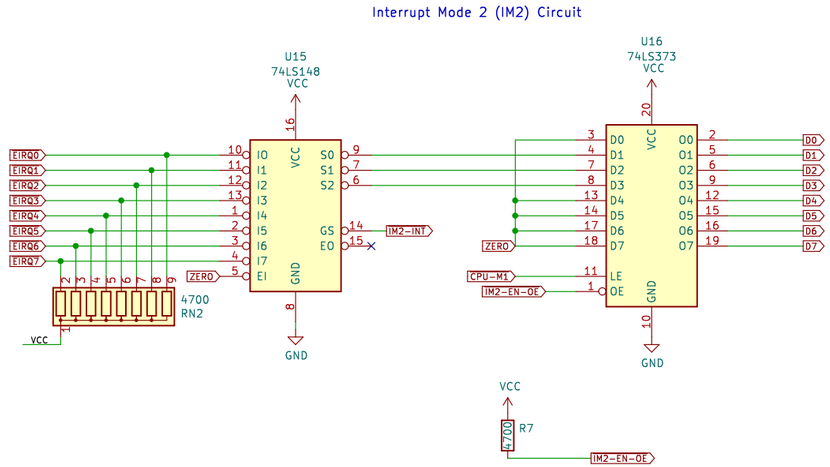
KiCad E.D.A. kicad (6.0.11) | Id: 6/11

Interrupt Mode 2 (IM2) Circuit



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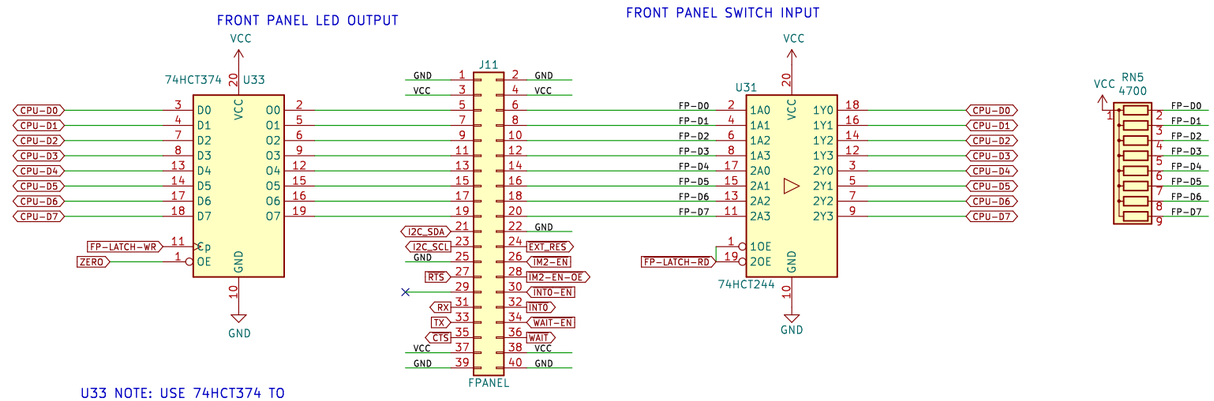
Size: B	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.11)		Id: 7/11



U33 NOTE: USE 74HCT374 TO SOURCE OR SINK ADEQUATE CURRENT TO DRIVE LEDS ON FRONT PANEL

J11 NOTE:

PINS 5, 7, 9, 11, 13, 15, 17, 19 ARE FOR LED STATUS FOR ROMWBW FRONT PANEL INDICATOR

PINS 6, 8, 10, 12, 14, 16, 18, 20 ARE FOR SWITCH INPUTS FOR ROMWBW FRONT PANEL

PINS 21, 23 ARE FOR I2C CONNECTION (SDA & SCL)

PINS 25, 27, 29, 31, 33, AND 35 ARE FOR TTL SERIAL CONNECTOR TO UART

PINS 29, 37 ARE FOR SERIAL VCC POWER ENABLE

PINS 22, 24 ARE FOR EXTERNAL RESET SWITCH

PINS 26, 28 ARE FOR IM2 CIRCUIT ENABLE

PINS 30, 32 ARE FOR INTERRUPT 0 ENABLE

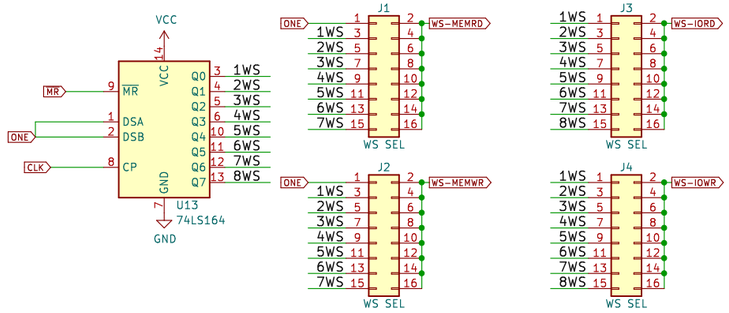
PINS 34, 36 ARE FOR WAIT STATE CIRCUIT ENABLE

Sheet: /fpanel/
File: fpanel.kicad_sch

Title:

Size: B	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.11)		Id: 8/11

Wait State Generator Circuit



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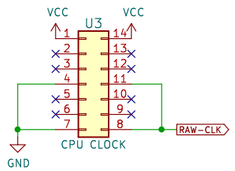
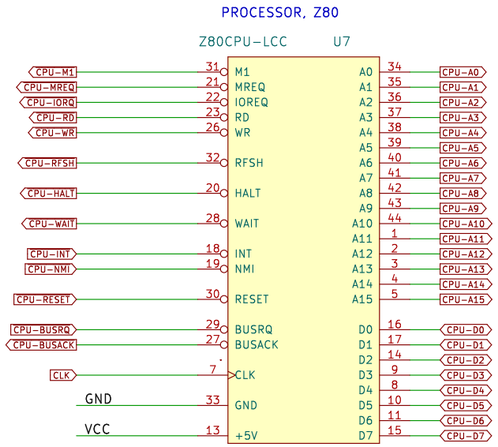
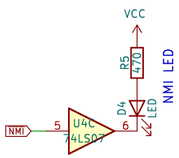
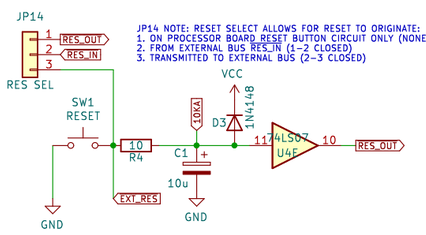




Tri-state address, data, & control bus during DMA





Reset Button Circuit

Sheet: /Z80CPU/
File: Z80CPU.kicad_sch

Title:

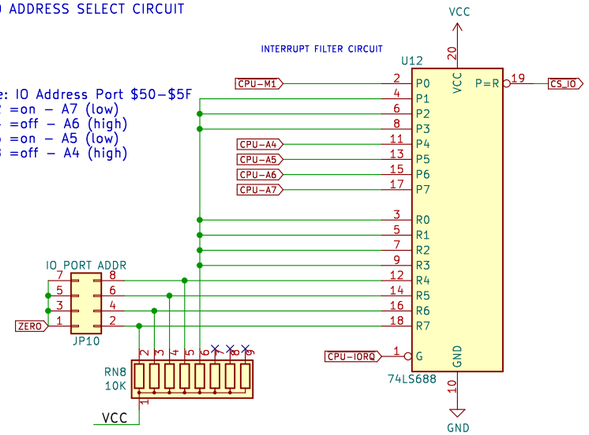
Size: B | Date: | **Rev:**
KiCad E.D.A. kicad (6.0.11) | Id: 10/11

Z80 MEMORY MAPPER AND
EXPANSION IO PORT DECODER

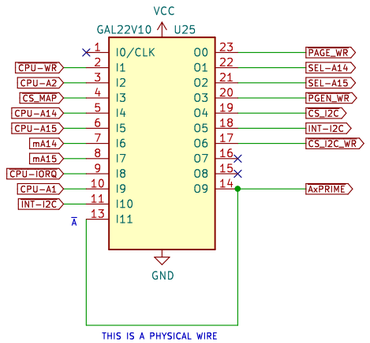
IO ADDRESS SELECT CIRCUIT

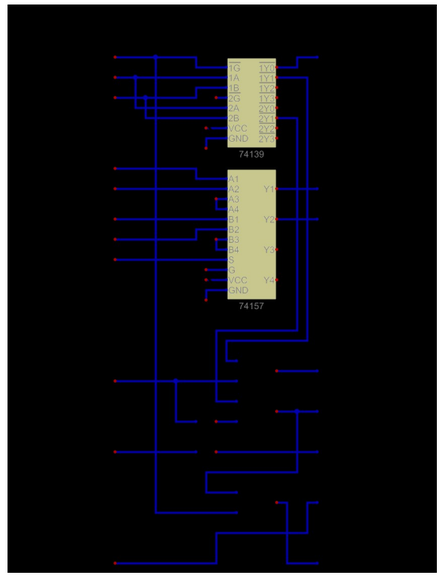
INTERRUPT FILTER CIRCUIT

Note: IO Address Port $50-$5F
1-2 =on - A7 (low)
3-4 =off - A6 (high)
5-6 =on - A5 (low)
7-8 =off - A4 (high)

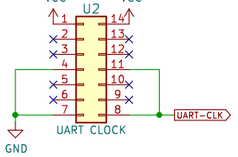


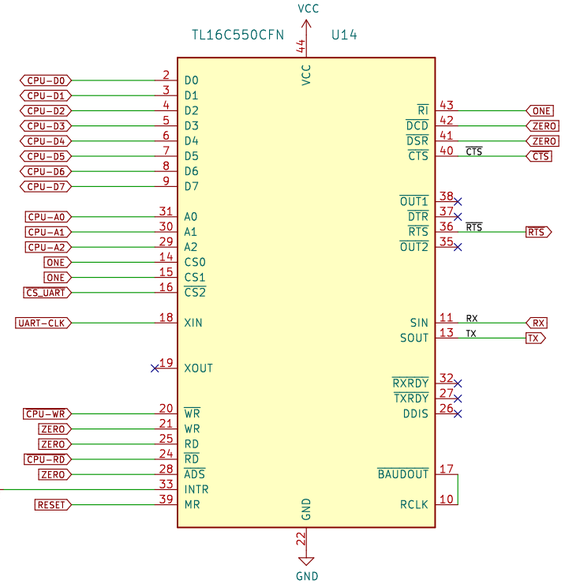
CPU MAPPER V3 GAL22V10



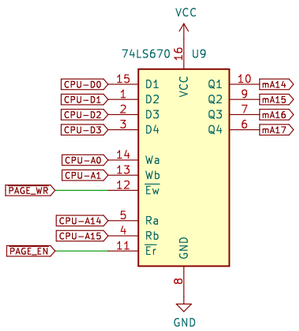


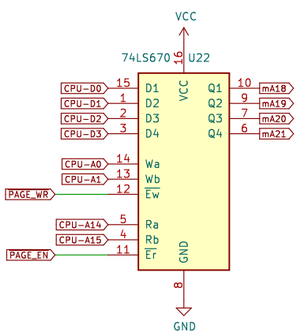
1.8432 OR 7.3728 MHz
TTL OSCILLATOR

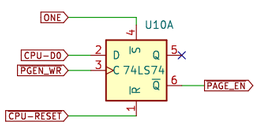




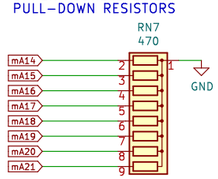
MEMORY PAGING SRAMS

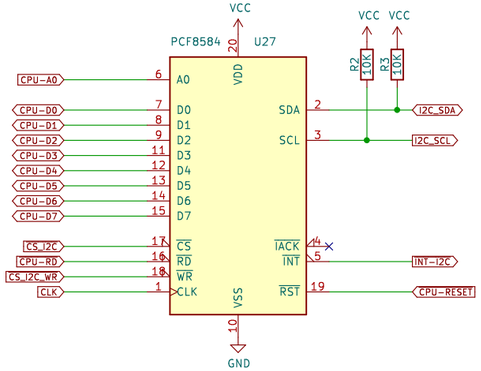


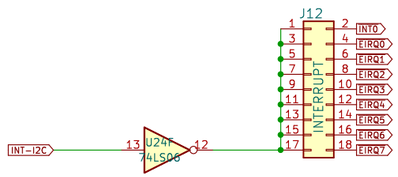




UPPER ADDRESS LINES
PULL-DOWN RESISTORS







NOTE: INTERRUPTS RELY ON 4700
OHM PULL UP RESISTOR ON PROCESSOR

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