bus

File: bus.kicad_sch
80C188CPU

File: CPU_80C188.kicad_sch

power

File: power.kicad_sch
Memory

File: Memory.kicad_sch

buffers

File: buffers.kicad_sch
bus sharing

File: bussharing.kicad_sch

fpanel

File: fpanel.kicad_sch
mapper

File: mapper.kicad_sch

Sheet: /
File: processor.80C188.kicad_sch
Title: Duodyne 80C188 CPU board
Size: B | Date: 2024-07-05 | Rev: V0.5
KiCad E.D.A. kicad (6.0.11) | Id: 1/9

P3
CONN_02X25

Left signal	Pin	Pin	Right signal
VCC	1	2	VCC
D15	3	4	D31
D14	5	6	D30
D13	7	8	D29
D12	9	10	D28
D11	11	12	D27
D10	13	14	D26
D9	15	16	D25
D8	17	18	D24
D7	19	20	D23
D6	21	22	D22
D5	23	24	D21
D4	25	26	D20
D3	27	28	D19
D2	29	30	D18
D1	31	32	D17
D0	33	34	D16
BUSERR	35	36	UDS
VPA	37	38	LDS
VMA	39	40	S2
BHE	41	42	S1
IPL2	43	44	S0
IPL1	45	46	AUXCLK3
IPL0	47	48	AUXCLK2
GND	49	50	GND

P2
CONN_02X25

Left signal	Pin	Pin	Right signal
VCC	1	2	VCC
A15	3	4	A31
A14	5	6	A30
A13	7	8	A29
A12	9	10	A28
A11	11	12	A27
A10	13	14	A26
A9	15	16	A25
A8	17	18	A24
+12V	19	20	+12V
A7	21	22	A23
A6	23	24	A22
A5	25	26	A21
A4	27	28	A20
A3	29	30	A19
A2	31	32	A18
A1	33	34	A17
A0	35	36	A16
−12V	37	38	−12V
IC3	39	40	TEND1
IC2	41	42	DREQ1
IC1	43	44	TEND0
IC0	45	46	DREQ0
AUXCLK1	47	48	AUXCLK0
GND	49	50	GND

P1
CONN_02X25

Left signal	Pin	Pin	Right signal
VCC	1	2	VCC
RD	3	4	E
WR	5	6	ST
IORQ	7	8	PHI
MREQ	9	10	INT2
M1	11	12	INT1
BUSACK	13	14	CRUCLK
bCLK	15	16	CRUOUT
INT0	17	18	CRUIN
NMI	19	20	RES_IN
RES_OUT	21	22	USER8
BUSRQ	23	24	USER7
WAIT	25	26	USER6
HALT	27	28	USER5
RFSH	29	30	USER4
EIRQ7	31	32	USER3
EIRQ6	33	34	USER2
EIRQ5	35	36	USER1
EIRQ4	37	38	USER0
EIRQ3	39	40	
EIRQ2	41	42	
EIRQ1	43	44	
EIRQ0	45	46	
I2C_SCL	47	48	I2C_SDA
GND	49	50	GND

D7
LED
470pF
POWER LED
GND

PWR_FLAG — +12V

PWR_FLAG — -12V

H1
MountingHole

H2
MountingHole

GND

VCC
NT3
NetTie_2 — ONE

NT4
NetTie_2 — ZERO

GND

VCC

| C36 | C37 | C38 | + C25 | C26 | C27 | C28 | C29 | C46 |
| 0.1u | 0.1u | 0.1u | 10u | 10u | 10u | 10u | 22u | 47uF |

VCC — VCC
GND — GND

GND

VCC

| C40 | C2 | C3 | C4 | C5 | C6 | C8 | C9 | C10 | C11 | C12 | C13 | C14 | C15 | C16 | C17 | C18 | C19 | C20 | C21 | C22 | C23 | C24 | C30 | C31 | C32 | C33 | C34 | C35 | C39 |
| 0.1u | 0.1u | 0.1u | 0.1u | 0.1u | 0.1u | 0.1u | 0.1u | 0.1u | 0.1u | 0.1u | 0.1u | 0.1u | 0.1u | 0.1u | 0.1u | 0.1u | 0.1u | 0.1u | 0.1u | 0.1u | 0.1u | 0.1u | 0.1u | 0.1u | 0.1u | 0.1u | 0.1u | 0.1u | 0.1u |

GND

PWR_FLAG
VCC

| U4G | U16E | U7G | 74LS74 | U2E | U23E | U1G |
| 74LS07 | 74LS08 | 74LS14 | U21C | 74LS32 | 74LS00 | 74LS04 |

PWR_FLAG
GND

SPARE GATES

U23A
74LS00

U16A
74LS08

U2B
74LS32

U23B
74LS00

U7E
74LS14

74LS74
U21B

U23C
74LS00

U7B
74LS14

U2C
74LS32

74LS04
U1C

U1B
74LS04

U2D
74LS32

Z80 BUS INTERFACE

U6
74LS244

CPU-A0	2	I0a O0a	18	A0
CPU-A1	4	I1a O1a	16	A1
CPU-A2	6	I2a O2a	14	A2
CPU-A3	8	I3a O3a	12	A3
CPU-A4	11	I0b O0b	9	A4
CPU-A5	13	I1b O1b	7	A5
CPU-A6	15	I2b O2b	5	A6
CPU-A7	17	I3b O3b	3	A7

188EN   1 OEa
        19 OEb

U11
74LS245

CPU-D0	2	A0 B0	18	D0
CPU-D1	3	A1 B1	17	D1
CPU-D2	4	A2 B2	16	D2
CPU-D3	5	A3 B3	15	D3
CPU-D4	6	A4 B4	14	D4
CPU-D5	7	A5 B5	13	D5
CPU-D6	8	A6 B6	12	D6
CPU-D7	9	A7 B7	11	D7

74LS32
U2A

188EN 1
G_DATA 2   3   DTR_TS

DTR_TS   1 A->B
         19 CE

VCC RN4
4700

RES_OUT
CPU-INT1
CPU-NMI
CPU-IRQ
CPU-HALT
BUSRQ
CPU-INT3
DREQ1

U8
74LS244

CPU-A8	2	I0a O0a	18	A8
CPU-A9	4	I1a O1a	16	A9
CPU-A10	6	I2a O2a	14	A10
CPU-A11	8	I3a O3a	12	A11
CPU-A12	11	I0b O0b	9	A12
CPU-A13	13	I1b O1b	7	A13
CPU-A14	15	I2b O2b	5	A14
CPU-A15	17	I3b O3b	3	A15

188EN   1 OEa
        19 OEb

U14
74LS244

HLDA	2	I0a O0a	18	BUSACK
BUSRQ	4	I1a O1a	16	HOLD
WAIT	6	I2a O2a	14	SRDY
CPU-M1	8	I3a O3a	12	M1
CPU-IORQ	11	I0b O0b	9	IORQ
CPU-MREQ	13	I1b O1b	7	MREQ
CPU-WR	15	I2b O2b	5	WR
CPU-RD	17	I3b O3b	3	RD

188EN   1 OEa
        19 OEb

VCC RN1
4700

DREQ0
CPU-DREQ1
CPU-M1
CPU-INT2
IORQ
MREQ
WR
RD

JP4
BUS CPU

U10
74LS244

CPU-A16	2	I0a O0a	18	A16
CPU-A17	4	I1a O1a	16	A17
CPU-A18	6	I2a O2a	14	A18
CPU-A19	8	I3a O3a	12	A19
CPU-RFSH	11	I0b O0b	9	RFSH
CLKOUT	13	I1b O1b	7	HALT
CPU-HALT	15	I2b O2b	5	HALT
DREQ0	17	I3b O3b	3	BDREQ

188EN   1 OEa
        19 OEb

GENERATE CLOCK
JP1
bCLK

U17
74LS244

	2	I0a O0a	18	
	4	I1a O1a	16	
bCPU-INT1	6	I2a O2a	14	CPU-INT1
bCPU-IRQ	8	I3a O3a	12	CPU-IRQ
bCPU-INT2	11	I0b O0b	9	CPU-INT2
bCPU-NMI	13	I1b O1b	7	CPU-NMI
	15	I2b O2b	5	
bCPU-INT3	17	I3b O3b	3	CPU-INT3

ENABLEINT 1 OEa
          19 OEb

J12
INT3 Selection

INT0	1	2	bCPU-INT3
EIRQ0	3	4	
EIRQ1	5	6	
EIRQ2	7	8	
EIRQ3	9	10	
EIRQ4	11	12	
EIRQ5	13	14	
EIRQ6	15	16	
EIRQ7	17	18	

J9
INT Selection

INT0	1	2	bCPU-IRQ
EIRQ0	3	4	
EIRQ1	5	6	
EIRQ2	7	8	
EIRQ3	9	10	
EIRQ4	11	12	
EIRQ5	13	14	
EIRQ6	15	16	
EIRQ7	17	18	

J5
NMI Selection

NMI	1	2	bCPU-NMI
EIRQ0	3	4	
EIRQ1	5	6	
EIRQ2	7	8	
EIRQ3	9	10	
EIRQ4	11	12	
EIRQ5	13	14	
EIRQ6	15	16	
EIRQ7	17	18	

J6
INT1 Selection

INT0	1	2	bCPU-INT1
EIRQ0	3	4	
EIRQ1	5	6	
EIRQ2	7	8	
EIRQ3	9	10	
EIRQ4	11	12	
EIRQ5	13	14	
EIRQ6	15	16	
EIRQ7	17	18	

J10
INT2 Selection

INT0	1	2	bCPU-INT2
EIRQ0	3	4	
EIRQ1	5	6	
EIRQ2	7	8	
EIRQ3	9	10	
EIRQ4	11	12	
EIRQ5	13	14	
EIRQ6	15	16	
EIRQ7	17	18	

FRONT PANEL LED OUTPUT

FRONT PANEL SWITCH INPUT

VCC

VCC

74LS374 U33

U31
74LS244

CPU-D0 3 D0 VCC 20 O0 2 **CPU-D0**
CPU-D1 4 D1 O1 5 **CPU-D1**
CPU-D2 7 D2 O2 6 **CPU-D2**
CPU-D3 8 D3 O3 9 **CPU-D3**
CPU-D4 13 D4 O4 12 **CPU-D4**
CPU-D5 14 D5 O5 15 **CPU-D5**
CPU-D6 17 D6 O6 16 **CPU-D6**
CPU-D7 18 D7 O7 19 **CPU-D7**

J11

GND 1 2 GND
VCC 3 4 VCC
5 6
7 8
9 10
11 12
13 14
15 16
17 18
19 20

FP-D0 2 I0a VCC 20 O0a 18 **CPU-D0**
FP-D1 4 I1a O1a 16 **CPU-D1**
FP-D2 6 I2a O2a 14 **CPU-D2**
FP-D3 8 I3a O3a 12 **CPU-D3**
FP-D4 11 I0b O0b 9 **CPU-D4**
FP-D5 13 I1b O1b 7 **CPU-D5**
FP-D6 15 I2b O2b 5 **CPU-D6**
FP-D7 17 I3b O3b 3 **CPU-D7**

VCC RN5
4700

FP-D0
FP-D1
FP-D2
FP-D3
FP-D4
FP-D5
FP-D6
FP-D7

VCC RN3
470

470A
470B
470C
470D
470E
470F
470G

FP-LATCH-WR 11 Cp
ZERO 1 OE

I2C_SDA 21 22 GND
I2C_SCL 23 24 **EXT_RES**
GND 25 26
RTS 27 28
29 30
RX 31 32
TX 33 34
CTS 35 36
VCC 37 38 VCC
GND 39 40 GND

FP-LATCH-RD 1 OEa
19 OEb

GND 10 GND

GND

GND 10

GND

FPANEL

U33 NOTE: USE 74HCT374 TO
SOURCE OR SINK ADEQUATE
CURRENT TO DRIVE LEDS ON
FRONT PANEL

J11 NOTE:

PINS 5, 7, 9, 11, 13, 15, 17, 19 ARE FOR LED STATUS
FOR ROMWBW FRONT PANEL INDICATOR

PINS 6, 8, 10, 12, 14, 16, 18, 20 ARE FOR SWITCH
INPUTS FOR ROMWBW FRONT PANEL

PINS 21, 23 ARE FOR I2C CONNECTION (SDA & SCL)

PINS 25, 27, 29, 31, 33, AND 35
ARE FOR TTL SERIAL CONNECTOR TO UART

PINS 22, 24 ARE FOR EXTERNAL RESET SWITCH

Title: Duodyne 80C188 CPU board

Size: B | Date: 2024-07-05 | **Rev: V0.5**
KiCad E.D.A. kicad (6.0.11) | Id: 8/9

Note: IO Address Port $96
1-2 =off - A7 (high)
3-4 =on - A6 (low)
5-6 =on - A5 (low)
7-8 =off - A4 (high)
9-10 =on - A3 (low)
11-12 =off - A2 (high)
13-14 =off - A1 (high)
15-16 =on - A0 (low)

U22
74LS688

RN2
10KΩ
J1
IO Address Select

U7C
74LS14

74LS08
U16C

74LS08
U16D

88TOGGLE

A bit of delay . . . .

VCC

R9
1KΩ

88TOGGLE

U21A
74LS74

188ACTIVE

U4F
74LS07

BUSRQ

RES_OUT

GND

188ACTIVE
188EN
J3
80C188 ONLY

GND

1&2 - stand alone
2&3 - secondary CPU

80C188 RESET
J2

RES_OUT
188RST
188EN

1&2 - stand alone
2&3 - secondary CPU

74LS04
188EN   U1E   188EN

74LS04
80C188
188EN   U1F   470G
D4

GND
U12
80C188
VSS

FROM UART

STAT188.JED
P/N 18801-01
U15
GAL22V10

CPU 2X oscillator must be
an EVEN number Mhz
50.0, 40.0, 32.0, 24.0

CPU CLOCK
TTL OSCILLATOR
U9
CPU CLOCK
VCC   VCC
GND

RUN/HALT LEDS

RUN GREEN
HALT RED

NMI LED
INT LED

pin 18 is connected
so ACT or AHCT may
be used

U3
74ALS373
VCC
GND

U19
74ALS373
VCC
GND

HLDA

J4
RES SEL
NOTE: RESET SELECT ALLOWS FOR RESET TO ORIGINATE:
1. ON PROCESSOR BOARD RESET BUTTON CIRCUIT ONLY (NONE)
2. FROM EXTERNAL BUS RES_IN (1-2 CLOSED)

SW1
RESET
1N4148
74LS07
U4E
RES_OUT
DS1233
U13
GND
RES_OUT
VCC
EXT_RES
GND
Reset Button Circuit

RetroBrew Computer Group
Based on a design by John R Coffman.

Sheet: /80C188CPU/
File: CPU_80C188.kicad_sch
Title: Duodyne 80C188 CPU board
Size: USLedger   Date: 2024-07-05   Rev: V0.5
KiCad E.D.A. kicad (6.0.11)   Id: 10/9

ROM

FLASH 39SF010 (128K)
       ALTERNATES: 39SF020, 29F020, 29F010
       39SF040, 29F040 (512K) NOT RECOMMENDED

CMOS 27C010 (128K, 32pin)
       ALTERNATE 27C020
  28pin: 27C512(64K), 27C256(32K)

DEFAULT CHIP: 39SF010 (128K FLASH)
DEFAULT JUMPERS: 1-2, 1-2 (BOTH)

29F040 SHOWS ALL PIN ASSIGNMENTS

U26
29F040

12 A0	D0 13
11 A1	D1 14
10 A2	D2 15
9 A3	D3 17
8 A4	D4 18
7 A5	D5 19
6 A6	D6 20
5 A7	D7 21
27 A8	
26 A9	
23 A10	
25 A11	
4 A12	
28 A13	
29 A14	
3 A15	
2 A16	
30 A17	
1 A18	
31 PGM	
22 CE	
24 OE	

A0–A18, D0–D7

VCC

R1
22K

J13
FLASH OR CMOS
A17

UCS → CE
RD → OE

1-2 FLASH OR CMOS (32-PIN)
2-3 28-PIN CMOS

A18
J14
FLASH OR CMOS
WR

OFF FLASH WRITE PROTECT
     OR CMOS UP TO 128K
1-2 FLASH (DEFAULT) NO WP
2-3 CMOS (512K)
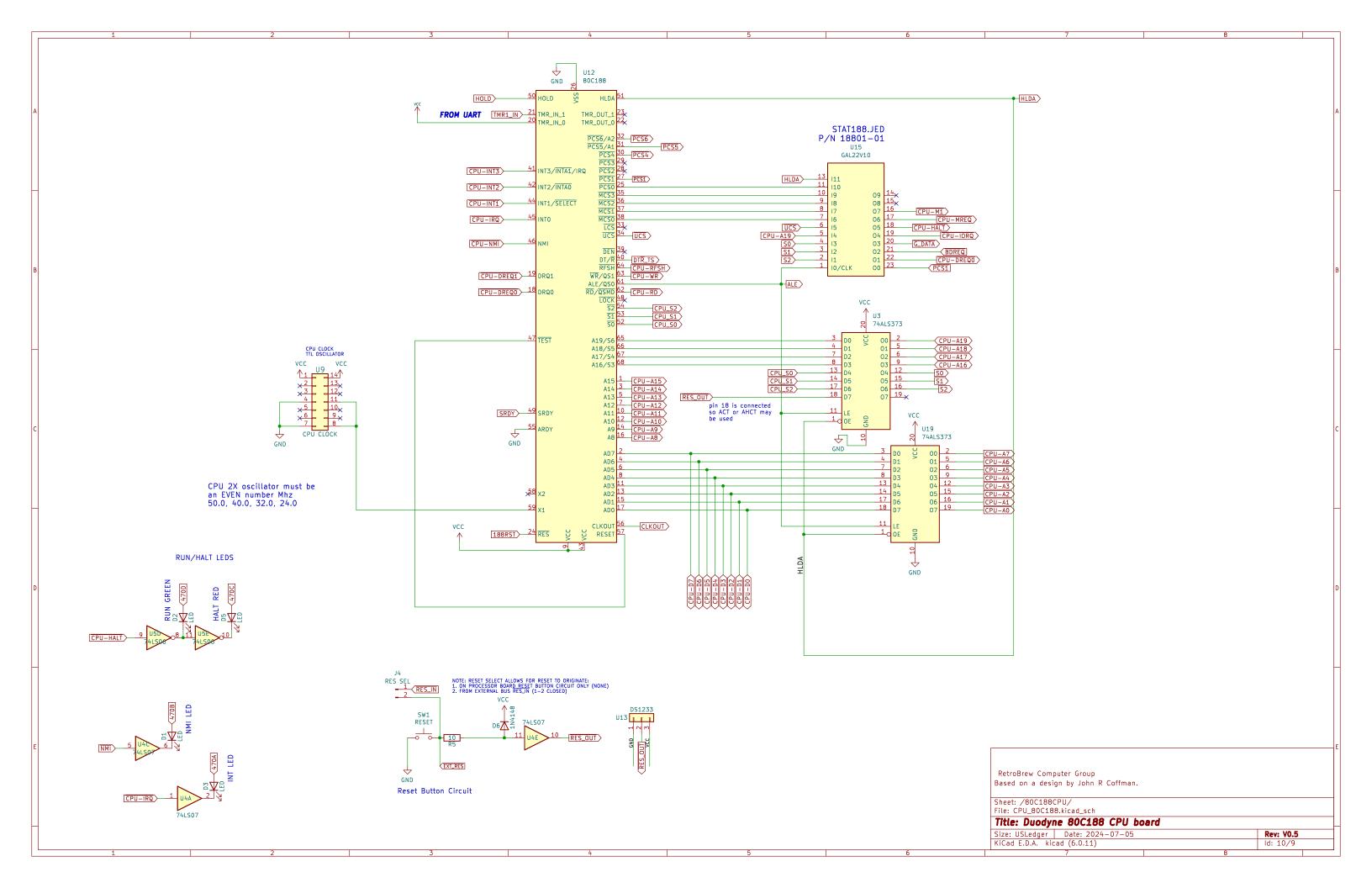
RetroBrew Computer Group
Based on a design by John R Coffman.

Sheet: /Memory/
File: Memory.kicad_sch
Title: Duodyne 80C188 CPU board
Size: USLedger | Date: 2024-07-05
KiCad E.D.A. kicad (6.0.11)
Rev: V0.5
Id: 10/9

U25
GAL22V10

ALE
PCS4
PCS5
PCS6
CPU-A6
CPU-A5
CPU-A4
CPU-WR
CPU-RD
S2

I0/CLK
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11

O0
O1
O2
O3
O4
O5
O6
O7
O8
O9

FP-LATCH-RD
FP-LATCH-WR
RES_OUT
CS_UART
CS_I2C
CS_I2C_WR
WR_LS259

S2 aka ST2
(latched)
rev. 003

PERIF188.JED
P/N 18802-01

470E
D9
LED
UART LED

CS_UART
U4B
74LS07

INT-I2C

J7
I2C IRQ Selection
INT0
EIRQ0
EIRQ1
EIRQ2
EIRQ3
EIRQ4
EIRQ5
EIRQ6
EIRQ7

1.8432 OR 7.3728 MHz
TTL OSCILLATOR
VCC   VCC
U18

GND
UART CLOCK
UART-CLK

UART_INT
U7A
74LS14

J8
UART IRQ Selection
INT0
EIRQ0
EIRQ1
EIRQ2
EIRQ3
EIRQ4
EIRQ5
EIRQ6
EIRQ7

VCC
TL16C550CFN   U20
VCC

CPU-D0
CPU-D1
CPU-D2
CPU-D3
CPU-D4
CPU-D5
CPU-D6
CPU-D7

D0
D1
D2
D3
D4
D5
D6
D7

RI
DCD
DSR
CTS

ONE
ZERO
ZERO
CTS

CPU-A0
CPU-A1
CPU-A2
ONE
ONE
CS_UART

A0
A1
A2
CS0
CS1
CS2

OUT1
DTR
RTS
OUT2

RTS

UART-CLK
XIN

SIN   RX
SOUT TX

RX
TX

XOUT

RXRDY
TXRDY
DDIS

CPU-WR
ZERO
CPU-RD
ZERO

WR
WR
RD
RD
ADS

BAUDOUT

UART_INT
INTR
MR

RCLK

GND

U1D
74LS04

RES_OUT

VCC
RN6
470

UART-CLK
U23D
74LS00
TMR1_IN
TO CPU

LED
LED
LED
LED
LED

VCC
PCF8584   U27
VDD

CPU-A0
A0

CPU-D0
CPU-D1
CPU-D2
CPU-D3
CPU-D4
CPU-D5
CPU-D6
CPU-D7

D0
D1
D2
D3
D4
D5
D6
D7

VCC VCC
R2   R3
10K 10K

SDA
SCL

I2C_SDA
I2C_SCL

PCF CLOCK
TTL OSCILLATOR
VCC   VCC
U28

GND
PCF CLOCK

CS_I2C
CPU-RD
CS_I2C_WR

CS
RD
WR
CLK

IACK
INT

RST

INT-I2C

RES_OUT

GND

U24
74LS259

CPU-D0
D   VCC
CPU-A0
CPU-A1
CPU-A2
A0
A1
A2
WR_LS259
E
RES_OUT
Clr
GND

Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7

ENABLEINT

GND