

1	2	3	4	5	6	7	8
A							A
B	buffers	power	bus				
	File: buffers.kicad_sch RTC	File: power.kicad_sch battery	File: bus.kicad_sch GALS				
C							
	File: RTC.kicad_sch IO	File: battery.kicad_sch RAM	File: GALS.kicad_sch ROM				
D							
E							
1	2	3	4	5	6	7	8

Sheet: /
File: memory.ROMRAM.kicad_sch

Title:

Size: B

Date:

Rev:

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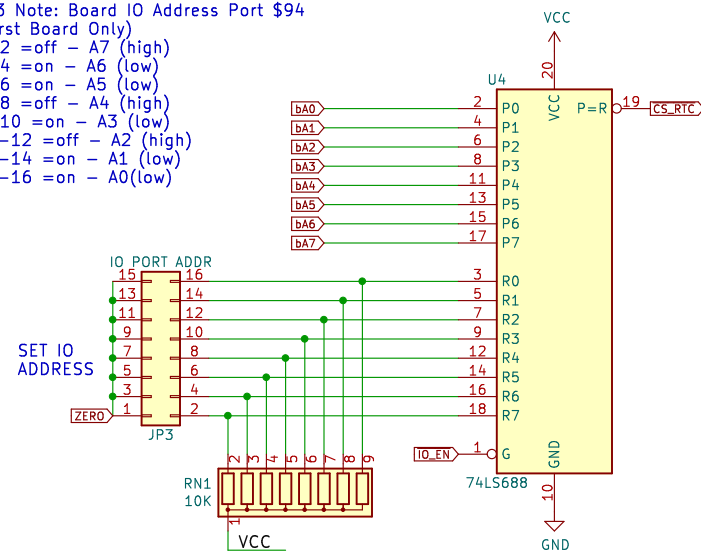
Id: 1/10

1	2	3	4	5	6	7	8	
---	---	---	---	---	---	---	---	--

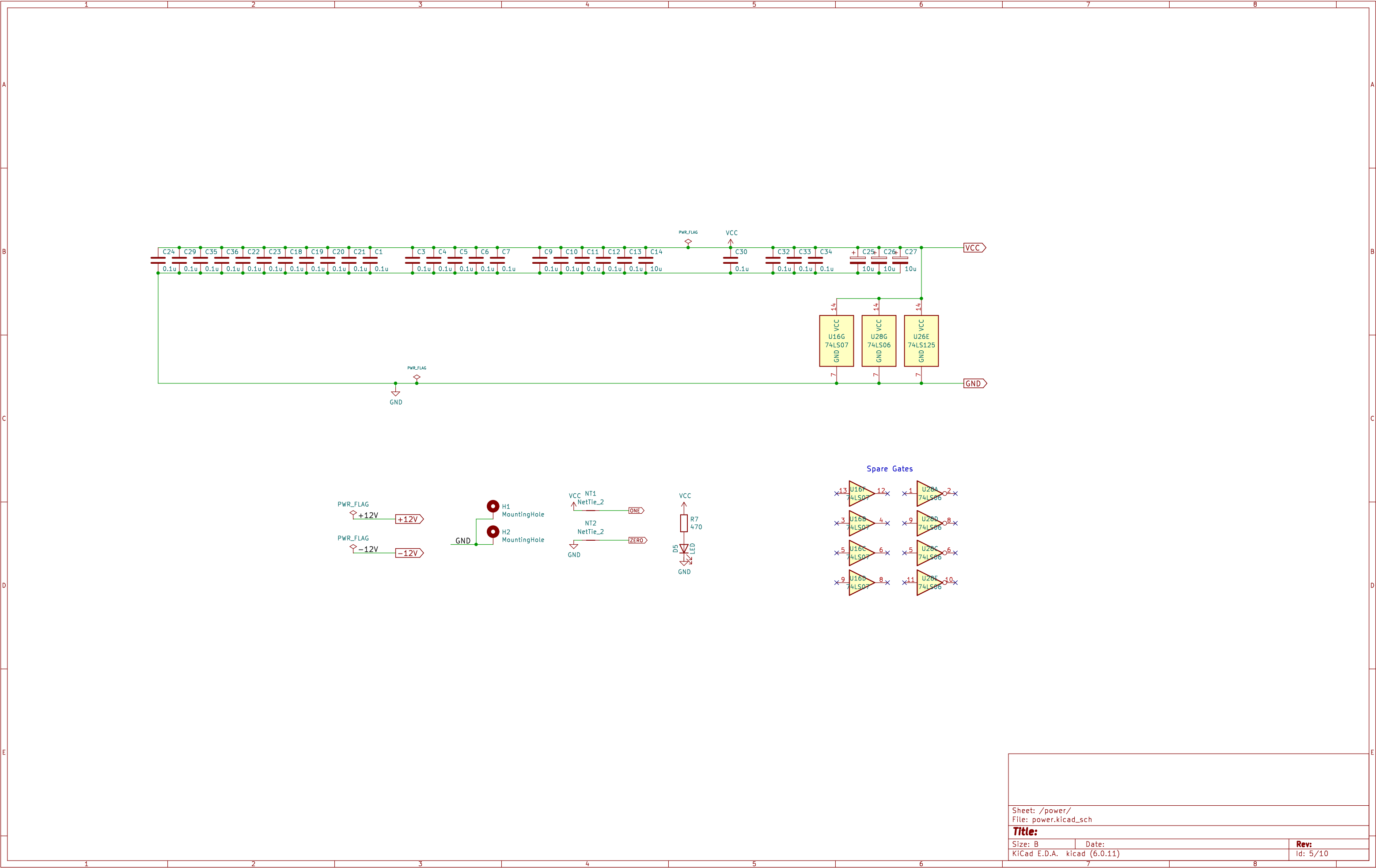
IO ADDRESS SELECT CIRCUIT
RTC

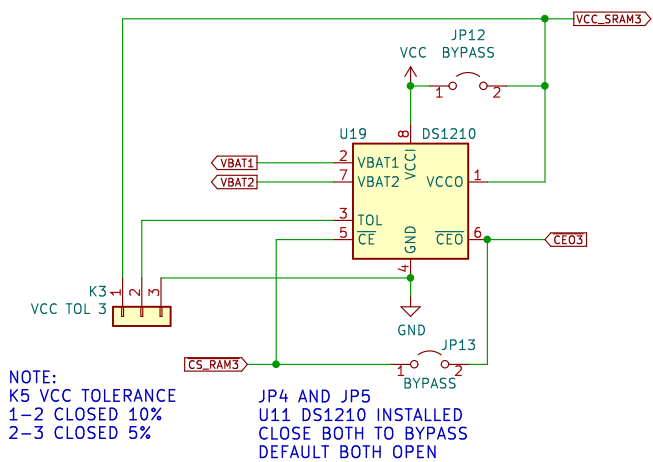
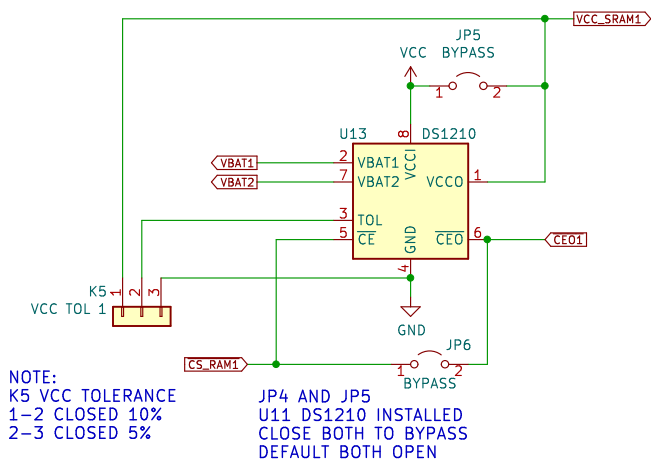
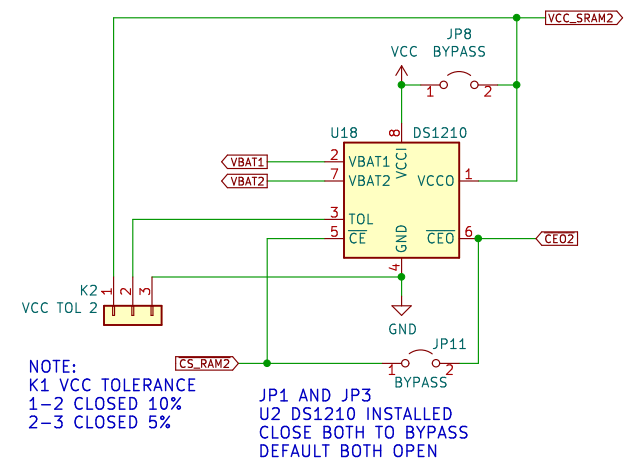
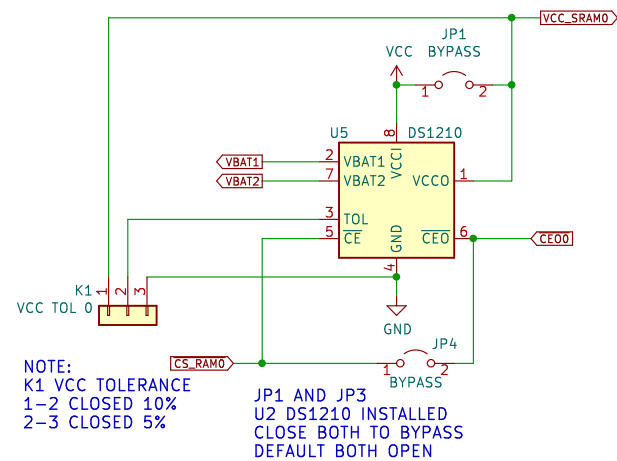
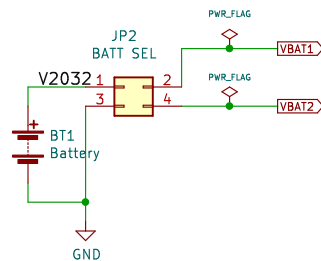
JP3 Note: Board IO Address Port \$94
(First Board Only)

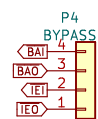
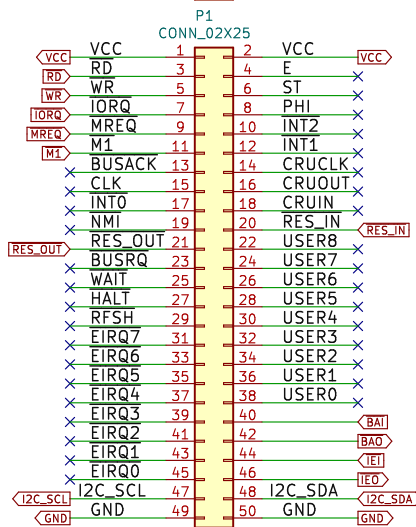
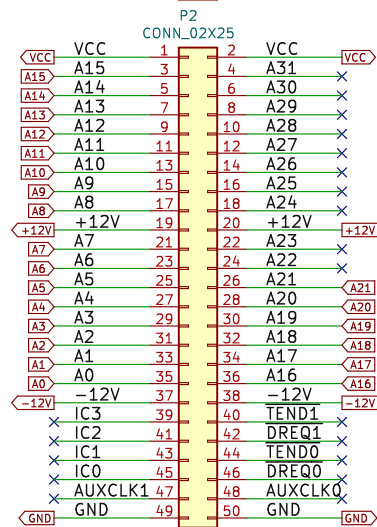
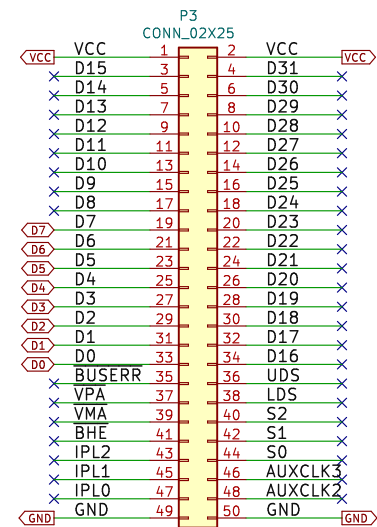
- 1-2 = off - A7 (high)
- 3-4 = on - A6 (low)
- 5-6 = on - A5 (low)
- 7-8 = off - A4 (high)
- 9-10 = on - A3 (low)
- 11-12 = off - A2 (high)
- 13-14 = on - A1 (low)
- 15-16 = on - A0 (low)

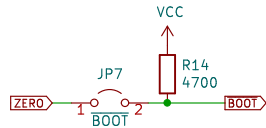
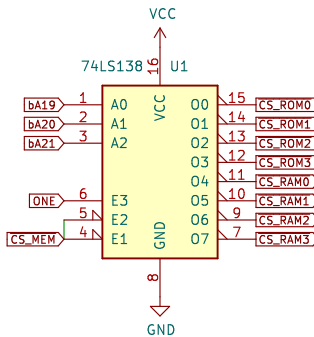
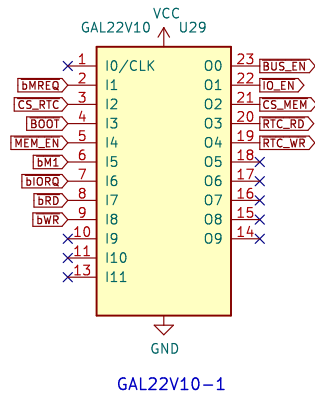
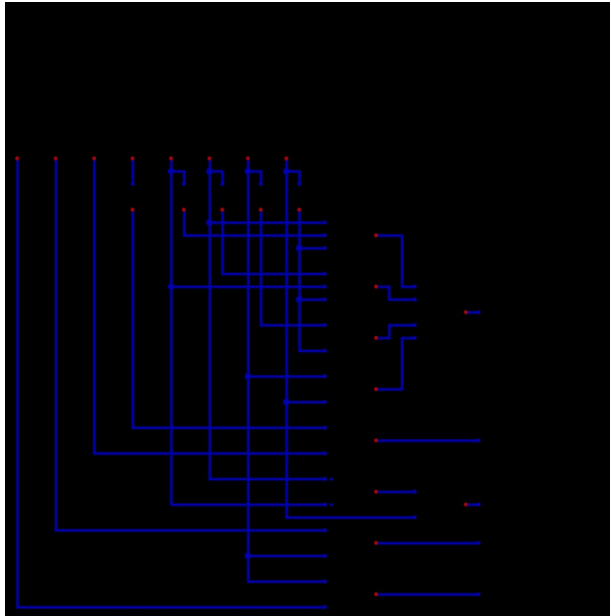


NOTE: MULTIPLE BOARDS INSTALLED
MUST HAVE UNIQUE IO PORT ADDRESSES





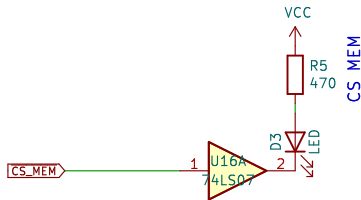




JP7 NOTE: FIRST ROM & RAM BOARD IN SYSTEM MUST HAVE JP7 JUMPER INSTALLED. ALSO MUST HAVE ROM INSTALLED IN U20 WITH BOOT CODE. FIRST BOARD ONLY RESPONDS WHEN MEM_EN LOW (BY DEFAULT).

SECOND ROM & RAM BOARD INSTALLED IN SYSTEM MUST HAVE JP7 JUMPER NOT INSTALLED. ALSO SECOND BOARD ONLY RESPONDS WHEN MEM_EN IS HIGH.

ACCESS IS CONTROLLED BY SOFTWARE TO ENSURE THAT ONLY ONE OF BOARDS HAS MEM_EN HIGH AT ANY GIVEN TIME OR BUS CONTENTION.



Sheet: /GALS/
File: GALS.kicad_sch

Title:

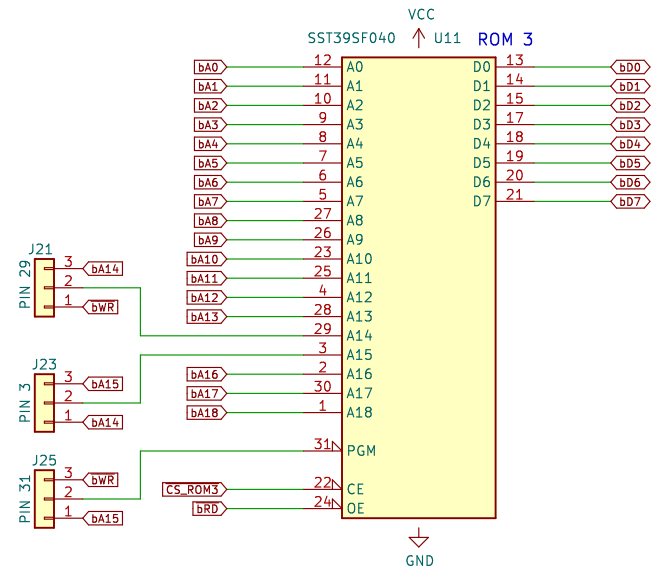
Size: B

Date:

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Rev:

Id: 9/10



The schematic illustrates the connection of two I2C modules, J33 and J35, to a common bus. Each module consists of a 24LC512 EEPROM (U25 and U30) and a serial memory chip (SER MEM 2 and SER MEM 3). The modules are connected via a ribbon cable to a terminal block labeled RN3 10K. Power connections include VCC and GND.