

12345678

bus

power

buffers

fpanel

Z80CPU

File: bus.kicad\_sch  
DMA

File: power.kicad\_sch  
GALS

File: buffers.kicad\_sch  
IM2

File: fpanel.kicad\_sch  
waitstate

File: Z80CPU.kicad\_sch  
mapper

File: DMA.kicad\_sch

File: GALS.kicad\_sch

File: IM2.kicad\_sch

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File: processor.Z80.kicad\_sch

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Size: B

Date:

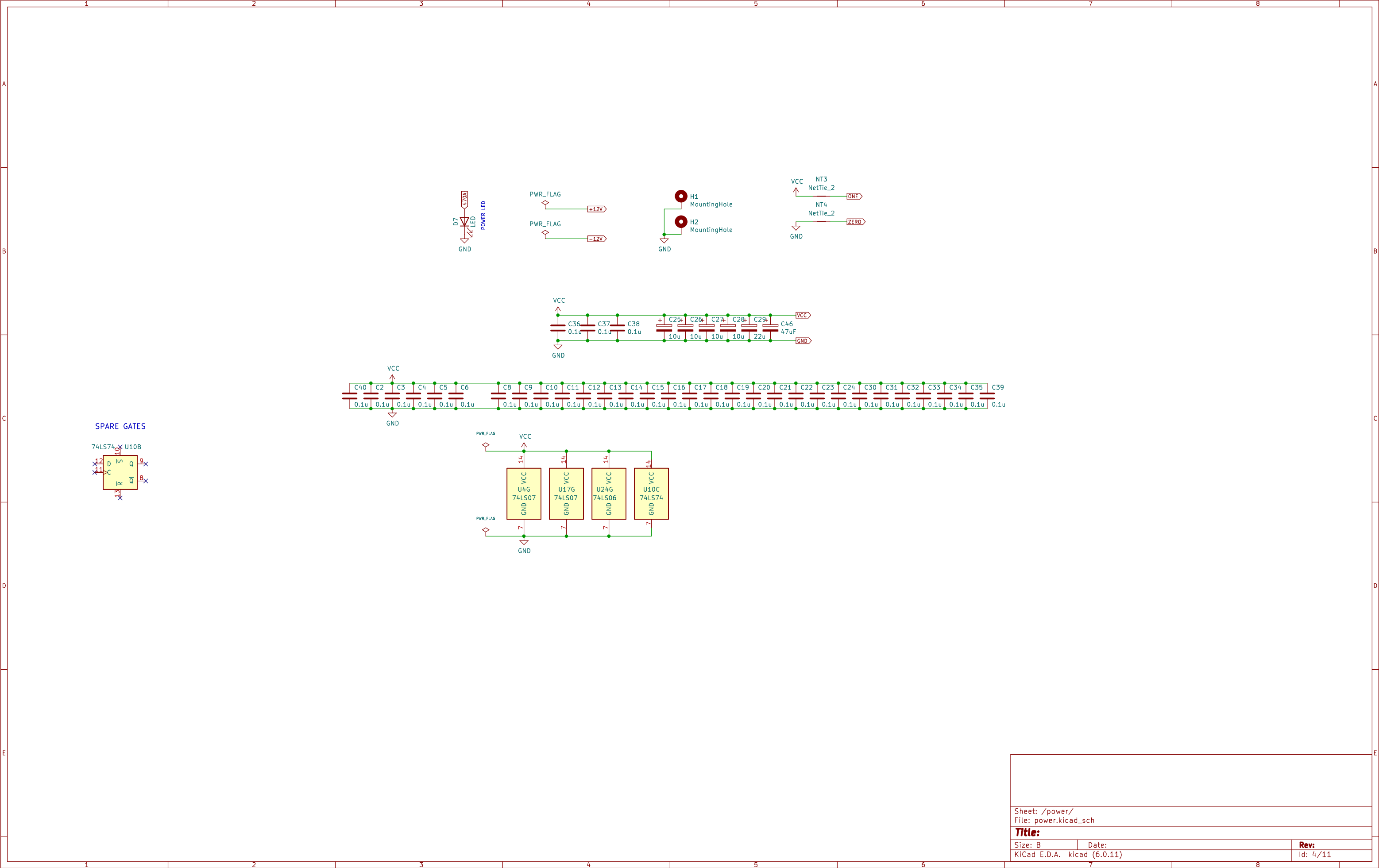
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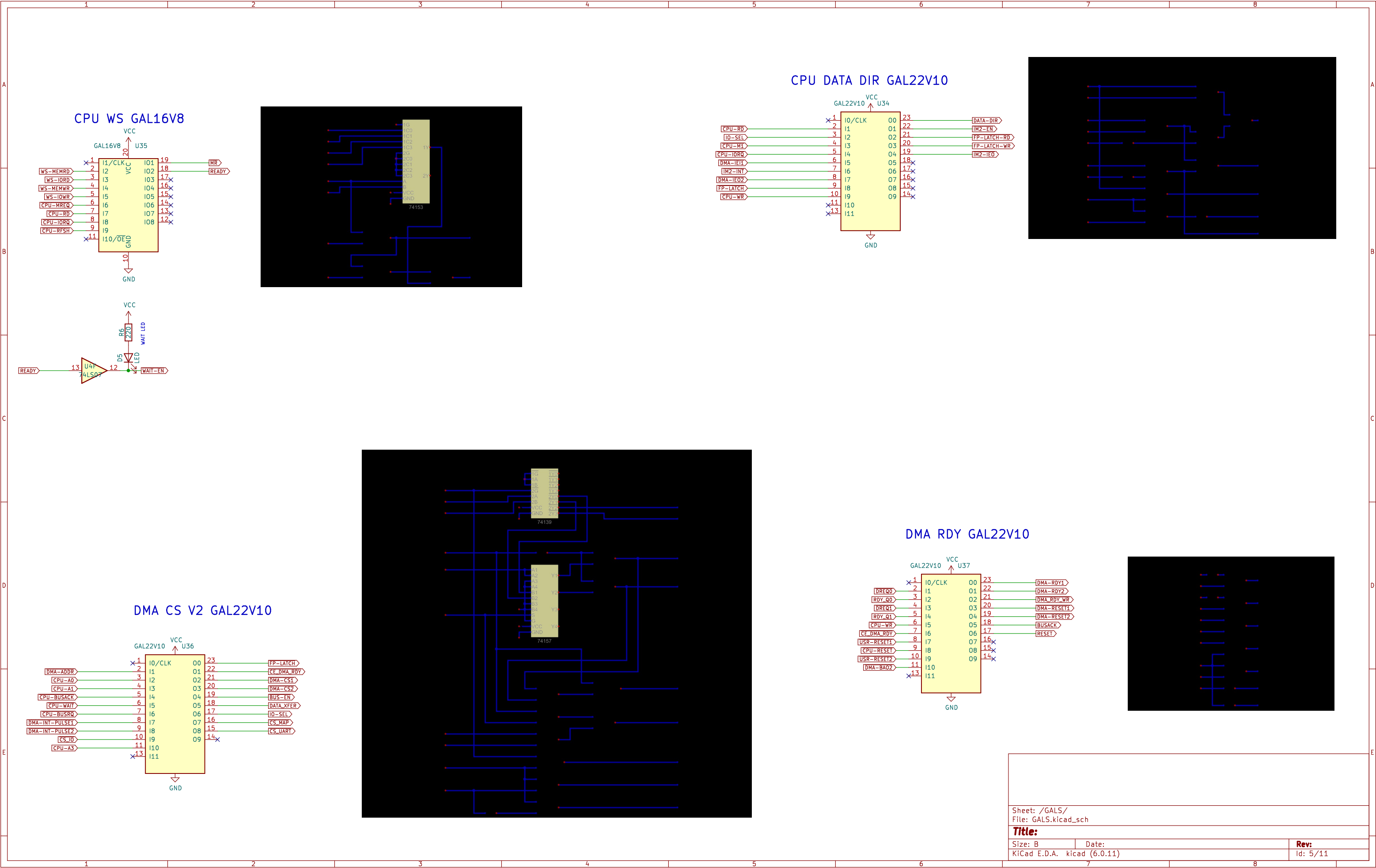
KiCad E.D.A.   kicad (6.0.11)

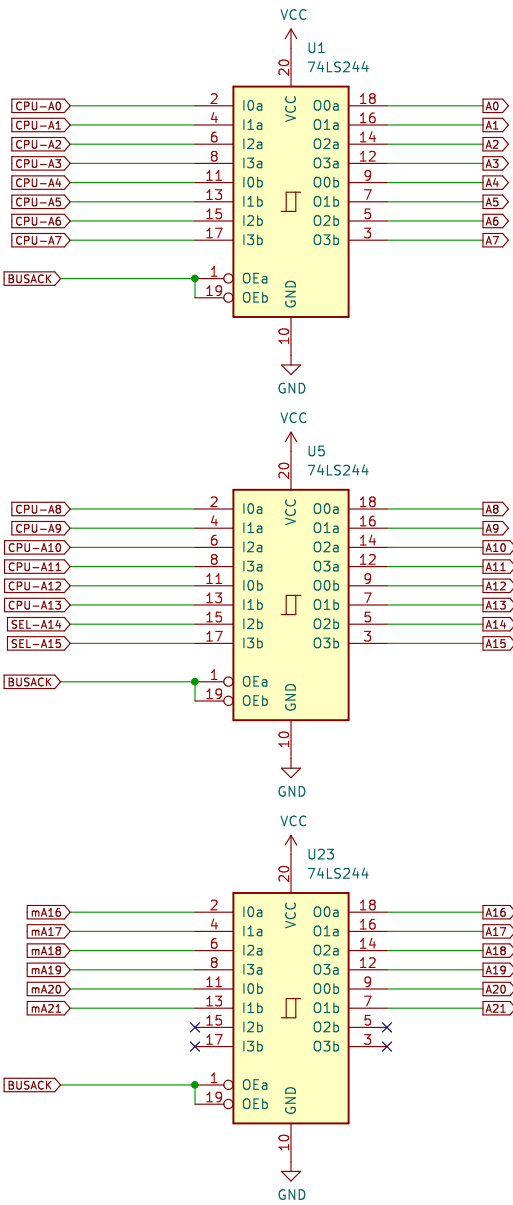
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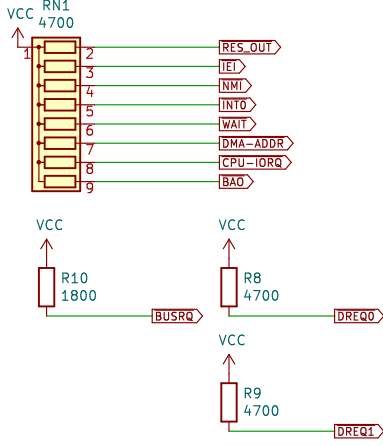
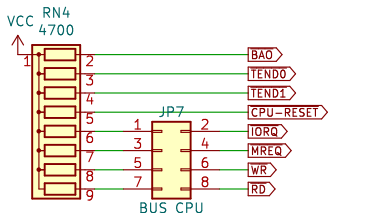
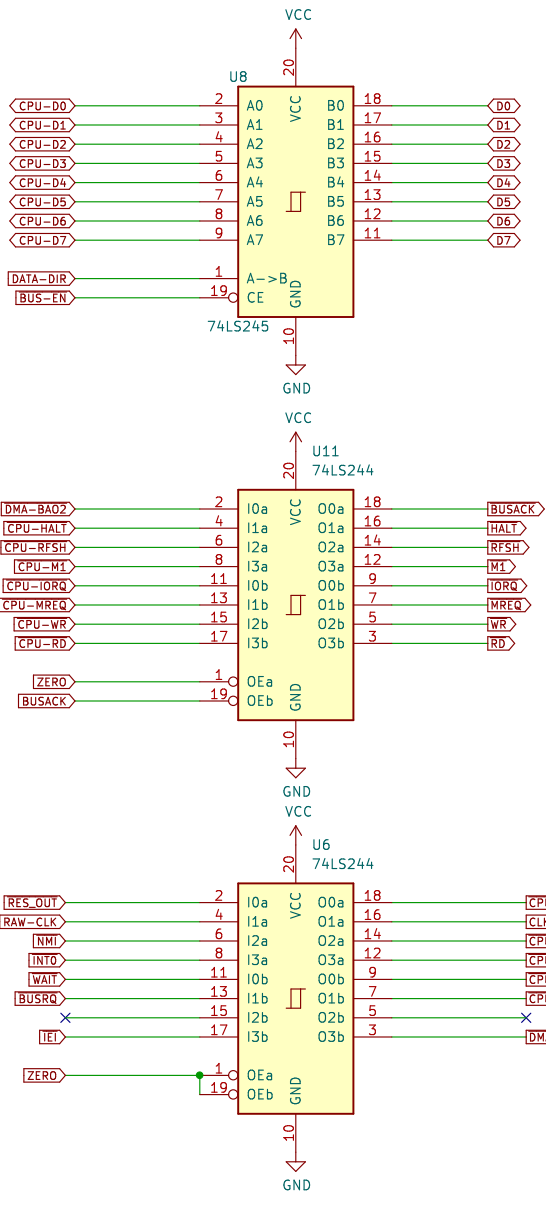








Z80 BUS INTERFACE



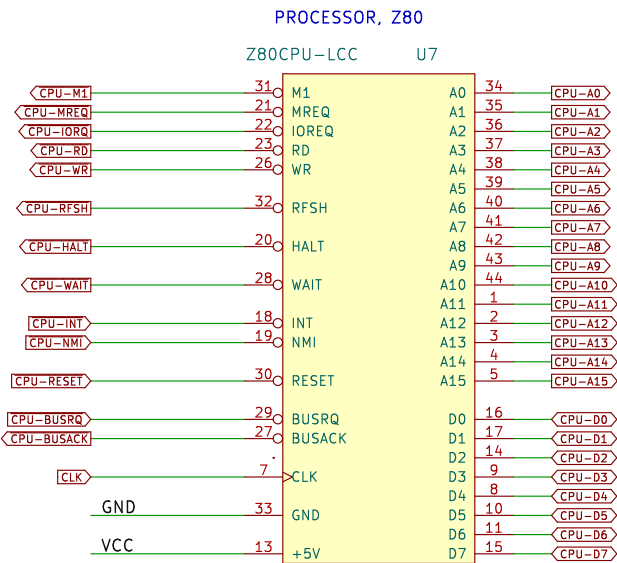
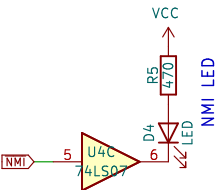
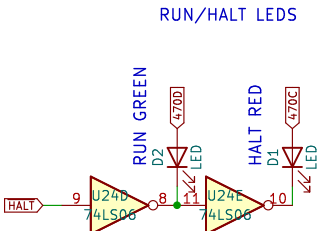
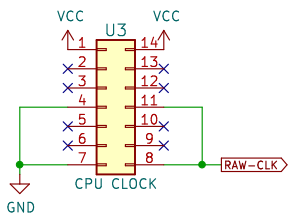




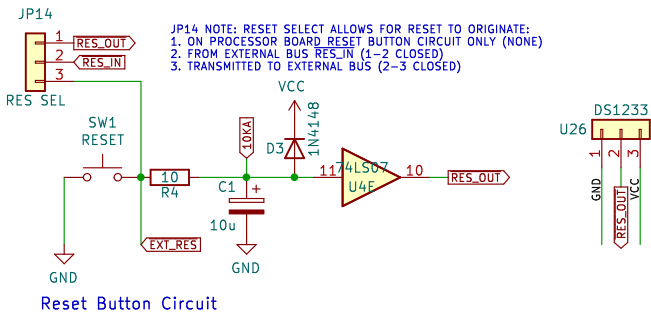
PINS 34, 36 ARE FOR WAIT STATE CIRCUIT ENABLE







Tri-state address, data, & control bus during DMA



Sheet: /Z80CPU/  
File: Z80CPU.kicad\_sch

**Title:**

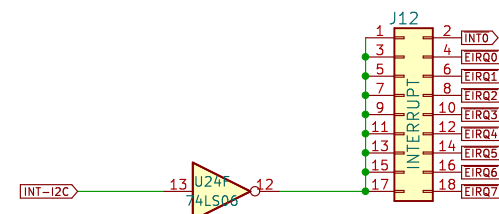
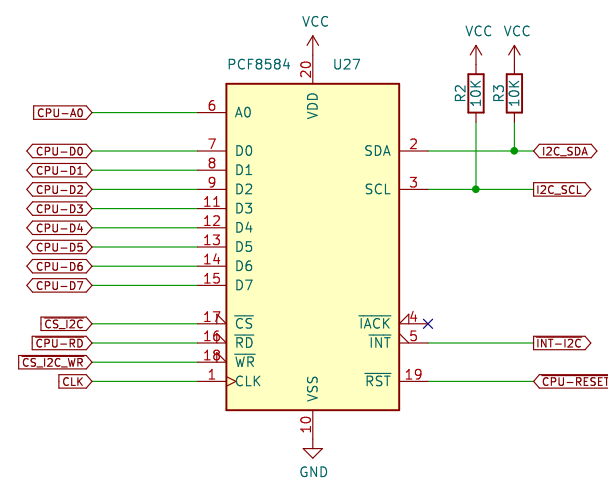
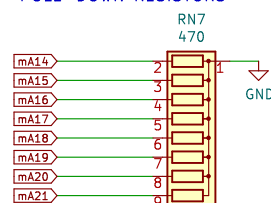
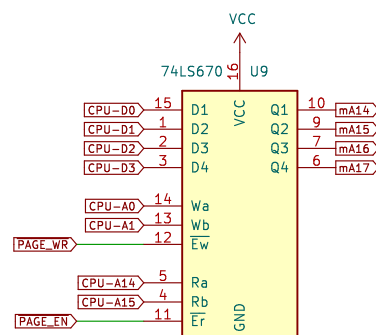
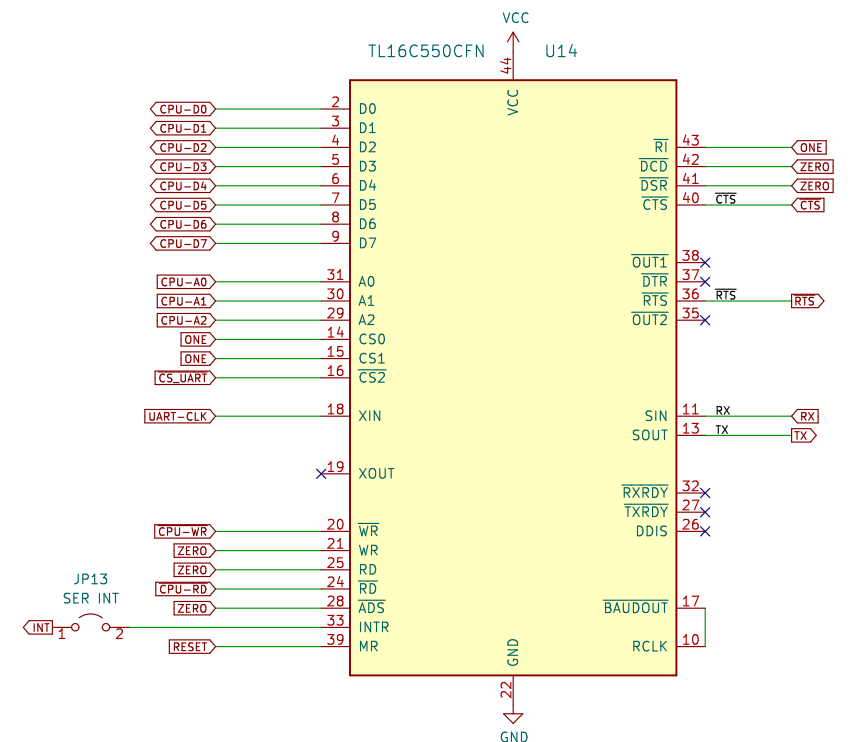
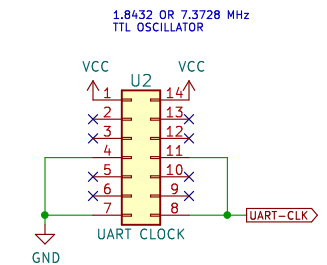
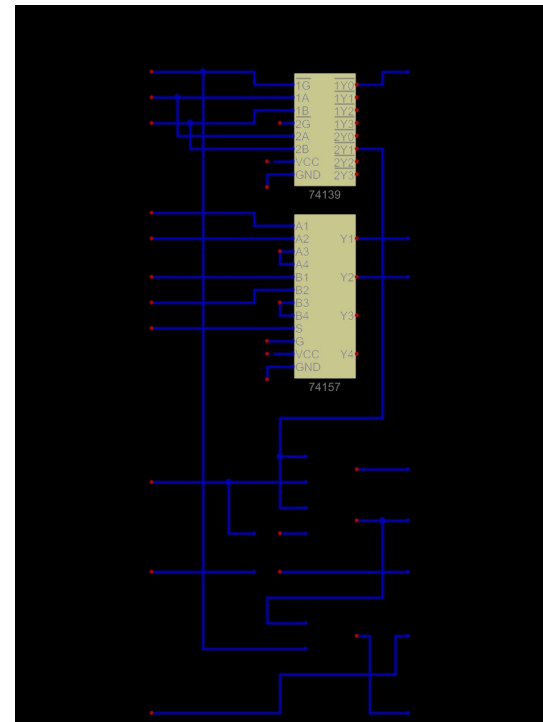
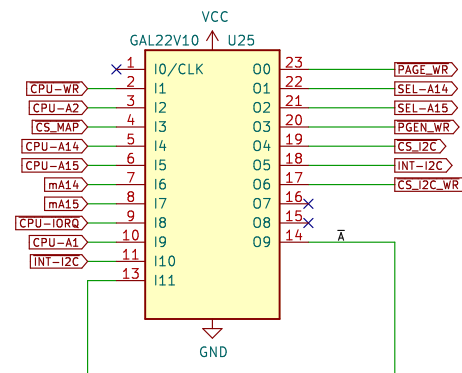
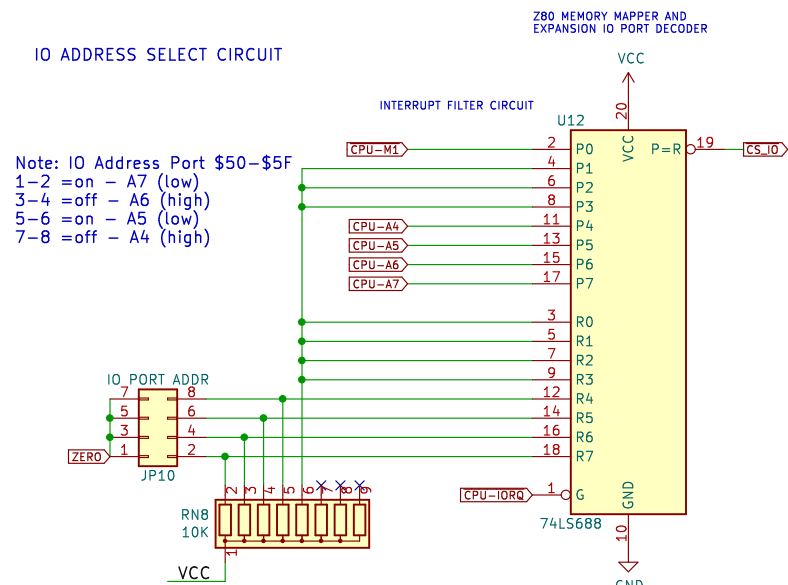
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NOTE: INTERRUPTS RELY ON 4700  
OHM PULL UP RESISTOR ON PROCESSOR

