

12345678

A

bus

power

buffers

B

File: bus.kicad_sch
TMS9995CPU

File: power.kicad_sch
GALS

File: buffers.kicad_sch
bus sharing

IO

C

File: TMS9995CPU.kicad_sch

File: GALS.kicad_sch

File: bussharing.kicad_sch

File: io.kicad_sch

D

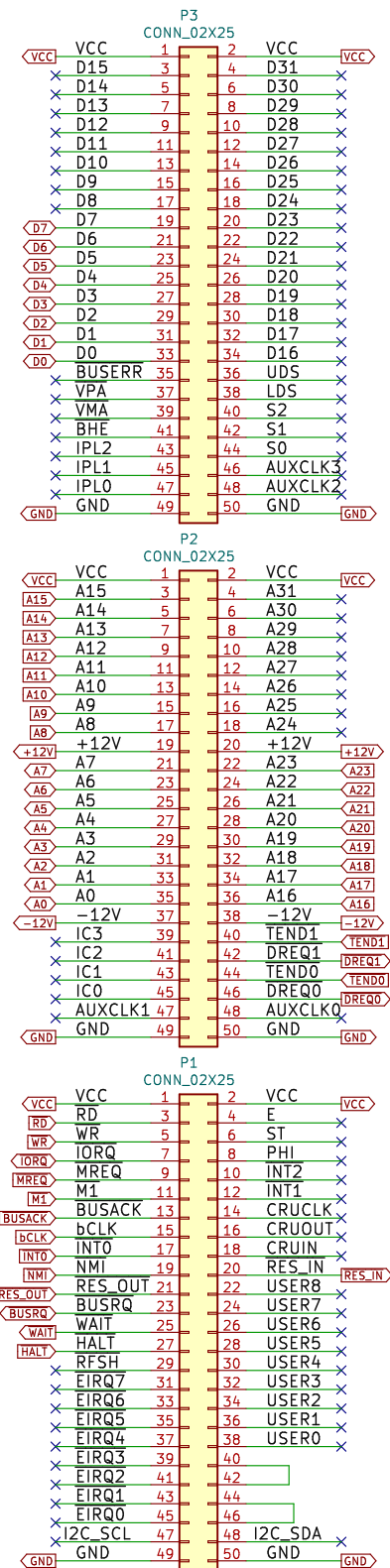
E

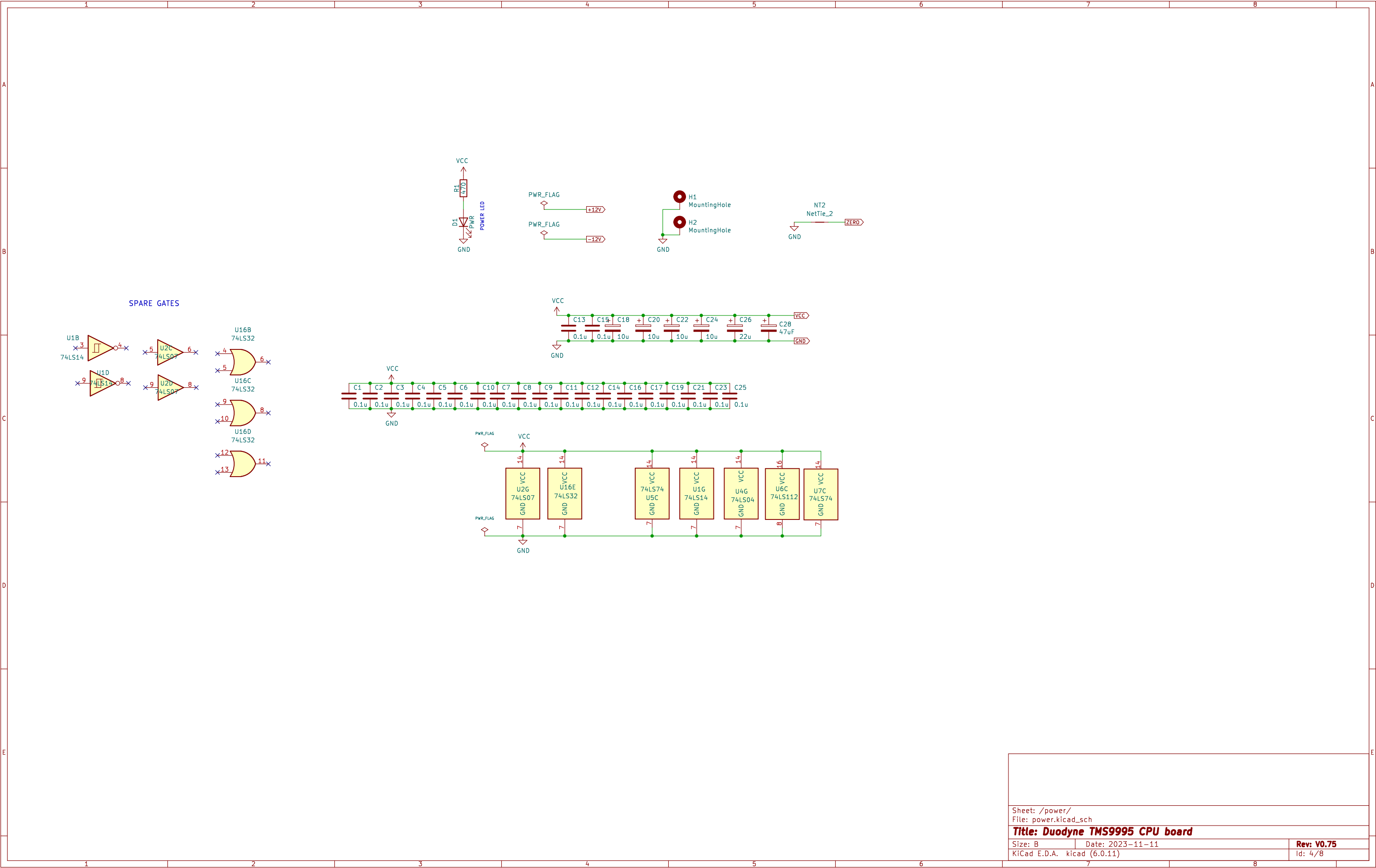
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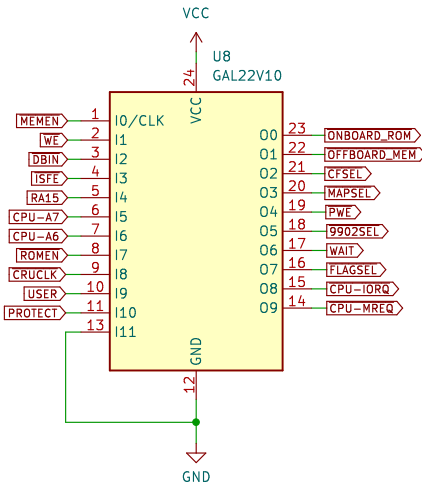
Sheet: /
File: processor.tms9995.kicad_sch

Title: Duodyne TMS9995 CPU board

Size: BDate: 2023-11-11KiCad E.D.A. kicad (6.0.11)Rev: V0.75Id: 1/8







$$\begin{aligned} &= \text{MEMEN} + \text{ROMEN} + \text{RA15} \\ &= \text{MEMEN} + !\text{ROMEN} * !\text{RA15} * \text{WE} + !\text{ISFE} * \text{RA15} \\ &= \text{MEMEN} + \text{ISFE} + !\text{RA15} + \text{CPU-A7} + \text{CPU-A6} + \text{USER} \\ &= \text{MEMEN} + \text{ISFE} + !\text{RA15} + \text{CPU-A7} + !\text{CPU-A6} + \text{USER} \\ &= \text{WE} + \text{PROTECT} * \text{USER} \\ &= !\text{MEMEN} + \text{ISFE} + \text{RA15} + \text{CPU-A7} + \text{CPU-A6} + \text{USER} \\ &= !\text{ROMSEL} + !\text{CFSSEL} \\ &= \text{CRUCLK} + \text{ISFE} + \text{RA15} + \text{CPU-A7} + !\text{CPU-A6} \\ &= \text{MEMEN} + \text{ISFE} + !\text{RA15} + !\text{CPU-A7} + \text{CPU-A6} + \text{USER} \\ &= !\text{CPU-IORQ} + \text{OFFBOARD_MEM} \end{aligned}$$

Equation ('+' is 'OR', '*' is 'AND')

The memory map is shown in the table below.

Memory Address	Mapped To
>0000 - >7FFF	ROM when enabled, otherwise RAM
>8000 - >EFFF	RAM
>F000 - >F0FB	TMS 9995 internal RAM
>F0FC - >F0FF	RAM
>FE00 - >FE3F	CF card ATA registers (FIX INCOMPLETE DECODING WITH NEXT REVISION)
>FE40 - >FE7F	Memory mapper registers 0-15 (>FE40 - >FE4F, repeats at >FE50 etc. . . FIX INCOMPLETE DECODING WITH NEXT REVISION)
>FE80 - >FEBF	Offboard IO (ports \$80-\$BF)
>FEC0 - >FFFF	RAM
>FFFA - >FFFF	TMS 9995 internal RAM

CRU Address	Mapped To
>0000 - >003F	TMS 9902 registers
>0040 - >007F	Control signal latch (further details here)
(Plus processor internal CRU bits)	

Sheet: /GALS/
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Size: B	Date: 2023-11-11	Rev: V0.75
KiCad E.D.A. kicad (6.0.11)	Id: 5/8	

