bus

File: bus.kicad_sch

power

File: power.kicad_sch

buffers

File: buffers.kicad_sch

fpanel

File: fpanel.kicad_sch

6809CPU

File: 6809CPU.kicad_sch

GALS

File: GALS.kicad_sch

bus sharing

File: bussharing.kicad_sch

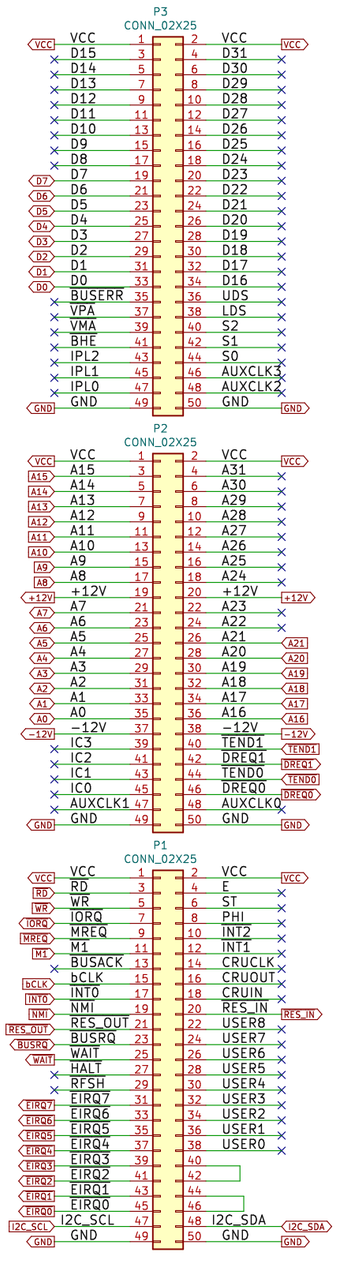
mapper

File: mapper.kicad_sch

Sheet: /
File: processor.6809.kicad_sch

Title: Duodyne 6809 CPU board

Size: B	Date: 2024-05-14	**Rev: V1.2**
KiCad E.D.A. kicad (6.0.11)		Id: 1/9



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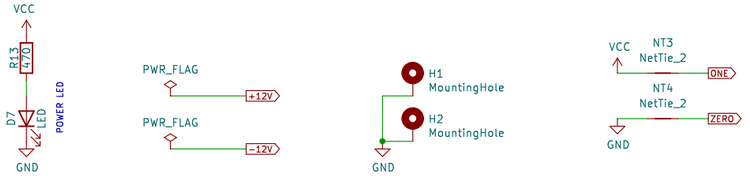
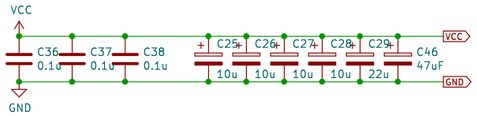
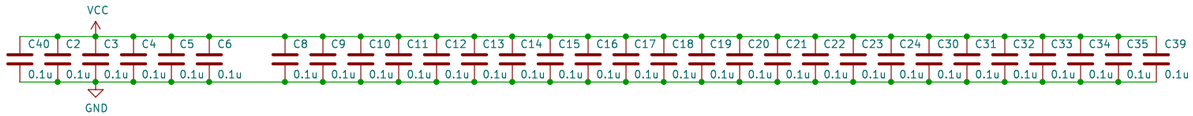
File: bus.kicad_sch

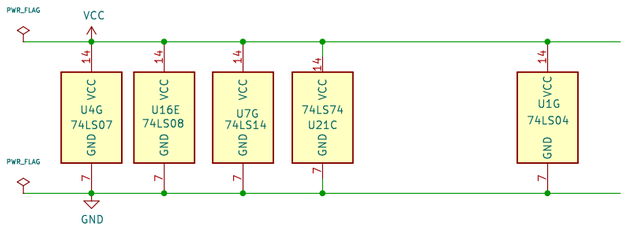
Title: Duodyne 6809 CPU board

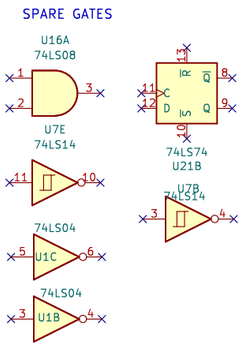
Size: B	Date: 2024-05-14	**Rev: V1.2**
KiCad E.D.A. kicad (6.0.11)		Id: 2/9











Sheet: /power/
File: power.kicad_sch

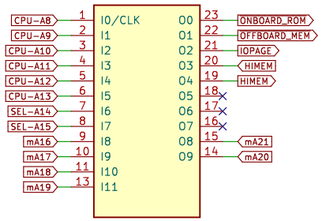
Title: Duodyne 6809 CPU board

Size: B	Date: 2024-05-14	**Rev: V1.2**
KiCad E.D.A. kicad (6.0.11)		Id: 4/9

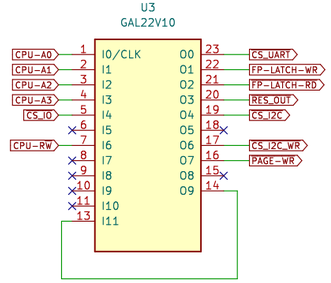
IO Address Port $50-$5F

$50 PAGER BANK 0(WR)
$51 PAGER BANK 1(WR)
$52 PAGER BANK 2(WR)
$53 PAGER BANK 3(WR)
$54 Front Panel (RW)
$55 RESET SYSTEM
$56-$57 I2C(RW)
$58-$5F UART (RW)

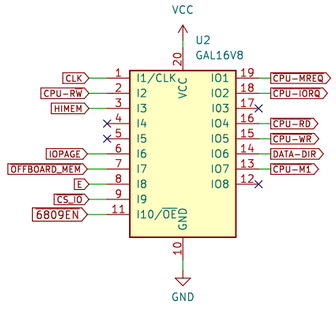
ADDRESS DECODER



IO DECODER

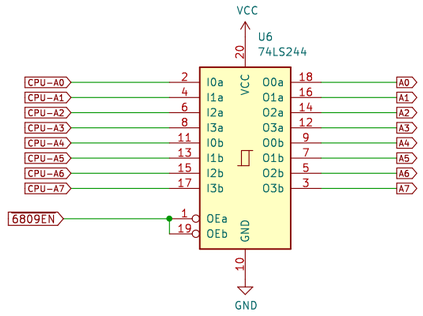


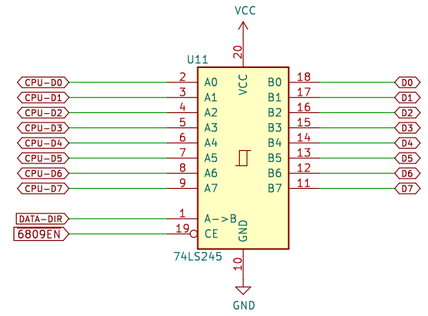
BUS SIGNALS

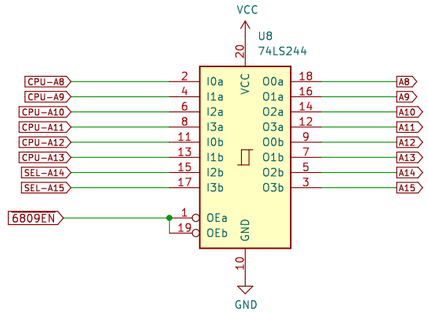


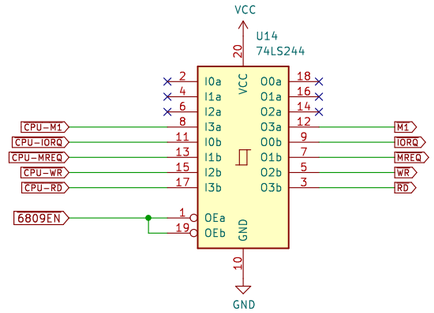
Sheet: /GALS/		
File: GALS.kicad_sch		
Title: Duodyne 6809 CPU board		
Size: B	Date: 2024-05-14	**Rev: V1.2**
KiCad E.D.A. kicad (6.0.11)		Id: 5/9

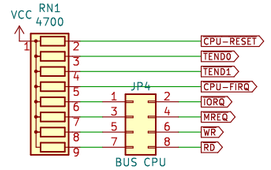
Z80 BUS INTERFACE

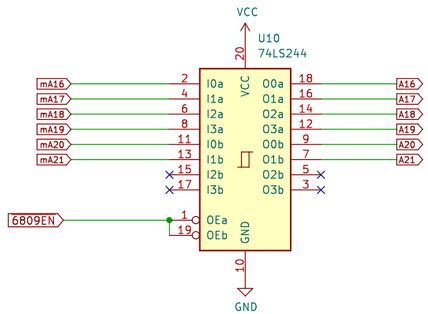


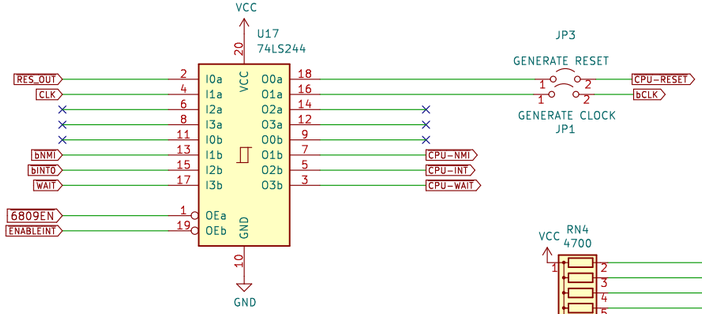


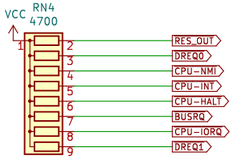


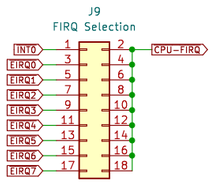


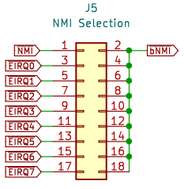


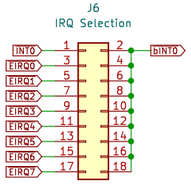










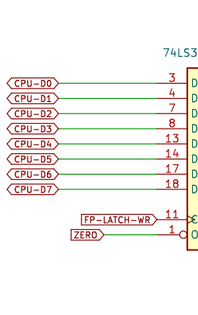


Sheet: /buffers/
File: buffers.kicad_sch

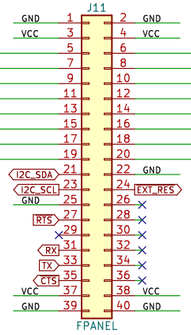
Title: Duodyne 6809 CPU board

Size: B	Date: 2024-05-14	**Rev: V1.2**
KiCad E.D.A. kicad (6.0.11)		Id: 6/9

FRONT PANEL LED OUTPUT



U33 NOTE: USE 74HCT374 TO SOURCE OR SINK ADEQUATE CURRENT TO DRIVE LEDS ON FRONT PANEL



J11 NOTE:

PINS 5, 7, 9, 11, 13, 15, 17, 19 ARE FOR LED STATUS FOR ROMWBW FRONT PANEL INDICATOR

PINS 6, 8, 10, 12, 14, 16, 18, 20 ARE FOR SWITCH INPUTS FOR ROMWBW FRONT PANEL

PINS 21, 23 ARE FOR I2C CONNECTION (SDA & SCL)

PINS 25, 27, 29, 31, 33, AND 35 ARE FOR TTL SERIAL CONNECTOR TO UART

PINS 29, 37 ARE FOR SERIAL VCC POWER ENABLE

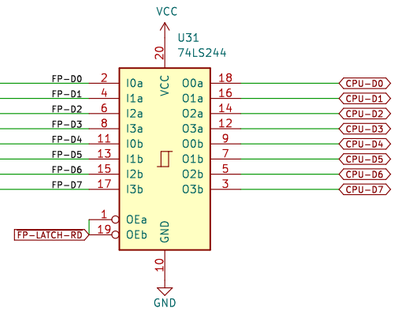
PINS 22, 24 ARE FOR EXTERNAL RESET SWITCH

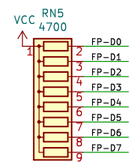
PINS 26, 28 ARE FOR IM2 CIRCUIT ENABLE

PINS 30, 32 ARE FOR INTERRUPT 0 ENABLE

PINS 34, 36 ARE FOR WAIT STATE CIRCUIT ENABLE

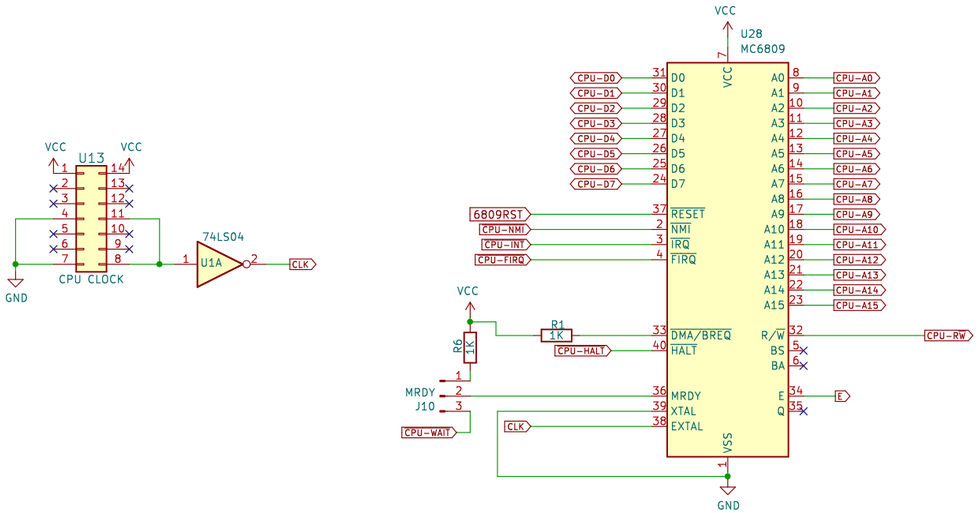
FRONT PANEL SWITCH INPUT

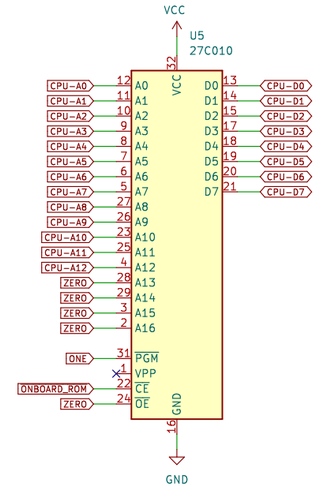


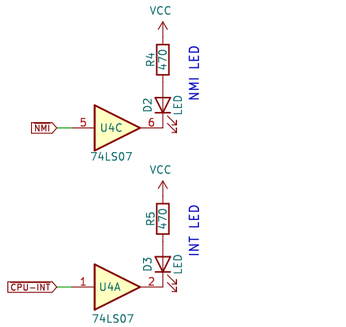


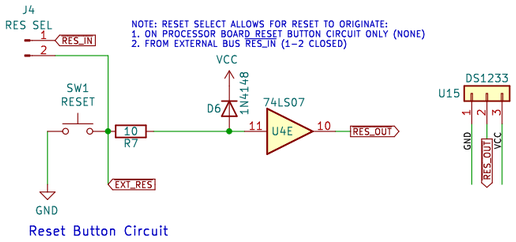
Sheet: /fpanel/		
File: fpanel.kicad_sch		
Title: Duodyne 6809 CPU board		
Size: B	Date: 2024-05-14	**Rev: V1.2**
KiCad E.D.A. kicad (6.0.11)		Id: 8/9

PROCESSOR, 6809









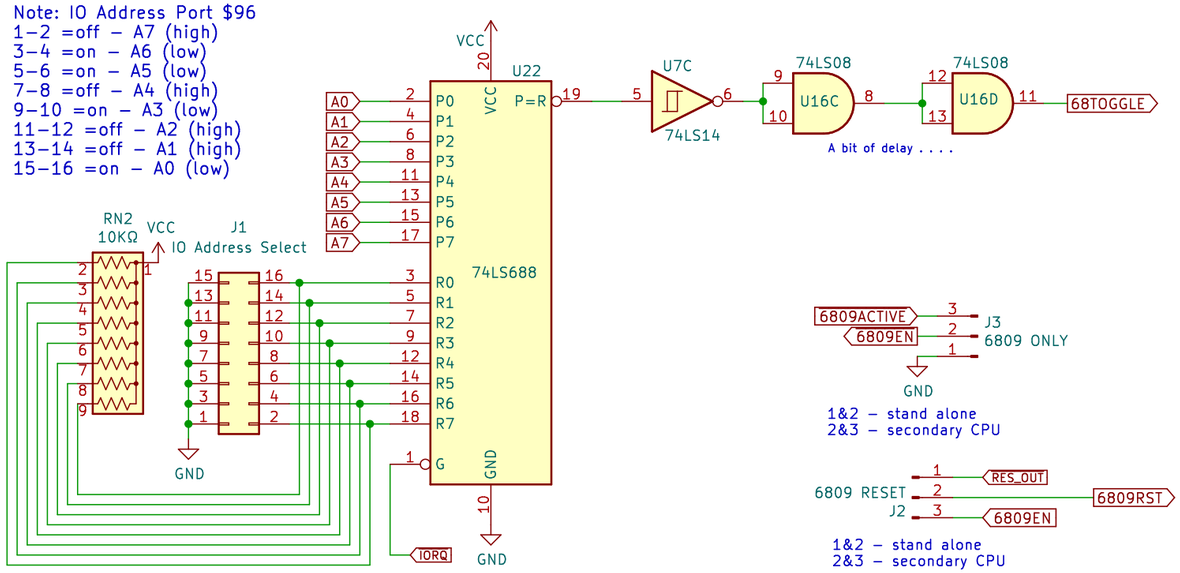
NOTE: RESET SELECT ALLOWS FOR RESET TO ORIGINATE:
1. ON PROCESSOR BOARD RESET BUTTON CIRCUIT ONLY (NONE)
2. FROM EXTERNAL BUS RES_IN (1-2 CLOSED)

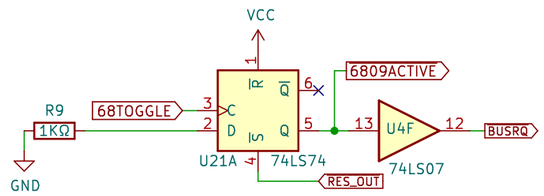
Sheet: /6809CPU/
File: 6809CPU.kicad_sch

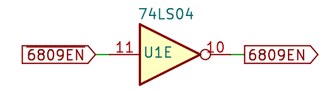
Title: Duodyne 6809 CPU board

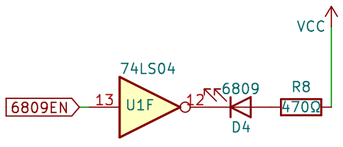
Size: USLedger	Date: 2024-05-14	**Rev: V1.2**
KiCad E.D.A. kicad (6.0.11)		Id: 9/9

Note: IO Address Port $96
1–2 =off – A7 (high)
3–4 =on – A6 (low)
5–6 =on – A5 (low)
7–8 =off – A4 (high)
9–10 =on – A3 (low)
11–12 =off – A2 (high)
13–14 =off – A1 (high)
15–16 =on – A0 (low)

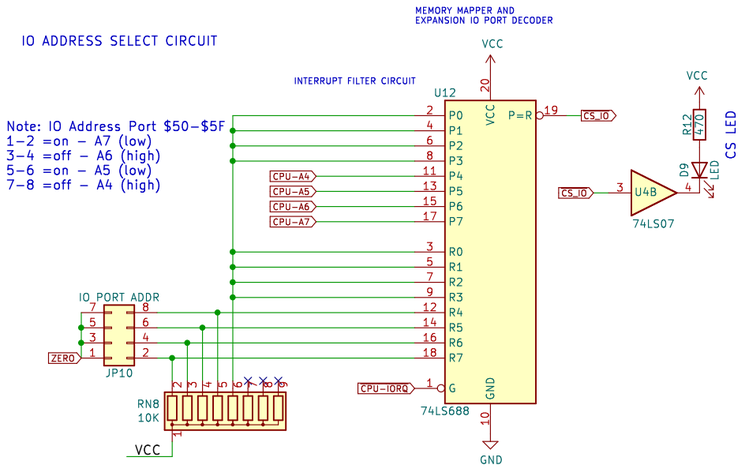


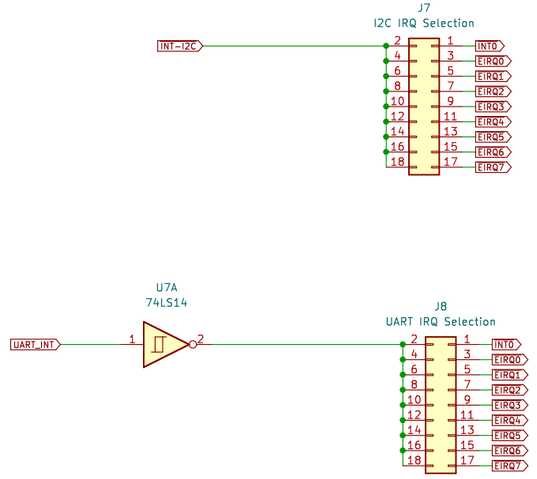


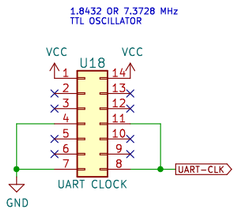


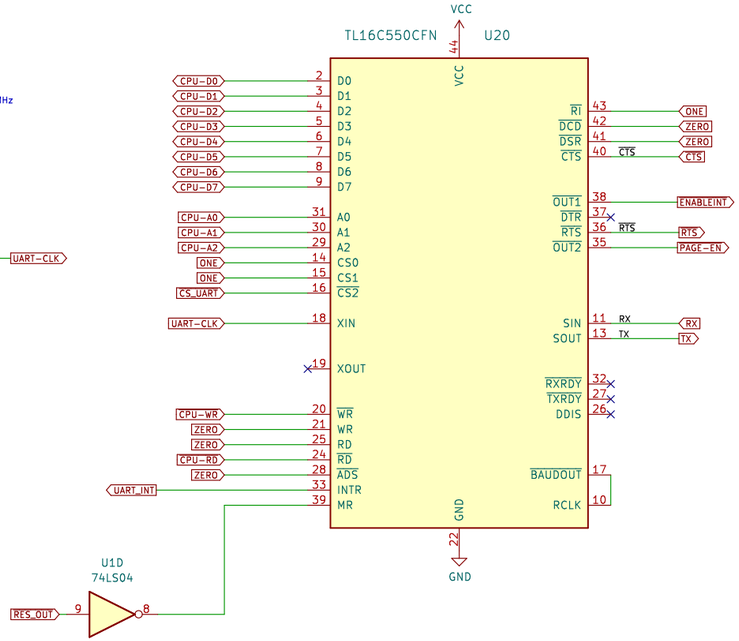


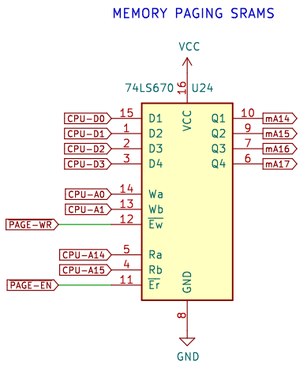
Sheet: /bus sharing/ File: bussharing.kicad_sch		
Title: Duodyne 6809 CPU board		
Size: A4	Date: 2024-05-14	**Rev: V1.2**
KiCad E.D.A. kicad (6.0.11)		Id: 9/9

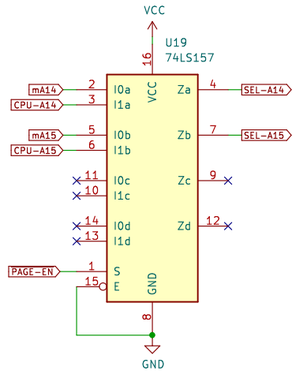


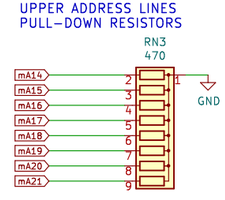


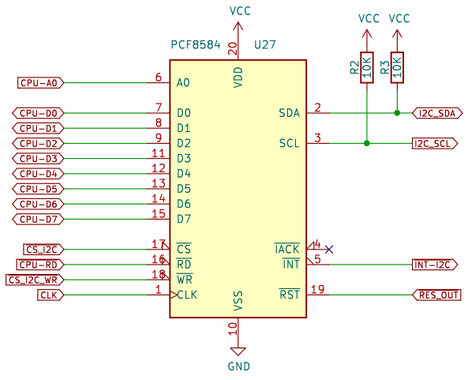












Sheet: /mapper/
File: mapper.kicad_sch

Title: Duodyne 6809 CPU board

Size: B	Date: 2024-05-14	**Rev: V1.2**
KiCad E.D.A. kicad (6.0.11)		Id: 11/9