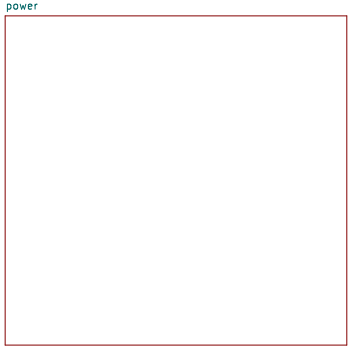
bus

File: bus.kicad_sch

power

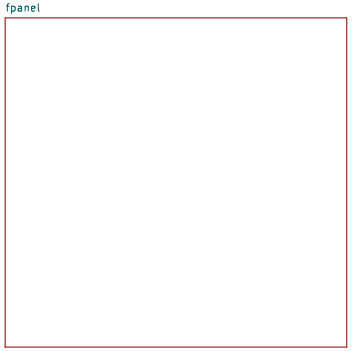


File: power.kicad_sch

buffers

File: buffers.kicad_sch

fpanel

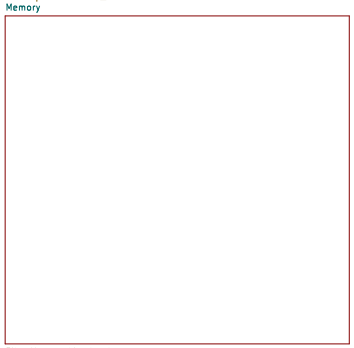


File: fpanel.kicad_sch

80C188CPU

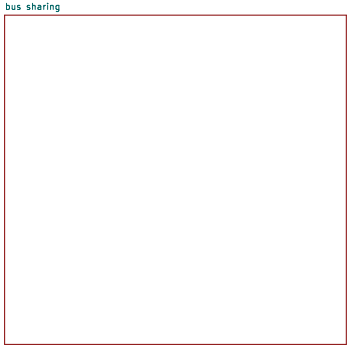
File: CPU_80C188.kicad_sch

Memory



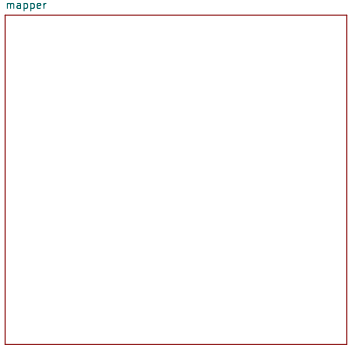
File: Memory.kicad_sch

bus sharing



File: bussharing.kicad_sch

mapper



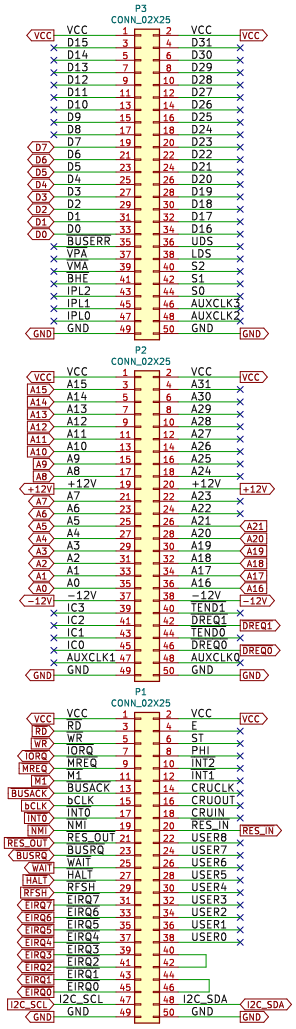
File: mapper.kicad_sch

RetroBrew Computer Group
Based on a design by John R Coffman.

Sheet: /
File: processor.80C188.kicad_sch

Title: Duodyne 80C188 CPU board

Size: B	Date: 2024-10-20	**Rev: V0.8**
KiCad E.D.A. kicad (6.0.11)		Id: 1/9

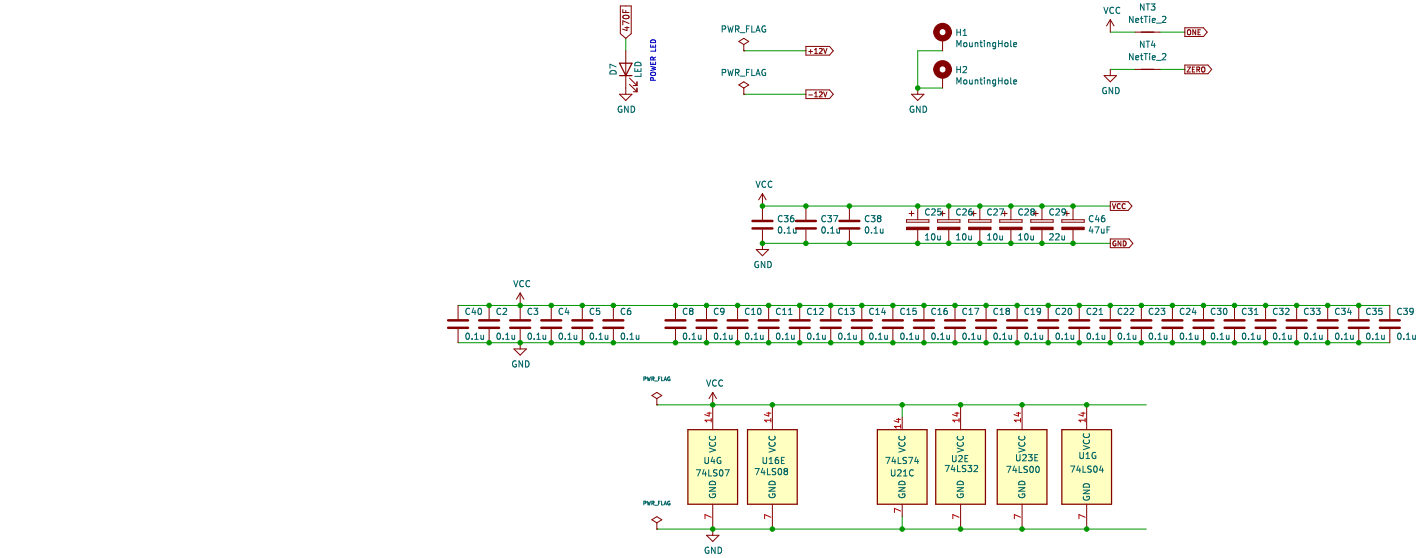


RetroBrew Computer Group
Based on a design by John R Coffman.

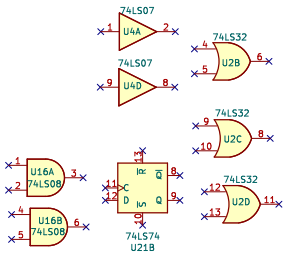
Sheet: /bus/
File: bus.kicad_sch

Title: Duodyne 80C188 CPU board

Size: B	Date: 2024-10-20	**Rev: V0.8**
KiCad E.D.A. kicad (6.0.11)		Id: 2/9



SPARE GATES

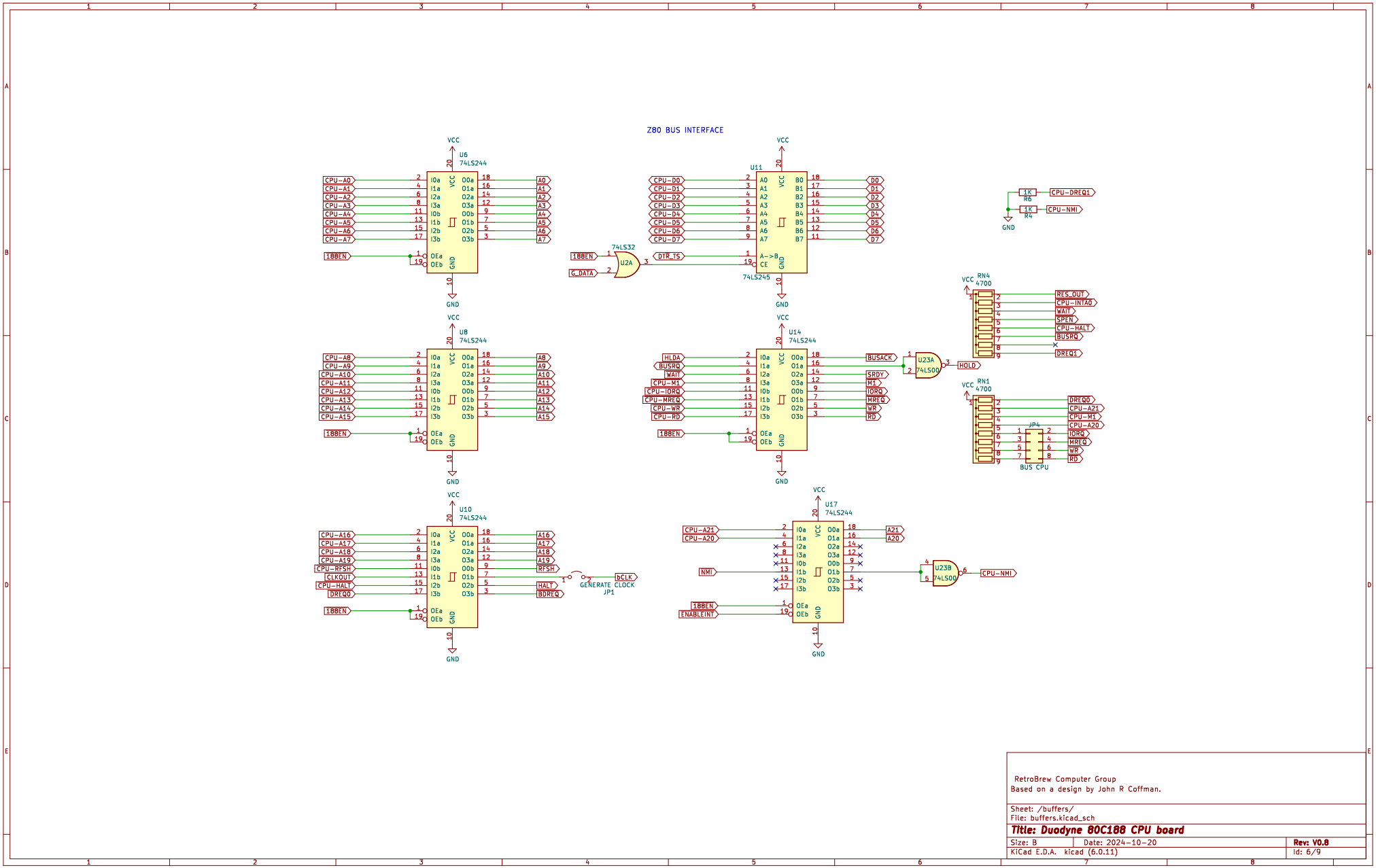


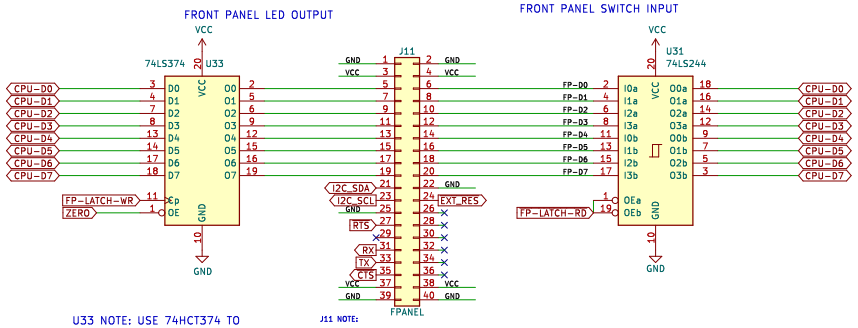
RetroBrew Computer Group
Based on a design by John R Coffman.

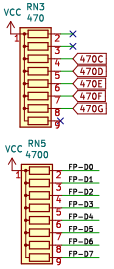
Sheet: /power/
File: power.kicad_sch

Title: Duodyne 80C188 CPU board

Size: B	Date: 2024-10-20	**Rev: V0.8**
KiCad E.D.A. kicad (6.0.11)		Id: 4/9


Z80 BUS INTERFACE
U6
74LS244
U8
74LS244
U10
74LS244
U11
74LS245
U14
74LS244
U17
74LS244
U2A
74LS32
U23A
74LS00
U23B
74LS00
RN4
4700
RN1
4700
JP4
BUS CPU
JP1
GENERATE CLOCK
R6
1K
R4
1K
CPU-DREQ1
CPU-NMI
RetroBrew Computer Group
Based on a design by John R Coffman.
Sheet: /buffers/
File: buffers.kicad_sch
Title: Duodyne 80C188 CPU board
Size: B
Date: 2024-10-20
Rev: V0.8
KiCad E.D.A. kicad (6.0.11)
Id: 6/9



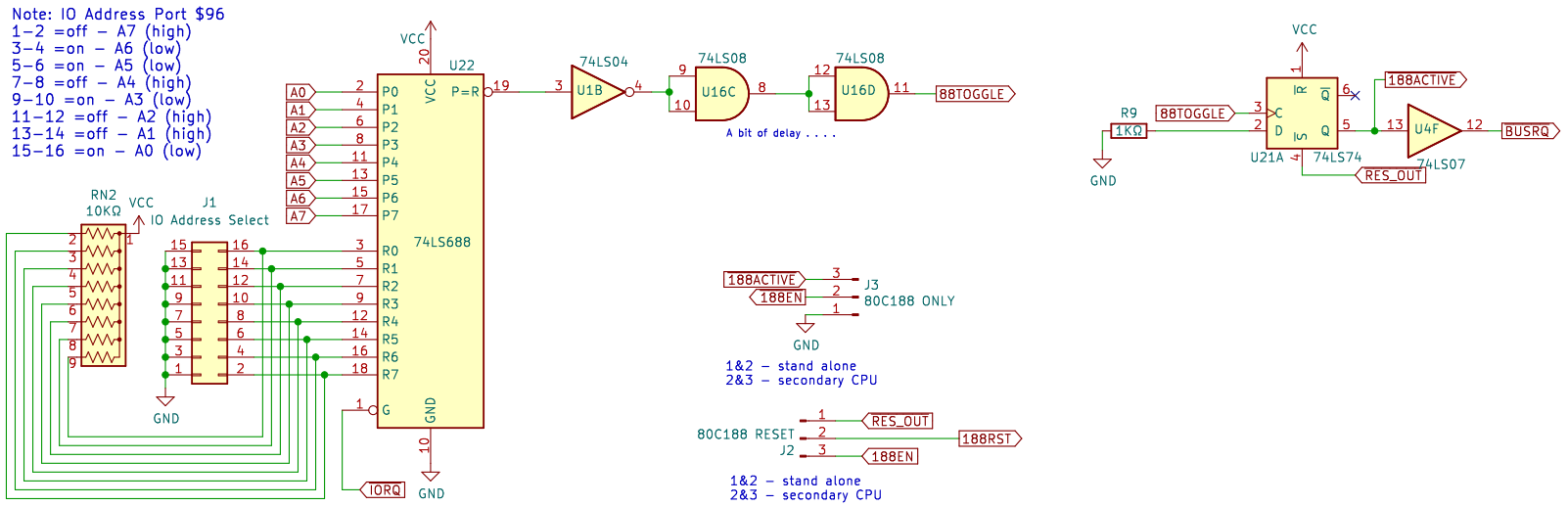


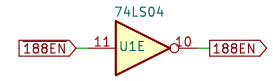
RetroBrew Computer Group
Based on a design by John R Coffman.

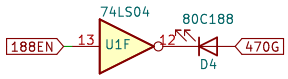
Sheet: /fpanel/
File: fpanel.kicad_sch

Title: Duodyne 80C188 CPU board

Size: B	Date: 2024-10-20	**Rev: V0.8**
KiCad E.D.A. kicad (6.0.11)		Id: 8/9





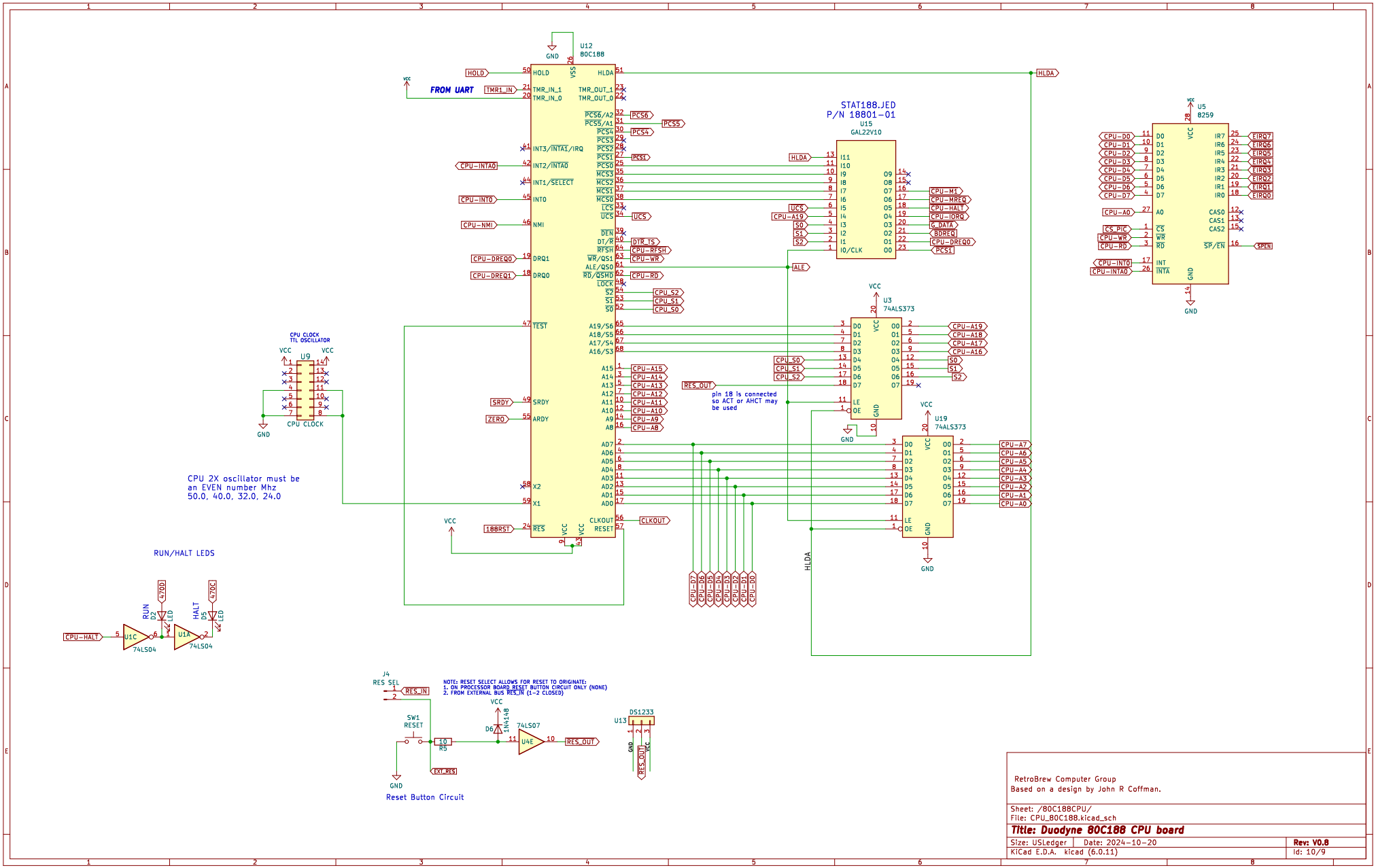


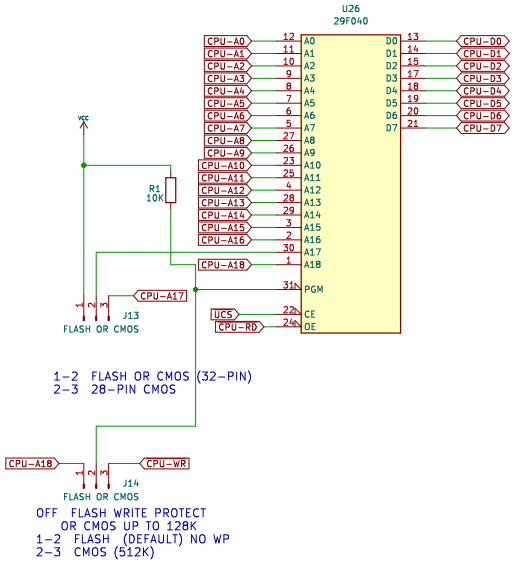
RetroBrew Computer Group
Based on a design by John R Coffman.

Sheet: /bus sharing/
File: bussharing.kicad_sch

Title: Duodyne 80C188 CPU board

Size: A4	Date: 2024-10-20	**Rev: V0.8**
KiCad E.D.A. kicad (6.0.11)		Id: 9/9


U12
80C188
FROM UART
TMR1_IN
HOLD
HLDA
INT3/INTA1/IRQ
INT2/INTA0
INT1/SELECT
INT0
NMI
DRQ1
DRQ0
TEST
SRDY
ARDY
X2
X1
RES
CLKOUT
RESET
CPU-INTA0
CPU-INT0
CPU-NMI
CPU-DREQ0
CPU-DREQ1
188RST
STAT188.JED
P/N 18801-01
U15
GAL22V10
U3
74ALS373
U19
74ALS373
U5
8259
CPU CLOCK
TTL OSCILLATOR
U9
CPU CLOCK
CPU_2X oscillator must be
an EVEN number Mhz
50.0, 40.0, 32.0, 24.0
pin 18 is connected
so ACT or AHCT may
be used
RUN/HALT LEDS
RUN
HALT
74LS04
J4
RES SEL
SW1
RESET
D6
1N4148
74LS07
DS1233
NOTE: RESET SELECT ALLOWS FOR RESET TO ORIGINATE:
1. ON PROCESSOR BOARD RESET BUTTON CIRCUIT ONLY (NONE)
2. FROM EXTERNAL BUS RES_IN (1-2 CLOSED)
Reset Button Circuit
RetroBrew Computer Group
Based on a design by John R Coffman.
Sheet: /80C188CPU/
File: CPU_80C188.kicad_sch
Title: Duodyne 80C188 CPU board
Size: USLedger
Date: 2024-10-20
KiCad E.D.A. kicad (6.0.11)
Rev: V0.8
Id: 10/9



ROM

FLASH 39SF010 (128K)
ALTERNATES: 39SF020, 29F020, 29F010
39SF040, 29F040 (512K) NOT RECOMMENDED

CMOS 27C010 (128K, 32pin)
ALTERNATE 27C020
28pin: 27C512(64K), 27C256(32K)

DEFAULT CHIP: 39SF010 (128K FLASH)
DEFAULT JUMPERS: 1-2, 1-2 (BOTH)

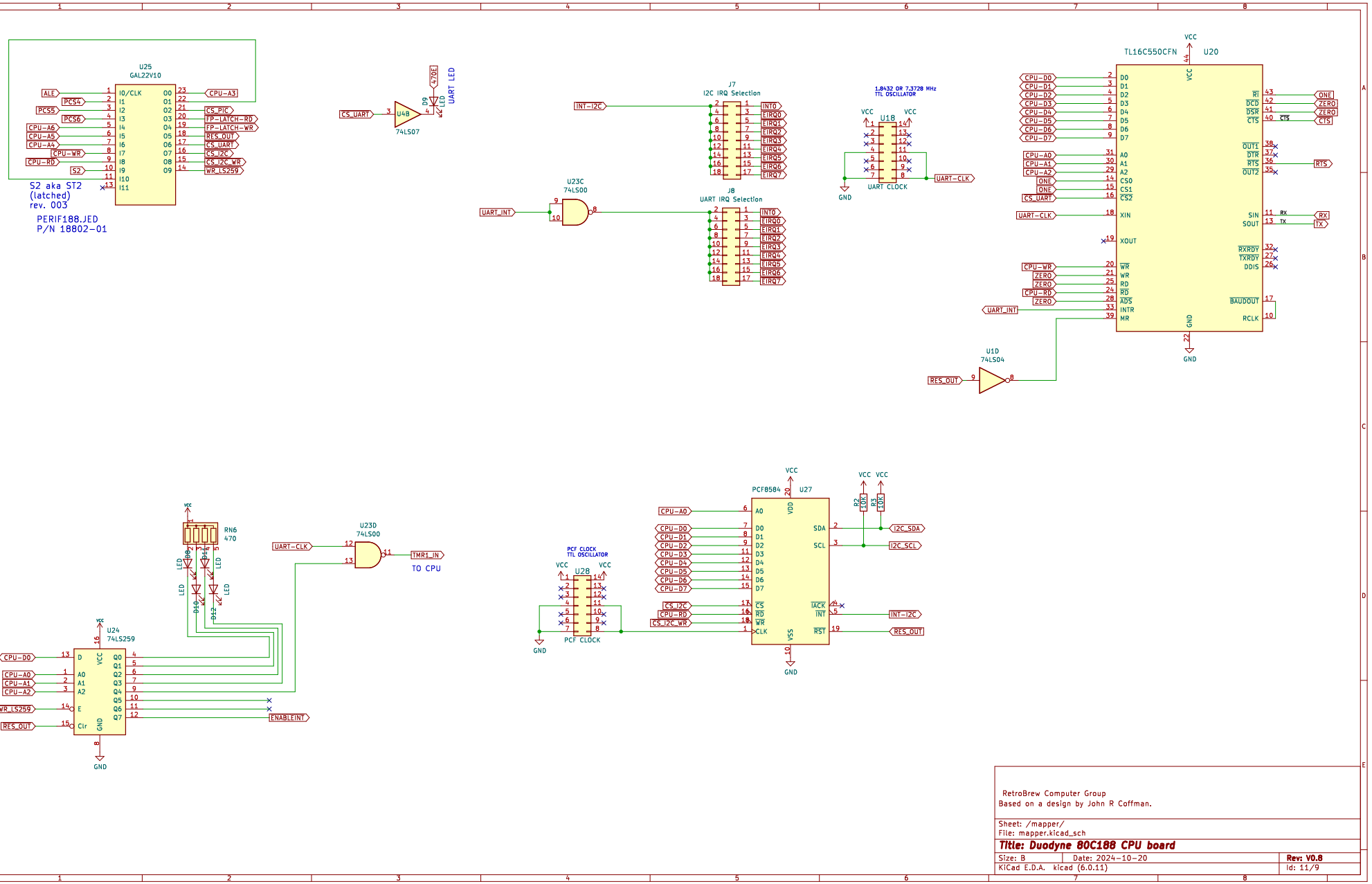
29F040 SHOWS ALL PIN ASSIGNMENTS

RetroBrew Computer Group
Based on a design by John R Coffman.

Sheet: /Memory/
File: Memory.kicad_sch

Title: Duodyne 80C188 CPU board

Size: USLedger | Date: 2024-10-20 | **Rev: V0.8**
KiCad E.D.A. kicad (6.0.11) | Id: 10/9


U25
GAL22V10
S2 aka ST2
(latched)
rev. 003
PERIF188.JED
P/N 18802-01
U4B
74LS07
UART LED
J7
I2C IRQ Selection
J8
UART IRQ Selection
U23C
74LS00
1.8432 OR 7.3728 MHz
TTL OSCILLATOR
U18
UART CLOCK
TL16C550CFN
U20
U1D
74LS04
U23D
74LS00
TO CPU
RN6
470
U24
74LS259
PCF8584
U27
PCF CLOCK
TTL OSCILLATOR
U28
PCF CLOCK
RetroBrew Computer Group
Based on a design by John R Coffman.
Sheet: /mapper/
File: mapper.kicad_sch
Title: Duodyne 80C188 CPU board
Size: B
Date: 2024-10-20
Rev: V0.8
KiCad E.D.A. kicad (6.0.11)
Id: 11/9