bus

File: bus.kicad_sch

power

File: power.kicad_sch

buffers

File: buffers.kicad_sch

fpanel

File: fpanel.kicad_sch

Z80CPU

File: Z80CPU.kicad_sch

DMA

File: DMA.kicad_sch

CPLDs

File: CPLDs.kicad_sch

IM2

File: IM2.kicad_sch

waitstate

File: waitstate.kicad_sch

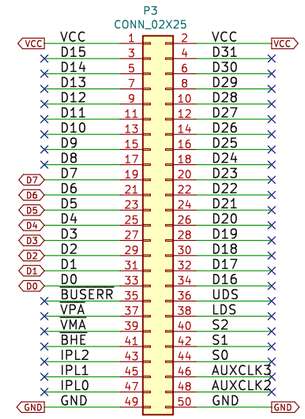
mapper

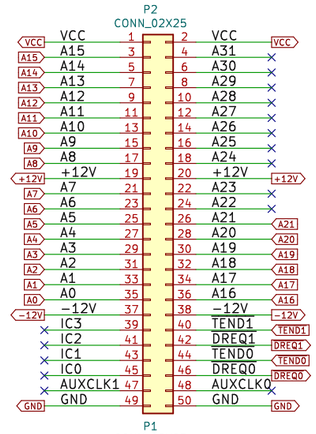
File: mapper.kicad_sch

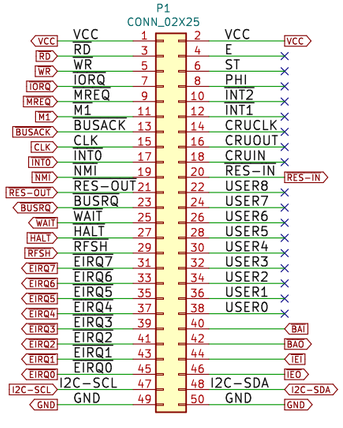
Sheet: /
File: Slick.kicad_sch

Title:

Size: B	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.11)		Id: 1/11



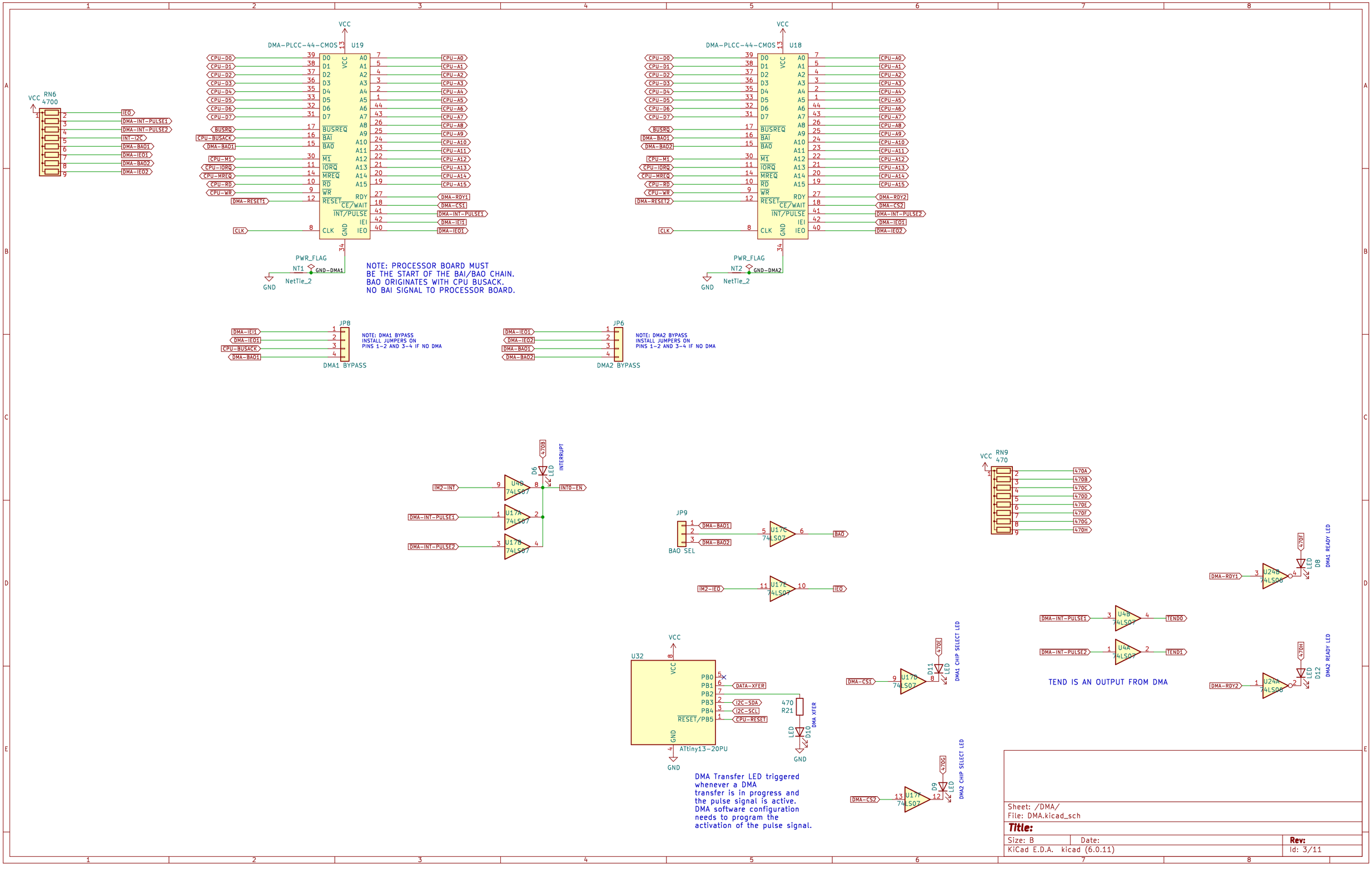


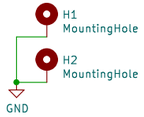


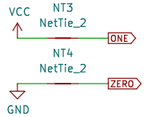
Sheet: /bus/
File: bus.kicad_sch

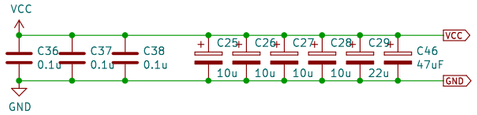
Title:

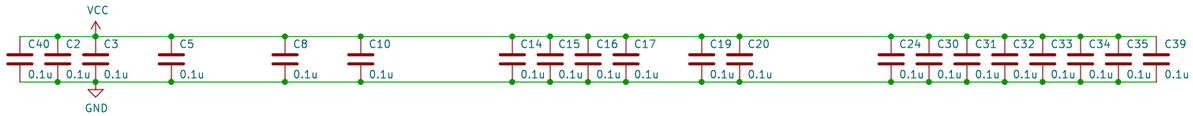
Size: B | Date: | **Rev:**
KiCad E.D.A. kicad (6.0.11) | Id: 2/11


DMA-PLCC-44-CMOS
U19
U18
VCC
GND
CPU-D0
CPU-D1
CPU-D2
CPU-D3
CPU-D4
CPU-D5
CPU-D6
CPU-D7
BUSRQ
CPU-BUSACK
DMA-BAO1
DMA-BAO2
CPU-M1
CPU-IORQ
CPU-MREQ
CPU-RD
CPU-WR
DMA-RESET1
DMA-RESET2
CLK
CPU-A0
CPU-A1
CPU-A2
CPU-A3
CPU-A4
CPU-A5
CPU-A6
CPU-A7
CPU-A8
CPU-A9
CPU-A10
CPU-A11
CPU-A12
CPU-A13
CPU-A14
CPU-A15
DMA-RDY1
DMA-RDY2
DMA-CS1
DMA-CS2
DMA-INT-PULSE1
DMA-INT-PULSE2
DMA-IEI1
DMA-IEI2
DMA-IEO1
DMA-IEO2
PWR_FLAG
NT1
NT2
GND-DMA1
GND-DMA2
NetTie_2
RN6
4700
INT-I2C
RN9
470
470A
470B
470C
470D
470E
470F
470G
470H
NOTE: PROCESSOR BOARD MUST
BE THE START OF THE BAI/BAO CHAIN.
BAO ORIGINATES WITH CPU BUSACK.
NO BAI SIGNAL TO PROCESSOR BOARD.
JP8
DMA1 BYPASS
NOTE: DMA1 BYPASS
INSTALL JUMPERS ON
PINS 1-2 AND 3-4 IF NO DMA
JP6
DMA2 BYPASS
NOTE: DMA2 BYPASS
INSTALL JUMPERS ON
PINS 1-2 AND 3-4 IF NO DMA
JP9
BAO SEL
BAO
IM2-INT
INT0-EN
INTERRUPT
IM2-IEO
IEO
U48
74LS07
U17A
U17B
U17C
U17E
U17F
U24A
U24B
U4A
U4B
74LS08
D6
D8
D9
D10
D11
D12
LED
DMA1 READY LED
DMA2 READY LED
DMA1 CHIP SELECT LED
DMA2 CHIP SELECT LED
DMA XFER
TEND0
TEND1
TEND IS AN OUTPUT FROM DMA
U32
ATtiny13-20PU
PB0
PB1
PB2
PB3
PB4
RESET/PB5
DATA-XFER
I2C-SDA
I2C-SCL
CPU-RESET
R21
DMA Transfer LED triggered
whenever a DMA
transfer is in progress and
the pulse signal is active.
DMA software configuration
needs to program the
activation of the pulse signal.
Sheet: /DMA/
File: DMA.kicad_sch
Title:
Size: B
Date:
Rev:
KiCad E.D.A. kicad (6.0.11)
Id: 3/11

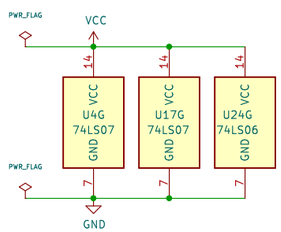








SPARE GATES



Sheet: /power/		
File: power.kicad_sch		
Title:		
Size: B	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.11)		Id: 4/11

REMOVE JUMPER
BEFORE CPLD
PROGRAMMING

JP1
CPLD VCC1

PWR_FLAG

C41 C42 C43 C44 C45 C47 C48 C49
0.1u 0.1u 0.1u 0.1u 0.1u 0.1u 0.1u 0.1u

REMOVE JUMPER
BEFORE CPLD
PROGRAMMING

JP2
CPLD VCC2

PWR_FLAG

C50 C51 C52 C53 C54 C55 C56 C57
0.1u 0.1u 0.1u 0.1u 0.1u 0.1u 0.1u 0.1u

J7
JTAG CONNECTOR
EPM7064S #1

U12
EPM7064S-PLCC-84

CPLD1-CPU

J10
JTAG CONNECTOR
EPM7064S #2

U13
EPM7064S-PLCC-84

CPLD2-DMA

DMA ADDRESS
DMA ADDR

IO ADDRESS
IO ADDR

RN2
10K

IO ADDRESS SELECT CIRCUIT
DMA1, DMA2, FRONT-PANEL, DMA LATCH

Note: IO Address Port $40-$43
1-2 =on - A7 (low)
3-4 =off - A6 (high)
5-6 =on - A5 (low)
7-8 =on - A4 (low)
9-10 =on - A3 (low)
11-12 =on - A2 (low)

IO ADDRESS SELECT CIRCUIT
UART, MAPPER, I2C

Note: IO Address Port $50-$5F
1-2 =on - A7 (low)
3-4 =off - A6 (high)
5-6 =on - A5 (low)
7-8 =off - A4 (high)

NT5
NetTie_2

NT6
NetTie_2

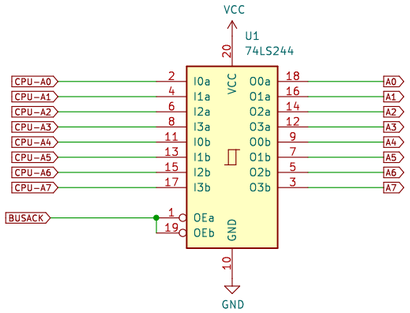
NT7
NetTie_2

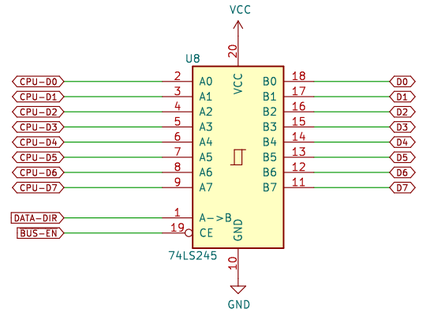
U4F
74LS07

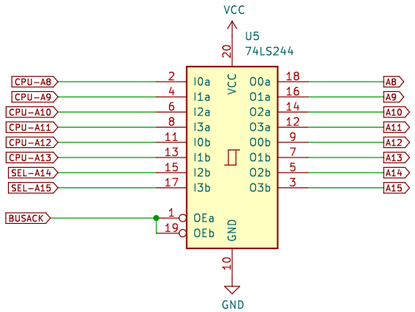
WAIT LED

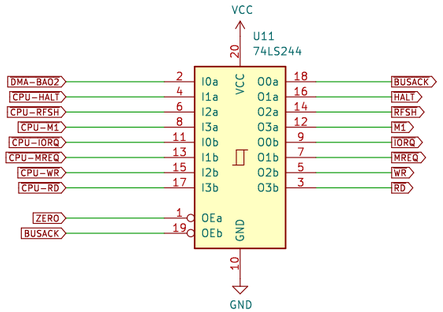
Sheet: /CPLDs/	
File: CPLDs.kicad_sch	
Title:	
Size: B	Date:
KiCad E.D.A. kicad (6.0.11)	Rev: Id: 5/11

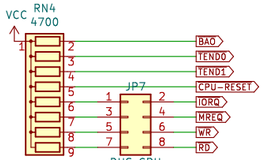
Z80 BUS INTERFACE

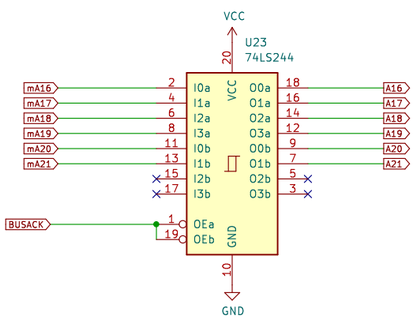


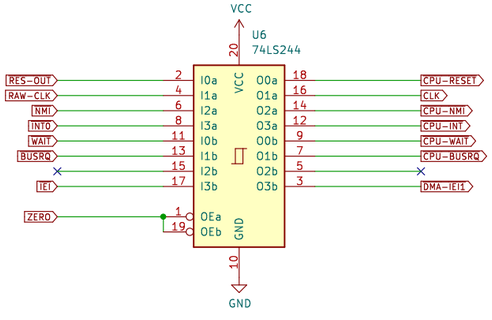


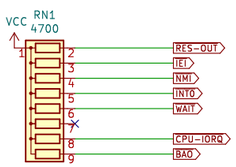


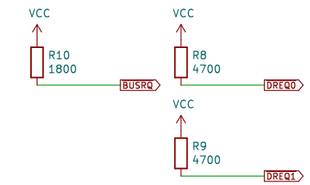












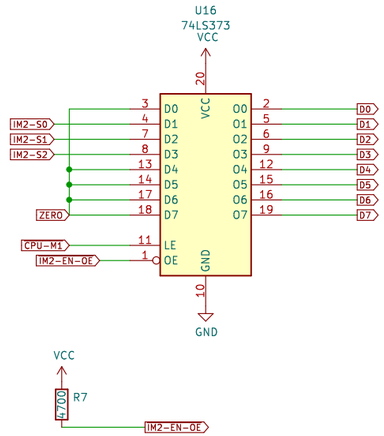
Sheet: /buffers/
File: buffers.kicad_sch

Title:

Size: B | Date: | **Rev:**

KiCad E.D.A. kicad (6.0.11) | Id: 6/11

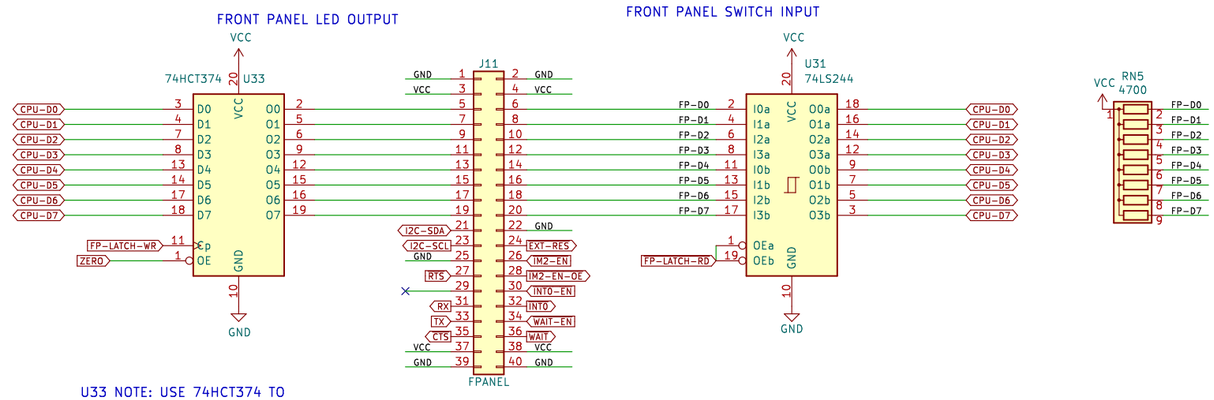
Interrupt Mode 2 (IM2) Circuit



Sheet: /IM2/
File: IM2.kicad_sch

Title:

Size: B | Date: | **Rev:**
KiCad E.D.A. kicad (6.0.11) | Id: 7/11



U33 NOTE: USE 74HCT374 TO SOURCE OR SINK ADEQUATE CURRENT TO DRIVE LEDS ON FRONT PANEL

J11 NOTE:

PINS 5, 7, 9, 11, 13, 15, 17, 19 ARE FOR LED STATUS FOR ROMWBW FRONT PANEL INDICATOR

PINS 6, 8, 10, 12, 14, 16, 18, 20 ARE FOR SWITCH INPUTS FOR ROMWBW FRONT PANEL

PINS 21, 23 ARE FOR I2C CONNECTION (SDA & SCL)

PINS 25, 27, 29, 31, 33, AND 35 ARE FOR TTL SERIAL CONNECTOR TO UART

PINS 29, 37 ARE FOR SERIAL VCC POWER ENABLE

PINS 22, 24 ARE FOR EXTERNAL RESET SWITCH

PINS 26, 28 ARE FOR IM2 CIRCUIT ENABLE

PINS 30, 32 ARE FOR INTERRUPT 0 ENABLE

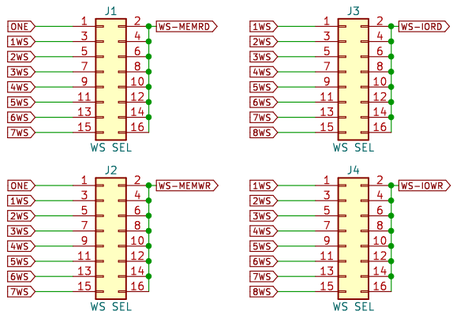
PINS 34, 36 ARE FOR WAIT STATE CIRCUIT ENABLE

Sheet: /fpanel/
File: fpanel.kicad_sch

Title:

Size: B | Date: | **Rev:**
KiCad E.D.A. kicad (6.0.11) | Id: 8/11

Wait State Generator Circuit



Sheet: /waitstate/	
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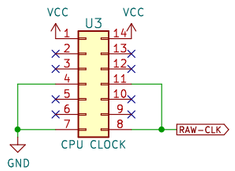
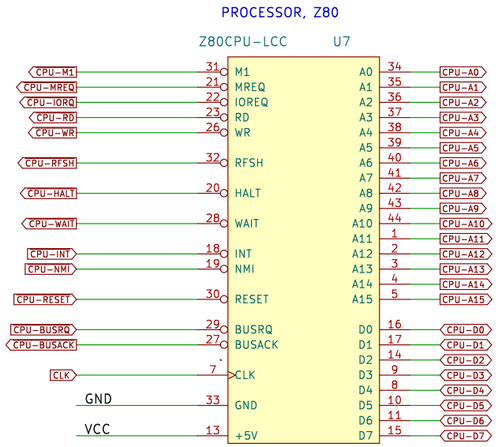
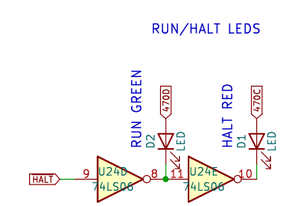
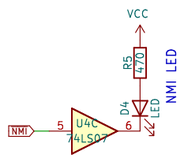
Title:	
Size: B	Date:
KiCad E.D.A. kicad (6.0.11)	Id: 9/11

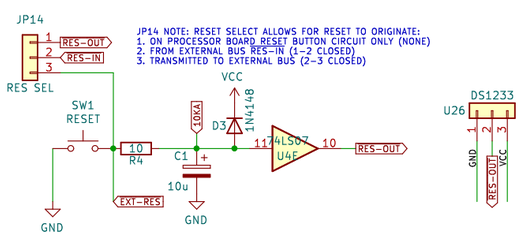






Tri-state address, data, & control bus during DMA





Reset Button Circuit

Sheet: /Z80CPU/		
File: Z80CPU.kicad_sch		
Title:		
Size: B	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.11)		Id: 10/11

1.8432 OR 7.3728 MHz
TTL OSCILLATOR

VCC VCC
U2
1 2 3 4 5 6 7 14 13 12 11 10 9 8
UART-CLK
UART CLOCK
GND

VCC
TL16C550CFN U14
44 VCC

CPU-D0	2	D0	
CPU-D1	3	D1	
CPU-D2	4	D2	
CPU-D3	5	D3	
CPU-D4	6	D4	
CPU-D5	7	D5	
CPU-D6	8	D6	
CPU-D7	9	D7	
CPU-A0	31	A0	
CPU-A1	30	A1	
CPU-A2	29	A2	
ONE	14	CS0	
ONE	15	CS1	
CS-UART	16	CS2	
UART-CLK	18	XIN	
	19	XOUT	
CPU-WR	20	WR	
ZERO	21	WR	
ZERO	25	RD	
CPU-RD	24	RD	
ZERO	28	ADS	
INT	33	INTR	
RESET	39	MR	
	43	RI	ONE
	42	DCD	ZERO
	41	DSR	ZERO
CTS	40	CTS	CTS
	38	OUT1	
	37	DTR	
RTS	36	RTS	RTS
	35	OUT2	
RX	11	SIN	RX
TX	13	SOUT	TX
	32	RXRDY	
	27	TXRDY	
	26	DDIS	
	17	BAUDOUT	
	10	RCLK	
	22	GND	

GND

MEMORY PAGING SRAMS

VCC
74LS670 U9
16 VCC GND 8

CPU-D0	15	D1	
CPU-D1	1	D2	
CPU-D2	2	D3	
CPU-D3	3	D4	
	10	Q1	mA14
	9	Q2	mA15
	7	Q3	mA16
	6	Q4	mA17
CPU-A0	14	Wa	
CPU-A1	13	Wb	
PAGE-WR	12	Ew	
CPU-A14	5	Ra	
CPU-A15	4	Rb	
PAGE-EN	11	Er	

GND

VCC
74LS670 U22
16 VCC GND 8

CPU-D4	15	D1	
CPU-D5	1	D2	
CPU-D6	2	D3	
CPU-D7	3	D4	
	10	Q1	mA18
	9	Q2	mA19
	7	Q3	mA20
	6	Q4	mA21
CPU-A0	14	Wa	
CPU-A1	13	Wb	
PAGE-WR	12	Ew	
CPU-A14	5	Ra	
CPU-A15	4	Rb	
PAGE-EN	11	Er	

GND

UPPER ADDRESS LINES
PULL-DOWN RESISTORS

RN7
470

mA14	2
mA15	3
mA16	4
mA17	5
mA18	6
mA19	7
mA20	8
mA21	9
	1

GND

VCC
U28
8 VCC GND 4

PB0	5	
PB1	6	UART-CLK
PB2	7	
PB3	2	I2C-SCL
PB4	3	I2C-SDA
RESET/PB5	1	CPU-RESET

ATtiny13-20PU
GND

OPTIONAL SYSTEM
TICK TIMER

R11
1000
Q1
2N3904
GND

J6
TICK INTERRUPT

1	2		
3	4		
5	6		
7	8		
9	10		
11	12		
13	14		
15	16		
		EIRQ0	EIRQ0
		EIRQ1	EIRQ1
		EIRQ2	EIRQ2
		EIRQ3	EIRQ3
		EIRQ4	EIRQ4
		EIRQ5	EIRQ5
		EIRQ6	EIRQ6
		EIRQ7	EIRQ7

VCC
PCF8584 U27
20 VDD VSS 10

CPU-A0	6	A0	
CPU-D0	7	D0	
CPU-D1	8	D1	
CPU-D2	9	D2	
CPU-D3	11	D3	
CPU-D4	12	D4	
CPU-D5	13	D5	
CPU-D6	14	D6	
CPU-D7	15	D7	
CS-I2C	17	CS	
CPU-RD	16	RD	
CS-I2C-WR	18	WR	
CLK	1	CLK	
		SDA	2
		SCL	3
	4	IACK	
	5	INT	INT-I2C
	19	RST	CPU-RESET

VCC VCC
R2 10K
R3 10K
I2C-SDA
I2C-SCL
GND

J12
I2C INTERRUPT

1	2		
3	4		
5	6		
7	8		
9	10		
11	12		
13	14		
15	16		
		EIRQ0	EIRQ0
		EIRQ1	EIRQ1
		EIRQ2	EIRQ2
		EIRQ3	EIRQ3
		EIRQ4	EIRQ4
		EIRQ5	EIRQ5
		EIRQ6	EIRQ6
		EIRQ7	EIRQ7

INT-I2C
U24F
74LS08
13 12

NOTE: INTERRUPTS RELY ON 4700
OHM PULL UP RESISTOR ON PROCESSOR

J5
UART INTERRUPT

1	2		
3	4		
5	6		
7	8		
9	10		
11	12		
13	14		
15	16		
		EIRQ0	EIRQ0
		EIRQ1	EIRQ1
		EIRQ2	EIRQ2
		EIRQ3	EIRQ3
		EIRQ4	EIRQ4
		EIRQ5	EIRQ5
		EIRQ6	EIRQ6
		EIRQ7	EIRQ7

INT
R1
4700
GND
U24E
74LS08
5 6

Sheet: /mapper/
File: mapper.kicad_sch

Title:

Size: B	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.11)		Id: 11/11