

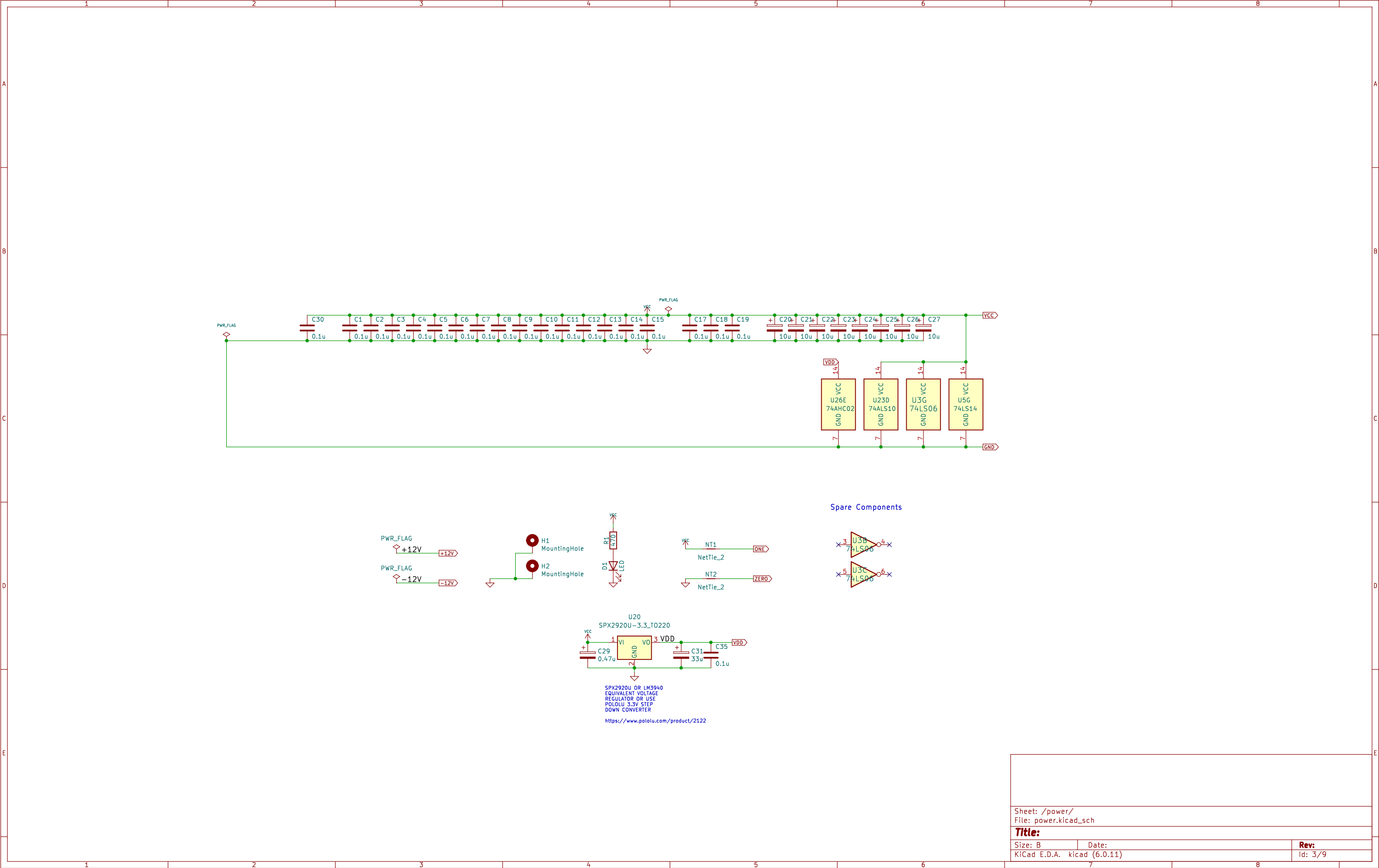
The diagram is a schematic layout of components arranged in a 2x4 grid. The components are labeled as follows:

- bus** (File: bus.kicad\_sch)
- PPIDE** (File: PPIDE.kicad\_sch)
- GAL** (File: GAL.kicad\_sch)
- IO** (File: IO.kicad\_sch)
- power** (File: power.kicad\_sch)
- FDC** (File: FDC.kicad\_sch)
- buffers** (File: buffers.kicad\_sch)
- WIZNET** (File: WIZNET.kicad\_sch)

The diagram is framed by a grid with columns 1-8 and rows A-E. The components are located in the top-left quadrant of the grid.



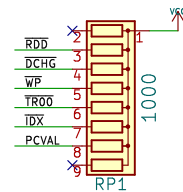
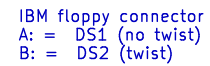
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KiCad E.D.A. kicad (6.0.11)		Id: 2/9



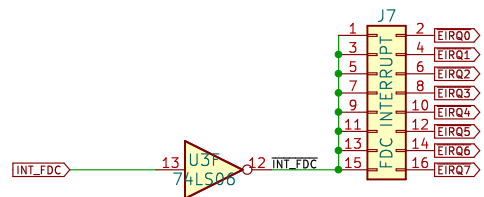


IO Ports

x0	read Main Status Register
x1	read/write Data In/Out
x2	read/write Terminal Count
x3	read/write User Reset FDC
x4	<none>
x5	write Load Control Register
x6	read DMA Acknowledge/write Load Operations Register
x7	read DMA Acknowledge and Terminal Count

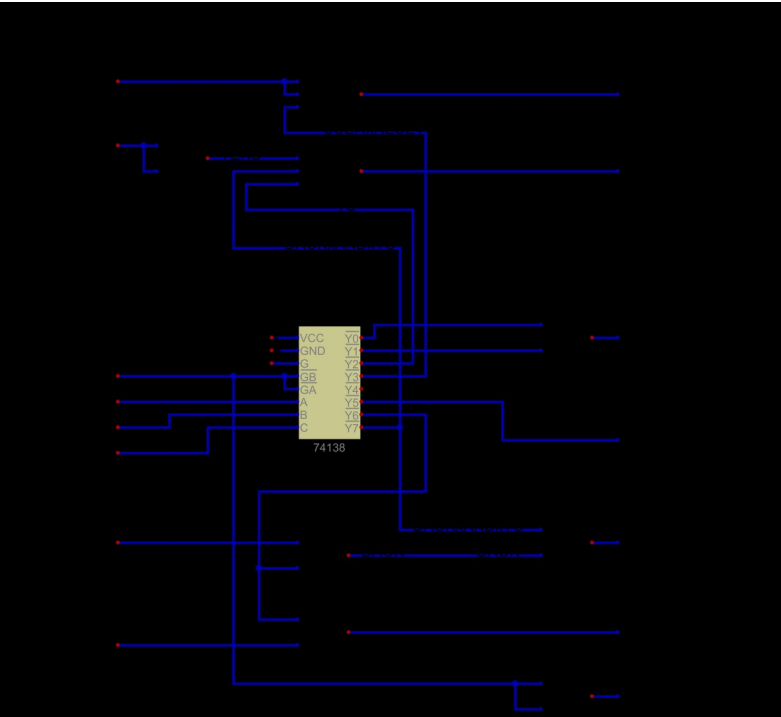
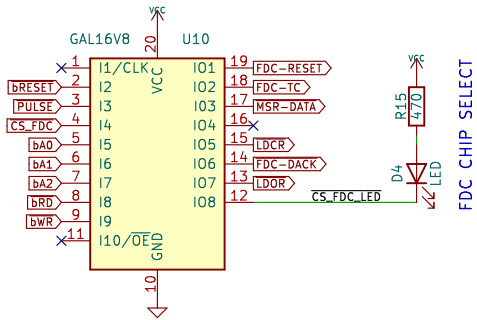


## EXTERNAL DMA INTERFACE

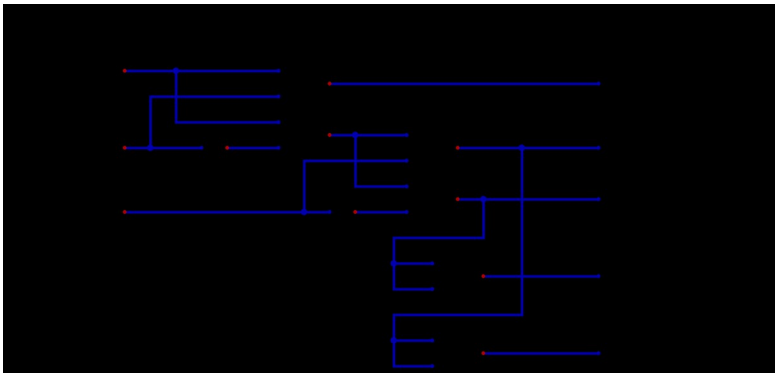
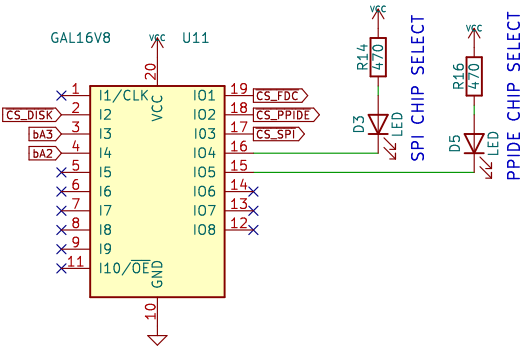


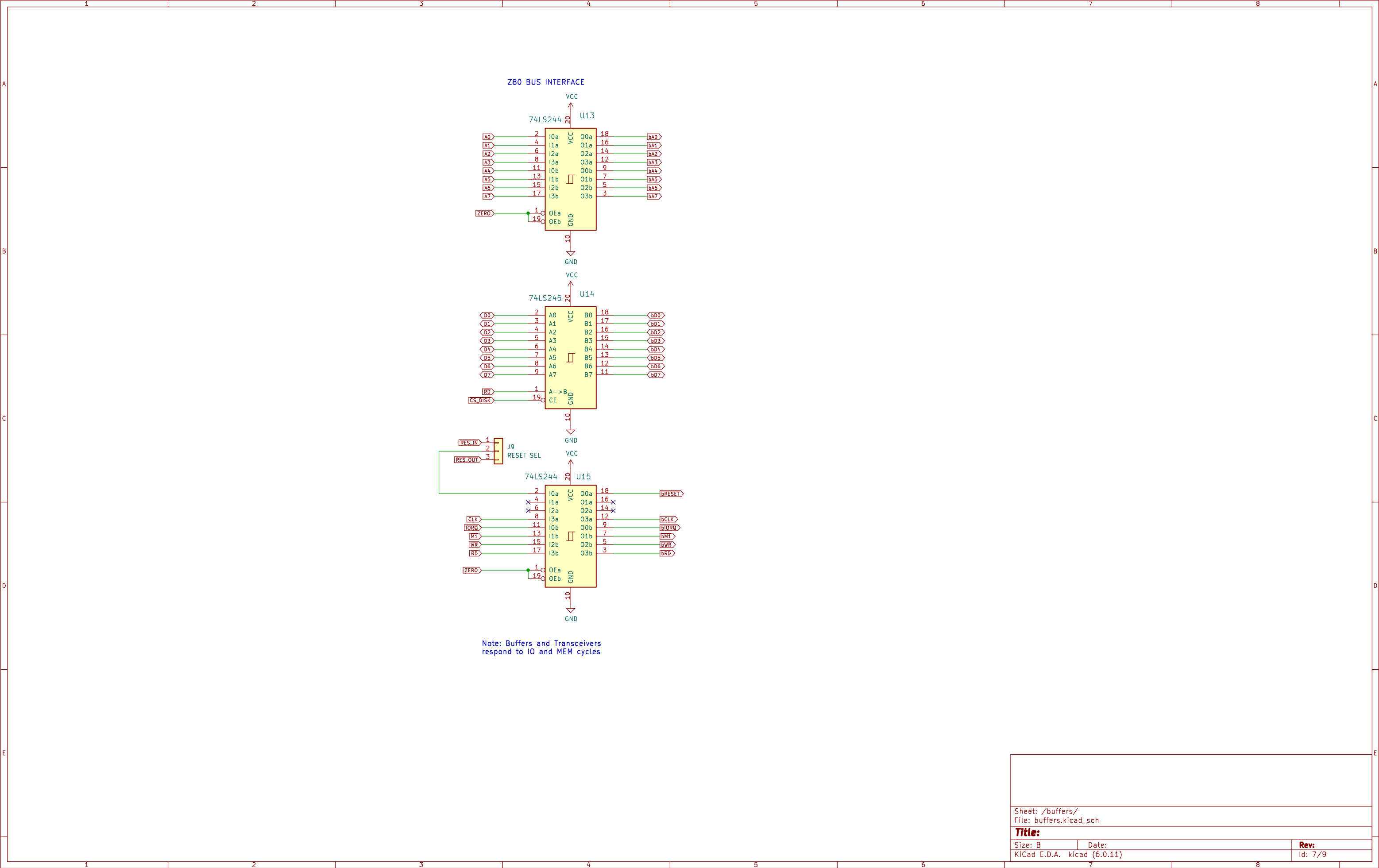
NOTE: RELIES ON 4700 OHM PULL UP  
RESISTOR ON Z80 PROCESSOR BOARD

FDC DMA GAL16V8



DISK CS GAL16V8



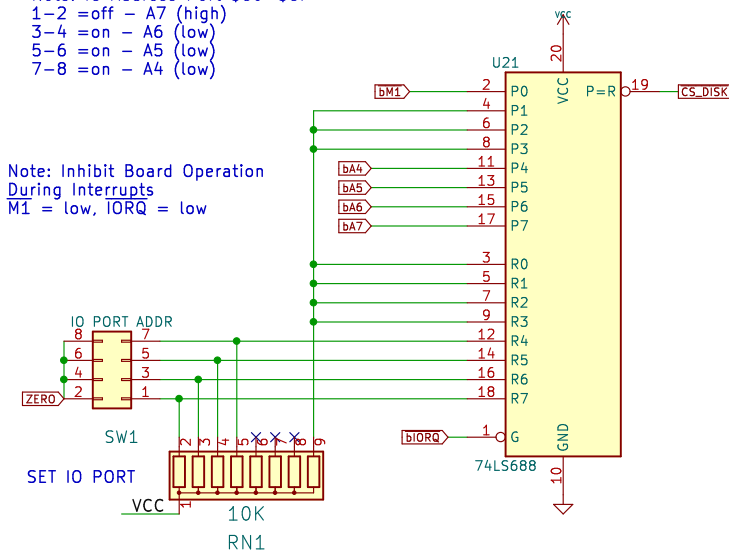


## IO SELECTION CIRCUIT

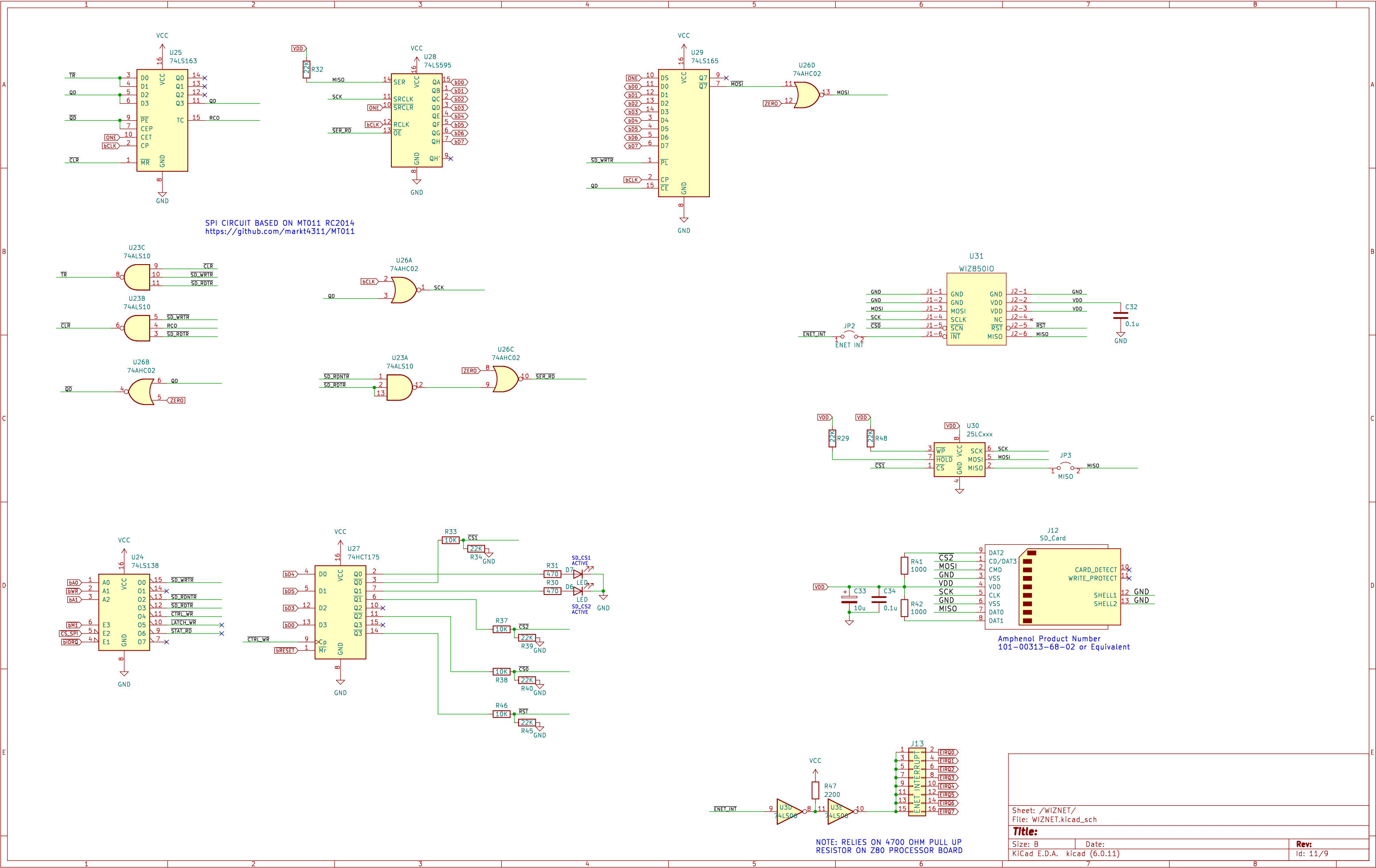
### FDC, PPIDE, SPI-SD

Note: IO Address Port \$80-\$8F  
 1-2 =off - A7 (high)  
 3-4 =on - A6 (low)  
 5-6 =on - A5 (low)  
 7-8 =on - A4 (low)

Note: Inhibit Board Operation  
During Interrupts  
 $\overline{M1} = \text{low}$ ,  $\overline{IORQ} = \text{low}$







SPI CIRCUIT BASED ON MT011 RC2014  
<https://github.com/markt4311/MT011>

Amphenol Product Number  
101-00313-68-02 or Equivalent

Sheet: /WIZNET/ File: WIZNET.kicad_sch		
<b>Title:</b>		
Size: B	Date:	Rev:
KiCad E.D.A. kicad (6.0.11)		Id: 11/9