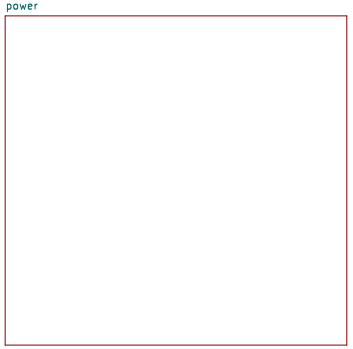
bus

File: bus.kicad_sch

power

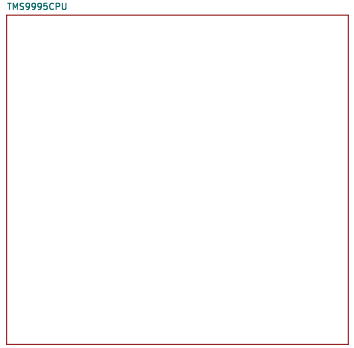


File: power.kicad_sch

buffers

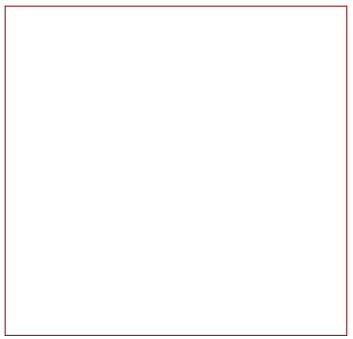
File: buffers.kicad_sch

TMS9995CPU



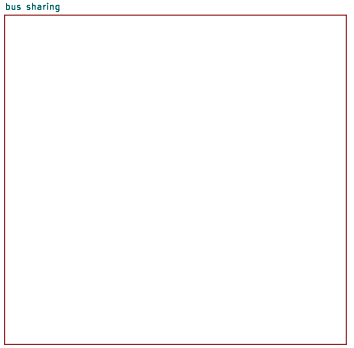
File: TMS9995CPU.kicad_sch

GALS



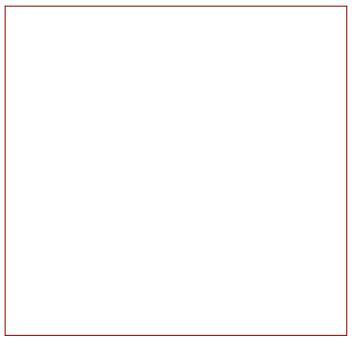
File: GALS.kicad_sch

bus sharing



File: bussharing.kicad_sch

IO

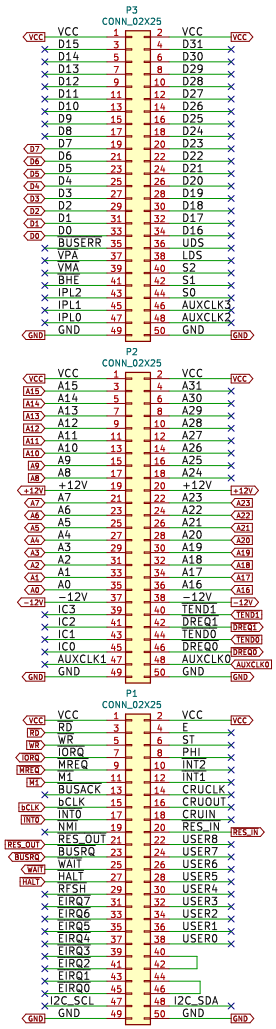


File: io.kicad_sch

Sheet: /
File: processor.tms9995.kicad_sch

Title: Duodyne TMS9995 CPU board

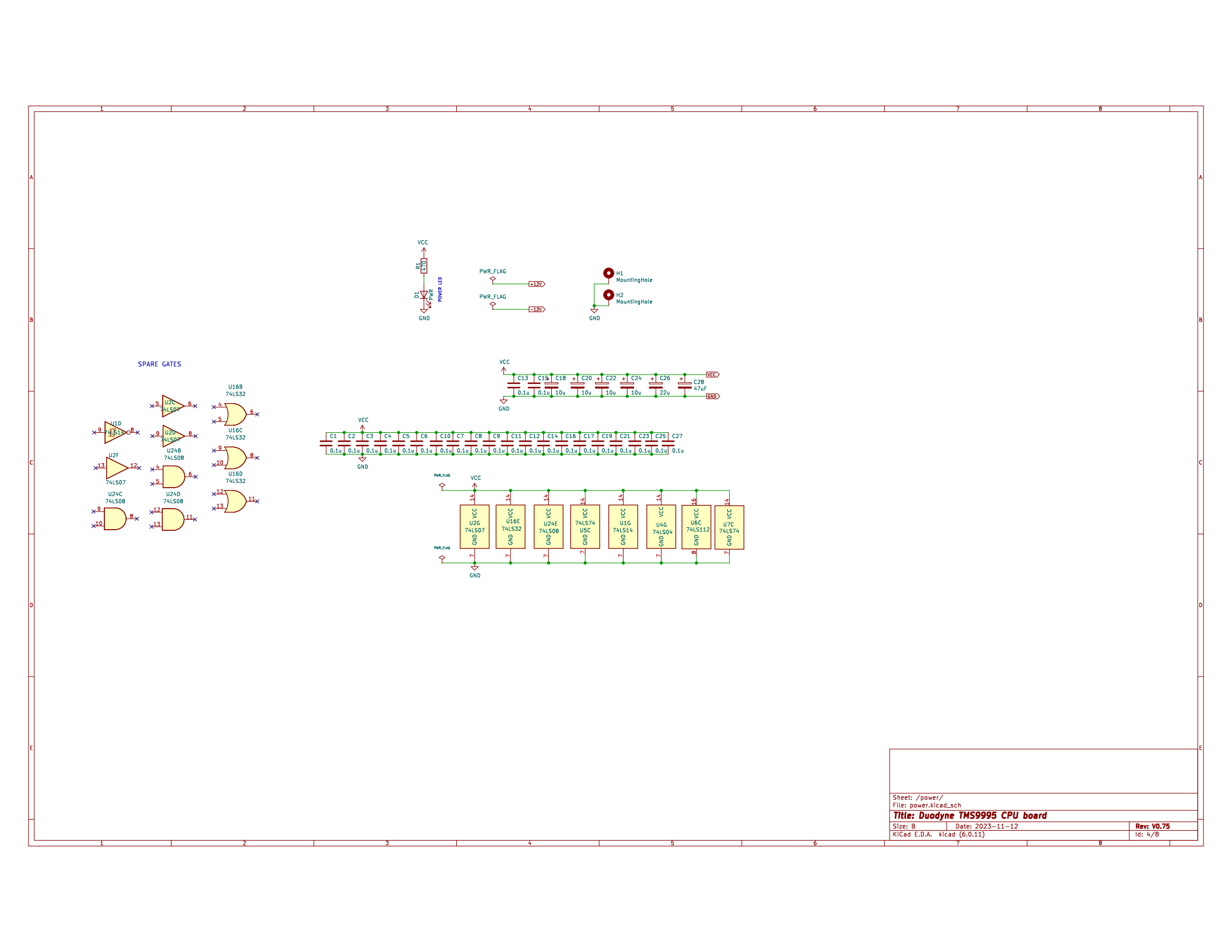
Size: B	Date: 2023-11-12	**Rev: V0.75**
KiCad E.D.A. kicad (6.0.11)		Id: 1/8



Sheet: /bus/
File: bus.kicad_sch

Title: Duodyne TMS9995 CPU board

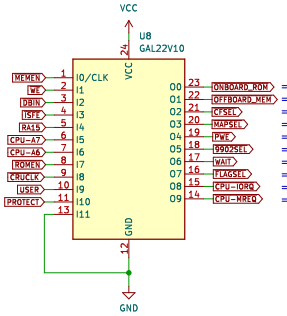
Size: B	Date: 2023-11-12	**Rev: V0.75**
KiCad E.D.A. kicad (6.0.11)		Id: 2/8



Sheet: /power/
File: power.kicad_sch

Title: Duodyne TMS9995 CPU board

Size: B	Date: 2023-11-12	**Rev: V0.75**
KiCad E.D.A. kicad (6.0.11)		Id: 4/8



=$\overline{MEMEN}$+$\overline{ROMEN}$+RA15

=$\overline{MEMEN}$+(!$\overline{ROMEN}$*!RA15*$\overline{WE}$) + (!ISFE * RA15)

=$\overline{MEMEN}$+$\overline{ISFE}$+!RA15+CPU-A7+CPU-A6+USER

=$\overline{MEMEN}$+$\overline{ISFE}$+!RA15+CPU-A7+!CPU-A6+USER

=$\overline{WE}$+(PROTECT*USER)

=!$\overline{MEMEN}$+$\overline{ISFE}$+RA15+CPU-A7+CPU-A6+USER

=!$\overline{ROMSEL}$+!$\overline{CFSEL}$

=$\overline{CRUCLK}$+$\overline{ISFE}$+RA15+CPU-A7+!CPU-A6

=$\overline{MEMEN}$+$\overline{ISFE}$+!$\overline{CFSEL}$+!$\overline{MAPSEL}$+!9902SEL+USER+!RA15

=(!ISFE * RA15)+$\overline{OFFBOARD\_MEM}$

Equation ('+' is 'OR', '*' is 'AND')

The memory map is shown in the table below.

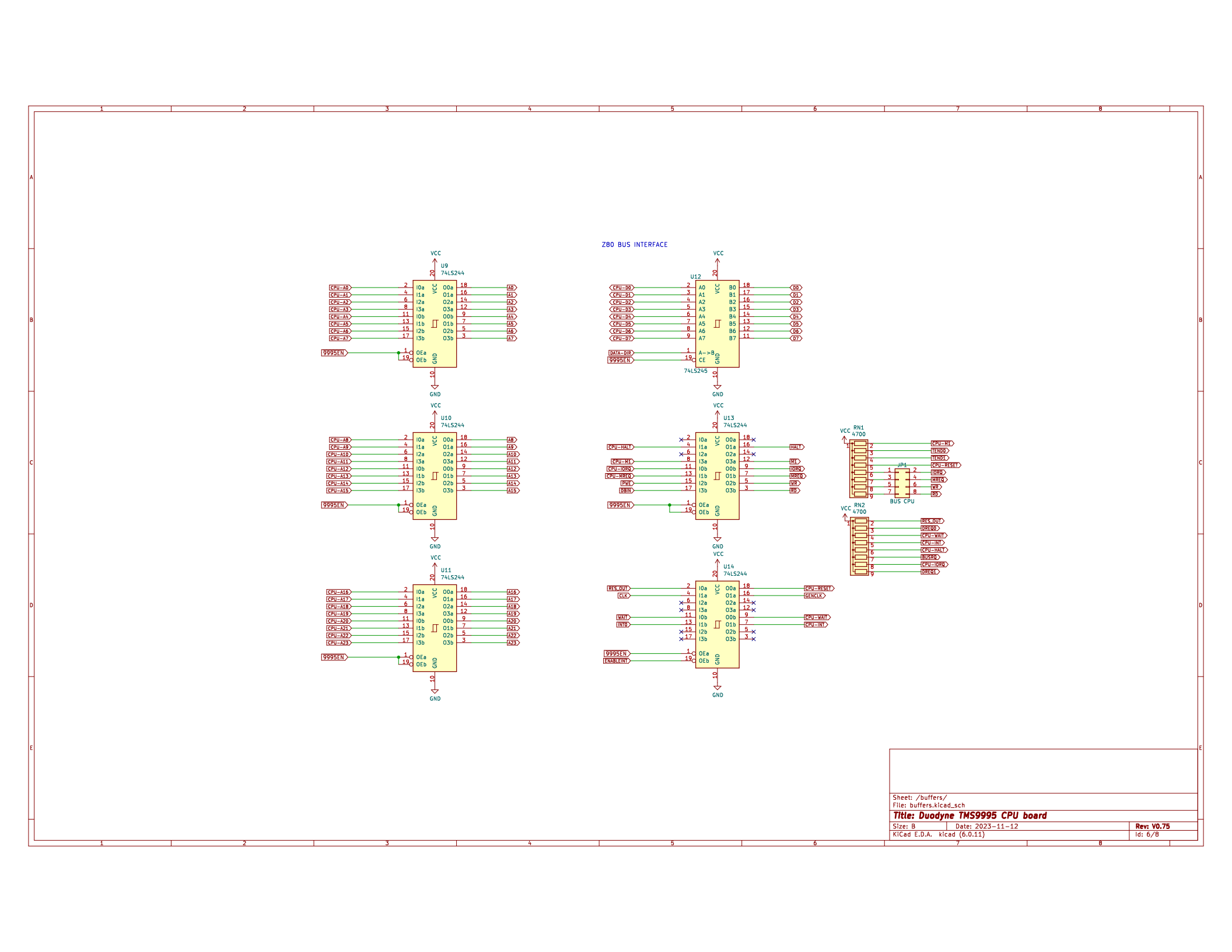
Memory Address	Mapped To
>0000 – >7FFF	ROM when enabled, otherwise RAM
>8000 – >EFFF	RAM
>F000 – >F0FB	TMS 9995 internal RAM
>F0FC – >FDFF	RAM
>FE00 – >FE3F	CF card ATA registers (FIX INCOMPLETE DECODING WITH NEXT REVISION)
>FE40 – >FE7F	Memory mapper registers 0–15 (>FE40 – >FE4F, repeats at >FE50 etc... FIX INCOMPLETE DECODING WITH NEXT REVISION)
>FE80 – >FEBF	Offboard IO (ports $80–$FF)
>FFF0 – >FFF9	RAM
>FFFA – >FFFF	TMS 9995 internal RAM

CRU Address	Mapped To
>0000 – >003F	TMS 9902 registers
>0040 – >007F	Control signal latch (further details here)
	(Plus processor internal CRU bits)

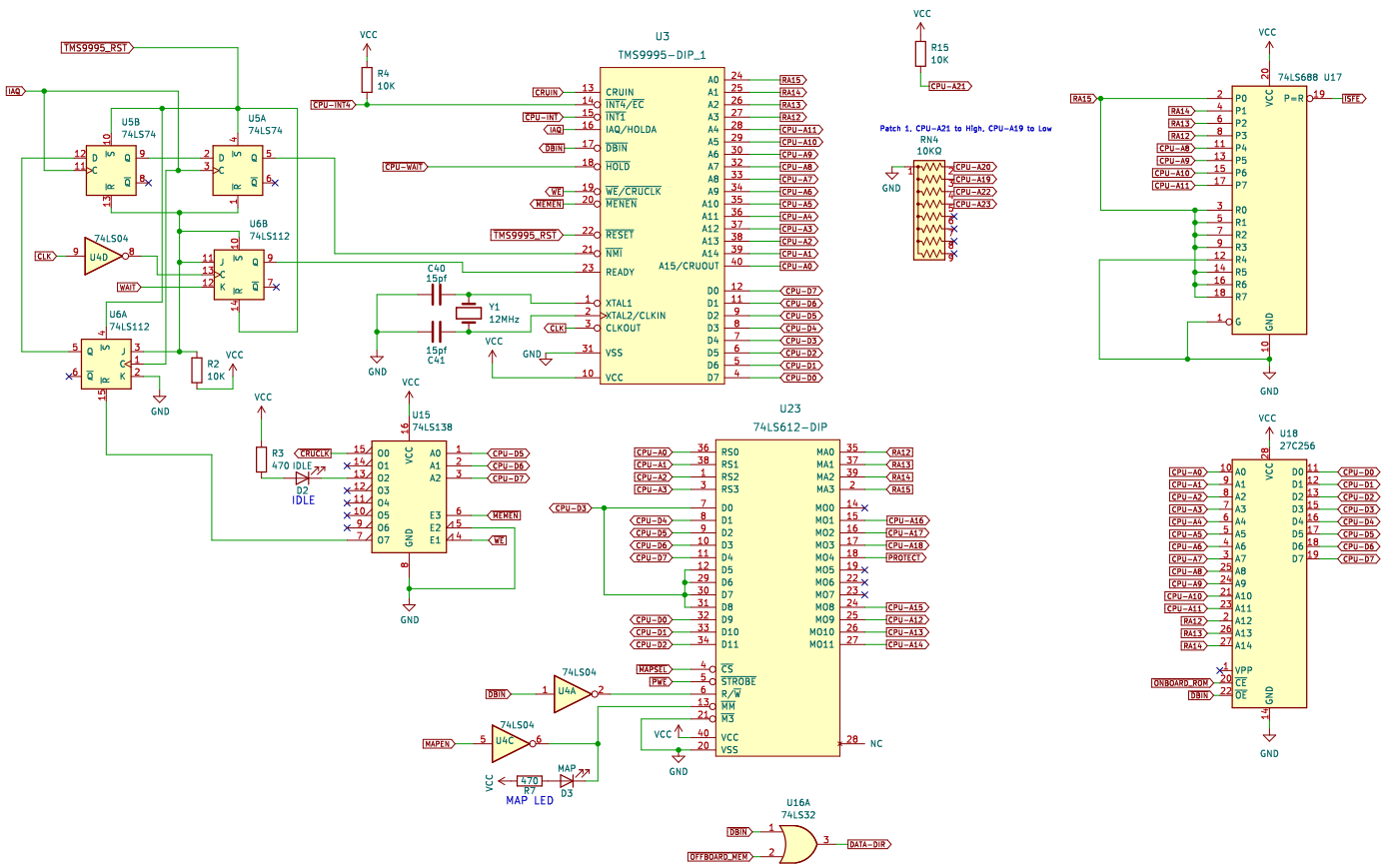
Sheet: /GALS/
File: GALS.kicad_sch

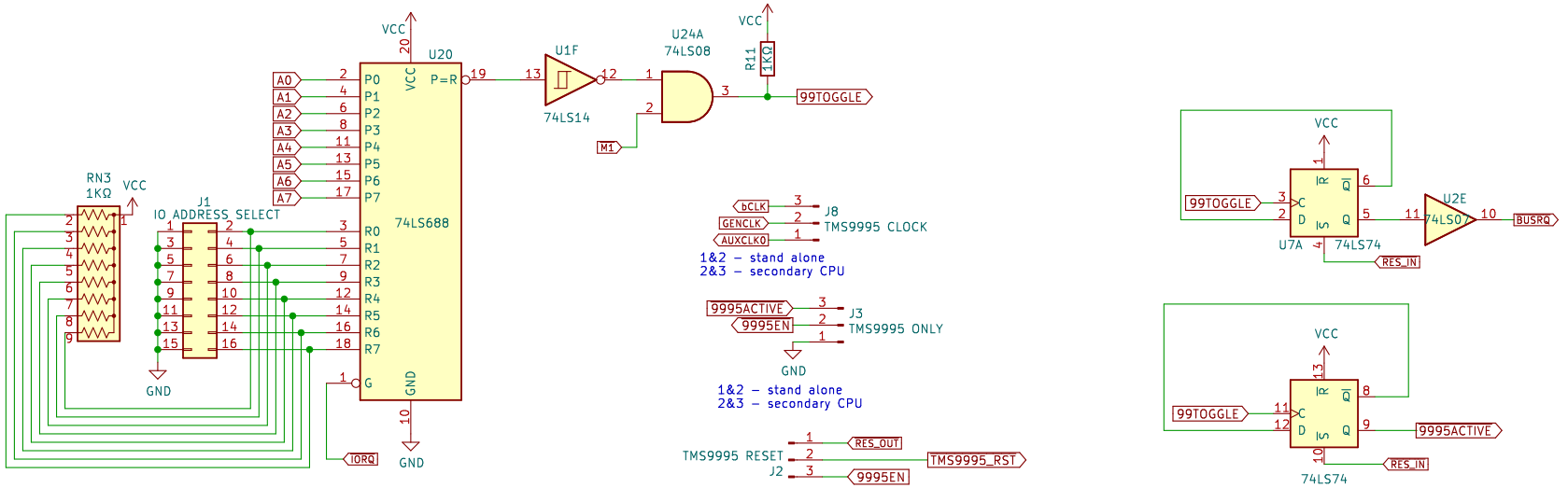
Title: Duodyne TMS9995 CPU board

Size: B	Date: 2023-11-12	**Rev: V0.75**
KiCad E.D.A. kicad (6.0.11)		Id: 5/8

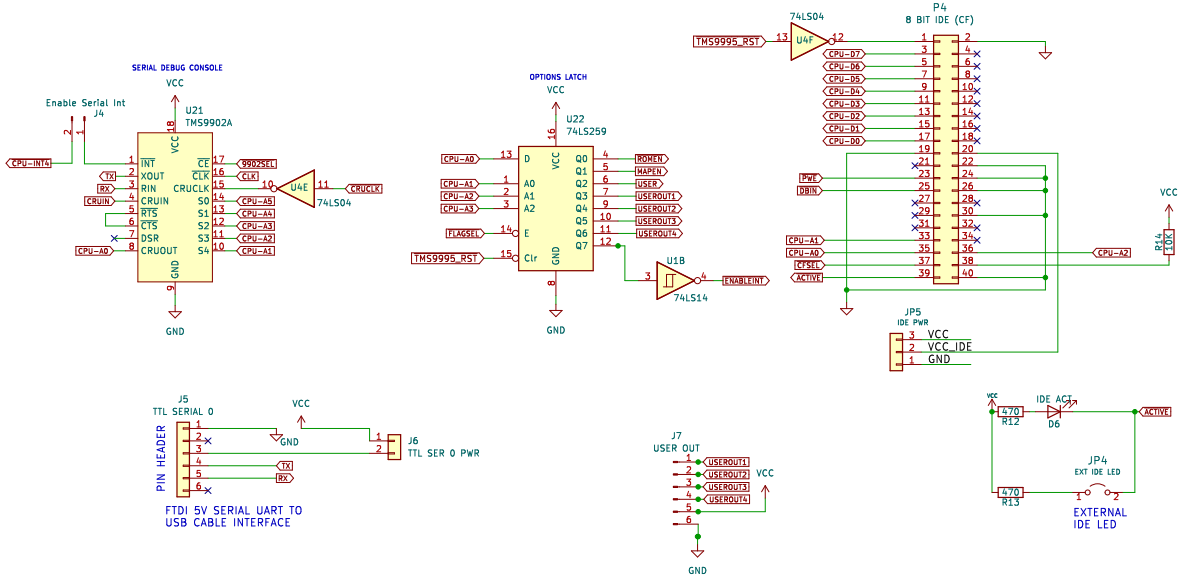


Sheet: /buffers/		
File: buffers.kicad_sch		
Title: Duodyne TMS9995 CPU board		
Size: B	Date: 2023-11-12	**Rev: V0.75**
KiCad E.D.A. kicad (6.0.11)		Id: 6/8


TMS9995_RST
IAQ
U5B
74LS74
U5A
74LS74
U6B
74LS112
U6A
74LS112
U4D
74LS04
CLK
WAIT
R2
10K
VCC
GND
R4
10K
CPU-INT4
U3
TMS9995-DIP_1
CRUIN
INT4/EC
INT1
IAQ/HOLDA
DBIN
HOLD
WE/CRUCLK
MEMEN
RESET
NMI
READY
A15/CRUOUT
XTAL1
XTAL2/CLKIN
CLKOUT
VSS
VCC
CPU-WAIT
CPU-INT
WE
MEMEN
C40
15pf
C41
15pf
Y1
12MHz
R15
10K
CPU-A21
Patch 1, CPU-A21 to High, CPU-A19 to Low
RN4
10KΩ
74LS688 U17
P=R
ISFE
U15
74LS138
R3
470 IDLE
D2
IDLE
CRUCLK
MEMEN
WE
U23
74LS612-DIP
MAPSET
PWE
MAPEN
U4A
U4C
74LS04
R7
470
D3
MAP
MAP LED
U16A
74LS32
DBIN
OFFBOARD_MEM
DATA-DIR
U18
27C256
ONBOARD_ROM
NOTE: RESET SELECT ALLOWS FOR RESET TO ORIGINATE:
1. ON PROCESSOR BOARD RESET BUTTON CIRCUIT ONLY (NONE)
2. FROM EXTERNAL BUS RES_IN (1-2 CLOSED)
3. TRANSMITTED TO EXTERNAL BUS (2-3 CLOSED)
JP2
RES SEL
RES_OUT
RES_IN
SW1
RESET
R8
10
C42
10u
EXT_RES
D4
1N4148
U1E
74LS14
U2A
74LS07
R9
10K
U4B
74LS04
JP3
RES OUT
DS1233
U19
Reset Button Circuit
Sheet: /TMS9995CPU/
File: TMS9995CPU.kicad_sch
Title: Duodyne TMS9995 CPU board
Size: USLedger
Date: 2023-11-12
Rev: V0.75
KiCad E.D.A. kicad (6.0.11)
Id: 9/8



Sheet: /bus sharing/		
File: bussharing.kicad_sch		
Title: Duodyne TMS9995 CPU board		
Size: A4	Date: 2023-11-12	**Rev: V0.75**
KiCad E.D.A. kicad (6.0.11)		Id: 9/8



Sheet: /IO/		
File: io.kicad_sch		
Title: Duodyne TMS9995 CPU board		
Size: B	Date: 2023-11-12	**Rev: V0.75**
KiCad E.D.A. kicad (6.0.11)		Id: 11/8