

Z80 NOP / HALT Instruction Tester

Instruction Manual & Functional Description



Document History

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Contents

1	Introduction.....	4
1.1	NOP Instruction	4
1.2	HALT Instruction	4
1.3	The Tester's Trick.....	4
1.4	Expected Behavior - NOP.....	4
1.5	What it Tests.....	4
1.6	What You Can See	4
1.7	What You Can Measure.....	4
1.8	Expected Behavior - HALT.....	4
1.9	What it Tests.....	5
1.10	What You Can See	5
1.11	What You Can Measure.....	5
2	Components	6
3	Construction.....	7
3.1	Before you start construction.....	7
3.2	Order of construction	7
3.3	Note on USB C	7
4	Functionality	8
4.1	Order of Operation.....	8
4.2	Operation Speed.....	8
4.3	Expected Output - NOP	8
4.4	Expected Output - HALT	8
5	Notes on Components	10
6	Errata.....	11
7	Design Files	12
8	Reference Images.....	15
8.1	PCB.....	15
8.2	Built.....	16

1 Introduction

A Z80 NOP / HALT tester is a simple diagnostic tool used to check whether a Z80 microprocessor is basically functional — specifically, whether it can fetch and execute instructions from memory.

1.1 NOP Instruction

In Z80 assembly, NOP (No Operation) is the opcode 0x00.

When executed, the CPU does nothing for one machine cycle and then increments the program counter (PC) to fetch the next instruction.

1.2 HALT Instruction

In Z80 assembly, HALT is the opcode 0x76.

When executed, the CPU halts normal operation and can only be restarted by a reset, interrupt or power cycle. Despite execution halting, bus cycles to maintain memory refresh cycles continue. This is useful to check refresh operations are concurrently correctly.

1.3 The Tester's Trick

The tester provides the Z80 with a "fake" memory where every address returns 0x00 (NOP) or 0x76 (HALT)

1.4 Expected Behavior - NOP

With only NOPs available, the Z80 should:

- Continuously fetch opcodes (all NOPs).
- Increment the PC from 0x0000 to 0xFFFF, then wrap around.
- Output the address on the address bus sequentially, one step per instruction cycle.

1.5 What it Tests

- Clock circuit (CPU is being driven).
- Reset circuit (PC starts at 0x0000).
- Address bus (sequential counting).
- Basic instruction fetch and decode mechanism.

1.6 What You Can See

- A display of the address bus contents as it increments
- Status of HALT, RFSH, M1 and MREQ signals

1.7 What You Can Measure

- Test points for clock, OV and 5V
- Test points for s RFSH, M1, MREQ, RD IORQ, WR, HALT, BUSACK (Useful if your Z80 is mis-behaving)

1.8 Expected Behavior - HALT

With only HALTs available, the Z80 should:

- HALT LED goes blank (Active low)
- Cease incrementing the PC

- Output the address on the address bus sequentially for refresh. only lower 7 bits (A0..A6). A7 to A15 should remain off in this mode

1.9 What it Tests

- Clock circuit (CPU is being driven).
- Reset circuit (CPU enters HALT mode).
- Address bus (sequential counting for refresh only).
- Basic instruction fetch and decode mechanism.

1.10 What You Can See

- A display of the address bus contents as it increments
- Status of HALT, RFSH, M1 and MREQ signals

1.11 What You Can Measure

- Test points for clock, OV and 5V
- Test points for s RFSH, M1, MREQ, RD IORQ, WR, HALT, BUSACK (Useful if your Z80 is mis-behaving)

With this it is possible to confirm basic IC functionality while looking at expected signal quality (if you have a scope to hand)

2 Components

Reference	Value	Qty	Part
BAR1	LED_Bar_10	1	OSX10201-G
BAR2	LED_Bar_10	1	OSX10201-RGG
C1	100nF	1	Ceramic
C2	1nf	1	Ceramic (*)
C3	100uF	1	Electrolytic
C4	10nF	1	Ceramic
J1	USB_C_Receptacle_PowerOnly_6P	1	USB4125-GF-A
J2	USB_A	1	KUSBX-AS1N
J5	Barrel Jack	1	Wurth 694108301002
R1	22K	1	
R3	1K	1	
R4	4.7K	1	
R6, R7	5.1K	2	Optional on J1 being fitted
RN1	4.7K	1	4116R-1-472
RN2, RN3	1K	2	4609M-101-102LF
RN4	1K	1	4605X-101-102LF
RV1	2M	1	PT10LV10-205A2020-S
SW1	Switch Push	1	
SW1	Switch Slide	1	
TP1	5V	1	
TP2	0V	1	
TP3	Clock	1	
TP4	BUSACK	1	
TP5	IORQ	1	
TP6	RD	1	
TP7	WR	1	
TP8	HALT	1	
TP9	MREQ	1	
TP10	M1	1	
TP11	RFSH	1	
U1	555 Timer	1	LM555CN
U2	Z80	1	Test Item

(*) Can be changed to give a different clock range. See section 5

3 Construction

3.1 Before you start construction

Inspect the PCB for any visible signs of damage

Select your components:

- Turned pin sockets are recommended due to robustness and reliability

3.2 Order of construction

The recommended order of construction is:

- Resistors
- Sockets
- Resistor packs
- LED's
- Power connectors
- Reset switch
- ZIF Socket
- Insert IC

3.3 Note on USB C

If the USB C connector is not to be fitted then the two 5.1K resistors (R6 & R7) are also not required.

4 Functionality

4.1 Order of Operation

To test a CPU, the following steps are required

- Put the CPU in the ZIF socket and clamp it
- Select either NOP or HALT mode
- Apply power via one of the power inputs
- Press the reset button

4.2 Operation Speed

Depending on the clock speed selected A0 may appear fully lit or flicker due to the rate of change

The time taken / speed of operation is controlled by the variable resistor RV1. In standard configuration this gives an approximate clock of between 325Hz and 22KHz

It is possible to change C1 and C2 to give other ranges if required. For example, using C1 @ 47nF and C2 at 2.2nF gives an approximate clock of between 150Hz and 10KHz

The original C1, C2 values have been chosen to give reasonable time performance while making the address bus changes visible.

4.3 Expected Output - NOP

The LED's representing A0 through A15 should now count in the sequence as the CPU runs through addresses 0000 to FFFF

The four LED's representing HALT, RFSH, M1 and MREQ should all stay lit. RFSH, M1 and MREQ do change state but too quickly to be easily visible. Using a scope on their test points if recommended if exact operation needs to be observed.

4.4 Expected Output - HALT

The LED's representing A0 through A6 should now count in the sequence as the CPU runs through its refresh address generation. A7 through A15 should not light.

The three LED's representing RFSH, M1 and MREQ should all stay lit. They do change state but too quickly to be easily visible. Using a scope on their test points if recommended if exact operation needs to be observed.

The HALT LED should not be lit. This indicates the CPU is in HALT mode

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5 Notes on Components

All the components used have been selected at time of design to be readily available via eBay and other sources.

All components with the exception of the USB C connector are through hole so specialist tooling is not required

It is recommended that all through hole resistors are rated at 0.5W for over-rating reliability

The ZIF socket can be soldered directly to the board. You may wish to consider using a socket to mount the ZIF socket into as they can be expensive and easy to damage via soldering.

Make sure the reset button is oriented correctly before soldering

Not all 555's seem to be created equal. I strongly recommend using an LM555CN

The capacitor at C2 is set to 1nF. This gives a range of approximately 325Hz to 22KHz. This may be changes as follows:

Capacitor	Approx Min	Approx Max
1nF	325Hz	22KHz
2.2nF	150Hz	10KHz
4.7nF	75Hz	5KHz

6 Errata

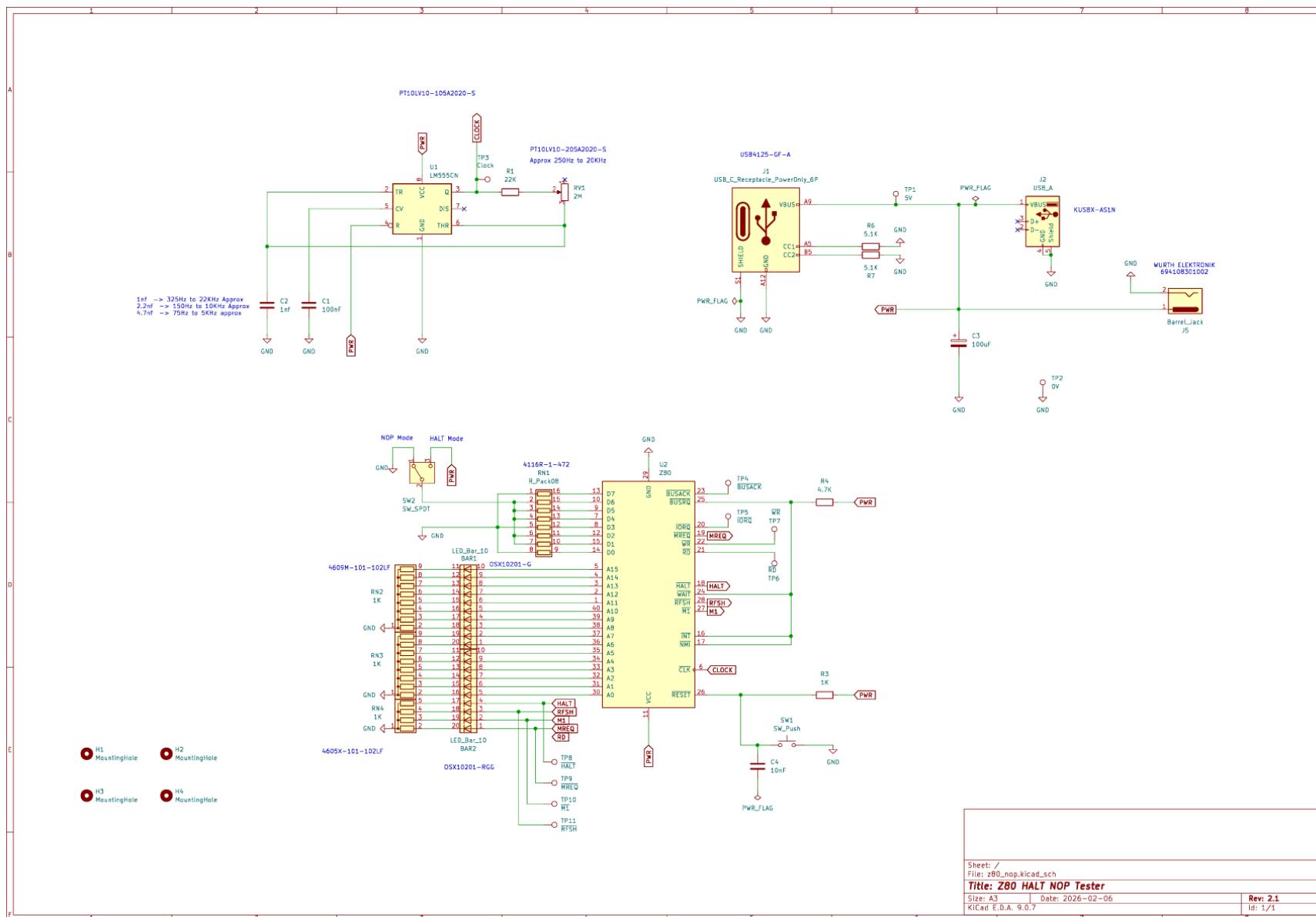
None so far ...

7 Design Files

https://github.com/codesqueak/Z80_NOP

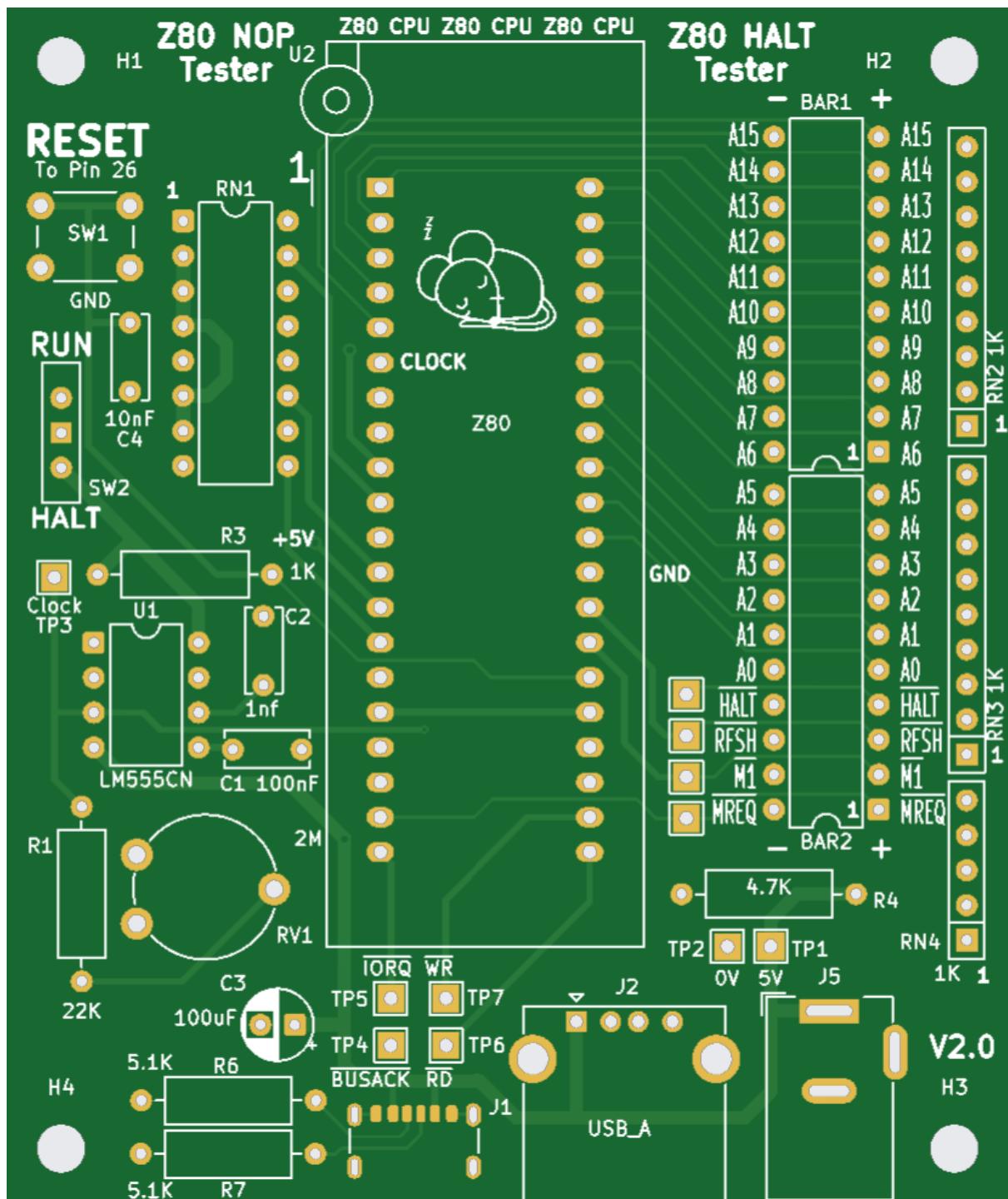
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Z80 NOP / HALT Instruction Tester



8 Reference Images

8.1 PCB



8.2 Built

