DC-Ripple-Energy Adaptive-Minimization (DREAM) Modulation Scheme for a High Power Density Inverter

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***Abstract*— The DC bus capacitor is one of the major power-density and reliability hurdles of electric drive systems. It is hard to shrink because it is constrained by the DC bus RMS ripple current, which is only load dependent. A dual-inverter based segmented drive can reduce the ripple current by ~50% compared to a non-segmented case. This paper analyzes the origin of this ripple current and points out the path for minimization. An optimal DC-ripple-energy adaptive-minimization (DREAM) modulation method is proposed to further reduce the ripple current. It is observed in experimental results that the proposed method can achieve additional 38% reduction over the traditional segmented drive system.**

Keywords*— *Segmented drive, capacitor ripple current, space vector modulation, high density, SiC

I. Introduction

With the rapid market adoption of electric vehicles, the US Department of Energy targets [1] include more than eight times increase in the power density of traction inverters. In order to achieve this challenging goal, wide bandgap devices have been extensively researched to improve the power density of the power modules [2] and advanced thermal management concepts are proposed to minimize the heatsink size [3]. The DC bus capacitor takes up a large space in the motor drive inverter and cannot be shrunk by using higher switching frequencies, as the selection is mainly determined by the RMS value of the ripple current. A dual inverter system with segmented motor configuration has proven to reduce the capacitor RMS current by ~50% by properly interleaving the switching pulses [4] but further reductions are needed to hit the 2025 goal. Reduction of capacitor current can shrink the capacitor volume and also reduce the capacitor power loss and temperature, benefiting reliability and lifetime. Existing research based on either carrier [5], [6] or space vector based [7], [8] modulation relies on optimizing the phase shift between the pulse-width-modulated voltages of the dual inverters and thus cannot fully harvest the benefits of design freedom of the dual-inverter setup.

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II. The Origin of the DC Bus Capacitor Current

Fig. 1 shows a block diagram of the segmented drive system. The dual 3-phase inverter system comprises of six power semiconductor switches for each inverter and a DC bus filter capacitor. The battery voltage is chopped by those switches according to a certain pulse width modulation (PWM) scheme to regulate the motor current (i_x, x = a, b, c) and voltage. The switching operations generates large ripple currents in the DC bus, thus necessitating the use of the DC bus filter capacitor to absorb the ripple currents so that a relatively constant current flows into the battery. In one switching period, the motor currents are relatively constant and the inverter dc side current i_{inv} is the sum of the three top switch currents, determined by

$$i_{inv} = (S_{a1}+S_{a2})\cdot i_a+(S_{b1}+S_{b2})\cdot i_b+(S_{c1}+S_{c2})\cdot i_c, \quad (1)$$

where S_{x1} and S_{x2} (x = a, b, c), represent the dual inverters' switching functions for the phase leg x and only have values of 1 and 0, depending on whether the top or low side switch is on. For example, i_{inv} will equal to $-2i_c$ when $S_{x1} = S_{x2} = \{1,1,0\}$ and switch to i_a-i_c when S_{x1} stays as {1,1,0} and S_{x2} flips to {1,0,0} within a switching period due to modulation needs. Therefore, i_{inv} will switch between two current values at the switching frequency, which creates current ripple flowing to the bus capacitor. In practical implementations, the switching functions (S_{x1}, S_{x2}) are determined by the modulation scheme.

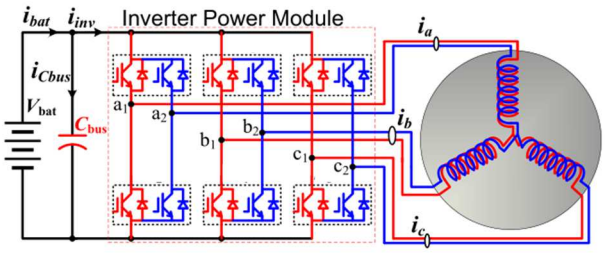

Fig. 1. A Segmented Drive System.

Based on the selected modulation scheme, i_{inv} has 19 possible values depending on the switching function combinations while some will be preferrable over others in order to minimize the capacitor ripple current. Theoretically, if $i_{inv} = i_{bat}$, the capacitor current i_{Cbus} will equal to zero. In practice, since i_{inv} only has 19 possible discrete values, $i_{inv} = i_{bat}$ cannot be guaranteed but the closest values of i_{inv} should be selected, in order to minimize capacitor current ripple. This serves as the foundation of the modulation method proposed in this work.

At each time instant, the 19 possible values of i_{inv} consist of 9 positive, 9 negative and 1 zero values. Fig. 2 shows all the positive i_{inv} current values that can be selected within a phase angle ranging from 0 to π/3 when the amplitude of the sinusoidal current is normalized to be 1 (i.e. $i_a = \cos(\theta)$, thus $2i_a = 2\cos(\theta)$). Depending on the amplitude of i_{bat} and the phase angle, certain current values are closer to i_{bat}. For example, at phase = 0, the closest current values to a given i_{bat} in Fig. 2 are $-2i_c$, i_a-i_c, and i_a-i_b. If one can design a modulation method that selects those three current values, the capacitor ripple current will be minimized. This serves as the foundation of the proposed DC-Ripple-Energy Adaptive-Minimization (DREAM) modulation method, as will be elaborated in the next section.

III. DC-RIPPLE-ENERGY ADAPTIVE-MINIMIZATION (DREAM) MODULATION

Space vector modulation (SVM) provides a high degree of design freedom in terms of pulse positioning and sequencing, and therefore is used in this paper. Fig. 3 depicts the possible vectors under the dual-inverter setup and shows the resultant DC side current values (i_{inv}). Compared to a single inverter setup, the dual inverter SVM introduces additional 6 long vectors and 6 medium vectors besides the original 6 short vectors. The total 18 non-zero vectors triples the possible current values of i_{inv} which can be used to synthesize a bus current that is closer to the battery current i_{bat}, thus reducing the capacitor current. This is the mechanism foundation of the capacitor current reduction capability in a dual-inverter segmented system.

Even with this fundamental concept laid out, the implementation of this new SVM scheme still needs additional elaboration and consideration. In this section, we will firstly give an example case explained in detail in Section A and generalize the modulation method in Section B.

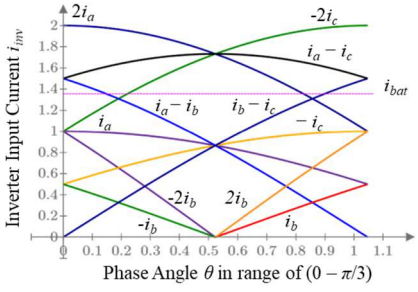

Fig. 2. Possible i_{inv} positive values for a given battery current (all normalized). By selecting the closest current values to synthesize the targeted battery current, the capacitor current ripple can be minimized.

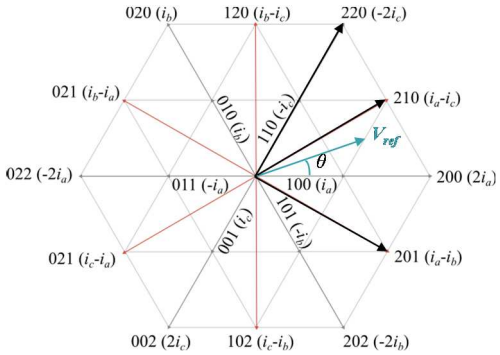

Fig. 3. Space vector representation.

A. An Example Case

In this example, we consider a case of modulation index M = 0.9, and power factor (PF) = 1, in which M is defined as

$$M = V_{ref(pk)} / (V_{dc}/2). \tag{2}$$

The battery current i_{bat} will also be normalized and equal to

$$i_{bat} = 3/2 \cdot M \cdot PF. \tag{3}$$

In this case, battery current ibat equals to 1.35, and is drawn in the dashed line in Fig. 2 for comparison. With phase θ between 0 and π/6, the closest current values to the given i_{bat} in Fig. 2 are $-2i_c$, $i_a - i_c$, and $i_a - i_b$. The switching functions corresponding to those current values can be determined according to the space vector representation of a dual-inverter system, depicted as (220), (210), and (201) in Fig. 3. As a further note, the switching vector of (210) means the combination of (110) for inverter 1 and (100) for inverter 2, or vice versa. For vector (210) to be active for a period of t, inverter 1 and inverter 2's vectors, (110) and (100), will also be active for the same amount of time t.

Once the closet three vectors have been selected (220), (210), (201), the switching duty cycle (d_1 , d_2 , d_3 , where $d_1 + d_2 + d_3 = 1$) for each vector can then be calculated according to the need of synthesizing the required reference voltage, V_{ref} (shown in Fig. 3). Equations for calculating the duties for $\theta \in [0, \pi/6]$ are summarized below:

$$\begin{aligned} d_1 &= 3 - 3 \cdot M \cdot \cos(\theta) \\ d_2 &= \left(\frac{9}{2} \cdot \cos(\theta) + \frac{\sqrt{3}}{2} \cdot \sin(\theta) \right) \cdot M - 4 \\ d_3 &= 2 - \frac{3}{2} \cdot M \cdot \left(\cos(\theta) + \frac{1}{\sqrt{3}} \cdot \sin(\theta) \right) \end{aligned} \tag{4}$$

The duties are plotted against θ in Fig. 4. By assigning the corresponding duty cycle to each of the selected vectors, the phase output voltage will equal to V_{ref} at each phase angle.

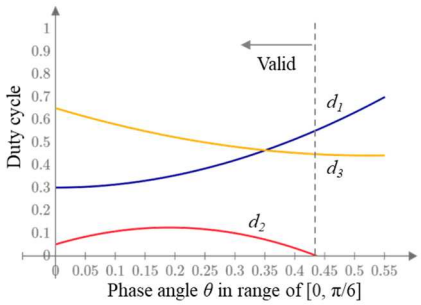

Fig. 4. Calcualted duty cycle of the three selected vectors (220), (210), and (201) for phase angle ranging from 0 to π/6, at M = 0.9, PF = 1.

However, it's worth noting that as phase angle θ increases to a certain value, d_2 becomes negative thus the solutions are no longer valid. It means the selected three vectors, although theoretically can provide the lowest current ripple in the capacitor, in practice will be unable to synthesize the required output voltage. This specific angle can be solved as 0.436 by reversely setting $d_2 = 0$ for equation (4). As a result, sub-optimal vectors will have to be selected to account for this portion. In this region, the highest amplitude current $i_a - i_c$ (210) within the original selected three vectors, is replaced by the closest small vector i_a (100). The three current vectors for this region are therefore $-2i_c$, $i_a - i_c$, and $i_a - i_b$, with the voltage vectors (220), (100), and (201). Using the same duty cycle annotations for those three vectors, the derivation can be repeated to obtain

$$\begin{aligned} d_1 &= \left(\frac{3}{2}\cdot cos(\theta) + \frac{\sqrt{3}}{2}\cdot sin(\theta)\right)\cdot M - 1 \\ d_2 &= 4 - \left(\frac{9}{2}\cdot cos(\theta) + \frac{\sqrt{3}}{2}\cdot sin(\theta)\right)\cdot M \\ d_3 &= -2 + 3\cdot M\cdot cos(\theta) \end{aligned} \quad (5)$$

and plotted in Fig. 5. It is clear that with the new set of vectors, the valid range is complementary to that shown in Fig. 5. By combining the two cases of equation (4) and (5), solution for the full range between 0 to π/6 is obtained.

Similar derivation processes can be repeated for [π/6, π/3] and solution can be obtained for the entire range of this SVM sector 1, where θ is within [0, π/3]. The selected vectors for this SVM sector are summarized in TABLE I. The calculated duty cycles are plotted in Fig. 6.

Once the switching duty cycles are determined, the switching sequence needs to be properly arranged in order to minimize switching actions within one switching period. The switching arrangments are summarized in TABLE I. We can see in each switching period, one phase leg will not switch at all, which is beneficial for switching loss reduction.

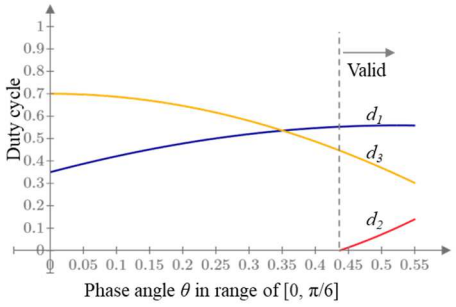

Fig. 5. Calcualted duty cycles of the three selected vectors (220), (100), and (201) when phase angle ranges from 0.436 to π/6, at M = 0.9, PF = 1.

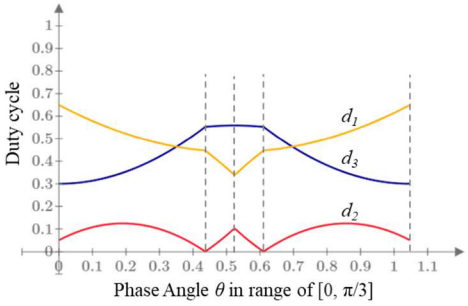

Fig. 6. Calcualted duty cycle of d1, d2, d3, when phase angle ranges from 0 to π/3, at conditions of M = 0.9, PF = 1.

TABLE I. VECTOR SELECTION AND SWITCHING SEQUENCE ARRANGMENT FOR SECTOR 1

0 < θ < 0.436	**Duty Cycle**	**Overall Vector**	**Inverter 1**	**Inverter 2**	**Current**
Interval 1	$d_1/2$	220	110	110	$-2i_c$
Interval 2	$d_2/2$	210	110	100	$i_a - i_c$
Interval 3	$d_3/2$	201	100	101	$i_a - i_b$
Interval 4	$d_3/2$	201	101	100	$i_a - i_b$
Interval 5	$d_2/2$	210	100	110	$i_a - i_c$
Interval 6	$d_1/2$	220	110	110	$-2i_c$
0.436 < θ < π/6	**Duty Cycle**	**Overall Vector**	**Inverter 1**	**Inverter 2**	**Current**
Interval 1	$d_1/2$	220	110	110	$-2i_c$
Interval 2	$d_2/2$	100	100	111	i_a
Interval 3	$d_3/2$	201	100	101	$i_a - i_b$
Interval 4	$d_3/2$	201	101	100	$i_a - i_b$
Interval 5	$d_2/2$	100	111	100	i_a
Interval 6	$d_1/2$	220	110	110	$-2i_c$
π/6 < θ < 0.611	**Duty Cycle**	**Overall Vector**	**Inverter 1**	**Inverter 2**	**Current**
Interval 1	$d_1/2$	200	100	100	$-2i_a$
Interval 2	$d_2/2$	110	110	000	$-i_c$
Interval 3	$d_3/2$	120	110	010	$i_b - i_c$
Interval 4	$d_3/2$	120	010	110	$i_b - i_c$
Interval 5	$d_2/2$	110	000	110	$-i_c$
Interval 6	$d_1/2$	200	100	100	$-2i_a$
0.611 < θ < π/3	**Duty Cycle**	**Overall Vector**	**Inverter 1**	**Inverter 2**	**Current**
Interval 1	$d_1/2$	200	100	100	$2i_a$
Interval 2	$d_2/2$	210	100	110	$i_a - i_c$
Interval 3	$d_3/2$	120	110	010	$i_b - i_c$
Interval 4	$d_3/2$	120	010	110	$i_b - i_c$
Interval 5	$d_2/2$	210	110	100	$i_a - i_c$
Interval 6	$d_1/2$	200	100	100	$-2i_a$

B. Generalized DREAM Realization

Following the example case of the previous section, the vector selection, conduction duty cycle, and switching sequence arraignment can be similarly derived for all the other Sectors. Fig. 7 shows the generalized design flowchart of the proposed modulation method for the dual-inverter setup. Starting with a given power factor and modulation index, the targeted i_{bat} can be determined. Three vectors that lead to the closest current values to i_{bat} will be selected. The three optimal vectors will be used to synthesize the required reference voltage (V_{ref} in Fig. 3) and the time duration of each vector is calculated following similar methodology explained in the previous section. However, the optimal three vectors may not be able to synthesize a specific V_{ref}, for which a sub-optimal solution is selected. The loop continues until the V_{ref} synthesizing algorithm can result in a fixed solution. The selected vectors are then fed into a PWM pulse/sequence planning procedure to avoid multiple turn-on/off of one phase-leg within one switching period. This is important to reduce switching loss. Deadtime compensation can be used to improve the performance.

With the above SVM implementation, the switching pulses of the two inverters are generated synthetically. In contrast, the traditional schemes individually modulate the PWMs of each inverter and apply a phase shift in between, which cannot fully harvest the benefits of the dual-inverter setup.

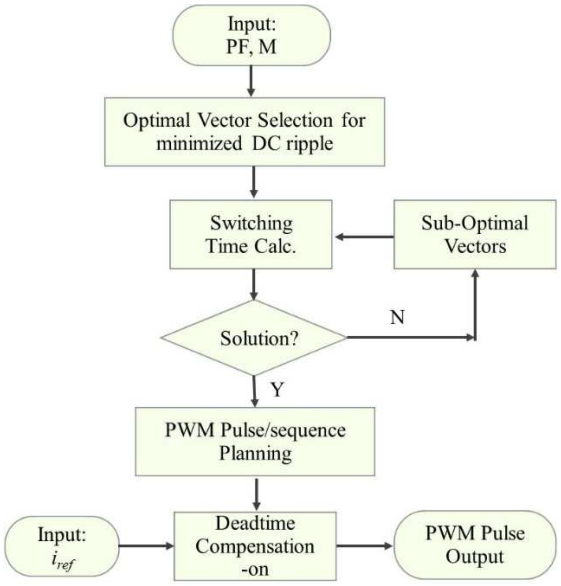

Fig. 7. DREAM modulation flow chart.

IV. Simulation Results

Fig. 8 shows simulated normalized capacitor ripple current waveforms with modulation index M = 0.9 and power factor (PF) = 1. The proposed DREAM segmented dual-inverter system is compared with the non-segmented single-inverter scheme and the traditional segmented dual-inverter scheme. Both the non-segmented and traditional segmented schemes use alternating-zero-vector SVM [9]. The two inverters for the traditional segmented scheme uses 180 degree phase shift between the two inverters. We can clear see the ripple reduction progressively by moving to the segmented and then DREAM segmented. Normalized current in the three cases are measured as 0.81, 0.48 and 0.26, respectively. The modulation index is swept for all three schemes and the normalized capacitor currents are shown in Fig. 9. If the capacitor current rating is designed from the worst case, then we can see the proposed DREAM SVM scheme achieves additional 46% reduction on top of the 47% of reduction from switching to segmented drive scheme.

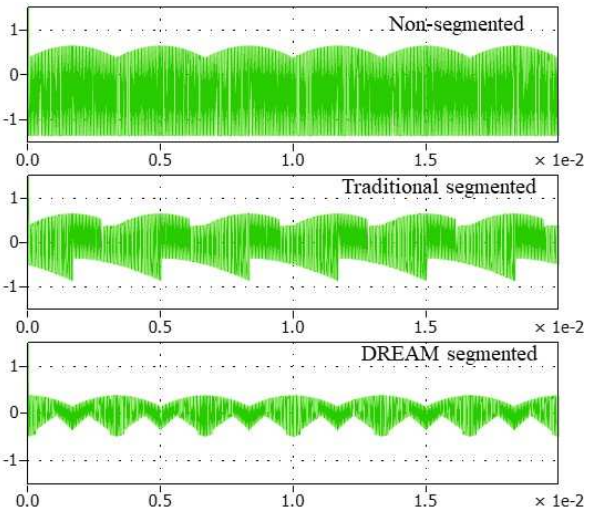

Fig. 8. Simulated normalized capacitor current waveforms at M = 0.9, PF = 1.

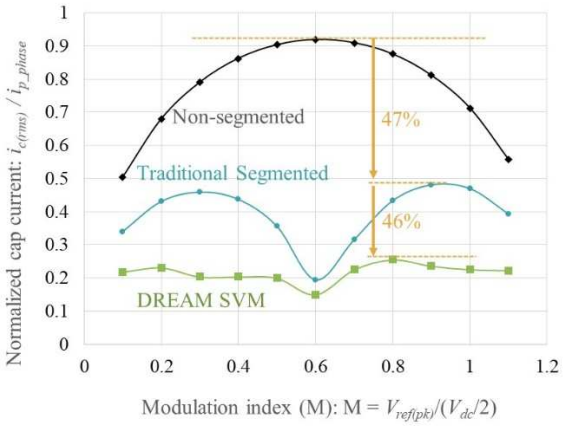

Fig. 9. Simulated normalized capacitor current with different modulation index M. PF = 1.

V. Experimental Setup and Results

A traction drive dual-inverter prototype was designed and built using six SiC MOSFET phase-leg modules rated at 1200 V/120 A, four film dc bus capacitors with a total 880 µF of capacitance, a water-cooled cold plate (36 x 12.7 cm), a 3D-printed mounting frame, and other fixture components, as shown in Fig. 10. The system was tested with two set of Y-connected RL load of 4.5 Ω and 0.5 mH. Modulation index is set to be 0.9, delivering 5.6 kW power at 200 V input voltage. The currents of capacitor number 1 and 4 (C1 and C4 in Fig. 10) were measured using two separate Rogowski coil current probes for non-intrusive, easy access of measurement. Switching frequency is

40 kHz and fundamental frequency is 50 Hz. Tested waveforms are shown in Fig. 11 to Fig. 13, which compared the cases of non-segmented, traditional non-segmented, and the proposed DREAM method. We can see when all three modulation schemes can deliver required sinusoidal output and similar output power, the capacitor current ripple amplitude and pattern are very different (zoomed-in waveforms shown at the bottom of each figure), while the proposed DREAM method achieves the lowest ripple.

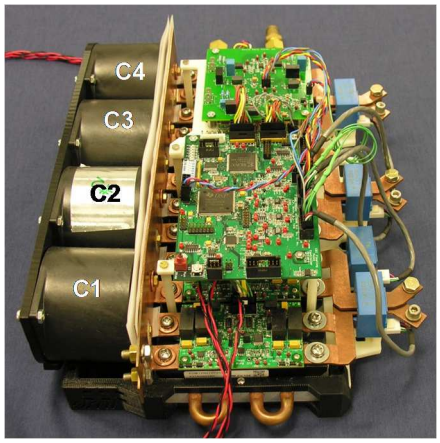

Fig. 10. SiC dual-inverter prototype.

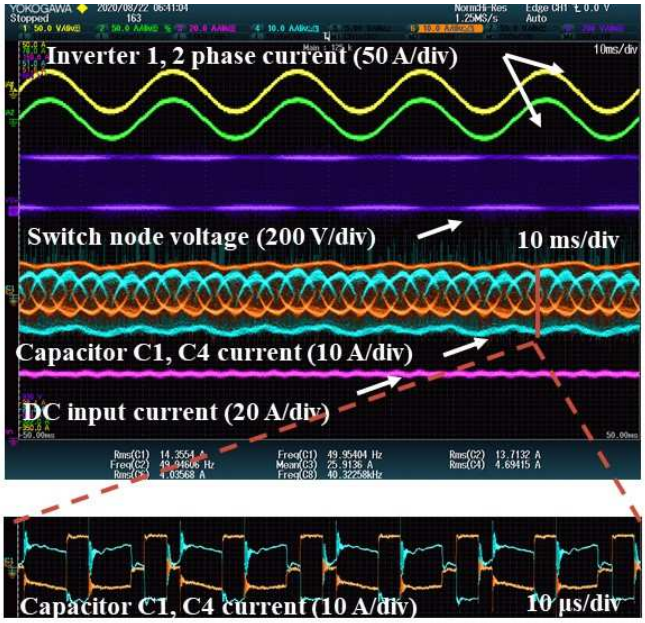

Fig. 11. Waveforms of the non-segmented case.

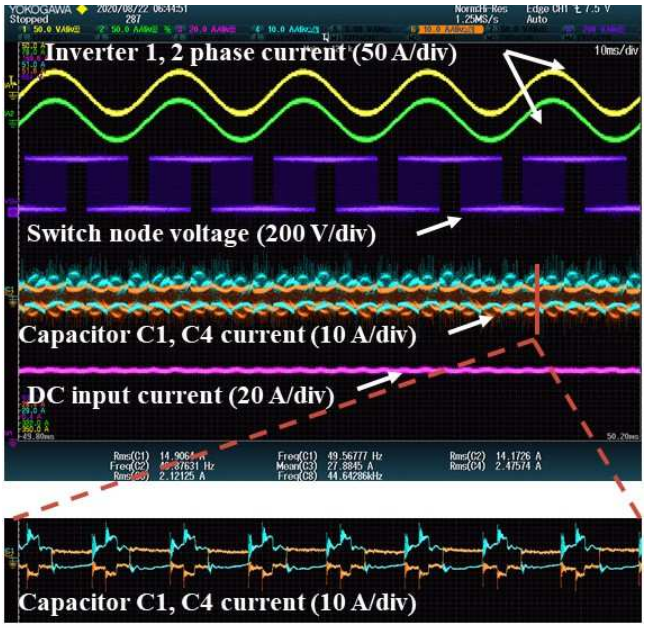

Fig. 12. Waveforms of the traditional segmented case.

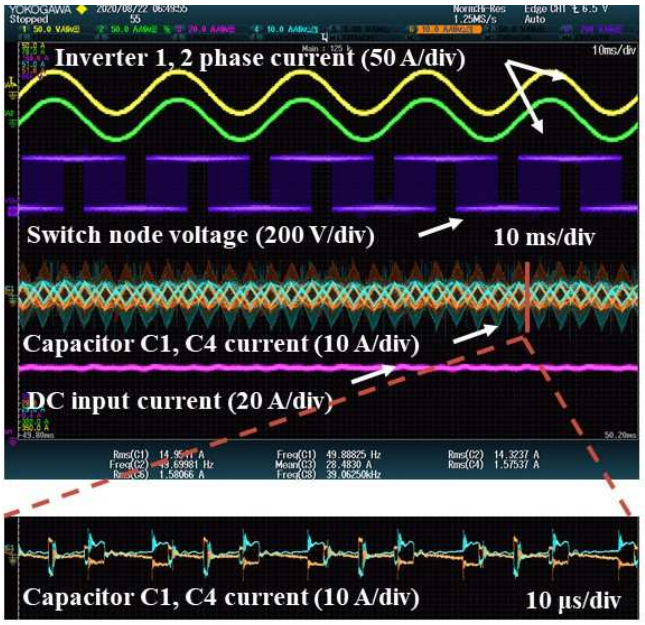

Fig. 13. Waveforms of DREAM modulation case.

The scope measurement values of capacitor currents are summarized in TABLE II. , where V_{bat} and I_{bat} represent the DC side input voltage and current, respectively. I_{a1} and I_{a2} are the measured RMS current of Phase A from the two inverters. There are four DC capacitors used in the setup. Two of capacitors, the one closest to and the one furthest from the DC input terminal are selected to be measured since they can represent best the current distribution among the capacitor banks. High bandwidth Rogowski coil current probes were used to conduct the current measurement. For each capacitor current, we can see consistent reduction after switched to the segmented solutions from the non-segmented: the ripple current is reduced by 51% with the traditional segmented method and an additional 38% reduction

with the proposed DREAM scheme. It is lower than the simulated 46% reduction, mainly due to the phase current ripple (zero-ripple assumed in simulation) and deadtime. We can also see the DREAM modulation improves the current balancing between the capacitors.

TABLE II. TEST RESULTS SUMMARY

	Unit	Non-segmented	Traditional segmented	DREAM segmented
DC Input Voltage V_{bat}	(V)	200	200	200
DC Input Current I_{bat}	(A)	25.89	27.88	28.36
Inverter 1 Phase A RMS Current (I_{a1})	(A)	14.35	14.9	14.99
Inverter 2 Phase A RMS Current (I_{a2})	(A)	13.72	14.17	14.32
DC Capacitor C1 RMS Current (I_{C1})	(A)	4.69	2.48	1.56
DC Capacitor C4 RMS Current (I_{C4})	(A)	4.04	2.12	1.57
Normalized DC Capacitor C1 RMS Current (I_{C1} / I_{bat})	p.u.	0.181	0.089	0.055
Normalized DC Capacitor C4 RMS Current (I_{C4} / I_{bat})	p.u.	0.156	0.076	0.055

VI. CONCLUSIONS

Compared to the non-segmented drive system, the segmented drive can reduce the DC capacitor ripple by ~50%. The DC capacitor ripple minimization scheme proposed in this paper for the segmented drive system can theoretically further cut the ripple current by additional 46%, by optimally selecting and placing the space vectors for the dual inverters collaboratively. Simulation results verified the scheme. A SiC-based prototype has been built and experimental results demonstrated 38% reduction.

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