DC Link Capacitor Reduction with Feedforward Control in Series-Series Compensated Wireless Power Transfer Systems

Subhajyoti Mukherjee, Veda P. Galigekere, Omer Onar, and Burak Ozpineci
Power Electronics and Electric Machinery Group, Oak Ridge National Laboratory, Oak Ridge, TN
Emails : mukherjees1@ornl.gov, galigekerevn@ornl.gov, onaroc@ornl.gov, burak@ornl.gov

***Abstract*—This paper presents the use of feedforward control to reduce the input side DC link capacitance of series-series compensated wireless power transfer (WPT) systems. Compared to conventional control schemes for WPT systems, the proposed feedforward-based approach achieves significant reduction in the DC link capacitor without any complicated voltage or current sensing requirements from the secondary side. This results in more compact hardware architecture. The proposed method shows minimal increase in the turn-on switching loss of the inverter. The switching loss is analyzed, and detailed results are presented relating the switching loss to the DC link capacitance and voltage ripple for proper tradeoff between losses and capacitor size. Simulation and experimental results presented validate the proposed scheme.**

***Keywords*—Wireless power transfer, series-series compensation, DC link capacitor minimization, feedforward control, switching loss, soft-switching**

NOMENCLATURE

v_g	Grid voltage
i_g	Grid current
v_{DC}	DC link voltage
V_{DCnom}	Nominal value of DC link voltage
V_{gpk}	Peak value of grid voltage
I_{gpk}	Peak value of grid current
v_{ab}	Output voltage of primary bridge
V_{out}	Output voltage
v_{abfun}	Fundamental component of v_{ab}
i_{pri}	Primary side current
L_g	Grid side inductor
C_{DC}	DC link capacitor
C_P	Primary side compensating capacitor
C_S	Secondary compensating capacitor
L_P	Primary side self-inductance
L_S	Secondary side self-inductance
L_M	Mutual inductance
C_{out}	Output capacitor
k	Coupling factor
R_{eq}	Equivalent ac load
α	Phase-shift between the primary bridge phase legs
φ	Power factor angle between i_{pri} and v_{abfun}
ω_g	Grid frequency

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I. INTRODUCTION

Wireless charging systems for electric vehicles are a research topic of immense interest for the past few years. Majority of the wireless chargers work on the principle of inductive power transfer where power is transferred across loosely coupled coils over an air gap. A typical series-series compensated wireless power transfer (WPT) system is shown in Fig. 1. The input voltage of a WPT system is generally supplied by an active front-end converter which ensures the grid current is at unity power factor [1], [2]. The active front-end can be single-phase or three-phase. In case of single-phase or unbalanced 3-phase system, the DC link voltage, is contaminated with ripple voltage at twice the frequency of the grid. This second harmonic ripple leads to losses and, if uncompensated, will propagate to the output in the form of relatively large power ripples. The ripple voltage at the output of a WPT system is undesirable and needs to be contained, and if possible, completely eliminated. The ripple on the DC link is generally reduced by increasing the DC link capacitance, thereby increasing the volume, weight and cost of the system. DC link capacitors typically occupy 20-50% of the total volume and their reduction is essential for compact systems. The utilization of additional hardware circuit to limit the ripple and reduce the DC link capacitance is suggested in [3], [4]. However, this leads to increased component count, enhanced control requirements and higher system cost.

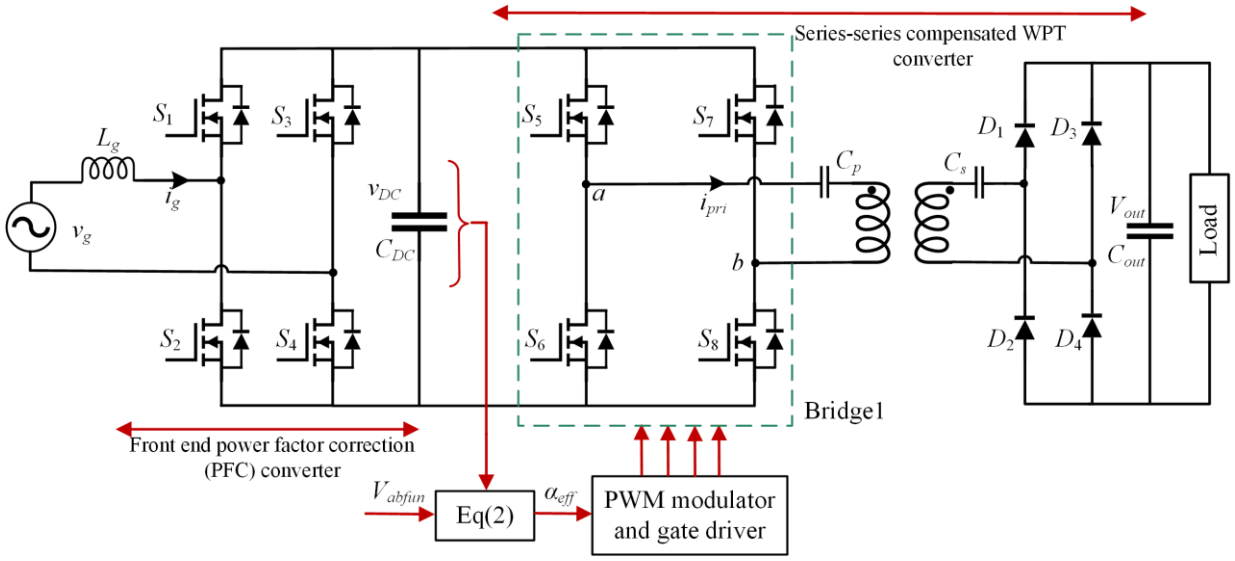

Fig. 1. Circuit of a WPT system supplied from 1-phase grid with the proposed feedforward control.

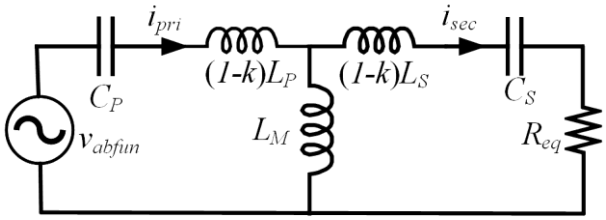

Fig. 2. Equivalent circuit of the resonant tank with equivalent load.

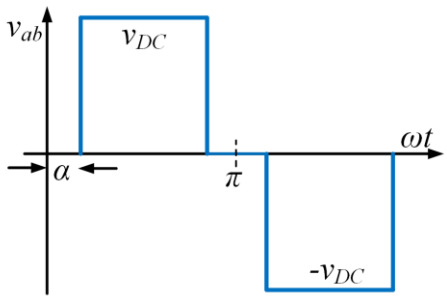

Fig. 3. Quasi square wave output of the inverter bridge

Sinusoidal charging which has been proposed in [5] is constrained by sinusoidal current being supplied to the load.

The ripple at the output of a WPT system can also be eliminated by feedback control. However, for WPT systems, the transmitter and receiver coils are physically separated, hence feedback of signals from the secondary to primary side has latencies larger than the switching period and might be unreliable. The secondary diode bridge rectifier (see Fig. 1) can be replaced by an active bridge whose modulation can be varied to eliminate the ripple from the output. However, this again increases the sensor count and gate drive requirements. Furthermore, active rectification on the secondary is challenging in terms of sensing and control since the high-frequency (~85 kHz) AC voltage at the input of receiver coil requires high bandwidth sensors. There is a need for a simple control system from the input side which ensures that the output of the WPT is steady while using reduced DC link capacitance.

Addressing the challenges mentioned above, this paper proposes a feedforward-based approach to modulate the switches on the primary of the WPT system as a function of the DC link voltage and maintain a steady output voltage under any DC bus conditions. The proposed control uses a voltage sensor for sensing the DC link voltage, which is free from high-frequency components; therefore, any low bandwidth cost-effective voltage sensor is sufficient to implement the proposed control scheme. The rest of the paper is organized as follows. The proposed control architecture is presented in details in Section II. The same section includes the effect and analysis of the proposed control scheme on converter losses. The simulation and experimental results are discussed in Section III, while the conclusions are presented in Section IV.

II. Control Architecture

A. Proposed Control Scheme to reduce DC Link Capacitance

A series-series compensated WPT converter supplied from the grid by a single-phase front-end PFC is shown in Fig. 1. The equivalent circuit of the resonant stage considering the first harmonic approximation is represented in Fig. 2. The proposed control will use feedforward control to modulate the switches in Bridge1 (S_5-S_8). Feedforward control is well established for DC-DC converters [6], [7]. The concept of feedforward control uses the information of the DC link voltage to directly modify the duty ratio of the switch to

achieve a desired output voltage (or current). Thus, for the application of feedforward control, the relation of the duty ratio of the switches, S_5-S_8, to the DC link voltage (v_{DC}) need to be established. In a WPT system, the switches S_5-S_8 operate at 50% duty ratio in complementary fashion and the output across the terminals '*a*' and '*b*' is generally varied by varying the phase-shift between the phase legs. Thus, for a WPT system to determine the desired feedforward algorithm, the relationship of the phase-shift to the DC link voltage is needed. The high-frequency inverter bridge output voltage, v_{ab}, can be a pure square wave or quasi-square wave. A typical v_{ab} in quasi-square wave mode of operation with phase-shift α between the phase legs is shown in Fig. 3. In his case, the magnitude of the fundamental component, v_{abfun}, is given as

$$v_{abfun} = \frac{4}{\pi} v_{DC} \cos\alpha \tag{1}$$

The proposed feedforward control will use v_{DC} to modify the phase-shift α and control v_{abfun} as desired. To produce the desired output voltage V_{abfun}, the phase-shift angle α_{eff} can be calculated as

$$\alpha_{eff} = \cos^{-1}\left(\frac{\pi}{4v_{DC}} V_{abfun}\right) \tag{2}$$

In (2) α_{eff}, is the required phase-shift α to obtain V_{abfun} under any v_{DC}. The DC bus voltage v_{DC} is already known through measurement. The phase-shift angle α_{eff} can be computed and the phase-shift between the phase legs modulated accordingly to maintain the output of Bridge1 as V_{abfun} under any DC bus conditions without the need of any feedback or secondary side control. Thus, a lower the DC link capacitance, C_{DC}, can be used allowing higher ripple on the DC bus. A block diagram implementation of the proposed control is shown in Fig. 1.

B. The Reduction in DC Link Capacitance

The application of feedforward control shows the potential in reducing the DC link capacitor, however, C_{DC}, cannot be reduced indefinitely and has a minimum allowable limit, C_{DCmin}. Using the small ripple approximation for the front-end stage [8], the DC link voltage ripple can be expressed as

$$\Delta V_{DC} = \frac{V_{gpk} I_{gpk}}{2\omega_g C_{DC} V_{DCnom}} \tag{3}$$

Using (3), the minimum DC link voltage can be expressed as

$$V_{DCmin} = V_{DCnom} - \frac{\Delta V_{DC}}{2} \tag{4}$$

The control objective is to keep the desired fundamental voltage, V_{abfun}, unchanged over the entire range of v_{DC}. Hence when v_{DC} is at its minimum value of V_{DCmin}, (1) can be modified as

$$V_{abfun} = \frac{4}{\pi} V_{DCmin} \left(\cos\alpha\right)_{max} \tag{5}$$

TABLE I
System Parameters

Grid Voltage (v_g)	480 V rms
Grid Frequency (ω_g)	60 Hz
Maximum Output Power	100 kW
Nominal DC link Voltage (V_{DCnom})	800 V
Primary and Secondary Inductance (L_P, L_S)	32.12 µH
Primary and Secondary Capacitance (C_P, C_S)	110 nF
Coupling Factor (k)	0.22
Switching Frequency (f_s)	85 kHz

In (5), $(\cos\alpha)_{max}$ is the maximum allowable value of $\cos\alpha$.

Substituting $(\cos\alpha)_{max} = 1$ in (5) results

$$V_{abfun} = \frac{4}{\pi} V_{DCmin} \tag{6}$$

Using (6) in (4)

$$\Delta V_{DC} = 2\left(V_{DCnom} - \frac{\pi}{4} V_{abfun}\right) \tag{7}$$

Again, using (7) in (3), the minimum DC link capacitance, C_{DCmin}, can be found as

$$C_{DCmin} = \frac{V_{gpk} I_{gpk}}{4\omega_g V_{DCnom}} \frac{1}{\left(V_{DCnom} - \frac{\pi}{4} V_{abfun}\right)} \tag{8}$$

An example of the reduction in DC link capacitance is demonstrated below. For a 100-kW application with the parameters as in Table1, DC link capacitance, C_{DC} of 16.6 mF is necessary to limit the DC link voltage ripple (ΔV_{DC}) to 2.5% of V_{DCnom}. For the same application, considering a maximum ripple voltage as 20% of V_{DCnom} of 800 V and considering $V_{abfun} = V_{DCmin}$, C_{DC} can be reduced to a minimum value of 2 mF thereby obtaining 87% reduction in the DC link capacitance.

C. Analysis of Converter Losses

The primary side high-frequency inverter (S_5-S_8 in Fig. 1) must achieve zero voltage turn-on (ZVS) conditions for high efficiency operation. Under quasi square wave mode of operation, two distinct situations may arise as depicted in Fig. 4. ZVS turn-on of the leading leg switches S_5 and S_6 is possible when the α is less than φ as shown in Fig. 4(a). In this scenario, during the switching transition from S_6 to S_5, the current through the corresponding phase leg (i_{pri}) is negative and vice versa. This facilitates natural discharging of the output capacitance of the incoming switch. However, in Fig. 4(b), where α is greater than φ, i_{pri} is positive during the transition from S_6 to S_5 and vice versa; therefore, in this scenario, ZVS turn-on of S_5 and S_6 is not possible. It can be observed from Fig. 4 that the lagging leg (S_7-S_8), undergoes ZVS in both switches as depicted by Fig. 4(a) and Fig. 4(b). The angle, φ, is

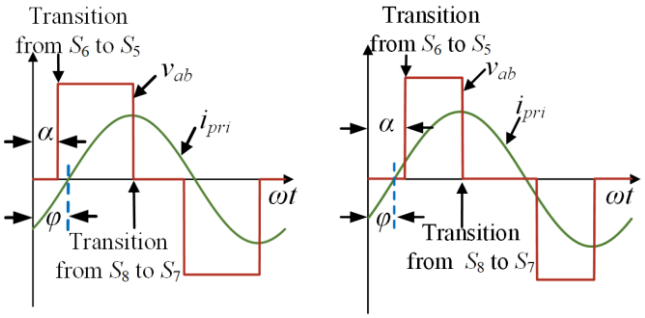

Fig. 4. Output of the inverter bridge and the primary side current of the WPT system, with (a) $\alpha<\varphi$ and (b) $\alpha>\varphi$.

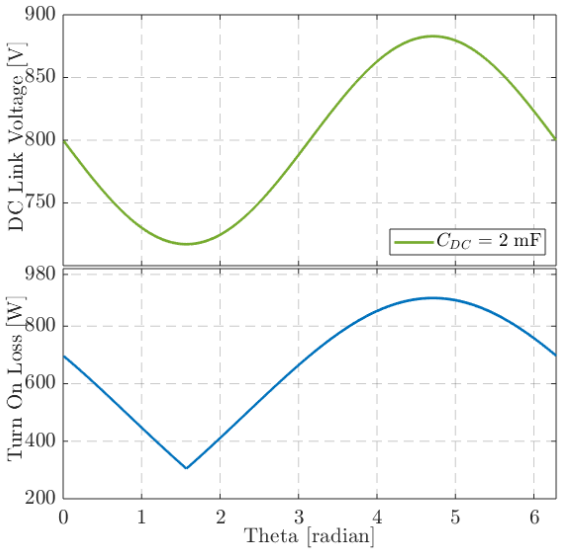

Fig. 6. Turn-on losses in S_5 for P_{out} = 100 kW with C_{DC} = 2 mF.

the angle of i_{pri} with respect to v_{abfun} and can be obtained by solving the equivalent circuit shown in Fig. 2, [9]-[12]. A series-series compensated WPT is operated at resonance frequency [9]-[12]. At this operating frequency, the primary current, i_{pri}, is in phase with v_{abfun}. Hence, the proposed feedforward control with quasi square wave output is analogous to the situation depicted in Fig. 4(b) and will incur additional switching losses which are due to the hard turn on of S_5 and S_6. Figs. 5-7 show the switching losses for a system using parameters listed in Table.1. The turn-on loss for switch S_5 is shown in Fig. 5 for one cycle of the DC link voltage with DC link capacitance of 2 mF. The peak to peak DC link ripple for an output power of 100 kW is 170 V (about 21% of the nominal DC link voltage of 800 V). The turn-on loss is minimum at the minimum value of the DC link voltage where the angle α approaches zero and is maximum at the peak of the DC link voltage, where α is maximum. The average turn-on loss is 665W which is 0.67% of the total output. It can also be observed from Fig. 5, that at the minimum DC link voltage where both α and φ are close to zero, the turn-on loss is not zero and has a finite value. This loss represents the output parasitic capacitance (C_{oss}) loss of the devices.

The turn-on loss for different DC link capacitance at output power of 100 kW is shown in Fig. 6. The plots show that with

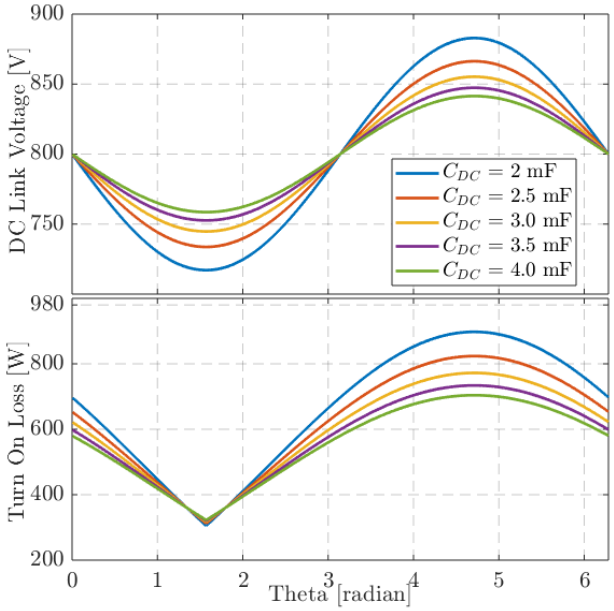

Fig. 4. Turn-on losses in S_5 for P_{out} = 100 kW for different C_{DC}.

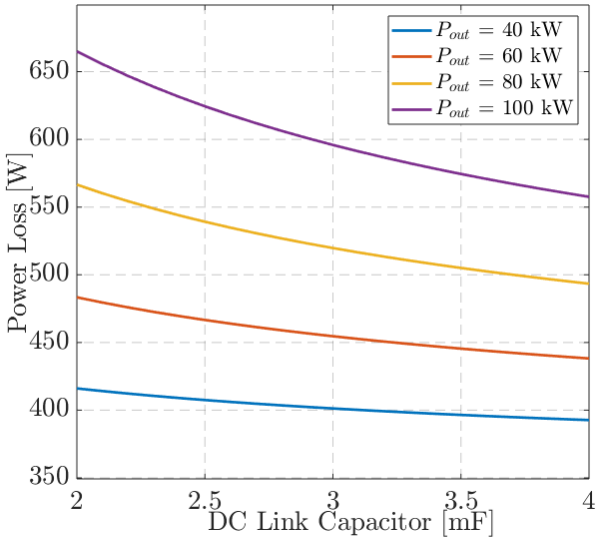

Fig. 5. Average turn-on losses in S_5 and S_6 for different P_{out} and C_{DC}.

reduction in DC link capacitance (corresponding to increased ripple voltage on the DC link) the turn on switching loss increases. This increase is attributed to the fact that at higher ripple voltage, the proposed control increases the phase-shift angle α, to maintain a steady value of v_{abfun}. With the increase in α, the current, i_{pri}, at the switching instant increases contributing to increased turn-on loss of S_5 and S_6. The load resistance is varied and the total switching loss (average) of the bridge is plotted (Fig. 7) for different DC bus capacitance at different output power levels. This figure shows the average increase in losses with reduction of the DC link capacitance. From the figure, it can be estimated that at an output power of 100 kW, a decrease in DC link capacitance of 50% (2 mF from 4 mF) increased switching losses by only 0.67%. At P_{out} of 40 kW the same decrease in DC link capacitance of 50% (2 mF

from 4 mF) increased switching losses by only 1.05%. Depending on the output power, the plots in Fig. 6 and Fig. 7 help to determine the tradeoff between the selection of the DC link capacitor and the minor reduction in efficiency. Additional ZVS assisting circuits as in [13], [14], can be added to ensure ZVS turn on of S_5 and S_6.

III. Results

A. Simulation Studies

The proposed feedforward control algorithm is verified through simulation in Piecewise Linear Electrical Circuit Simulation (PLECS) platform. The system parameters used for simulation studies are as in Table.1. The DC link capacitor, C_{DC}, is fixed at 2 mF and the results with and without the feedforward control is shown in Fig. 8. The figure shows that for 162 V (corresponding to 20% of V_{DCnom}) ripple on the input or front-end DC link, the output voltage has about 125 V ripple without the feedforward control, which reduced drastically with the proposed feedforward control. The figure confirms that for the same DC link capacitance, the proposed feedforward control can maintain a steady and non-oscillatory output voltage under varying DC link voltages (given in red trace). Simulation results showing the improvements of the proposed control with C_{DC} = 2 mF over conventional control with C_{DC} = 16.6 mF are presented in Fig. 9. For the same output power, the input DC link has a ripple of 162V for C_{DC} = 2 mF. Generally, this ripple is suppressed using higher capacitance value. For example, here C_{DC} = 16.6 mF reduced the DC link ripple to 20V. However, it can be seen from Fig. 10 that even with a higher C_{DC} of 16.6 mF, the output voltage with conventional open-loop control has more ripple (approximately 17 V) compared to the output under the proposed feedforward control with a C_{DC} of 2 mF. The proposed feedforward control achieves steadier output voltage with 1/8 of the original capacitance (2 mF compared to 16.6 mF).

The dynamic performance of the proposed feedforward control is presented in Fig. 10 and Fig. 11. The WPT system is started with an oscillatory input DC link (corresponding to C_{DC} = 2 mF) and then the proposed feed forward control is applied at t=0.06 seconds. The results are shown in Fig. 10, where it is observed that the oscillatory output voltage became constant and non-oscillatory as soon as the feedforward control is applied. The performance of the proposed feedforward control in regulating the output with change (both increase and decrease) in the input DC link oscillations is demonstrated in Fig. 11. The input DC link ripple is reduced from 160 V to 80 V and after 4 ripple cycles changed back to 160 V. It is seen from Fig. 11 that during both the high to low or low to high transitions in the DC link ripple the output voltage was steady and relatively constant with the proposed feedforward control.

B. Experimental Verification

Experiments were conducted at a reduced power of 2.5 kW to validate the proposed control scheme. The hardware setup used for the experimental results is shown in Fig. 12. In this setup, primary and secondary coil inductances are 74.83 µH and 85.77 µH, respectively. On each side, series resonant

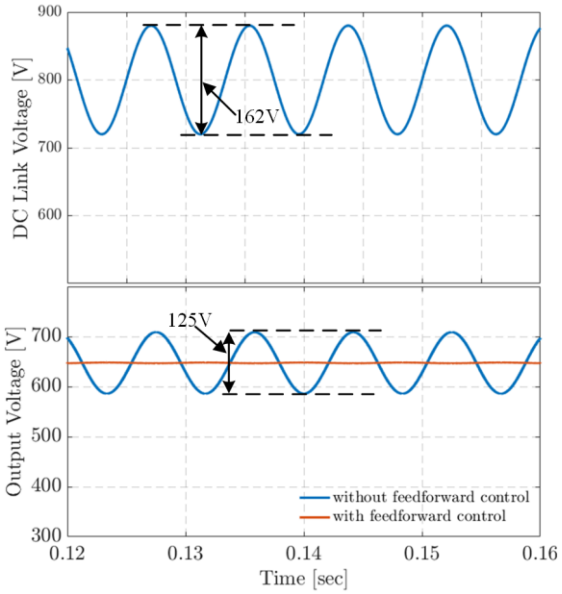

Fig. 8. DC link and output voltage with C_{DC} = 2 mF with and without the proposed control.

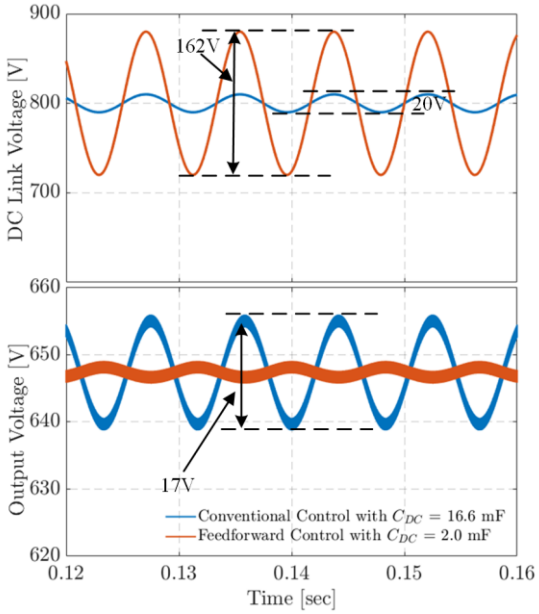

Fig. 9. DC link and output voltage with C_{DC} = 16.6 mF without the proposed control and C_{DC} = 2 mF with the proposed control.

tuning capacitances are calculated to tune-out these coil self-inductances at 85 kHz of nominal frequency. The coil dimensions are 711×711×20 (mm) and 381 × 482 × 25.4 (mm) for the primary and secondary couplers, respectively while the magnetic airgap is 6 inches.

The improvement of the output voltage under varying DC link voltages with and without the proposed feedforward control is demonstrated in Fig. 13. With a lower DC link capacitor, v_{DC}, has a ripple of about 26V (15% ripple). With the conventional open-loop control, this ripple is transferred to the output and is directly reflected on V_{out}. With the conventional

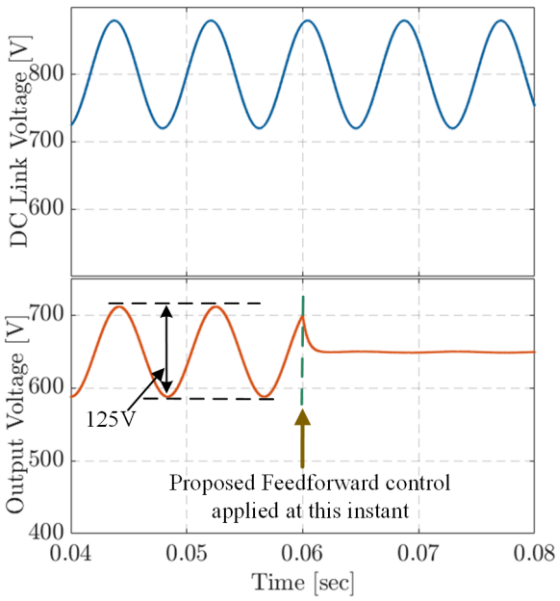

Fig. 10. Output voltage before and after applying the proposed control.

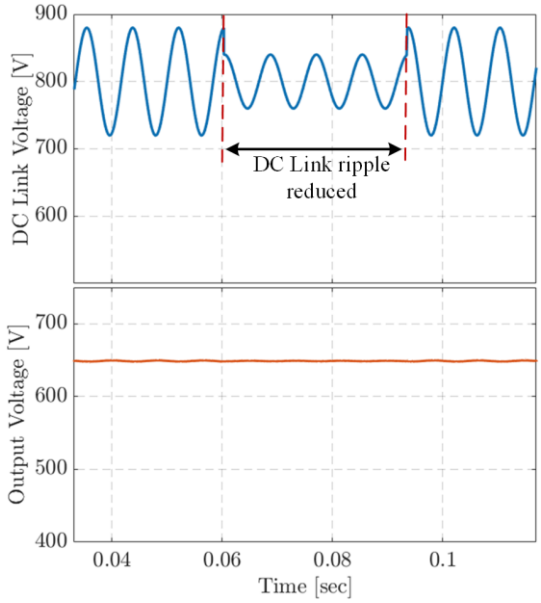

Fig. 11. Output voltage with the proposed control with variations of ripple voltage in the DC link.

control, as seen from Fig. 13, V_{out} has a ripple of about 20% (corresponding to 30V). However, with the proposed control, this ripple of V_{out} is reduced to 5% (corresponding to 7.5V).

The dynamic performance of the proposed control is demonstrated in Fig. 14 and Fig. 15. The input DC link voltage, v_{DC}, being unchanged, the controller is switched from uncompensated system to the proposed feedforward control algorithm and the results are shown in Fig. 14. It can be observed from the figure, that before the proposed control was initiated the output voltage, V_{out} had a significant ripple (about 30V). However, the ripple is drastically reduced and V_{out}

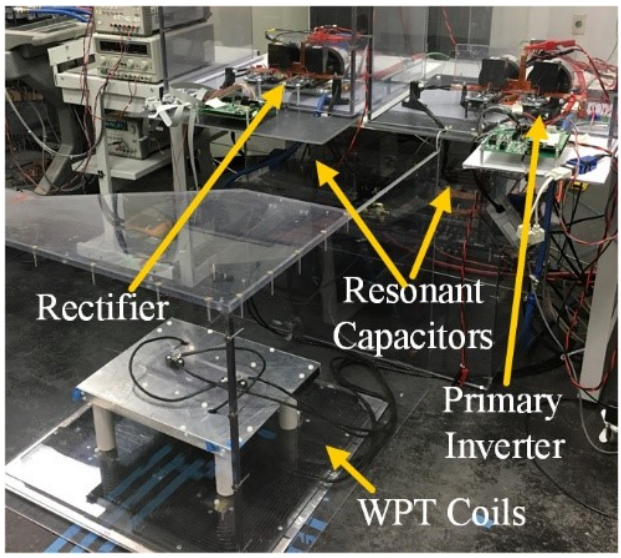

Fig. 12. Hardware prototype for experimental verification.

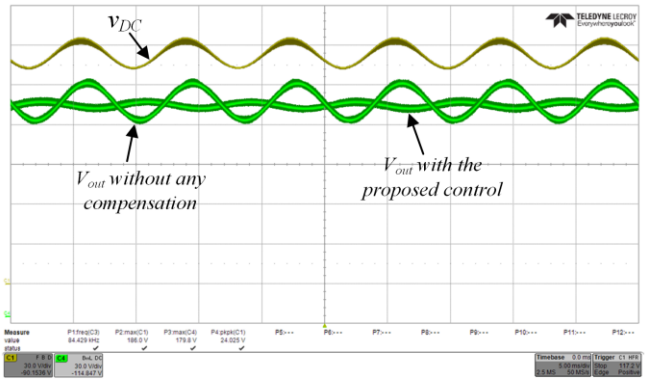

Fig. 13. Output voltage with and without the proposed feedforward control. (v_{DC} = 30V/div, V_{out} = 30V/div, x-axis (time) : 5ms/div)

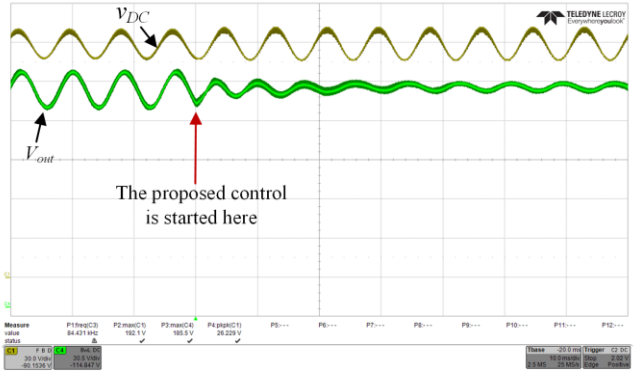

Fig. 14. Dynamic performance of the proposed control in reducing the output voltage ripple. (v_{DC} = 30V/div, V_{out} = 30V/div, x-axis (time): 5ms/div)

becomes steady as soon as the proposed control is started. With the system operating under the proposed control, v_{DC} is changed from zero ripple to 15% ripple as shown in Fig. 15. The figure shows that the proposed control was able to maintain steady V_{out} even under oscillatory v_{DC} conditions with

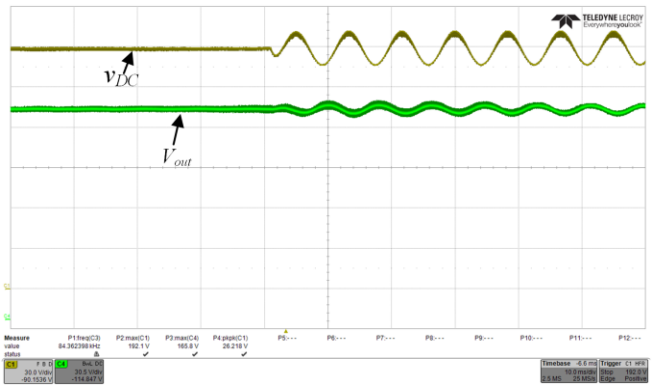

Fig. 15. Output voltage with introduction of oscillation in the DC link voltage. (v_{DC} = 30V/div, V_{out} = 30V/div, x-axis (time) : 5ms/div)

an output ripple less than 5%. The Figs. 14 and 15 confirm that the proposed feedforward control operates as expected during the transitions.

IV. Conclusion

This paper proposed a novel feedforward control to reduce the DC link capacitor in WPT systems, especially if supplied from single phase or three phase unbalanced grid. The feedforward algorithm is derived and its relation to the reduction of DC link capacitor is established. It is demonstrated that the proposed feedforward control approach has the potential of significant reduction of the DC link capacitance at a minimal increase in the switching loss. Simulation and experimental results presented support the validity of the control scheme.

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References

[1] S. Li, and C. Mi, "Wireless power transfer for electric vehicle applications," *IEEE J. Emerg. Sel. Topics Power Electron*, vol.3, no.1, pp.4,17, March 2015.

[2] J. M. Miller, O. C. Onar, and M. Chinthavali, "Primary-side power flow control of wireless power transfer for electric vehicle charging," *IEEE J. Emerg. Sel. Topics Power Electron*, vol. 3, no. 1, pp. 147-162, March 2015.

[3] H. Wang, H.-H. Chung, and W. Liu, "Use of a series voltage compensator for reduction of the DC-link capacitance in a capacitor-supported system," *IEEE Trans. Power Electron.*, vol. 29, pp. 1163–1175, March 2014.

[4] W. Ruxi, F. Wang, D. Boroyevich, R. Burgos, L. Rixin, N. Puqi, and K. Rajashekara, "A high power density single-phase pwm rectifier with active ripple energy storage," *IEEE Trans. Power Electron.*, vol. 26, pp. 1430-1443, 2011.

[5] L. Xue, D. Shen, D. Boroyevich, P. Mattavelli, and D. Diaz, "Dual active bridge-based battery charger for plug-in hybrid electric vehicle with charging current containing low frequency ripple," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 7299–7307, Dec. 2015.

[6] M. K. Kazimierczuk and A. Massarini, ``Feedforward control of DC-DC PWM boost converter," *IEEE Trans Circuits Syst.-I.*, vol. 44, no. 2, pp. 143-148, Feb. 1997.

[7] B. Arbetter and D. Maksimovic, "Feedforward pulse width modulators for switching power converters," *IEEE Trans. Power Electron*., vol. 12, no. 2, pp. 361–368, Mar. 1997.

[8] N. S. Gonzalez-Santini, B. Ozpineci, M. Chinthavali, and F. Z. Peng, "The effects of the resonant network and control variables on the dclink capacitor of a wireless charging system," in *IEEE Transportation Electrification Conference and Expo (ITEC)*, June 2017, Chicago, IL, USA.

[9] O.C. Onar, M. Chinthavali, S. L. Campbell, L. E. Seiber, C. P. White, V. P. Galigekere, "Modeling, Simulation, and Experimental Verification of a 20 kW Series-Series Wireless Power Transfer system for a Toyota RAV4 Electric Vehicle," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 874–880, June 2018, Long Beach, CA, USA .

[10] S. Y. Cho, I. O. Lee, S. C. Moon, B. C. Kim, and K. Y. Kim, "Series-series compensated wireless power transfer at two different resonant frequencies," in *Proc. IEEE ECCE Asia Downunder*, pp. 1052–1058, June 2013, Melbourne, VIC, Australia.

[11] W. Zhang and C. C. Mi, "Compensation topologies of high-power wireless power transfer systems," *IEEE Trans. Veh. Technol.*, vol. 65, no. 6, pp. 4768–4778, Jun. 2016.

[12] Z. U. Zahid, Z. M. Dalala, C. Zheng, R. Chen, W. E. Faraci, J. S. Lai, G. Lisi, D. Anderson, "Modeling and Control of Series-Series Compensated Inductive Power Transfer System," *IEEE J. Emerg. Sel. Topics Power Electron*, vol.3, no. 1, pp.111-123, Mar. 2015

[13] R. W. De Doncker and J. P. Lyons, "The auxiliary resonant commutated pole converter," in *Proc. IEEE Industry Applications Society Annual Meeting*, pp. 1228-1235 vol.2, Seattle, WA, USA, 1990.

[14] B. Ozpineci and B. K. Bose, "A soft-switched performance enhanced high frequency non-resonant link phase-controlled converter for ac motor drive," in *Proc. IEEE IECON Conf. Rec.*, 1998, pp. 733–739, Aachen, Germany, Sept 1998.