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Low-frequency dc bus ripple cancellation in single phase pulse-width modulation inverters

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Abstract: This study presents a topology for a single-phase pulse-width modulation (PWM) converter which achieves low-frequency ripple reduction in the dc bus even when there are grid frequency variations. A hybrid filter is introduced to absorb the low-frequency current ripple in the dc bus. The control strategy for the proposed filter does not require the measurement of the dc bus ripple current. The design criteria for selecting the filter components are also presented in this study. The effectiveness of the proposed circuit has been tested and validated experimentally. A smaller dc-link capacitor is sufficient to keep the low-frequency bus ripple to an acceptable range in the proposed topology.

1 Introduction

The use of pulse-width modulated (PWM) converters as active front ends are becoming quite popular as it not only facilitates bidirectional transfer of power between the ac grid and the dc bus bar; but also ensures very high power quality [1]. They have become quite indispensable in various distributed generation (DG) applications for interfacing the DG unit with the grid. However, the low-frequency dc ripple current in single-phase PWM converters is a critical issue when a battery or a DG source is connected to the dc bus [2, 3]. The ripple current heats up the battery and shortens its life [4, 5]. In photovoltaic applications, the dc bus ripple shifts the operating point of a panel away from the desired maximum power point tracking condition [6–9]. In fuel cell-based power conditioning system, the ripple current should be minimised to ensure energy efficient operation and to improve the life and durability of the fuel cell stack [10–14].

The low-frequency ripple in the dc bus arises because of energy fluctuations inherent in a single-phase system [15, 16]. These energy fluctuations have to be absorbed to tackle the issue of low-frequency ripple. A filter used for ripple cancellation should be able to store the ripple energy. The ripple energy can be stored in the electrostatic field of a capacitor [17, 18]. Here, sufficient amount of capacitance is needed in parallel to the dc bus so that the ripple current is bypassed by the capacitor as in Fig. 1*a*. In low voltage, high current applications, the value of capacitance necessary for effective ripple filtering can even go up to several farads in order to meet the tight voltage ripple requirement. Hence, this is not practically feasible in many situations. Another approach is to store the ripple energy in the electromagnetic field of an inductor. Although inductors are superior to capacitors in terms of ruggedness and reliability, they are inferior in terms of power density and weight. Power loss in inductors is also much higher than capacitors when working with switching inverter circuits [19]. So storing the ripple energy using only inductor is not preferred.

The next option is to use both inductor and capacitor for storing the ripple energy. There is a possibility that the good aspects of both the methods can be combined to get an optimum design. One such method is to use a passive inductor–capacitor (LC) resonant circuit in parallel to the dc bus as shown in Fig. 1*b*. The LC tuned trap filter is designed such that its resonance frequency matches with the ripple frequency [20–22]. The bandwidth of the filter is decided by L_{ac} and C_{ac} values. High L_{ac} and small C_{ac} imply narrow filter notch bandwidth whereas large C_{ac} and small L_{ac} imply larger bandwidth. In applications, such as micro-grid and traction, the frequency variations from 50 Hz are sufficiently large and cannot be neglected. As a result, the dc bus ripple frequency also changes. The filter becomes ineffective as its parameters are fixed unless its notch bandwidth is very high [23]. If the grid frequency varies significantly, passive circuits will not be useful. Hence, an active filter is preferable to handle the grid frequency variations.

Many active filter topologies for dc bus filtering are discussed in the literature [4, 5, 15, 16, 19, 22, 24–26]. Here also, the energy storage element can be a capacitor or an inductor. In [4], the ripple energy is stored in filter capacitors provided in the ac side by appropriately switching a third active leg. However, these input capacitors will introduce a phase lead in the ac side current which is undesirable. In [5], the ripple energy is stored purely in the inductor, L, as shown in Fig. 1*c* and a third active leg is added to a conventional single-phase PWM converter. This leg is switched for the minimisation of dc bus low-frequency current ripple. Since, the ripple energy is completely stored in the electromagnetic field, the cost and size of the filter will be high. However, the dc bus capacitor can be significantly reduced as it now has to handle only the switching frequency components. The third active leg and the filter inductor, L should be rated to handle the full ripple volt-ampere (VA). This leads to higher cost. An active filter variant which also makes use of inductive energy storage is proposed in [26]. A control algorithm is presented where the dc bus current needs to be sensed. This approach is difficult to implement as the dc bus is usually made of sandwiched copper plates to minimise the dc bus inductance. Any inserted dc bus current sensor would increase the dc bus parasitic inductance. In [19], the shortcomings of some of the existing active filter topologies are discussed. A new PWM converter topology is presented. Both inductor and capacitor are used to store the ripple energy by switching a third active leg. However, the active components have to be rated to handle the full ripple VA. Another commonly used approach is to introduce a power converter as a series element between the dc source and the dc bus as in [27, 28]. The control objective is to increase the effective impedance of the dc source as seen from the dc bus thereby forcing the double-frequency ripple current to flow through a smaller dc bus capacitance. The series element should be rated to handle the full power. This converter should also have bi-directional power flow capability if the dc source is a battery that requires charging.

In this paper, a novel shunt connected dc bus hybrid filter topology shown in Fig. 2 is discussed. The advantages of electrostatic as well as electromagnetic energy storage are utilised. The VA rating of the active components is reduced to a fraction of

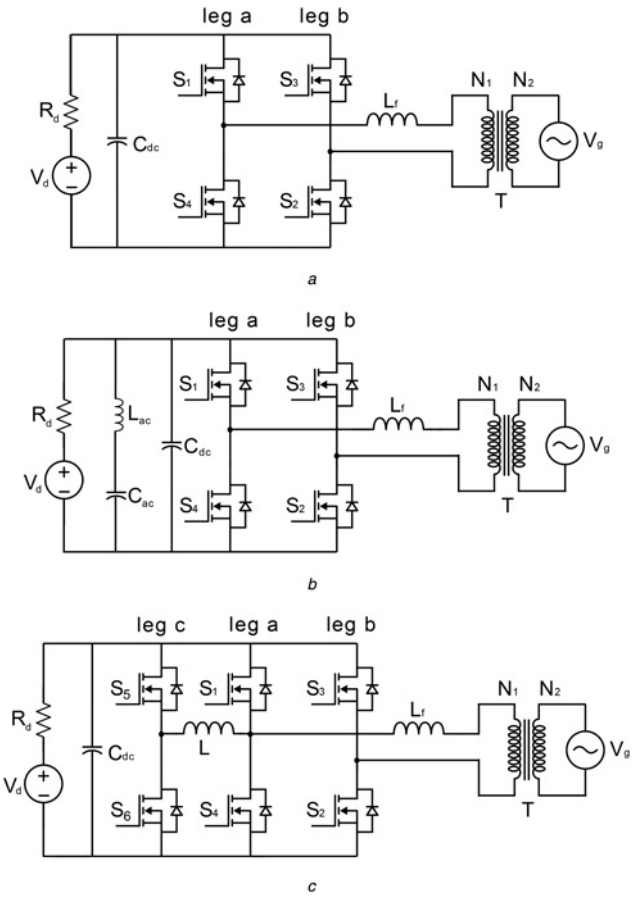

Fig. 1 *Single-phase PWM inverter with dc bus filter options*

a Purely capacitive filter using large dc bus capacitance
b Tuned LC filter
c Inductor-based active filter

the ripple VA. Grid frequency variations are actively accommodated. A systematic design procedure is presented to select the components for the proposed filter. The proposed topology has design flexibility to reduce the cost of the filter without compromising the system efficiency. A control method is proposed for the new topology that does not need to sense the dc bus current. A laboratory prototype is built and the validity of the proposed scheme is verified at a power level of 150 VA.

2 Power circuit topology

Fig. 2 shows the topology of the proposed PWM converter with the hybrid filter. The conventional PWM converter consists of switches

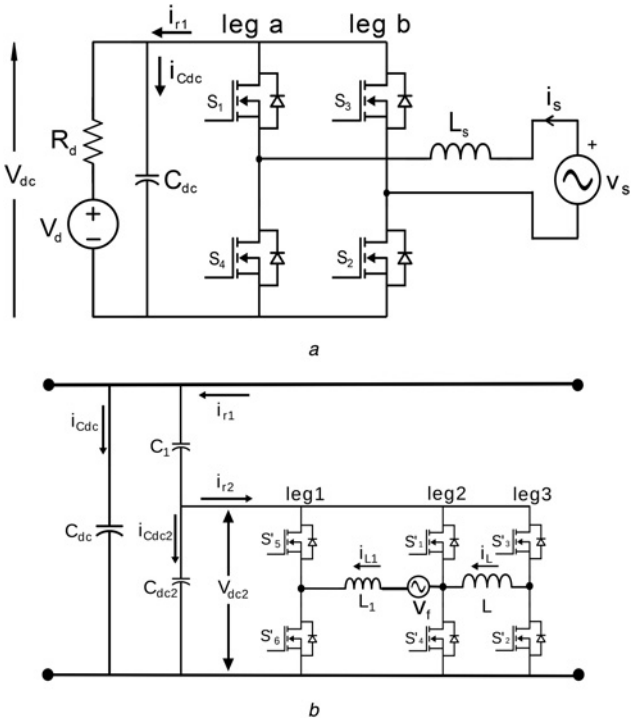

Fig. 3 *Schematic of the circuits used for ripple power analysis*

a Main single-phase converter
b Hybrid filter topology

S_1–S_4, dc bus capacitor, C_{dc} and filter inductor, L_s. It is connected to the grid through a transformer.

The hybrid filter consists of switches S_1'–S_6', dc bus capacitor, C_{dc2} and energy storage elements. The capacitor, C_1 and inductor, L are the energy storage elements of the hybrid filter. The hybrid filter is also connected to the grid through a transformer. The principle of operation of the single-phase converter with hybrid dc ripple filter is explained below.

2.1 Main converter

In [15], an analysis is presented to determine the low-frequency current ripple in the dc bus of a PWM converter operating as an active rectifier using instantaneous power theory. This concept has been extended in this work to obtain the ripple current injection required to compensate the dc bus voltage ripple at any operating power factor angle. This is then utilised to control the hybrid filter converter.

2.1.1 DC bus ripple analysis: Let v_s denotes the grid voltage and i_s is the grid current and their instantaneous polarities be as

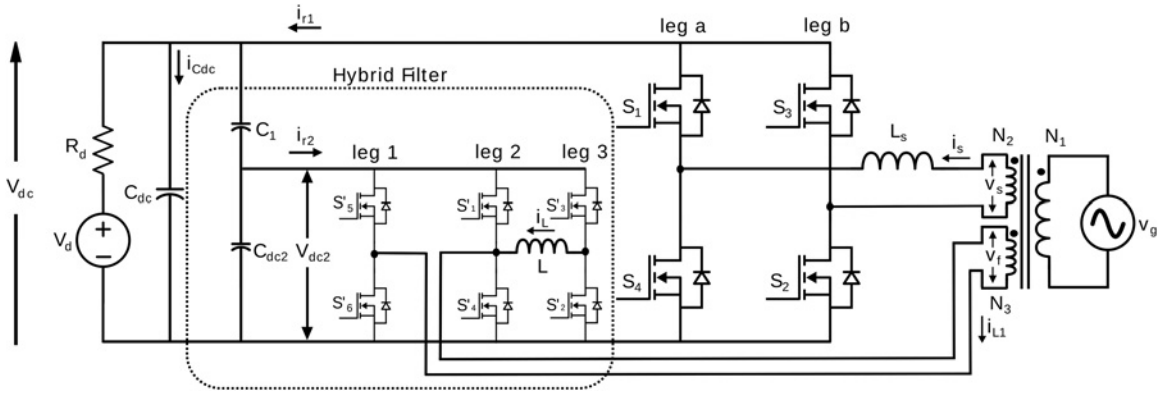

Fig. 2 *Circuit topology of the single-phase PWM inverter with reduced dc voltage hybrid filter*

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shown in Fig. 3*a*. Let the power factor angle be ϕ

$$v_s = \sqrt{2}V_s\sin(\omega t) \tag{1}$$

$$i_s = \sqrt{2}I_s\sin(\omega t + \phi) \tag{2}$$

where V_s and I_s are the root-mean-square values of voltage and current, respectively. The input power, P_s is given by

$$P_s = v_s i_s = V_s I_s[\cos\phi - \cos(2\omega t + \phi)] \tag{3}$$

The inductor L_s acts as a boost component to transfer power from ac side to dc side. The instantaneous power in the inductor is given by

$$P_{L_s} = i_s L_s \frac{\mathrm{d}i_s}{\mathrm{d}t} = \omega L_s I_s^2 \sin(2\omega t + 2\phi) \tag{4}$$

The power output of the converter or the dc side power, P_o is given by

$$\begin{aligned} P_o &= v_s i_s - i_s L_s \frac{\mathrm{d}i_s}{\mathrm{d}t} \\ &= V_s I_s\cos\phi - V_s I_s\cos(2\omega t + \phi) \\ &\quad - \omega L_s I_s^2\sin(2\omega t + 2\phi) \end{aligned} \tag{5}$$

The ripple component of output power is termed as ripple power and is denoted by P_r

$$P_r = -V_s I_s\cos(2\omega t + \phi) - \omega L_s I_s^2\sin(2\omega t + 2\phi) \tag{6}$$

Assuming a constant V_{dc}, the dc bus ripple current, i_{r1} is given by

$$\begin{aligned} i_{r1} &= \frac{P_r}{V_{dc}} \\ &= \frac{-V_s I_s\cos(2\omega t + \phi) - \omega L_s I_s^2\sin(2\omega t + 2\phi)}{V_{dc}} \\ &= -\frac{I_s\sqrt{(V_s^2 + \omega^2 L_s^2 I_s^2 + 2V_s\omega L_s I_s\sin\phi)}}{V_{dc}} \\ &\quad \times \sin(2\omega t + \psi) \end{aligned} \tag{7}$$

where

$$\psi = \tan^{-1}\left(\frac{\omega L_s I_s\sin 2\phi + V_s\cos\phi}{\omega L_s I_s\cos 2\phi - V_s\sin\phi}\right) \tag{8}$$

Equations (7) and (8) provide the necessary ripple current amplitude and the phase that needs to be compensated by the hybrid filter.

2.2 Hybrid filter

The hybrid filter consists of three legs as shown in Fig. 3*b*. Ripple energy is stored in both capacitor C_1 and inductor L. Here, leg 2 and leg 3 are switched so as to inject a ripple, i_{r2} in the auxiliary dc bus. By applying Kirchhoff's current law at the dc bus in Fig. 3*b*

$$i_{Cdc} = i_{r1} - (i_{r2} + i_{Cdc2}) \tag{9}$$

If $C_{dc2} \ll C_1$, then

$$i_{Cdc} \simeq i_{r1} - i_{r2} \tag{10}$$

This implies that, if the 100 Hz ripple current in the main converter is recreated in i_{r2}, then the 100 Hz ripple in C_{dc} will be eliminated. The value of C_{dc2} should be sufficiently small compared to C_1 to ensure that ripple current because of main converter is absorbed by the filter. The ripple current in the auxiliary dc bus, i_{r2} is determined by the compensation current, i_L and the modulation of legs 2 and 3 of the hybrid filter converter. The compensation current is obtained as explained in Section 2.3.

The voltage V_{dc2} should be kept constant for controlling the current in the inductor, L. If there is no mechanism to regulate V_{dc2}, it will keep on falling because of the losses in the hybrid filter converter. These losses mainly include the conduction and switching losses of the filter converter. The active power required to meet the losses has to be supplied. So an additional leg 1 is introduced to handle this which is connected to the grid as shown in Fig. 2. Leg 1 is switched to maintain V_{dc2} at a desired level.

The value of V_{dc2} can be made small with respect to V_{dc} in (15) to reduce the rating of active components in the system and the inductor. Even though, there are six switches in the filter converter, they have to handle only a fraction of the ripple VA as most of the ripple energy is stored in the capacitor, C_1. Hence, the losses associated with the hybrid filter are very small and the overall system efficiency is not compromised. Similarly, the VA rating of the inductor, L is also reduced. The cost and the size of the filter can thus be reduced by appropriately choosing V_{dc2}, as discussed in Section 3.4.

2.3 Compensation current for ripple cancellation

The instantaneous power in the dc bus of the filter converter is same as the instantaneous power in the inductor, L. The contribution from the source v_f and the inductor L_1 is not considered as they handle power which is just enough to meet the losses of the filter converter and is negligible compared to the power handled by the inductor, L. Assuming a constant V_{dc2}, the ripple current in the dc bus of the auxiliary converter is given by

$$i_{r2} = \frac{P_L}{V_{dc2}} = \frac{i_L L(\mathrm{d}i_L/\mathrm{d}t)}{V_{dc2}} \tag{11}$$

For ripple cancellation, the currents $i_{r2} = i_{r1}$ from (10). Hence, the instantaneous power in the filter inductor, L can be expressed by the following equation

$$\begin{aligned} i_L L\frac{\mathrm{d}i_L}{\mathrm{d}t} &= -\frac{V_{dc2}}{V_{dc}} I_s\sqrt{(V_s^2 + \omega^2 L_s^2 I_s^2 + 2V_s\omega L_s I_s\sin\phi)} \\ &\quad \times \sin(2\omega t + \psi) \end{aligned} \tag{12}$$

Let the required compensation current be of the form $i_L = A_{iL}\cos(\omega t + \psi/2)$, where ψ is given by (8)

$$L\frac{\mathrm{d}i_L}{\mathrm{d}t} = -A_{iL}L\omega\sin\left(\omega t + \frac{\psi}{2}\right) \tag{13}$$

$$i_L L\frac{\mathrm{d}i_L}{\mathrm{d}t} = -\frac{A_{iL}^2 L\omega}{2}\sin(2\omega t + \psi) \tag{14}$$

From (12) and (14), the amplitude of the compensation current can be analytically obtained as

$$A_{iL} = \sqrt{\frac{2V_{dc2}I_s}{L\omega V_{dc}}\sqrt{V_s^2 + \omega^2 L_s^2 I_s^2 + 2V_s\omega L_s I_s\sin\phi}} \tag{15}$$

Hence, the instantaneous compensation current is

$$i_L = A_{iL}\cos\left(\omega t + \frac{\psi}{2}\right) \tag{16}$$

where A_{iL} and ψ are given by (15) and (8), respectively.

2.4 Validity of the proposed strategy

For the control strategy to be valid, the instantaneous ripple power generated by the main converter should be equal to the instantaneous power generated by the hybrid filter which is the sum of the instantaneous powers in the capacitor, C_1 and the inductor, L. The instantaneous power in the link capacitor, C_1 is given by

$$\begin{aligned} P_{C1} &= i_r \frac{1}{C_1}\int i_r dt + i_r(V_{dc} - V_{dc2}) \\ &= -\frac{(V_s^2 + \omega^2 L_s^2 I_s^2 + 2V_s \omega L_s I_s \sin\phi) I_s^2}{4C_1 V_{dc}^2 \omega} \\ &\quad \times \sin(4\omega t + 2\psi) \\ &\quad - I_s\sqrt{(V_s^2 + \omega^2 L_s^2 I_s^2 + 2V_s \omega L_s I_s \sin\phi)} \\ &\quad \times \frac{(V_{dc} - V_{dc2})}{V_{dc}} \sin(2\omega t + \psi) \end{aligned} \tag{17}$$

The instantaneous power in filter inductor, L is given by

$$\begin{aligned} P_L &= i_L L \frac{di_L}{dt} \\ &= -\frac{V_{dc2}}{V_{dc}} I_s \sqrt{(V_s^2 + \omega^2 L_s^2 I_s^2 + 2V_s \omega L_s I_s \sin\phi)} \\ &\quad \times \sin(2\omega t + \psi) \end{aligned} \tag{18}$$

For absorbing the ripple power in (6) completely, $P_r = P_L + P_{C1}$. Hence, $P_L = P_r - P_{C1}$ can be expressed as

$$\begin{aligned} P_L &= \frac{(V_s^2 + \omega^2 L_s^2 I_s^2 + 2V_s \omega L_s I_s \sin\phi) I_s^2}{4C_1 V_{dc}^2 \omega} \\ &\quad \times \sin(4\omega t + 2\psi) \\ &\quad - I_s\sqrt{(V_s^2 + \omega^2 L_s^2 I_s^2 + 2V_s \omega L_s I_s \sin\phi)} \\ &\quad \times \frac{V_{dc2}}{V_{dc}} \sin(2\omega t + \psi) \end{aligned} \tag{19}$$

Comparing (18) and (19), the control strategy is valid if and only if the 4ω ripple in the link capacitor is negligible. That is, the ripple voltage in C_1 should be negligible compared to the dc voltage across it. Equations (8) and (15) provide the reference current for the auxiliary converter in terms of main converter current amplitude and power factor. The closed form expression for compensation current under unity power factor (UPF) and zero power factor (ZPF) conditions of the main power converter is tabulated in Table 1. In Table 1, the following operations are considered: inverter current is in phase with grid voltage (UPF rectification); inverter current leads the grid voltage by 90° (ZPF

Table 1 Expressions for compensation current under different operating modes of the main converter

Power factor	$i_L = A_{iL}\cos(\omega t + \psi/2)$
1 (UPF rectification)	$A_{iL} = \sqrt{\frac{2V_{dc2}I_s}{L\omega V_{dc}}\sqrt{V_s^2 + (\omega L_s I_s)^2}}$
	$\psi = \tan^{-1}\left(\frac{V_s}{\omega L_s I_s}\right)$
0 (ZPF lead)	$A_{iL} = \sqrt{\frac{2V_{dc2}I_s}{L\omega V_{dc}}(V_s + \omega L_s I_s)}$
	$\psi = \pi$
0 (ZPF lag)	$A_{iL} = \sqrt{\frac{2V_{dc2}I_s}{L\omega V_{dc}}(V_s - \omega L_s I_s)}$
	$\psi = 0$
1 (UPF inversion)	$A_{iL} = \sqrt{\frac{2V_{dc2}I_s}{L\omega V_{dc}}\sqrt{V_s^2 + (\omega L_s I_s)^2}}$
	$\psi = \tan^{-1}\left(\frac{-V_s}{\omega L_s I_s}\right)$

Table 2 Circuit parameters for the laboratory 1ϕ converter with the hybrid filter

main converter components		
MOSFET switches	$S_1 - S_4$	100 A, 50 V
input ac filter inductor	L_s	250 μH
DC Bus capacitor	C_{dc}	33 mF
transformer	$N1{:}N2$	16:1
hybrid filter components		
MOSFET switches	$S_1' - S_6'$	100 A, 50 V
DC bus capacitor	C_{dc2}	3.3 mF
filter inductor	L	270 μH
filter/link capacitor	C_1	33 mF
transformer	$N1{:}N3$	24:1

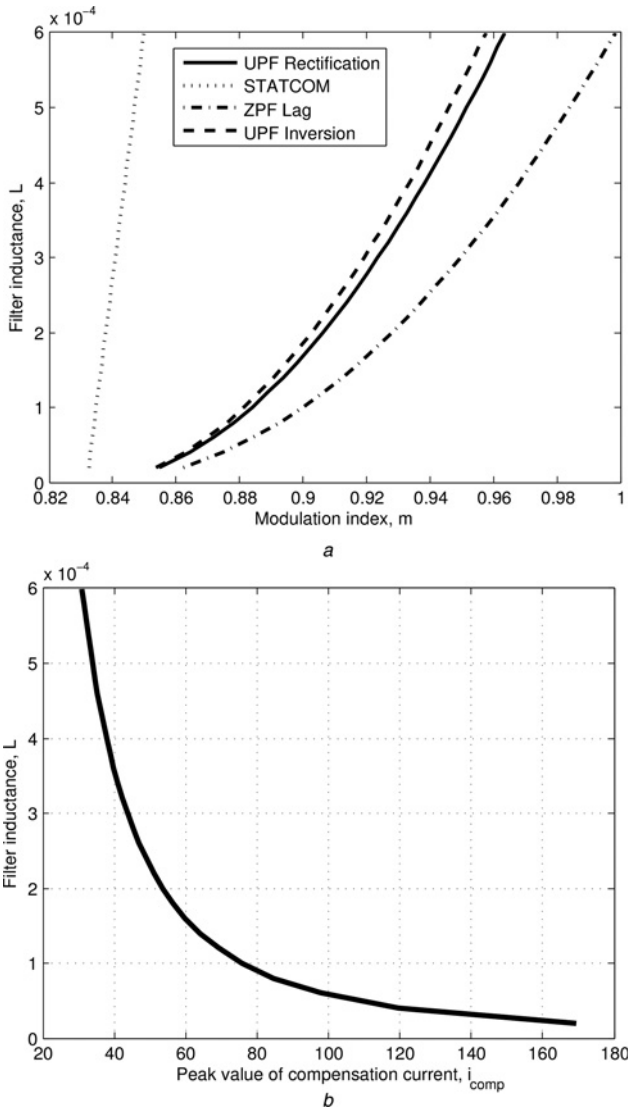

Fig. 4 *Choosing filter inductor, L of the hybrid filter converter based on*
a Modulation index
b Peak filter current

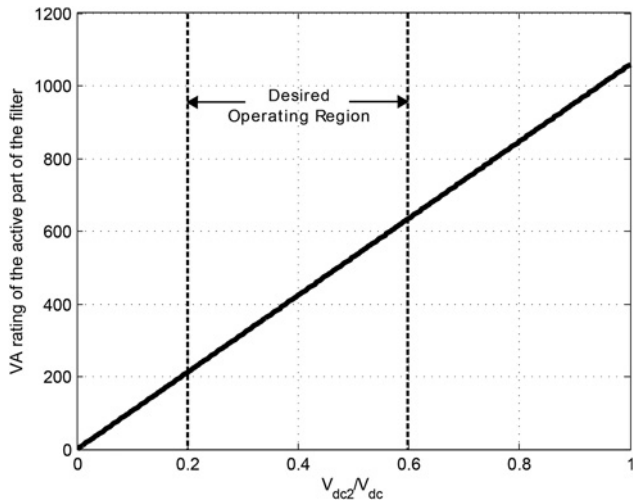

Fig. 5 *Effect of V_{dc2} on converter filter VA rating*

lead); inverter current lags the grid voltage by 90° (ZPF lag); and inverter current is out of phase with grid voltage (UPF inversion).

3 Selection of filter components

There are different constraints to be met while selecting the components for the hybrid filter. The procedure for selecting the different components is presented. The power circuit parameters used are listed in Table 2.

3.1 Selecting filter capacitance, C_1

It has been shown in Section 2.4 that, the 4ω ripple power in the capacitor C_1 should be small. So the capacitor has to be chosen large enough to minimise the ripple voltage in it. It is advisable to choose a capacitance value to limit the peak ripple to be about 5–10% of the dc voltage across C_1.

3.2 Selecting C_{dc2}

C_{dc2} is the dc bus capacitance of the filter converter if we consider the filter converter alone. However, when the whole system with the main converter and hybrid filter converter is considered, the effective dc bus capacitance of the filter converter is $(C_1C_{dc}/C_1 + C_{dc}) + C_{dc2}$. When the grid frequency current flows through the inductor, L a double-frequency ripple will appear at the dc bus of the filter converter. This current should flow through C_1 to the main dc bus and cancel out the ripple there rather than flowing into C_{dc2}. So C_{dc2} should be small compared to $(C_1C_{dc}/C_1) + C_{dc}$.

3.3 Selecting filter inductance, L

The energy to be handled by the inductor, L is decided by the ripple energy in the system. The energy, E_L handled by the inductor, L is given by

$$E_L = \frac{1}{2}Li_L^2 = \frac{V_{dc2}I_s}{\omega V_{dc}}\sqrt{V_s^2 + \omega^2 L_s^2 I_s^2 + 2V_s\omega L_s I_s \sin\phi} \times \cos^2\left(\omega t + \frac{\psi}{2}\right) \quad (20)$$

The sizing of the inductor is independent of L as E_L is decided by the operating conditions of the main converter, and it does not change with L based on (20). However, the inductance value decides the peak current to be handled by the filter converter switches and is given by (15). When the main converter is operating at full load, the modulation indices of legs 2 and 3 should be close to unity. This reflects the filter current, i_L fully back to obtain the dc bus current, i_{r2} as shown in Fig. 3*b*. The maximum modulation index and the peak current is used to decide the value of L. Fig. 4 gives the variation of modulation index and peak filter current with filter inductance under different operating power factor modes (UPF and ZPF) of the converter.

The maximum modulation index sets the upper limit on the value of filter inductance whereas the peak current sets the lower limit. The value of the filter inductance should be chosen such that, the peak current in the inductor is minimum, without over-modulating or crossing the maximum possible modulation index at all operating modes of the converter.

3.4 Choosing V_{dc2}

V_{dc2} is a crucial factor which decides the energy sharing between the inductor, L and the capacitor, C_1. To maximise the benefits of the proposed filter, V_{dc2} should be chosen much lesser than the main dc bus voltage, V_{dc}. There will be a 2ω voltage ripple across C_{dc2} which effectively cancels out the ripple voltage across C_1 so that the voltage across C_{dc} is devoid of any 2ω ripple. The lower limit of V_{dc2} is decided by this 2ω ripple across C_{dc2}. The peak-to-peak ripple voltage should not be more than 20% of V_{dc2}. Fig. 5 shows the effect of V_{dc2} on the VA rating of the filter converter.

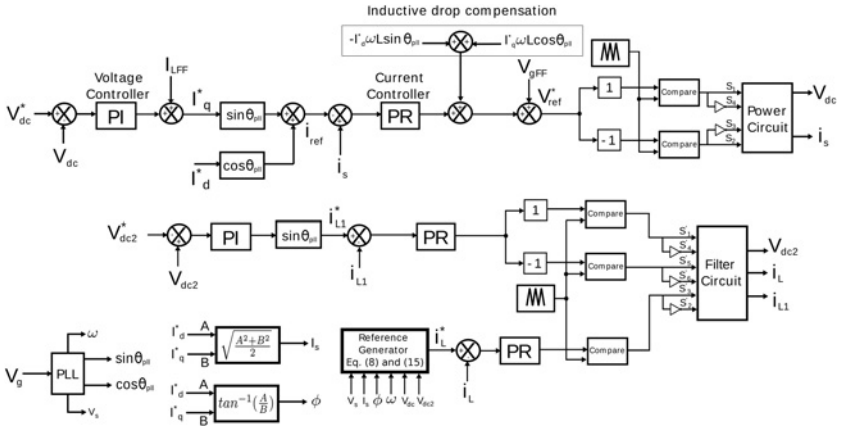

Fig. 6 *Control scheme of the single-phase converter and hybrid dc ripple filter*

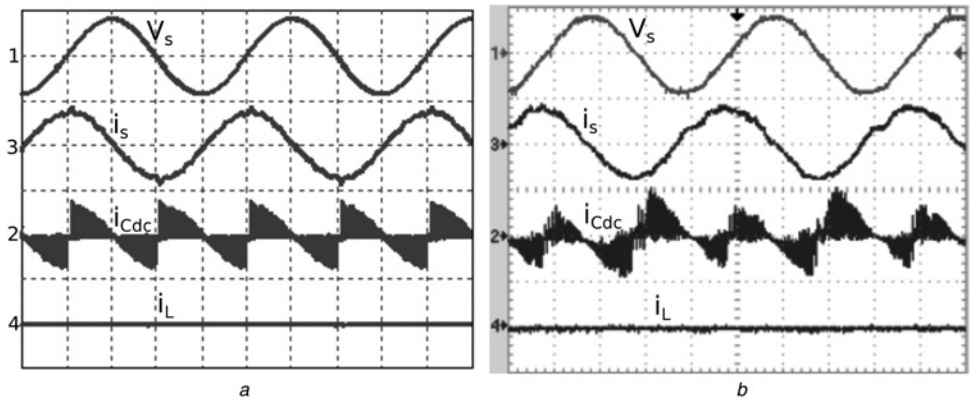

Fig. 7 *STATCOM mode without compensation*

a Simulation results
b Experimental results
V_s – sensed grid voltage (scale: 2 V/div); i_s – inverter side current (scale: 20A/div); i_{Cdc} – main dc bus capacitor current (scale: 20 A/div); i_L – compensation current (scale: 50 A/div)

4 Control scheme

4.1 Main converter

Vector control scheme is used to control the main power converter [29, 30]. The grid voltage phasor is aligned along the q axis. I_q^* and I_d^* refer to the peak value of real and reactive current references, respectively. A phase-locked loop (PLL) is needed as the main converter is grid connected. A second-order generalised integrator-based PLL is implemented [31]. The control scheme consists of an outer-voltage-loop and an inner-current-loop. The outer-voltage-loop maintains the dc bus voltage at the desired level. A proportional–integral (PI) controller is used for the purpose as the voltage reference is the dc. The output of the PI controller is the peak of the active current reference, I_q^*. To improve the dynamic performance of the controller, the dc load current demand is included as a feed-forward term. The actual current reference is obtained by multiplying I_q^* with the in phase unit vector $\sin\theta_{pll}$. Reactive current reference depends upon the amount of compensation needed in a static compensator (STATCOM) application and upon the operating power factor in an active front end converter (AFEC) application. It is obtained by multiplying I_d^* with the unit vector in quadrature with the grid voltage, $\cos\theta_{pll}$. Since the current reference is an ac quantity, a PI controller will introduce the steady-state error.

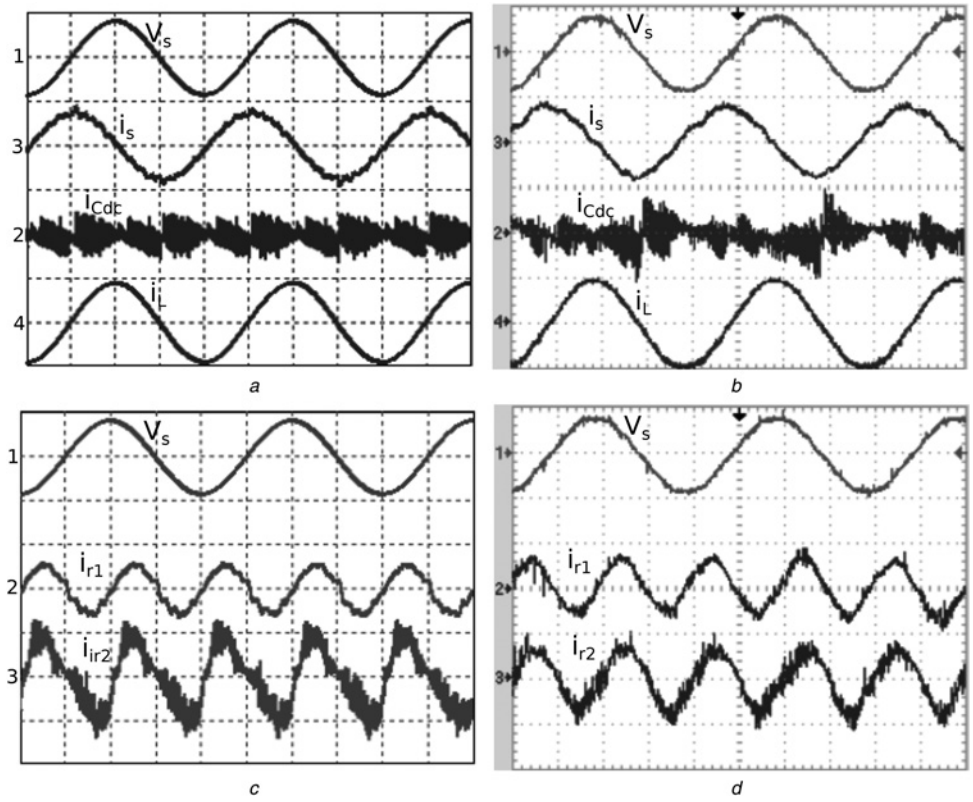

Fig. 8 *STATCOM mode with compensation*

a and *c* Simulation results
b and *d* Experimental results
V_s – sensed grid voltage (scale: 2 V/div); i_s – inverter side current (scale: 20 A/div); i_{Cdc} – main dc bus capacitor current (scale: 20 A/div); i_L – compensation current (scale: 50 A/div); i_{r1} – actual dc bus current ripple (scale: 10 A/div); i_{r2} – injected dc bus current ripple (scale: 10 A/div)

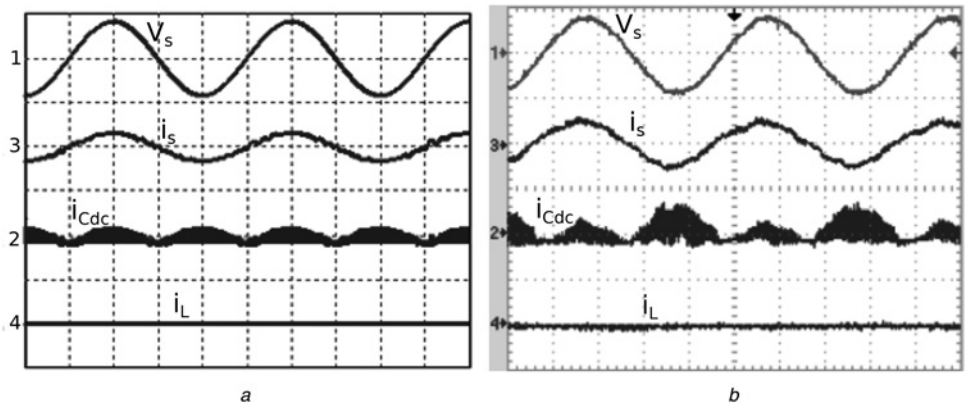

Fig. 9 *UPF rectification mode without compensation*

a Simulation results
b Experimental results
V_s – sensed grid voltage (scale: 2 V/div); i_s – inverter side current (scale: 20 A/div); i_{Cdc} – main dc bus capacitor current (scale: 20 A/div); i_L – compensation current (scale: 50 A/div)

So a proportional–resonant (PR) controller is used for current control [32].

The bandwidth of the outer-voltage-loop is selected such that it is much less than the bandwidth of the current loop. So, while designing the voltage loop, the inner-current-loop can be approximated by a gain without much error.

4.2 Auxiliary converter

The auxiliary converter also operates in grid interactive mode. This is to maintain the voltage across C_{dc2} constant. The converter draws just enough active power to meet its losses from the grid. There is an outer-voltage-loop and an inner-current-loop similar to that of the main converter. In addition to this, one more controller is used to regulate the compensation current through the filter inductor. Since the compensation current is an ac quantity, a PR controller is used here also. The reference generator provides the current reference for instantaneous ripple compensation as shown in Fig. 6.

5 Results

Simulation of a single-phase converter with the proposed dc side filter is carried out to validate the analysis. Laboratory prototype

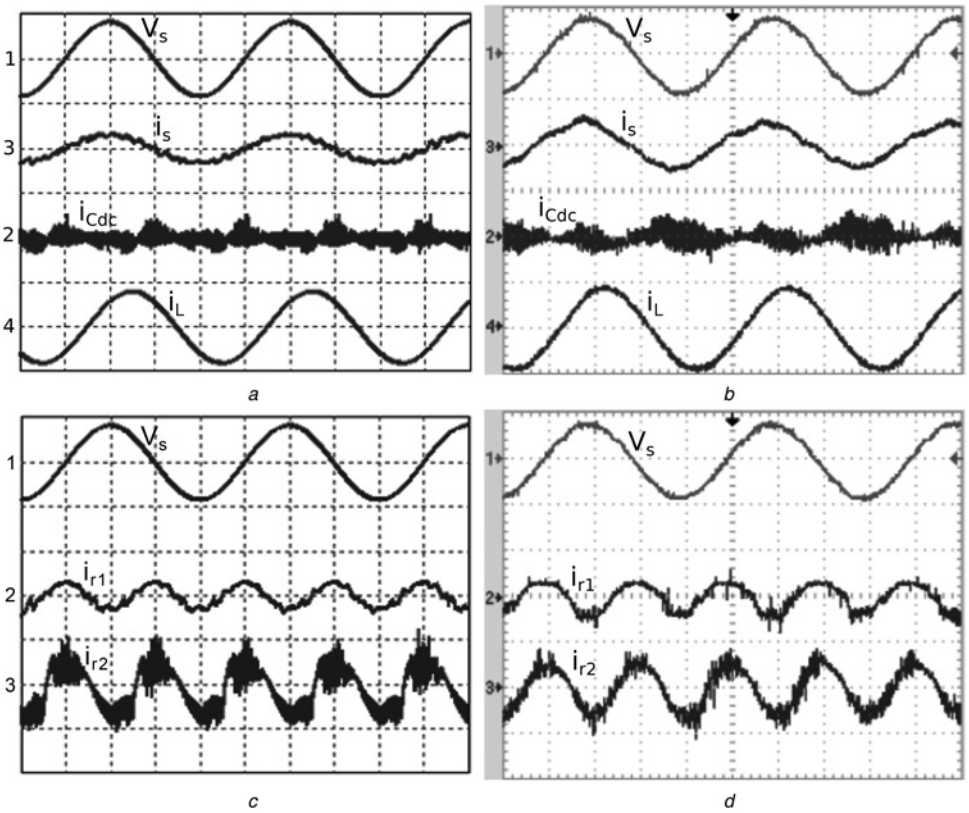

Fig. 10 *UPF rectification mode with compensation*

a and *c* Simulation results
b and *d* Experimental results
V_s – sensed grid voltage (scale: 2 V/div); i_s – inverter side current (scale: 20 A/div); i_{Cdc} – main dc bus capacitor current (scale: 20 A/div); i_L – compensation current (scale: 50 A/div); i_{r1} – actual dc bus current ripple (scale: 10 A/div); i_{r2} – injected dc bus current ripple (scale: 10 A/div)

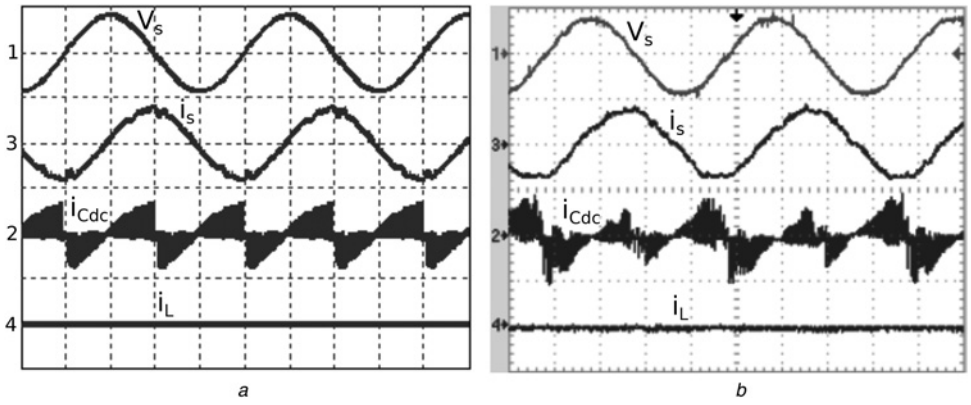

Fig. 11 *ZPF lag mode without compensation*

a Simulation results
b Experimental results
V_s – sensed grid voltage (scale: 2 V/div); i_s – inverter side current (scale: 20 A/div); i_{Cdc} – main dc bus capacitor current (scale: 20 A/div); i_L – compensation current (scale: 50 A/div)

hardware with the circuit parameters in Table 2 is also built. Tests are carried out under a variety of operating conditions corresponding to Table 1. Results for UPF rectification and ZPF operation (both lead and lag) are given below.

5.1 ZPF lead operation (STATCOM mode)

The main converter is run in STATCOM mode. The simulation and experimental results without and with compensation are shown in Figs. 7*a,b* and 8*a,b*, respectively. From Fig. 7, it can be seen that the inverter current leads the grid voltage by 90°. The 100 Hz ripple reduction is visible in the dc bus capacitor current waveform in Fig. 8*b*. It can also be seen that the main inverter current is unaffected by the operation of the hybrid filter. Figs. 8*c* and *d* show the actual 100 Hz component in the main dc bus, i_{r1} and the 100 Hz component injected into the auxiliary dc bus, i_{r2} when compensation is enabled. The peak value of the 100 Hz ripple current in the main dc bus capacitor, C_{dc} is reduced from 6 to 0.53 A.

5.2 UPF rectifier operation

The simulation and experimental results for UPF rectification mode without and with compensation are shown in Figs. 9*a, b* and 10*a, b*, respectively. From Fig. 9, it can be seen that the inverter current is in

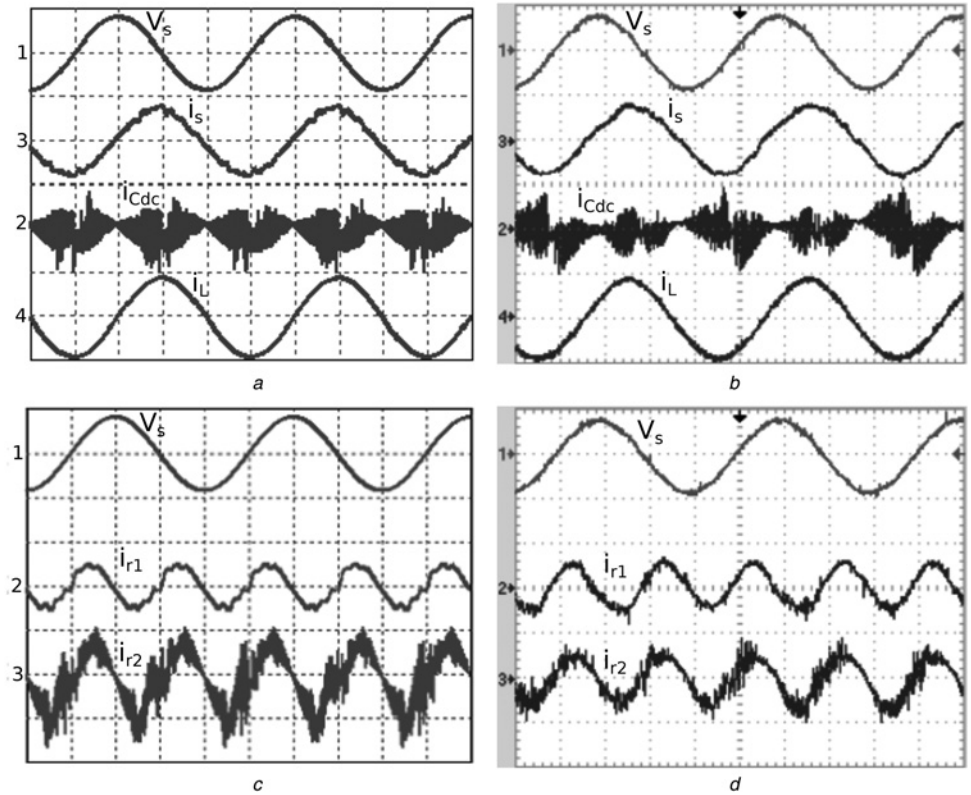

Fig. 12 *ZPF lag mode with compensation*

a and *c* Simulation results
b and *d* Experimental results
V_s – sensed grid voltage (scale: 2 V/div); i_s – inverter side current (scale: 20 A/div); i_{Cdc} – main dc bus capacitor current (scale: 20 A/div); i_L – compensation current (scale: 50 A/div); i_{r1} – actual dc bus current ripple (scale: 10 A/div); i_{r2} – injected dc bus current ripple (scale: 10 A/div)

Table 3 Peak value of the dc bus ripple current

		ZPF lead, A	ZPF Lag, A	UPF Rectification, A
experimental	no compensation	6	4.29	3.72
result	with compensation	0.53	0.51	0.97
simulation	no compensation	5.53	5.11	3.83
result	with compensation	0.48	0.52	0.89
theoretical	no compensation	5.60	5.60	3.75
result	with compensation	0	0	0

Table 4 Comparison of the proposed filter with inductor-based active filter for a 1 KVA system

Parameter	Proposed hybrid filter	Purely inductive filter, active	Tuned LC trap filter
C_{dc}	33 mF	10 mF	10 mF
C_{fil}	33 mF	nil	500 mF
L_{fil}	270 μH	270 μH	5 μH
$I_L(pk)$	$\sqrt{\frac{V_{dc2}}{V_{dc}}} \times 150$ A	150 A	47 A
VA rating of active switches	$(V_{dc2}/V_{dc}) \times 1000$ VA	1000 VA	nil
VA rating of filter inductor	$(V_{dc2}/V_{dc}) \times 1000$ VA	1000 VA	4 VA
VA rating of filter capacitor	$\frac{V_{dc} - V_{dc2}}{V_{dc}} \times 1000$ VA	nil	1000 VA
Efficiency	high	low	high
Frequency track	yes	yes	no
Control complexity	high	low	nil
Cost	medium	high	low

phase with the grid voltage. The 100 Hz ripple reduction is visible in the dc bus capacitor current waveform in Fig. 10*b*. Figs. 10*c* and *d* show the actual 100 Hz component in the main dc bus, i_{r1} and the 100 Hz component injected into the auxiliary dc bus, i_{r2} when compensation is enabled. The peak value of the 100 Hz ripple current in the main dc bus capacitor, C_{dc} is reduced from 3.72 to 0.97 A.

5.3 ZPF lag operation

The simulation and experimental results for ZPF lag mode without and with compensation are shown in Figs. 11*a*,*b* and 12*a*,*b*, respectively. From Fig. 11, it can be seen that the inverter current lags the grid voltage by 90°. Figs. 12*c* and *d* show the actual 100 Hz component in the main dc bus, i_{r1} and the 100 Hz component injected into the auxiliary dc bus, i_{r2} when compensation is enabled. The peak value of the 100 Hz ripple current in the main dc bus capacitor, C_{dc} is reduced from 4.29 to 0.51 A.

5.4 Summary of results

Table 3 gives a comparison between the experimental results, simulation results and theoretical results for cases corresponding to UPF rectification, ZPF lag and STATCOM (ZPF lead), respectively. The 100 Hz current ripple is clearly getting reduced as expected. In theoretical case, the small amount of active current drawn by both converters to meet their losses is not considered.

5.5 Comparison of filter topologies

Table 4 gives a comparison between the proposed hybrid filter and the inductor-based active filter in Fig. 1*c* for a 1 kVA system with 30 V dc bus. The dc bus capacitance is chosen such that only 3% of the ripple current flows into the battery. The battery impedance at 100 Hz is assumed to be 10 mΩ. For a purely capacitor filter, the dc bus capacitance value needed to achieve the filtering requirement is 5 F whereas in the proposed topology, it is reduced to 33 mF. The tuned LC trap filter is not capable of tracking the grid frequency. Also, the value of filter capacitance needs to be large for it to have a wide bandwidth around the 100 Hz frequency. The compensation current to be injected in the proposed hybrid filter is less than that of an inductor-based active filter for the same value of the filter inductance. The VA ratings of the active components are also less in the proposed method.

6 Conclusions

A novel hybrid filter topology is proposed to absorb the dc bus ripple current in a single-phase PWM converter. The ripple power and the dc bus current ripple are quantified under various operating power factor modes of the converter. The control of the hybrid filter converter is formulated using single-phase instantaneous power analysis. This provides closed form analytical solutions for the operation of the hybrid filter converter at arbitrary power factor angles of the main converter. It is also shown that the control of the hybrid filter converter can be performed without sensing the dc bus ripple current.

A design method is presented to choose the ratings of the filter components. The proposed circuit has design flexibility to reduce the cost and the size of the filter without compromising the overall system efficiency. The topology is found to be quite effective in compensating the dc bus ripple current. The prototype power converter built in the laboratory is operated in various power factor modes and in all cases, good filtering performance is observed.

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