
Design Document
for
AC Circuit Solver

Prepared by Rahul Nirania and
Abhishek Yadav

Under Guidance of Prof Huzur
Saran

March 19, 2018

Contents

| | | |
|----------|--------------------------------------|-----------|
| 1 | Introduction | 3 |
| 1.1 | Abstract | 3 |
| 1.2 | Operating Environment | 3 |
| 1.3 | Technical Skills Used | 3 |
| 2 | Overall Description | 4 |
| 2.1 | Software Perspective | 4 |
| 2.2 | Software Functions | 4 |
| 2.3 | Unfolding Abstraction | 4 |
| 3 | Parsing | 5 |
| 3.1 | Method | 5 |
| 3.2 | Failures | 5 |
| 4 | Circuit Rendering | 6 |
| 4.1 | SVG Format | 6 |
| 4.2 | Characteristics of Circuit | 6 |
| 4.3 | Clickable Circuit | 7 |
| 5 | AC Circuit Drawing | 8 |
| 6 | AC Circuit Analysis | 9 |
| 7 | Output | 10 |
| 7.1 | Result.txt | 10 |
| 8 | References | 11 |
| 8.1 | Reference document | 11 |

1 Introduction

1.1 Abstract

Given the netlist we will be displaying an AC circuit(containing active and passive elements) in SVG format.Further we will be doing AC circuit analysis and will be showing min and max value of current and voltage across all passive elements in result.txt file.

1.2 Operating Environment

- (1)Gcc compiler
- (2)Modern Web Browser

1.3 Technical Skills Used

- (1)C++
- (2)Svg image rendering
- (3)Ac circuit Analysis
- (4)Javascript and CSS

2 Overall Description

2.1 Software Perspective

This software is developed from educational purposes. This will help electrical enthusiasts to simulate their circuit.

2.2 Software Functions

This software will simulate electrical circuit containing passive elements. Circuit can be huge enough containing thousands of passive and active elements. To have a closer look at every node we will provide a zoom option in browser. Also, a clickable option will be provided to know details across any passive element.

2.3 Unfolding Abstraction

Exploiting the design principle "**Simple follow regularity**" we had divided our project into 5 stages of development. In each stage we will be listing our *strategy and failure* we may face. Each stage is dependent on its previous stage.

3 Parsing

3.1 Method

We had our hands on flex and bison. But unfortunately we were not able to start with bison and finally we had done parsing by reading line by line from top.cir. We had hard coded almost all cases. By parsing we had generated lexeme and had stored in vector array. Now depending on lexeme we will be calling draw function.

3.2 Failures

Since we had tried to formulate all error but there can be possibility that we can fail to detect error in top.cir. This inefficient method we had chosen due to time constraint.

4 Circuit Rendering

4.1 SVG Format

Scalable Vector Graphics (SVG) is an XML-based vector image format for two-dimensional graphics. We had drawn all active and passive components by ourself taking help of references provided below. All modern browser support svg rendering. The advantage of svg over png/jpg is that the image do not get distort also after zooming them. Svg image for all the component to be used in drawing circuit are shown below:

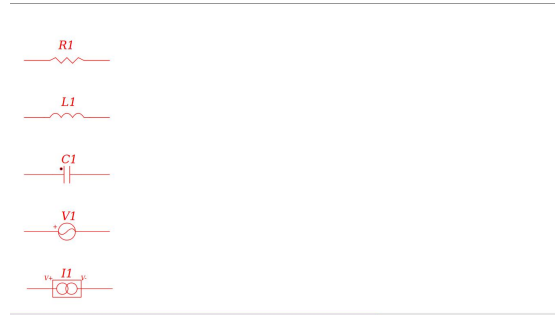


Figure 4.1: Svg .

Figure 4.1 shows a svg image.

4.2 Characteristics of Circuit

- (1) We will try to make circuit scalable in terms of nodes and will try that circuit can be represent in compact form.
- (2) Since number of nodes as can go as high as 1000 so we will make image zoomable.
- (3) Circuit rendered on browser will be also clickable so that by clicking on any passive element pop-up box will be displayed containing values of steady state current and voltage across that particular element.
- (4) We will flag error in case we find any node with degree one.

4.3 Clickable Circuit

There can be many nodes possible in any circuit. So for user convenience if s/he wants to check properties of any element while looking at svg image we are making a feature(as per assignment requirement) in which if user click on any of the component a popup will appear in which all the details will be written. We will be making popup window using javascript and css.**

5 AC Circuit Drawing

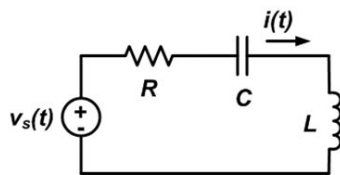
The circuit is drawn from the following algorithm. First of all we separate all the elements into two parts i.e. (R,L,C) and (V,I) in two vectors of vector of a struct consist of the component name, the two nets from which it is connected, its magnitude. Each vector of vectors will consist of all component connected with net i, where i is some integer. So with these setup we will construct any voltage or current source. Then we will name its ends according to its nets value. Then we put these two values of nets in an array. Then we will choose any one number from the array and also remove it from array. While checking that if other end is present in the array we start drawing them. If the other end is present in the array we will try to connect this element between these two nets. But if the other end is not present in the array we will construct it to other direction and name the other end as that particular net and put this value of net to the array. We will do this recursively until all the elements are drawn. If any two ends of same net value remained unconnected then we will join them.

6 AC Circuit Analysis

There can be various combination of R,L,C and we will be dividing circuit in parallel or series and applying corresponding formulae. We will be using formulae for parallel and series circuit from "AC circuit analysis notes".

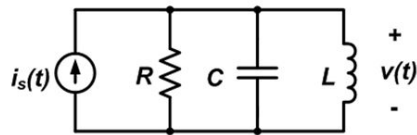
Summary: Series & parallel RLC circuits

- **Series RLC circuit:**



$$\frac{dv_s(t)}{dt} = L \frac{d^2 i(t)}{dt^2} + R \frac{di(t)}{dt} + \frac{1}{C} i(t)$$

- **Parallel RLC circuit**



$$\frac{di_s(t)}{dt} = C \frac{d^2 v(t)}{dt^2} + \frac{1}{R} \frac{dv(t)}{dt} + \frac{1}{L} v(t)$$

Figure 6.1: RLC .

Figure [6.1](#) shows a RLC circuit.

7 Output

7.1 Result.txt

- (1) We will display current and voltage across passive elements according to order provided in top.cir.
- (2) Magnitude and phase values will be displayed upto 3 decimal places only.
- (3) The convention is current flows from `¡Net_Connected_to_terminal¡` to `<Net_Connected_to_other_terminal>` (for example, if the given order of connection is N1 to N2) then we will be reporting our findings in that direction only.
- (4) Maximum and minimum values be reported across every passive element.

8 References

8.1 Reference document

- (1) For circuit analysis we will be taking help from <http://web.mit.edu/8.02t/www/802TEAL3D/visualizations/coursenotes/modules/guide12.pdf>
- (2) For SVG code https://www.w3schools.com/graphics/svg_examples.asp.

** We are writing this much only because we haven't applied it or studied it yet.