ELECTRONIC SYSTEM DESIGN
SIMULATION REPORT (FRONT END DESIGN)
ELEN90053

Demonstrator: Matthew Adams

Student: William Ngeow, 596301

Date: **4 September 2015**
Page Count: **10 (Not including cover page)**

Student Name: William Ngeow Kit Mun Student Number: 596301

1. INTRODUCTION

This report consists of the design of the front end of the Digital Storage Oscilloscope (DSO) and the results of the simulation executed in LT Spice. The simulation results are expanded in the following sections, in particular, the frequency and phase response of the ADC input, the input impedance of the circuit, the tabulated DC bias (operating points), observations reflecting the meeting of core specification criteria, discussion of issues and variations in the design.

2. FRONT-END CIRCUIT DESIGN

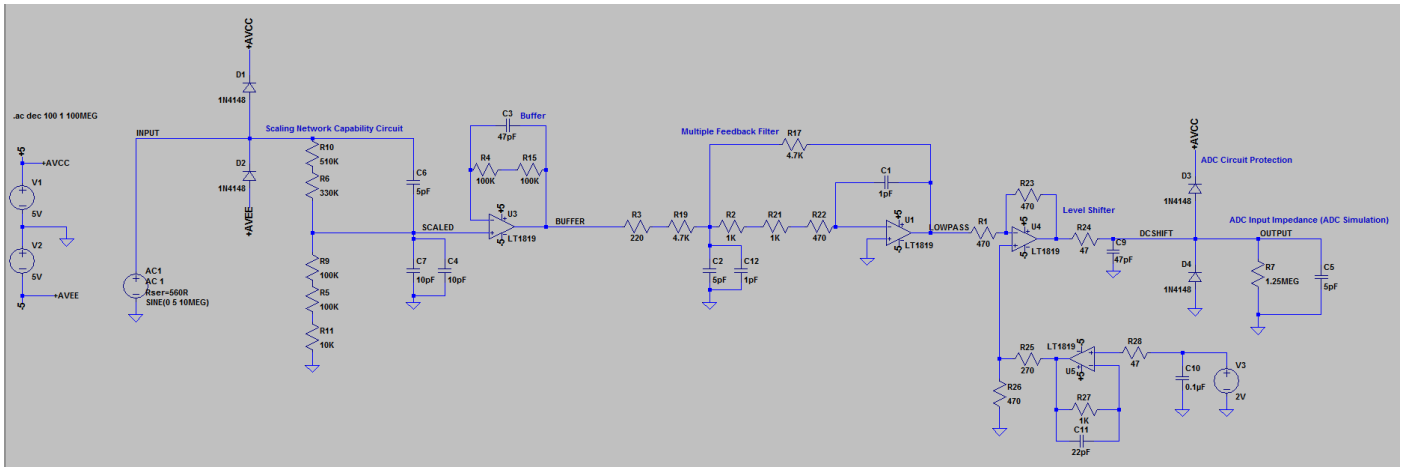

Figure 1: Front End Circuit in LT Spice

The front end circuit of the DSO is comprised of the following:

The DSO is to take an analog signal as an input, scale the input and feed it to an Analog-to-Digital Converter[1]. The front end circuit is designed to fulfill this performance specification.

The input passes through a scaling network circuit to scale down the amplitude for processing through the op amps in the circuit. A unity buffer then decouples the scaled input with the anti-aliasing filter due to differing input and output impedance requirements.

The anti-aliasing filter then removes frequencies above 20 MHz (since it is sampling at a rate of 40MSPS). Sampling must occur at a frequency higher than twice the highest frequency and since it is sampled at 40MSPS, the maximum frequency at which there will be reliably no aliasing is 20 MHz. This is achieved by an anti-aliasing filter with a cutoff frequency of 20 MHz.

After filtering, the filtered signal passes through a level shifter. The level shifter is needed since the ADC used (ADS830) requires the input to be in the range between 1.5V and 3.5V[2]. Hence, the DC shift should be 2V which is accomplished using a DC level shifter specified in the ADC datasheet[2]. The ADS830 datasheet also provides a design for the DC coupled level-shifter[2] which was used as a template for this section of the circuit. This DC coupled level-shifter is preferred as it uses an internal voltage reference in the ADC rather than an external voltage rail, thereby reducing the noise in the voltage used as the reference for the op amp.

[1] ELEN90053 Project Brief 2015 Rev.03, Matthew Adams
[2] http://www.ti.com/lit/ds/symlink/ads830.pdf

The shifted signal then passes through the ADC Protection Circuit which limits the current which can pass through, and is consequently fed into the ADC input.

3. FREQUENCY AND PHASE RESPONSE GRAPH FROM 0Hz TO 50MHz

Measured at the ADC Input (Simulation Output)

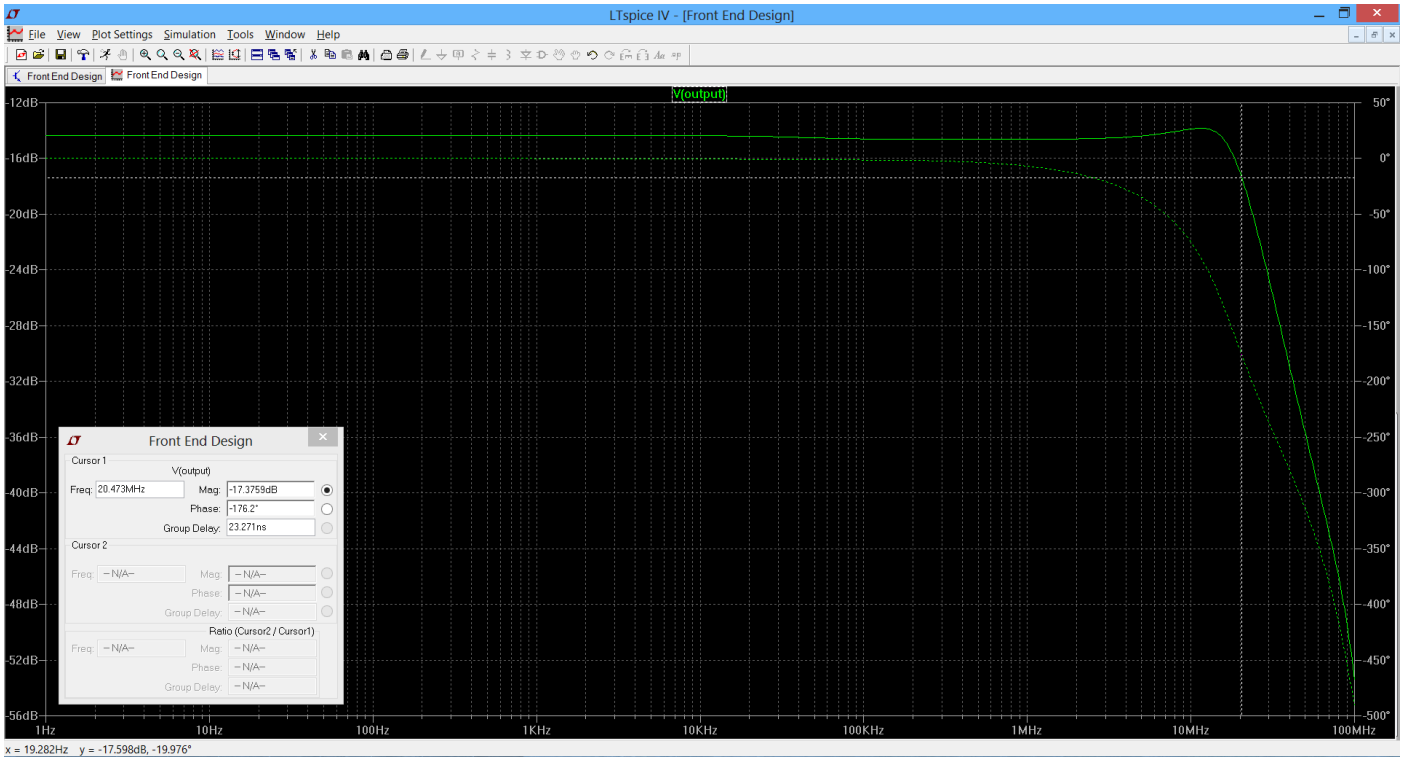

Figure 2: Frequency and phase response graph for ADC input from 0 Hz to 50 MHz

$$f_{cutoff} = 20.473\ MHz$$

3.1 Magnitude Response

The DC magnitude is -14.3759 dB and hence, the -3dB magnitude is -17.3759 dB.
Using the cursor, the cutoff frequency (when the magnitude drops by 3dB) is determined to be $f_{cutoff} = 20.473\ MHz$

That is, the amplitude of the signal drops to half or less of its original magnitude after 20.473 MHz.

3.2 Phase Response

The phase response is linear up to 1 MHz. There is no performance specification given for the phase response and since it is fairly linear throughout, the current phase response is sufficient is for our purposes. Any changes in phase can be rectified in the software.

3.3 Cutoff Frequency

In terms of the cutoff frequency, it fulfills Functional Specification 1.0.7[1] as $f_{cutoff} = 20.473\ MHz$. This is slightly above the designated cutoff frequency to allow for the high frequency signals to pass through without excessive attenuation. However, if any signal beyond 20 MHz is passed through the circuit, it will not function as per specifications and the signal will be attenuated.

It is also worth noting the slight rise in the magnitude response before the cutoff frequency. This feature in the frequency response is designed to compensate for any losses in high frequency signals as it approaches the cutoff frequency.

3.4 Ripple in Passband

The ripple in the passband does not exceed the maximum of $\pm 2\ dB$. This fulfills Functional Specification 1.0.7[1].

3.5 Filter Order

The 2nd order filter already fulfilled the specification, which is a minimum of a first order 20 dB per decade response as mentioned in Functional Specification 1.0.7[1]. The roll off in this case is more than 40 dB per decade.

4. INPUT IMPEDANCE GRAPH FROM 0Hz TO 50MHz

Measured at the BNC (Simulation Input)

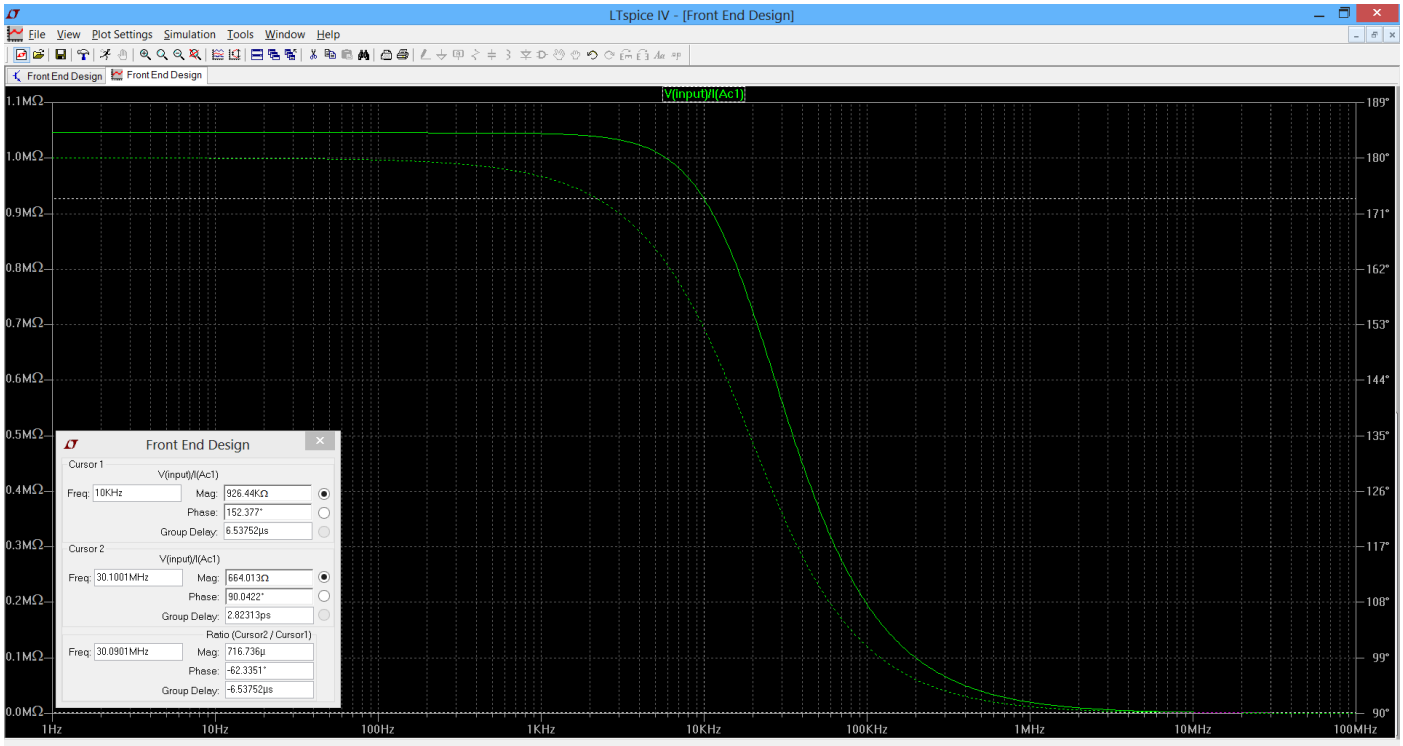

Figure 3: Input impedance graph of BNC input from 0 Hz to 50 MHz

$$Z_{10kHz} = 926440\Omega$$

The input impedance graph is obtained by utilising the fact that V=IZ. The input impedance can then be simply calculated and plotted by dividing the input voltage by the input current.

4.1 Input Impedance

The input impedance from DC to 10 kHz is between $0.92644\ M\Omega$ and $1.04565\ M\Omega$.
This fulfills Functional Specification 1.0.2[1] that the input impedance from DC to 10 kHz must be within $\pm 10\%\ of\ 1M\Omega$.

In the range of 10 kHz to 30 MHz, the input impedance is greater than 664.013 Ω. This fulfills Functional Specification 1.0.3[1] that the input impedance from 10 kHz to 30 MHz must be greater than 100 Ω.

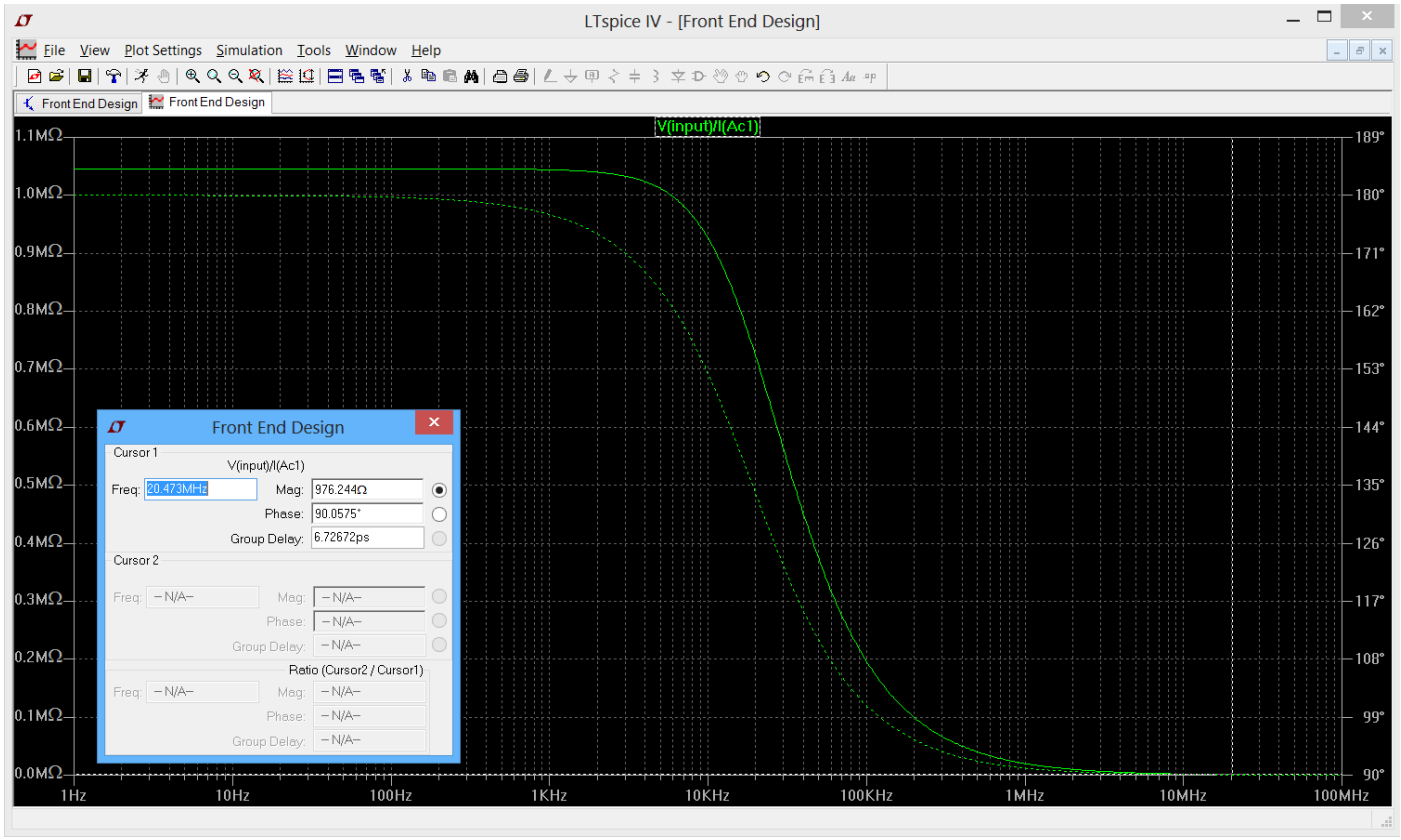

Figure 4: Input impedance graph of BNC input from 0 Hz to 50 MHz (at cutoff frequency)

4.2 Input Capacitance

The following formula is used to determine the input capacitance:

$$f_c = \frac{1}{2\pi RC}$$

We know that $f_c = f_{cutoff} = 20.473\ MHz$.

The impedance of the circuit at 20.473 MHz is given as 976.244 Ω as shown in the circuit above.
Therefore,

$$(20473000) = \frac{1}{2\pi(976.244)C}$$

$$C = 7.963\ pF$$

This fulfills the requirement that the input capacitance must be less than 60 pF in Functional Specification 1.0.4[1].

Student Name: William Ngeow Kit Mun Student Number: 596301

5. DC BIAS (OPERATING POINT) SIMULATION RESULTS

The voltage was measured at various points throughout the front end with reference to schematic extract below.

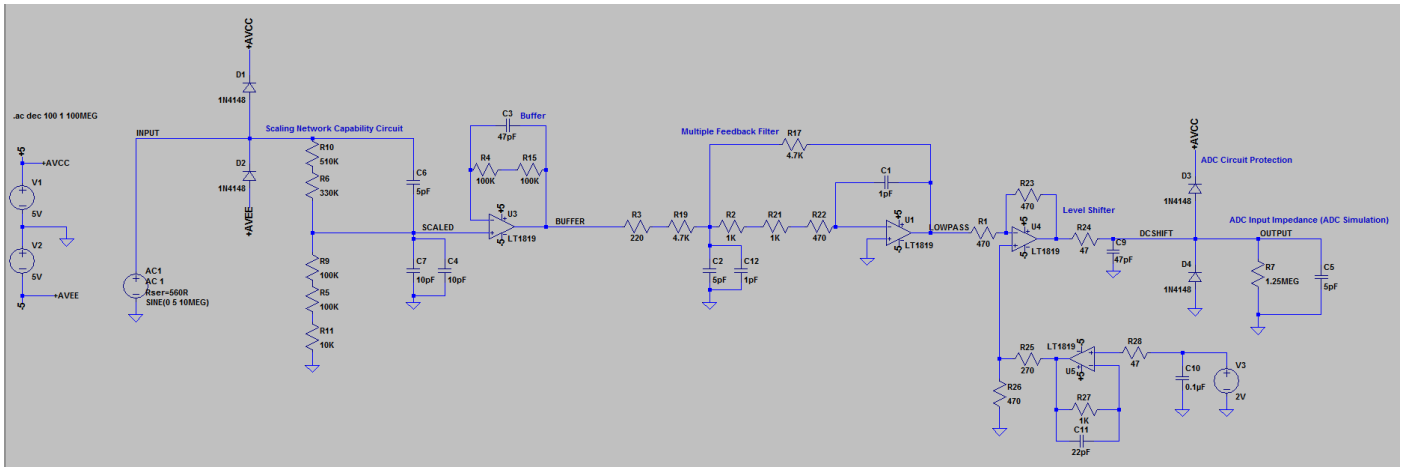

Figure 5: Front end circuit in LT Spice

Net labels are used to identify the points of interest on the circuit. The DC bias and operating points can be determined using the graph below.

Net Label	DC Bias (Operating Point)				Comment
	0 Hz	5 MHz	10 MHz	20 MHz	
V_{INPUT}	0V	0V	0V	0V	Operating point should be at 0V as expected.
V_{SCALED}	0.33V	0.33V	0.33V	0.33V	The residual effect of the scaling network is to increase the DC bias due to the effect of the resistor and capacitance. The capacitors act as small reservoir of energy, which shifts the DC bias up.
V_{BUFFER}	-0.06V	-0.06V	-0.06V	-0.06V	The buffer have resistance and capacitance in the (negative) feedback loop which contributes the shift in the DC bias, similar to above. It acts as a highpass filter, reducing the effect of the DC bias.
$V_{LOWPASS}$	0.04V	0.04V	0.04V	0.04V	The lowpass filter's feedback should result in no DC bias but due to deviation from ideal values, there is a slight upward shift in the operating voltage point. This can be attributed to the 220Ω in front of the filter. However, the DC bias is close enough to 0V as desired.
V_{OUTPUT}	2.49V	2.49V	2.49V	2.49V	The DC bias is as expected due to the effect of the level shifter, causing the output to oscillate within the 1.5V-3.5V range.

Table 1: DC Bias (Operating Point) of different points on the front end circuit in LT Spice

It is worth noting that the DC bias or operating point is independent of the frequency 0 Hz to 20 MHz. This is because the capacitances are small enough to negate the effect of frequency. However, at much higher frequencies before the anti-aliasing filter, the DC bias might be affected.

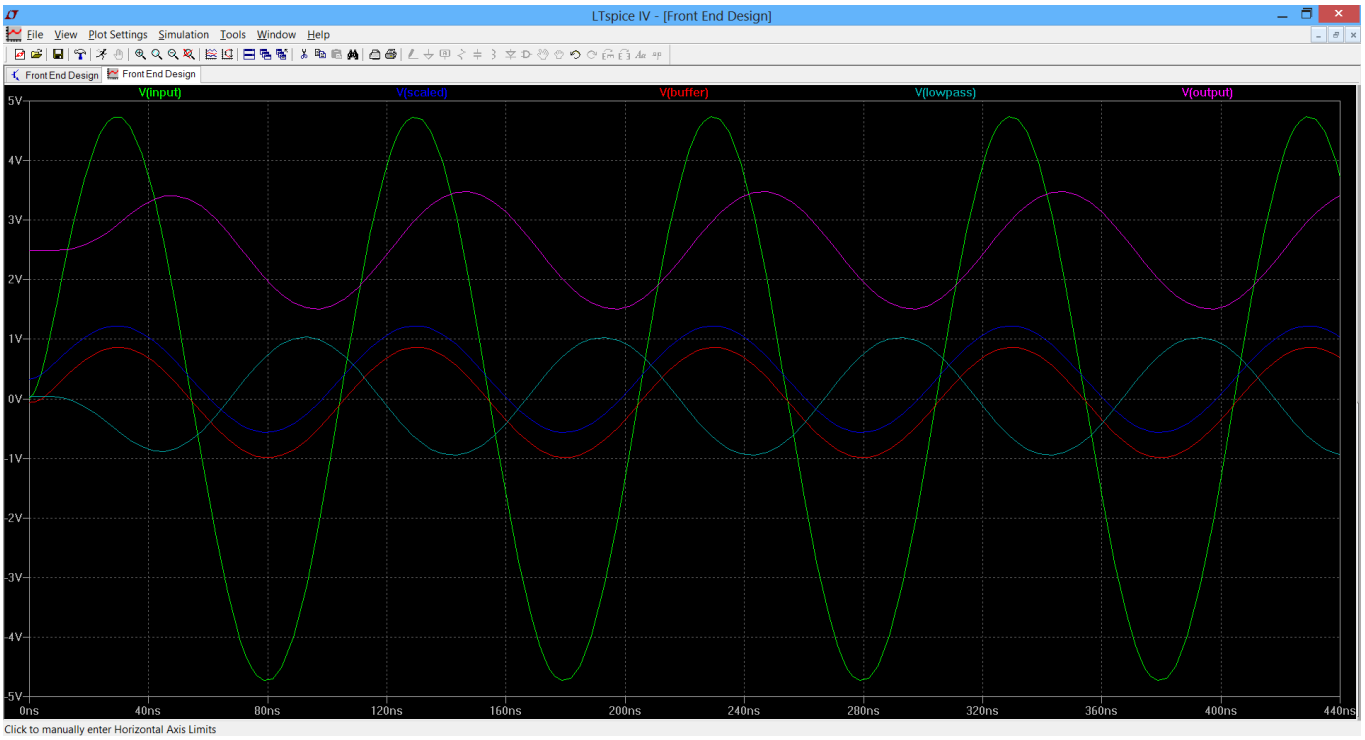

Figure 6: Time domain voltage response of various points of interest on the front end circuit in LT Spice

6. OBSERVATION OF RESULTS (CORE SPECIFICATION CRITERIA, ISSUES, AND VARIATION)

6.1 Core Specification Criteria

The meeting of core specification criteria has been discussed within the section of the simulation results above, in particular, Functional Specification 1.0.2, 1.0.3, 1.0.4, 1.0.6, 1.0.7[1].

For Functional Specification 1.0, there is only one analog input.

For Functional Specification 1.0.1, the BNC will be connected to the input of the scaling network.

For Functional Specification 1.0.5, the two 1N4148 diodes which are connected to AVCC and AVEE fulfills the criteria that the BNC input can accept a maximum of $\pm 5.6V$ after which clamping of the voltage input occurs. In this circuit, the diodes were connected to the $\pm 5V$ voltage rails which clamps it before the maximum voltage, ensuring that the criteria is satisfied.

For Functional Specification 1.0.8, all passive components are selected from the Passive Components List[3].

6.2 Issues

In terms of the anti-aliasing filter design, there is much to be discussed about the chosen design and warrants another whole report of its own. The design of the filter utilises formulas given in Workshop 3 and multiple iterations to reach an optimal design. The reference program given, TI Filter Pro was also used to produce similar potential filter designs. LT Spice was used to verify the performance of the chosen filter design and to confirm that it fulfils all desired specifications. However, the thought that has gone into the design has been distilled into the following points.

[3] Project Passive Components 2015, Matthew Adams

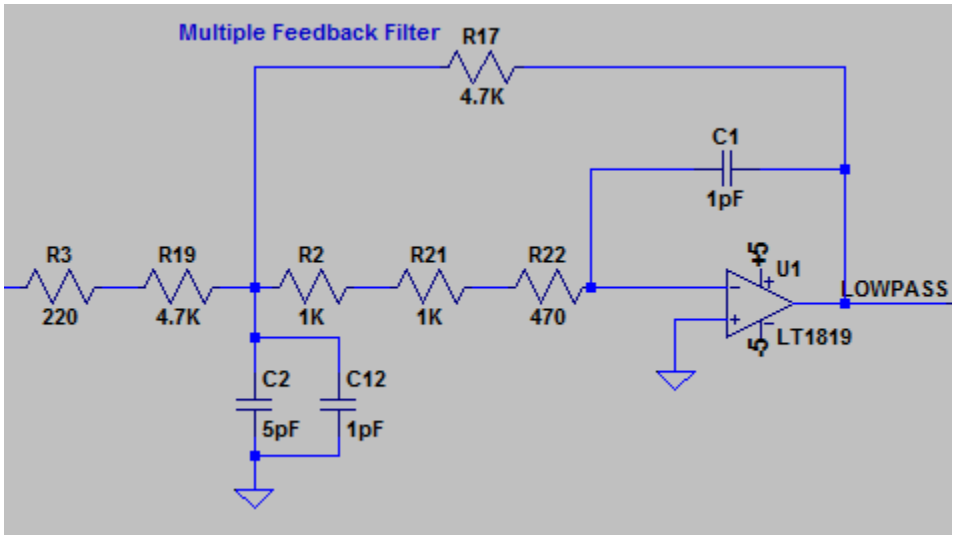

Figure 7: Anti-Aliasing Filter Design

For the filter order, the 2nd order filter was chosen against the 4th order filter because of the simplicity and number of components involved. The 2nd order filter already fulfilled the specification that requires the 20dB per decade response and the 4th order filter's advantage is the sharper roll off response after the cutoff frequency. However, it was difficult to design and required twice the number of parts compared to the 2nd order filter. Hence, the 2nd order filter was chosen.

For the filter topology, the Butterworth filter was chosen against the Chebyshev or Bessel filter because it provides the smoothest and flattest passband. This is because precise signal levels are required across a wide range of frequencies in the entire pass band. The monotonic characteristic of the Butterworth filter makes it ideal for an anti-aliasing filter.

For the filter implementation, the multiple feedback filter (MFB) was chosen against the Sallen Key filter. Although the Sallen Key filter requires one less component to build, the MFB was easier to design using the formulas given in Workshop 3[4] (there was no need to calculate an intermediate variable, m for the MFB as opposed to the Sallen Key).

The formulas, yielded a magnitude and frequency response which does not fulfill the expected criteria. The reason behind this occurence is because the op amp used (LT1819) deviates from ideality. Using the calculated resistances and capacitances, the values were individually modified to fit the desired specifications. For example, the first resistor on the left shifts the magnitude response vertically and the rise before the cutoff frequency. In another instance, capacitor in the feedback loop controls the cutoff frequency. Through many iterations, the above circuit is obtained, which fulfills all the functional specifications given.

Since the op amp is not ideal, it does not operate at the high speed as given in the datasheet of the LT1819. To compensate for this, a capacitor and resistor is added in parallel to decrease the slew rate and improve the phase margin. The resistor and capacitor must match the impedances in the scaling network which helps to improve the stability of the buffer.

Since the Functional Specification requires all passive components used to be from the Project Passive Components List 2015[3], most of the values of resistors and capacitors deviated slightly from their calculated figures. For values that were far from the standard passive component values, the parts were either cascaded in series or parallel to achieve the closest possible value to the designed resistance or capacitance.

[4] ELEN90053 Digital Systems Design – Workshop 3, Op-Amp Based Circuit Simulation with LTSpice, Department of Electrical & Electronic Engineering, The University of Melbourne 2015

6.3 Variation

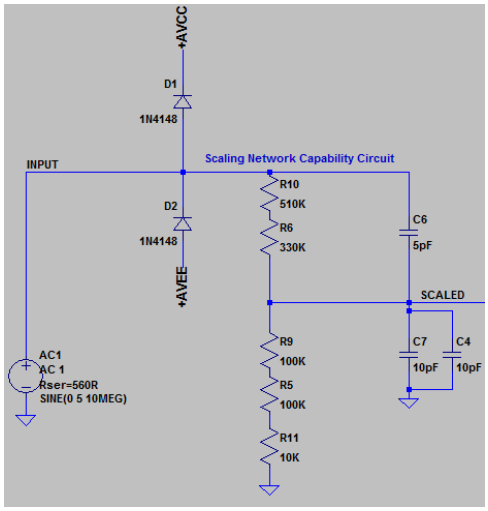

Figure 8: Scaling Network Circuit

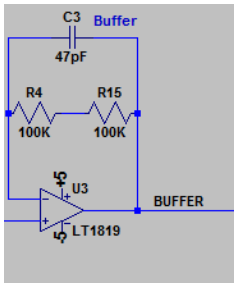

Figure 9: Buffer Circuit

As seen above, the clamping circuit (two 1N4148 diodes connected to AVCC and AVEE) are located before the scaling network circuit. Since the clamp limits are fixed in this case, there is no need to place it before the scaling network. However, in the event that a higher limit is desired, the clamping circuit should be repositioned after the scaling network circuit. This allows the scaled down input to pass through the clamping circuit, instead of the actual magnitude signal, thereby allowing lower values of AVCC and AVEE. However, this is not the case for this project and therefore, the position of the clamping circuit is of little significance.

The feedback loop of the buffer is replaced with a resistor and capacitor in parallel. This is because the unity buffer is highly unstable without any impedance in the feedback loop and to compensate for this, the resistor and capacitor are added. The addition helps to slow down the op amp and restore phase margin in view of the fact that the op amp is not unity gain stable.

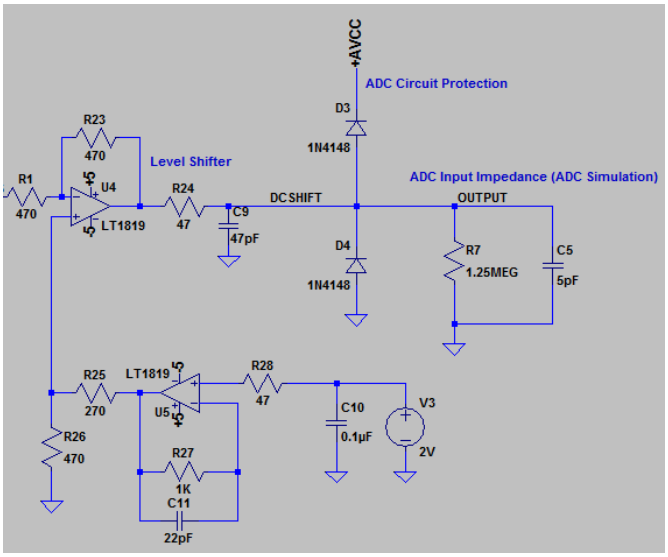

Figure 10: Level Shifter Circuit and ADC Circuit Protection

In the lower op amp of the level shifter, a 22pF capacitor is added in the feedback loop to decrease the slew rate of the op amp since the op amp does not operate as fast as indicated on the datasheet. This also reduces the oscillation and noise due to the resistor in the feedback loop.

7. FREQUENCY AND PHASE RESPONSES (BNC Input, Prior to Filter Stage, ADC Input)

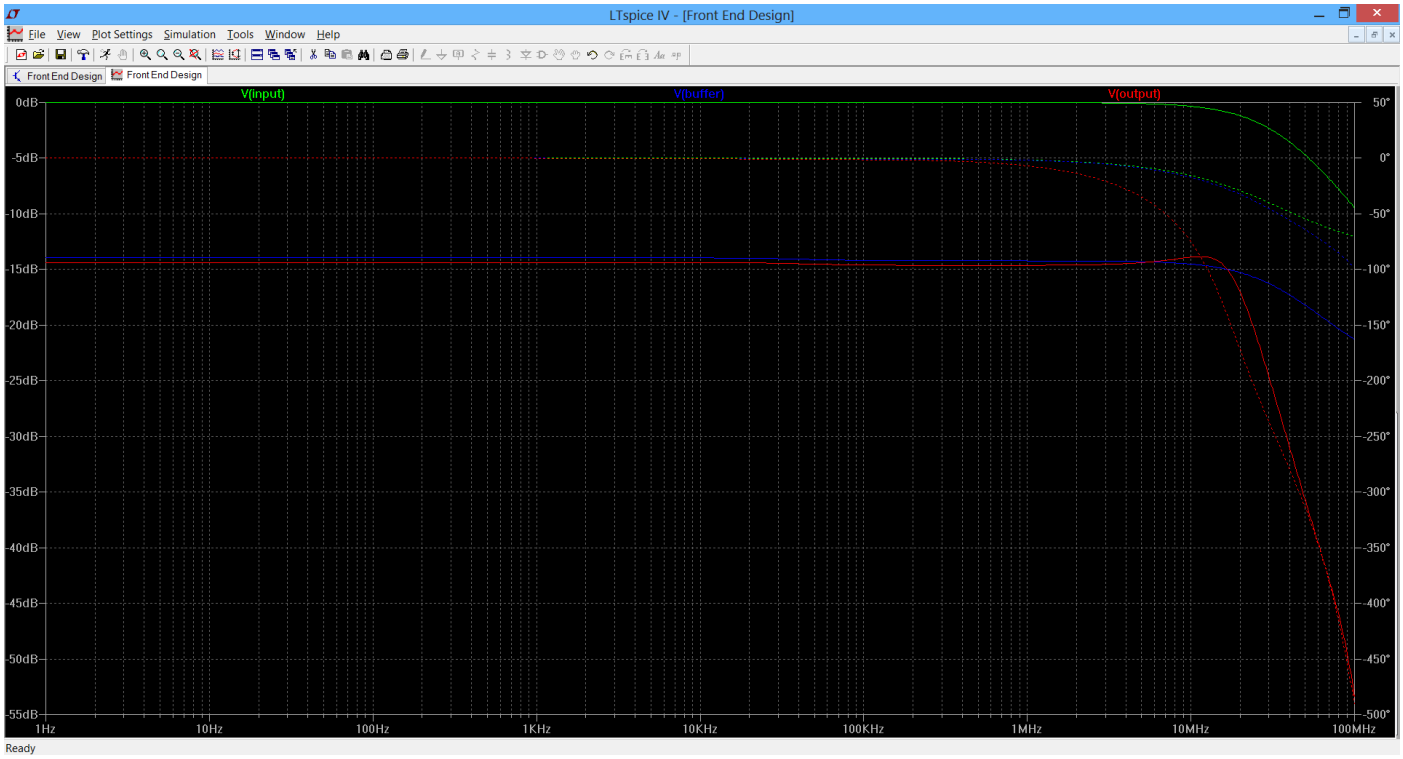

Figure 11: Frequency and phase responses of BNC input, prior to filter stage and ADC input

Green (BNC Input):
The BNC input from 0 Hz to 10 MHz is at 0 dB, showing the original signal at its original magnitude. The phase response remains largely linear as the frequency increases and only drops after 10 MHz.

Blue (Prior to Filter Stage):
The signal prior to the filter stage shows a very similar shape and response to the BNC input except that it is shifted down in magnitude. This is consistent with the presence of the scaling network circuit which significantly reduced the amplitude of the signal. This is a preface to the magnitude response of the output, shifting the magnitude down to the desired amplitude.

The phase response remains largely linear as the frequency increases and only drops after 10 MHz. It remains almost the same as the phase response of the BNC input.

Red (ADC Input):
The ADC input from 0 Hz to 10 MHz remains at a level of -14.38 dB which was aided by the scaling network circuit and buffer (prior to the filter stage). With the magnitude in the right range, all that is required is to set the cutoff frequency at 20 MHz. The frequency response of the output is consistent with the cutoff frequency at 20.473 MHz and a small rise before the cutoff frequency.

The phase response is largely linear until 1MHz. The anti-aliasing filter has an effect on the phase response, due to having an early cutoff frequency.

8. DISCUSSION

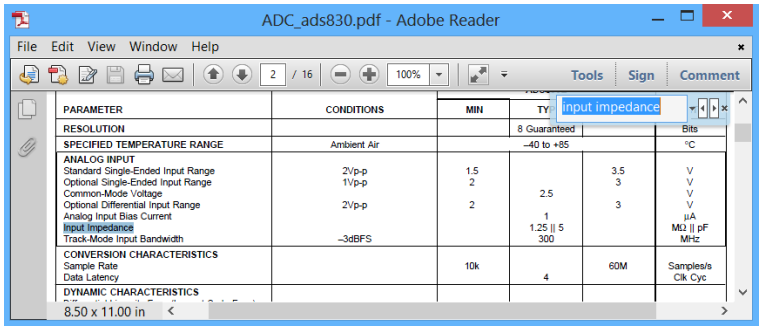

Figure 12: Screenshot of ADS830 datasheet[2]

The input impedance as found for the ADC (ADS830)[2] is $1.25M\Omega \;||\; 5\;pF$.
This is used to model the ADC input in the LT Spice simulation.

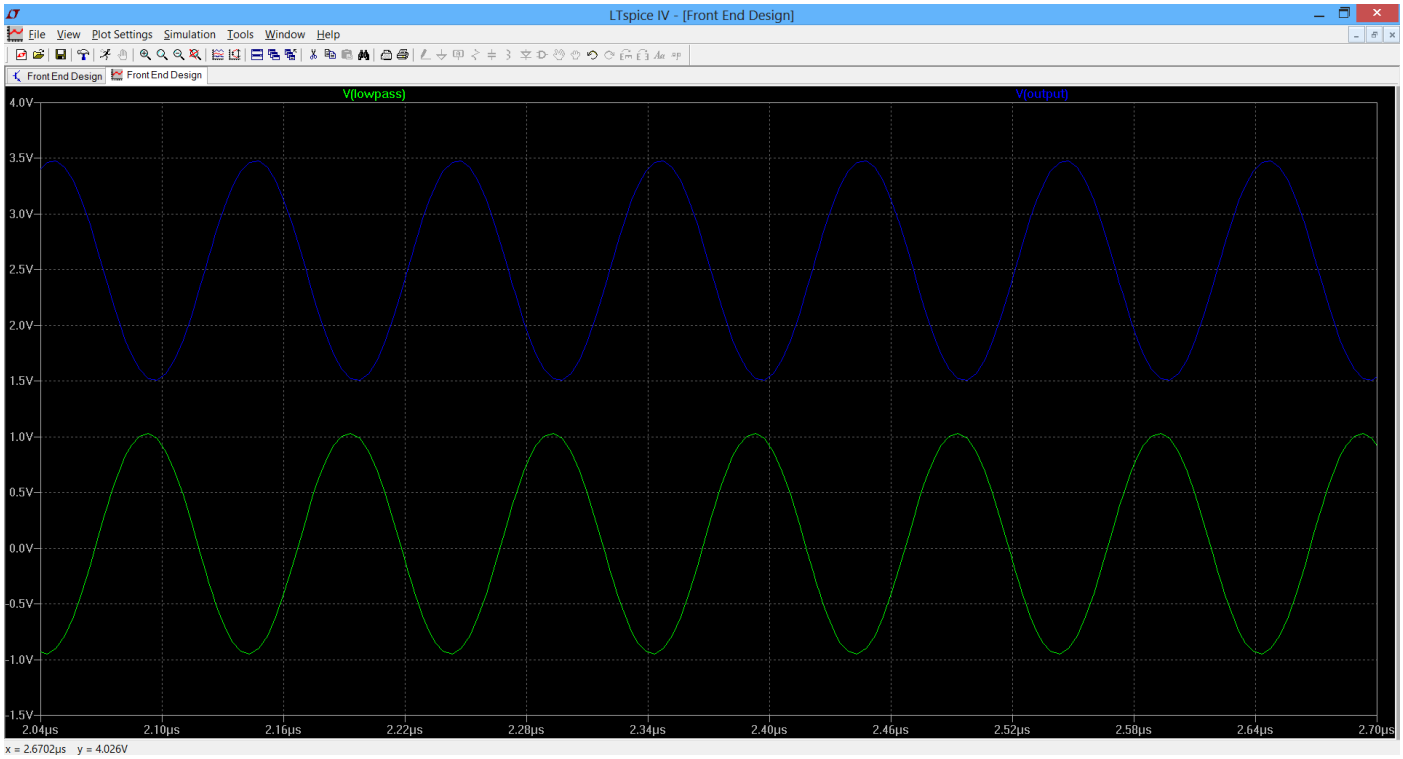

Figure 13: Time domain voltage response for filter output and level shifter output

The time domain response for the circuit is given as above. The green line refers to the output of the lowpass filter, showing how it has been scaled to 2Vpp from the original 5Vpp signal. This is to accommodate the specification of the ADS830 that the input must be between 1.5V-3.5V. The blue line refers to the output of the level shifter, showing that it fulfills the criteria specified by the datasheet of the ADS830.

Note that the phase of the signal is inverted by almost 180 degrees due to the nature of the inverting amplifier used. However, for our purposes the phase of the signal is insignificant compared to the ramifications of a change in magnitude.

9. CONCLUSION

The front end circuit design successfully achieves the functional specifications of the project, requiring multiple iterations. This is confirmed and verified by the simulation done in LT Spice. There are many approaches to design the front end circuit, each with advantages and disadvantages, and require decisions to be made regarding the tradeoffs.