

DIGITAL SYSTEM FOR SERIAL FSK MODULATED DATA RECEPTION

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ABSTRACT

This paper describes a complete software developed system, designed, implemented and tested, for the reception of serial, low rate, data transmitted employing binary FSK (Frequency Shift Keying) modulation. The FSK demodulation process is implemented using an algorithm for a digital version of a PLL (Phase Locked Loop) in software. The complete reception process is implemented using methodologies and techniques from the digital signal processing field and they are implemented using C language in a dsPIC microcontroller from Microchip.

KEYWORDS

Serial Data Transmission, FSK Modulation, Software PLL, Digital Signal Processing, Embedded Applications, Microcontrollers

1. INTRODUCTION

One of the main modern trends and challenges in engineering is to employ digital system for the realization of previously analog done signal processing tasks, in the different areas of application. Three tendencies for implementation are relevant: complete in Hardware, complete in Software or a mixed realization (Software and Hardware). In the project described here, a complete software realization is developed for the reception of a serial, low rate, data transmitted using binary FSK modulation. The recent advances in microcontrollers (MCU) capacities and speed of processing, makes possible the use of them to implement digital communication system blocks, by means of software processing, in communication links with low carry frequencies and data rates. This is the main goal of the system developed and described in this paper.

2. SYSTEM ARCHITECTURE AND SPECIFICATIONS

In Figure 1 a block diagram of the proposed reception system is presented and the technical specifications chosen for the system are detailed. The frequencies selected, as an example, for bit ‘1’ and bit ‘0’ correspond to the Bell 103 standard which defines the frequencies for data communication using FSK via dial-up telephone lines, where the answer modem uses a mark frequency (bit ‘1’) of 2225 Hz and a space frequency (bit ‘0’) of 2025 Hz [1]. The input signal is digitized by the ADC and then processed by software algorithms to realize the demodulation (Digital FSK demodulator block) and the byte extraction process. A sampling frequency of 20000 Hz is adopted which is roughly 10 times the maximum input frequency.

The Digital FSK demodulator may be designed employing one of two approaches: a) by using a two frequency discrimination system with digital band-pass filters, envelop detectors and a threshold device or b) by using a digital feedback demodulator, as for example, a digital PLL, which perform better than discriminators in the presence of noise [2]. The second approach is the one adopted for the built system, with the added novelty of the digital PLL being implemented by a software algorithm.

3. PLL BASIC FUNDAMENTALS

3.1. PLL as a FSK Demodulator

In Figure 2 the block diagram of an analog PLL (Phase Locked Loop) working as a FSK demodulator is presented along with its main features and signal relations [2].

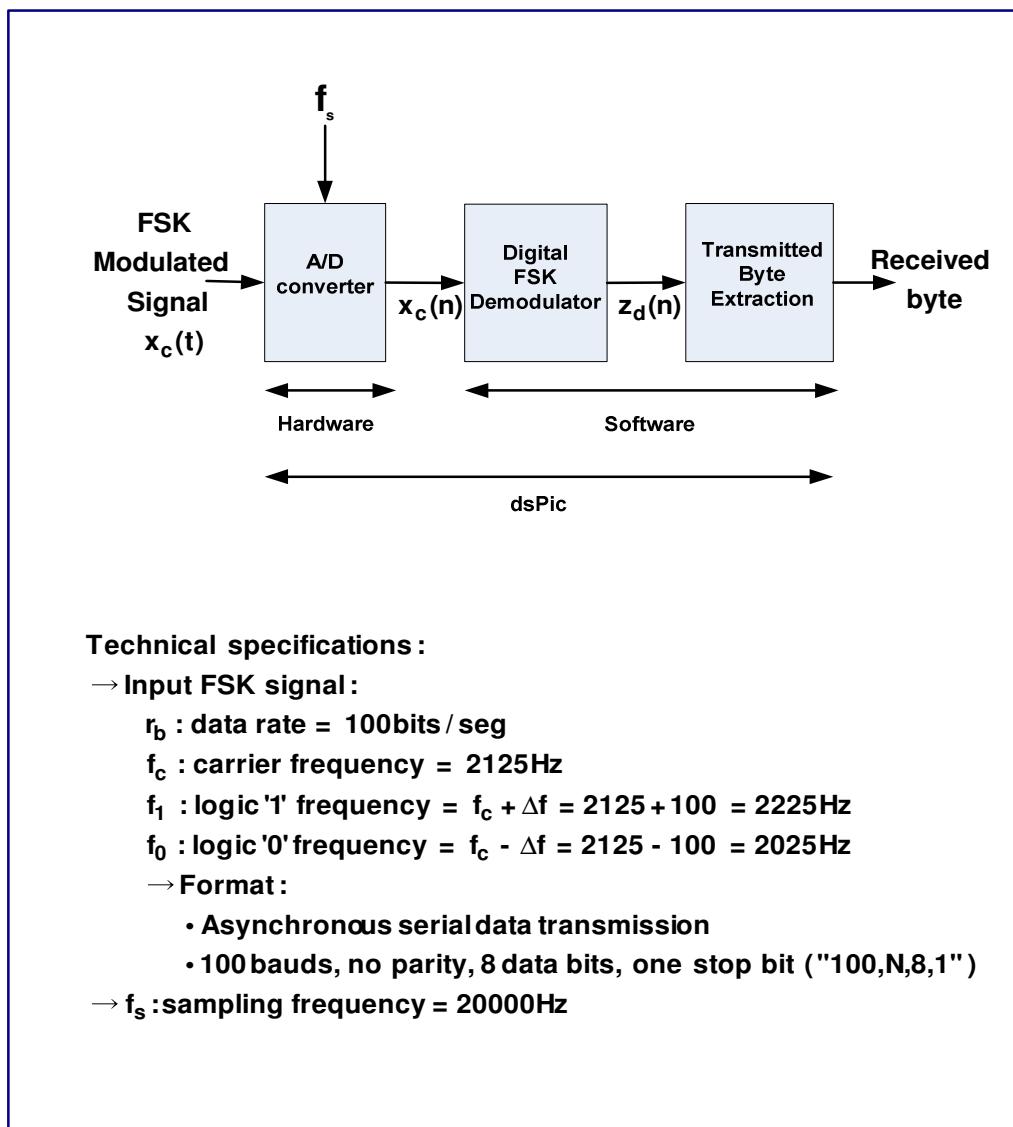


Figure 1. Proposed Digital System For Serial FSK Reception

3.2. Linear 2^o Order PLL

In Figure 3 a linearized model of a PLL is shown, built with the addition of a proportional + integral filter (loop filter), to obtain a PLL model having a second order transfer function M(s) with characteristic parameters: w_n (natural not damped frequency) and ζ (the damping ratio) defined there [2].

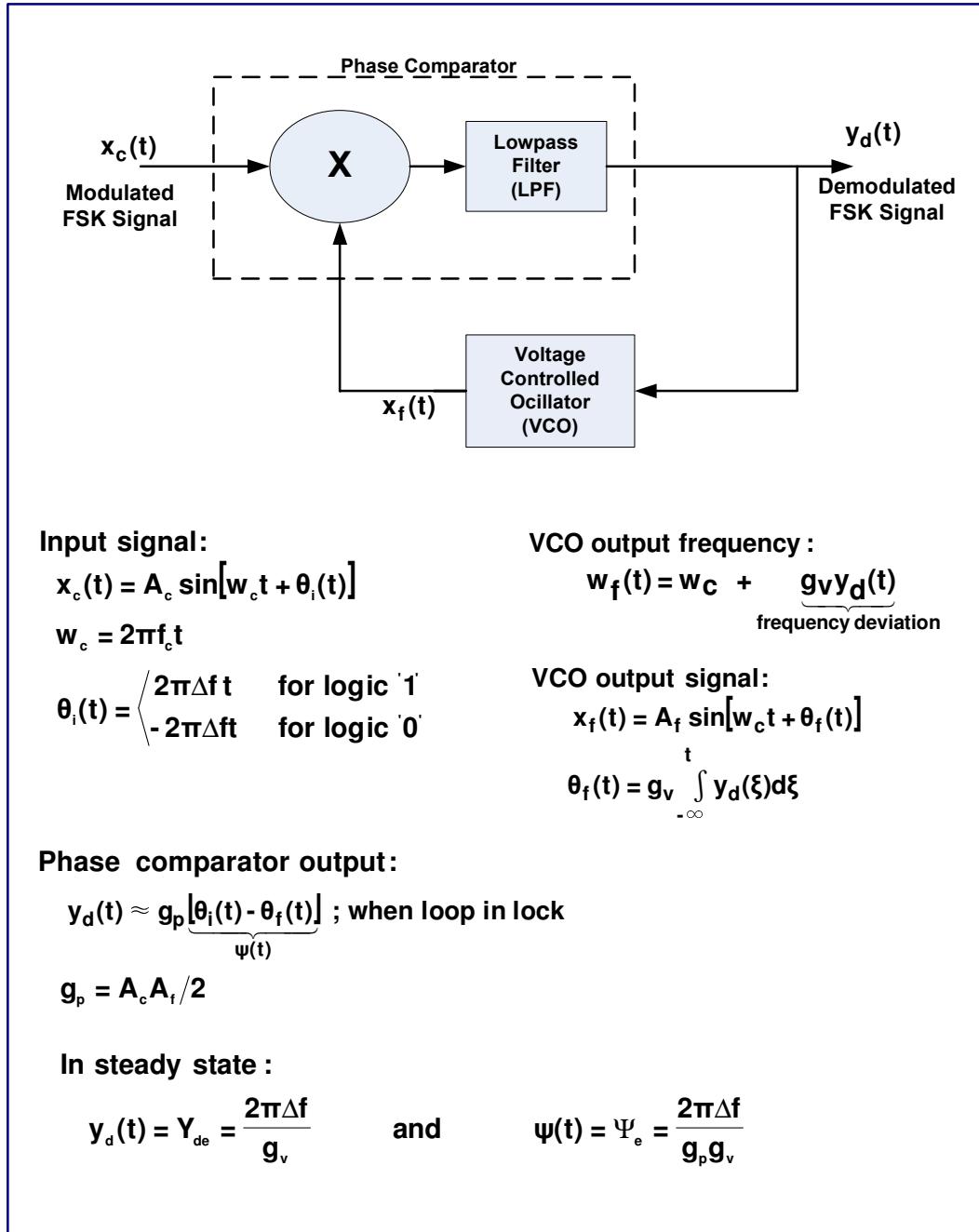


Figure 2. PLL as a FSK Demodulator

4. PLL DESIGN

General design criteria [2] [3] are also stated in Figure 3 along with the design parameters values calculated to fulfil these requirements.

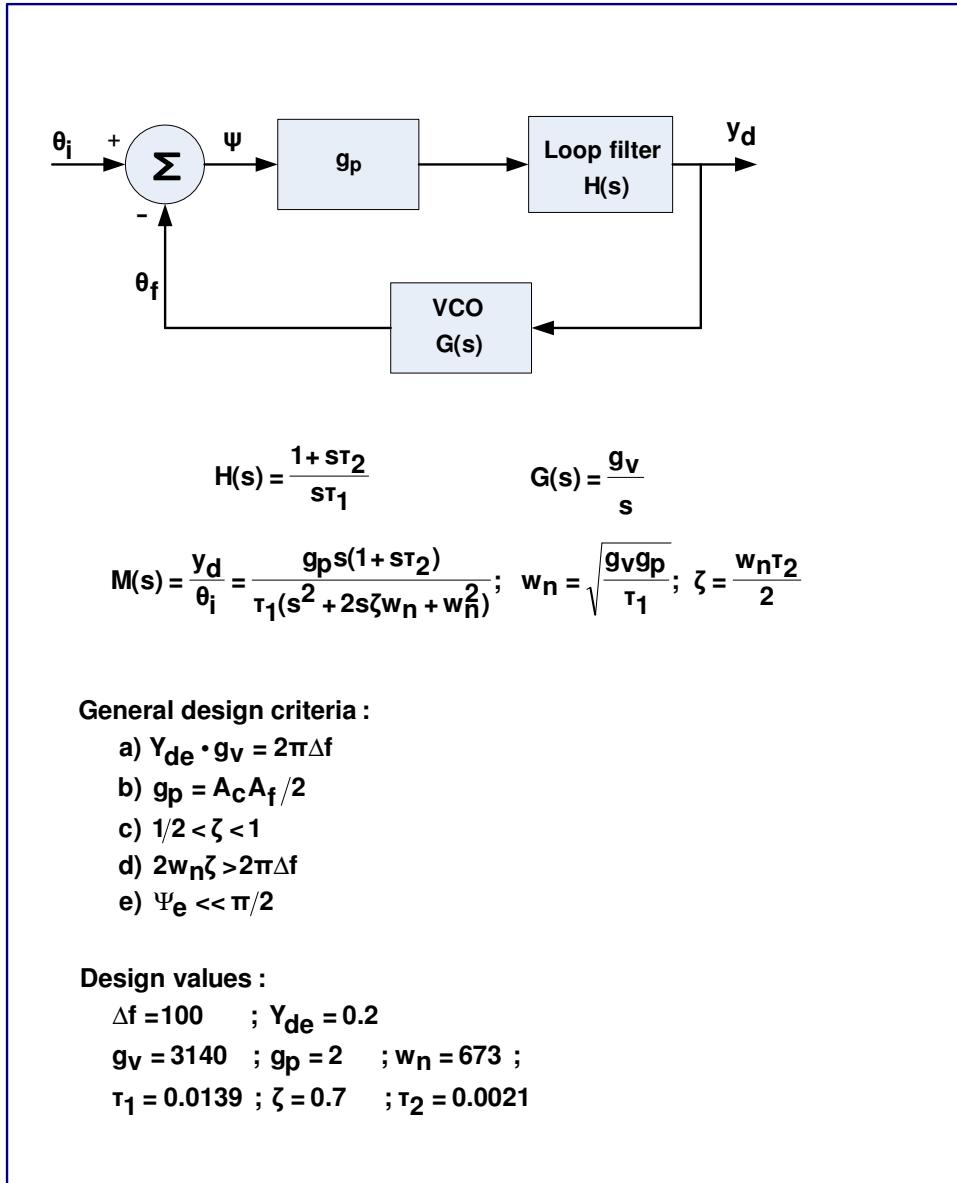


Figure 3.Linearized Model Approximation of a 2° Order PLL

5. DIGITAL PLL

A digital version, suitable to be implemented by software, is illustrated in Figure 4 [3]. The transfer function $H(z)$ for the previously defined analog loop filter is digitized employing the bilinear Z transform [3] to obtain a digital filter transfer function $H(z)$. The loop oscillator (VCO)

is replaced by a DCO: Digital Controlled Oscillator which produces a square wave with an instant frequency deviation proportional to the value of its input signal [3].

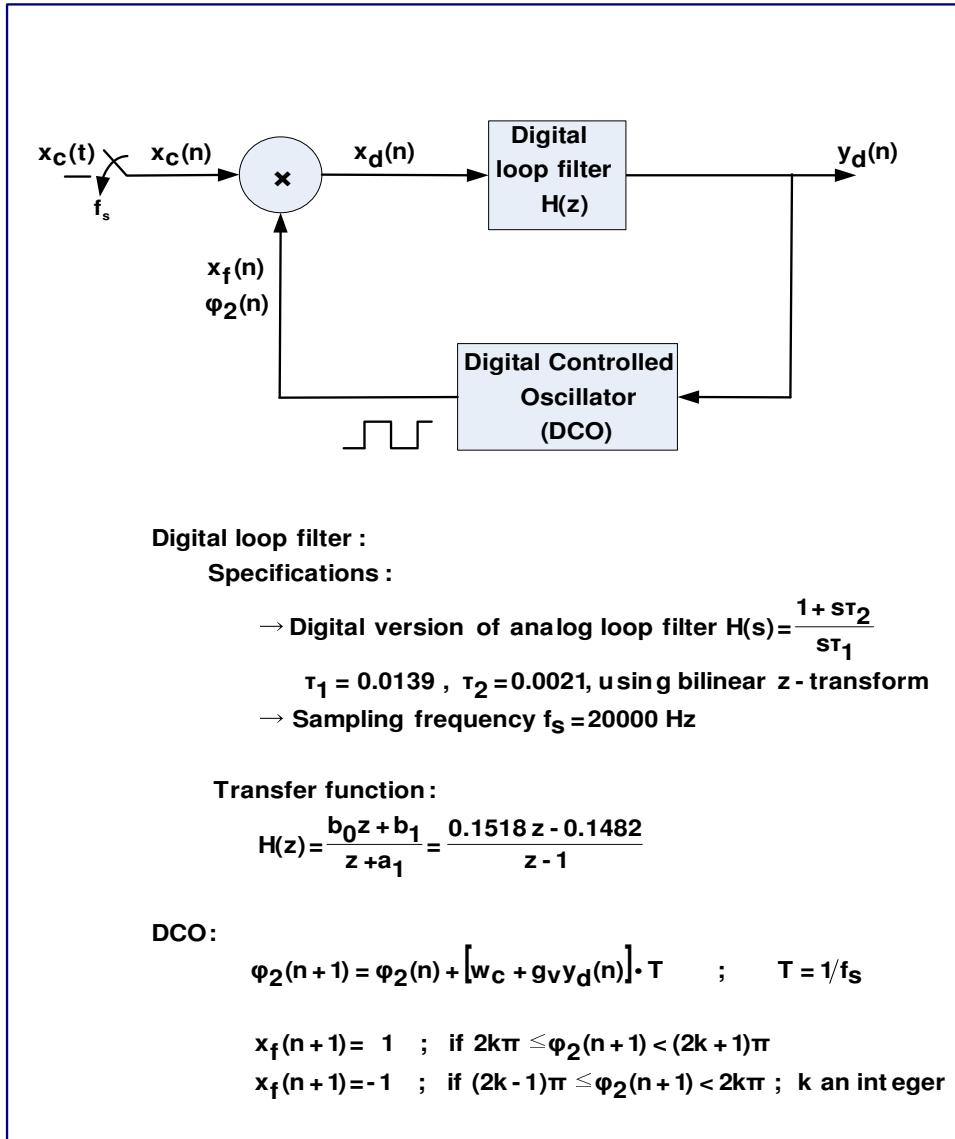


Figure 4. Digital PLL

5.1. PLL Software Algorithm

The flow diagram of an algorithm for the digital PLL is shown in Figure 5 [3].

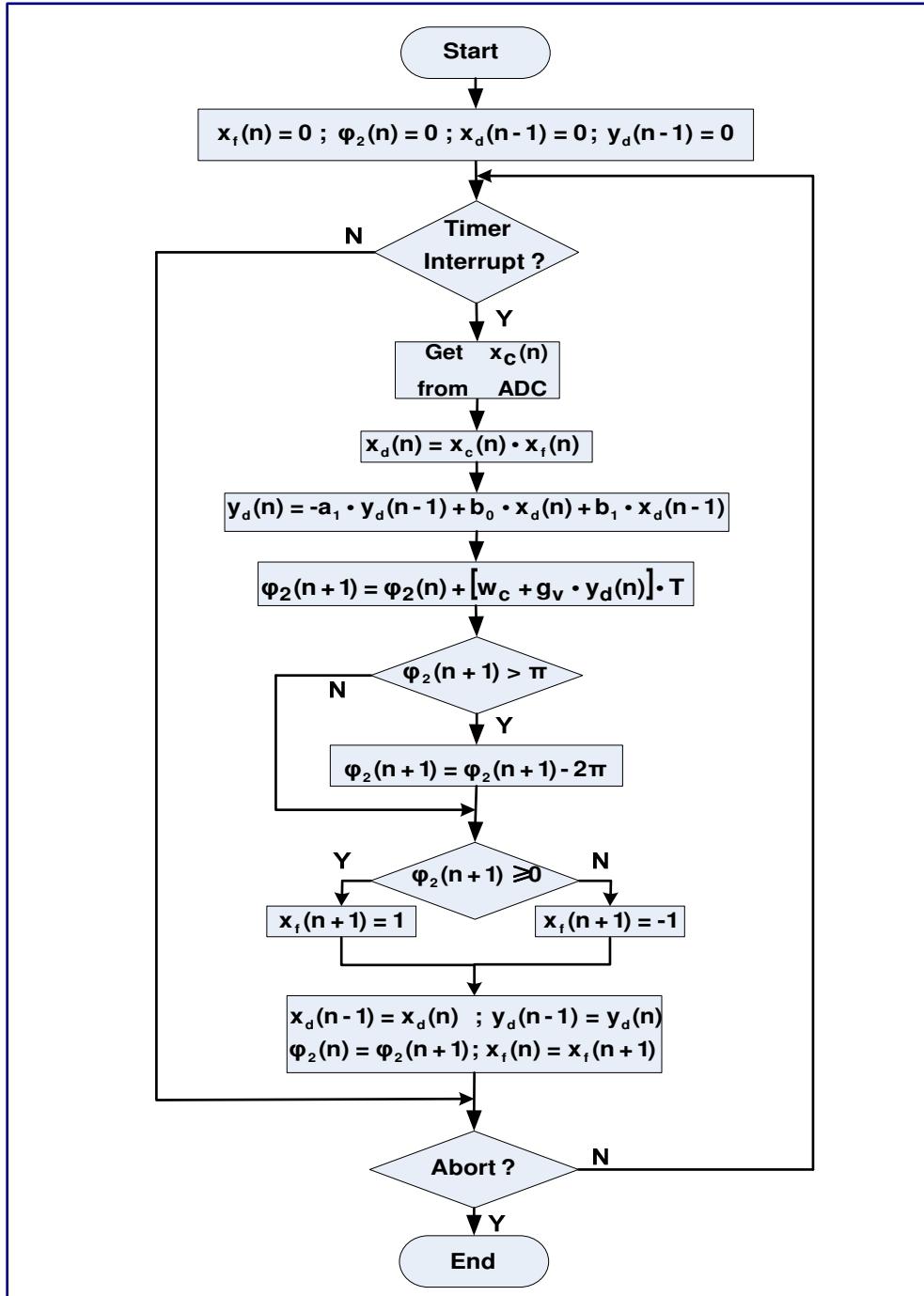


Figure 5. PLL Algorithm

6. DIGITAL FSK DEMODULATOR

The digital FSK demodulator employed was built using the software PLL and a digital low-pass smoothing filter, implemented also in software, to remove residual high frequency components present at the output of the PLL (Figure 6). The specifications and characteristics of the used filter

are described also in this Figure. The 68 Hz cutoff frequency selected, turned out to be an appropriate compromise value between two opposite requirements: amount of smoothing and speed of response.

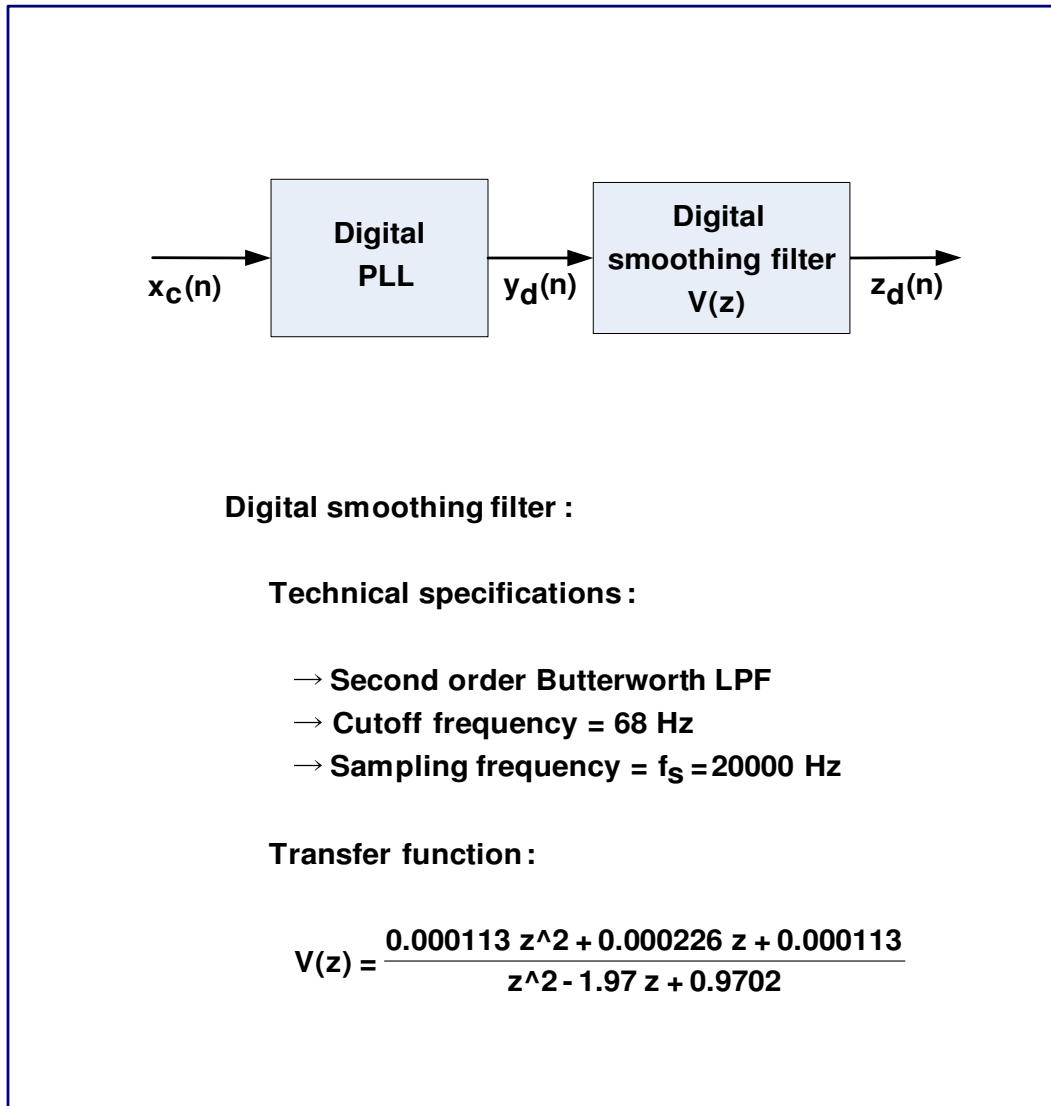


Figure 6. Digital FSK Demodulator

7. TRANSMITTED BYTE EXTRACTION

In Figure 7 the configuration for the subsystem to extract the transmitted byte is shown. The signal at the output of the digital FSK demodulator is converted to a two level signal (binary signal) employing a threshold level detection and this binarized signal is processed in a standard fashion to detect the start bit indicating the beginning of a byte transmission, to extract the following data bits, and to detect the stop bit indicating the end of transmission. The data bits conform to the received byte. This process is also implemented by software, to agree with the objective of a complete software implementation.

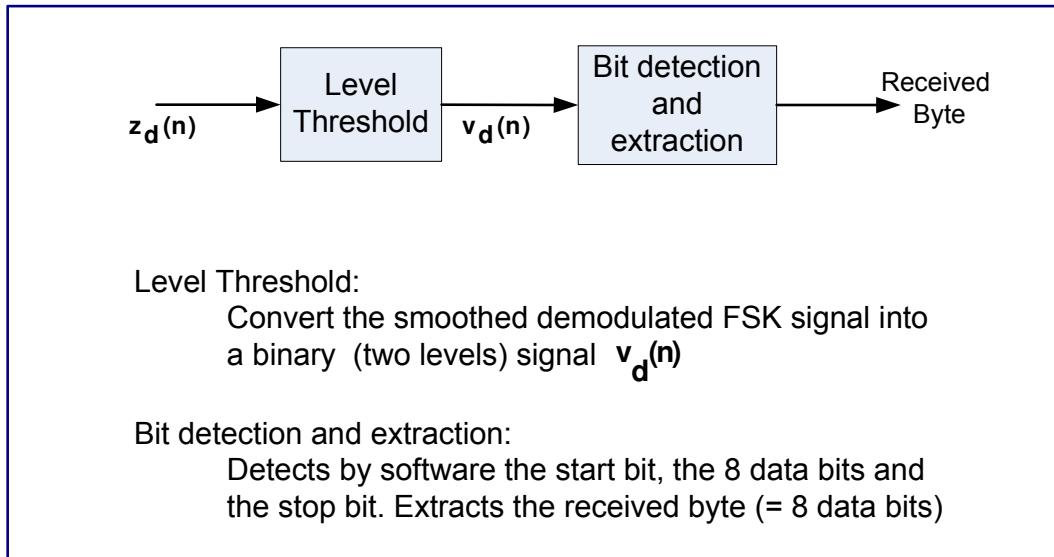


Figure 7. Transmitted Byte Extraction

8. SYSTEM IMPLEMENTATION

The digital reception system is completely software implemented in a dsPIC30F4011 microcontroller from Microchip. The dsPIC30F family are high performance digital signal controllers with a 16 bits architecture, offering the performance of a DSP with the simplicity of an MCU; with a single cycle MAC, up to 30 MIPS instruction execution operating speed, 40 bit accumulator and a variety of peripheral units [4]. The dsPIC30F4011 has 48 Kbytes of Flash Program Memory, 2048 Bytes of RAM, 30 I/O Pins and a 10 bit ADC analog peripheral capable of operating up to 1000 ks/s [5].

In this project the dsPIC30F4011 was operated with a 120 Mhz clock speed for a 30 MIPS instruction execution speed. The ADC was configured for an 8 bit operation. The entire software processing is performed in a timer based interrupt cycle of 50 micro seconds to accomplish a sampling frequency of 20000 Hz. The basic cycle of software processing is illustrated in Figure 8. The software was completely written in C language using a C free compiler version from Microchip [6]. The algorithm computation process was carried out using 16 bit fixed point representation to speed process calculation.

7. TEST SYSTEM

An infrared communication system was built to test the digital reception system performance. The block diagram is shown in Figure 9. The message contained in the transmitted data is visualized in an alphanumeric LCD. Samples of the internal processed signals are registered and sent to the laptop computer to be visualized and edited.

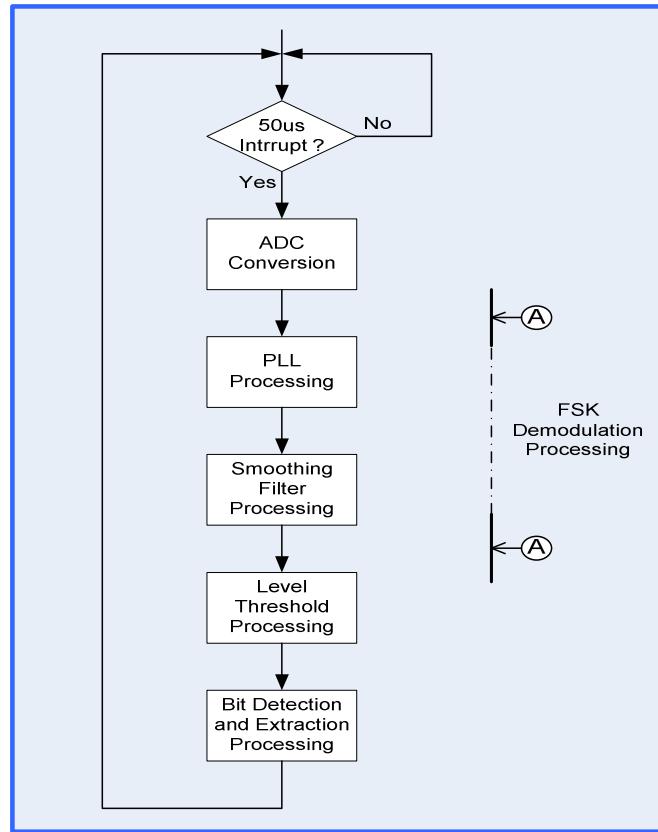


Figure 8. Basic Software Processing Cycle

8. RESULTS

The digital signals at the inputs and outputs of the different software processing blocks are displayed in Figure 10, for a data byte (01001011) transmission example (10 bits are transmitted in total, including the start bit and one stop bit), revealing a correct digital reception of the transmitted byte and a good performance operation of the proposed FSK demodulator block using the software PLL.

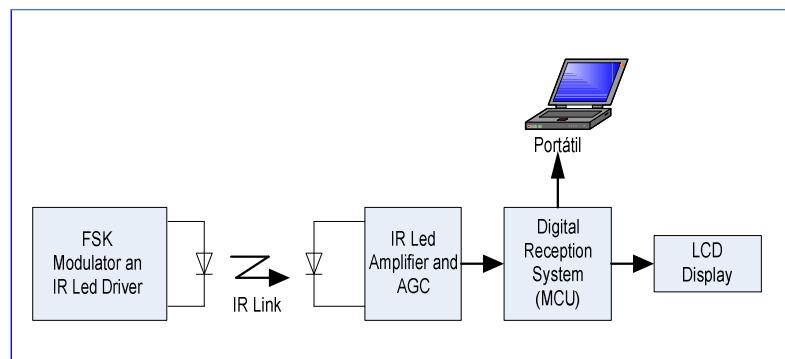


Figure 9. Test System

9. CONCLUSIONS

The recent advances in DSP processing capabilities and increased operation speed of modern MCU, has made feasible the realization of digital communication blocks, completely software implemented in a single chip, for low data rates communication links. As an example, is the digital reception process for serial FSK modulated data, implemented and described in this paper, which employs a software implementation version of a PLL for the digital signal demodulation processing.

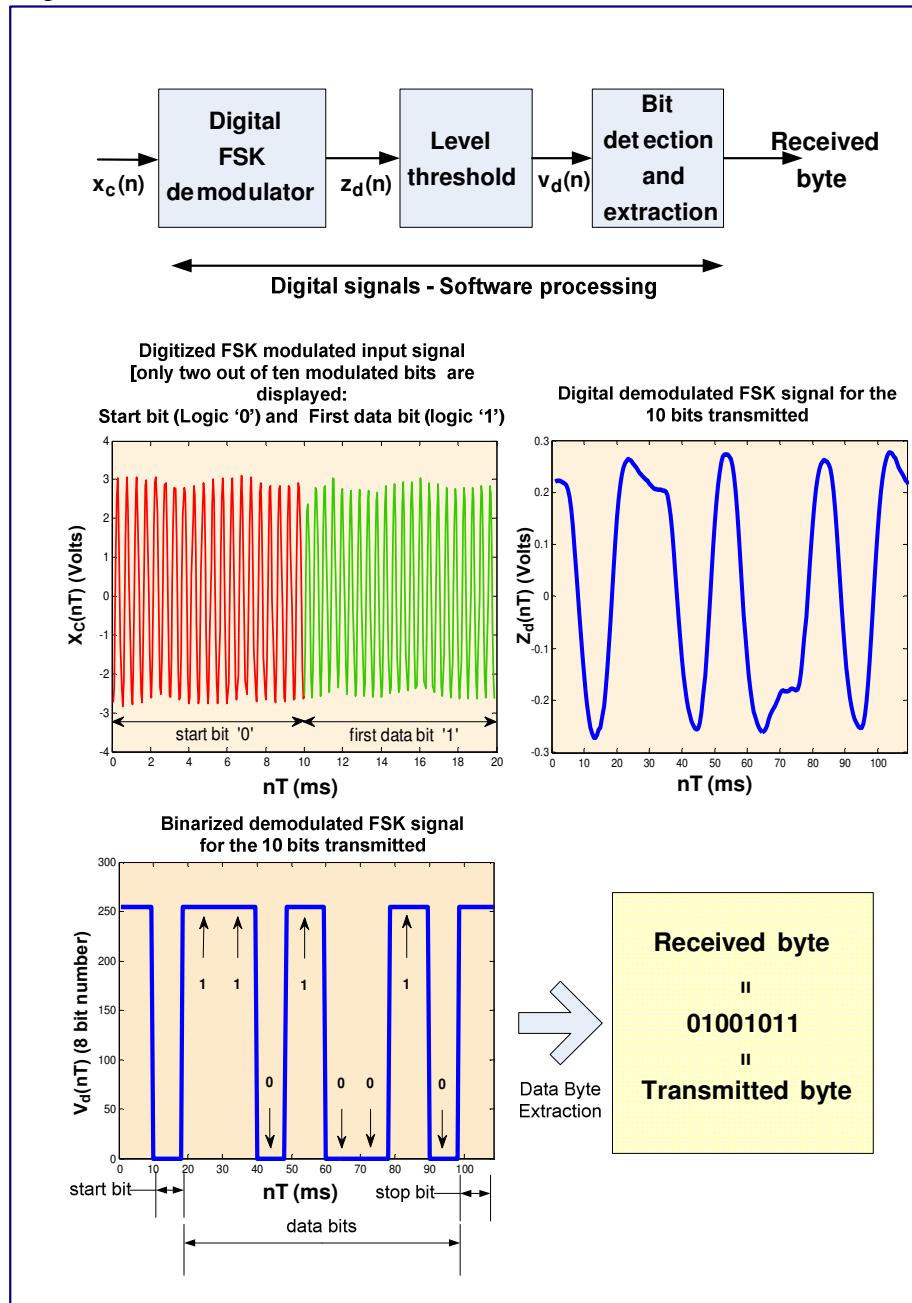


Figure 10. Digital Signals

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