

# Frequency-Shift Keying Modulation and Demodulation Using the Timer/Counter Peripherals on the AVR® EB

## TB3350

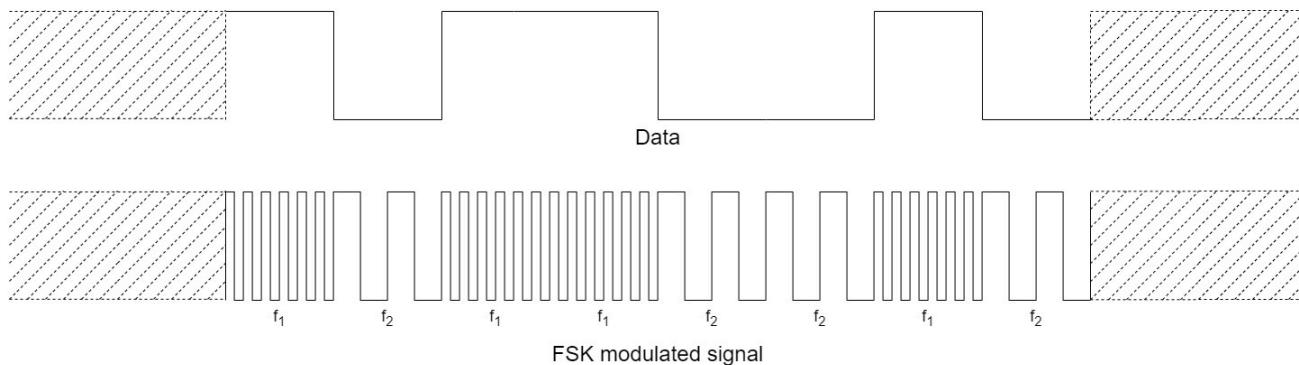


## Introduction

Frequency-shift keying (FSK) is a digital modulation technique that involves varying the frequency of a carrier signal to transmit digital information. The carrier signal is shifted between two or more frequencies to represent different binary states in FSK. The frequency shift between the two states is typically low, and the signal is demodulated by detecting the frequency shift. FSK is commonly used in applications such as wireless communication, RFID, and telemetry systems.

The FSK modulation method that only uses two frequencies is called Binary FSK (BFSK). The carrier signal frequency is shifted between the two frequencies to represent the binary data, while the phase of the carrier signal remains constant during this process. The frequency used to represent a binary 1 is known as "mark," while the one used to represent a binary 0 is known as "space."

**Figure 1.** FSK Working Principle



BFSK modulation and demodulation techniques using peripherals specific to the AVR® EB Family of microcontrollers (MCUs) are addressed in this technical brief. These techniques are implemented using the Timer/Counter Type F, E and B (TCF, TCE and TCB) peripherals. One code example was developed around the AVR16EB32 MCU, showcasing full-duplex communication between two Curiosity Nano (CNANO) boards through BFSK modulation and demodulation. The code example uses the MPLAB® Code Configurator (MCC) for the initial device and peripherals setup. It has a corresponding web page on the Microchip MPLAB Discover website, providing a comprehensive description of the hardware and software requirements.



Click to view code examples on MPLAB DISCOVER

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## 1. Peripherals Overview: Timer/Counters

The AVR EB Family of MCUs features multiple timer/counters with input capture, output compare, Pulse-Width Modulation (PWM) and frequency generation capabilities:

- Two 16-bit Timer/Counters type B (TCB) with input capture for capture and signal measurements
- One 16-bit Timer/Counter type E (TCE) with four compare channels and a Waveform Extension (WEX) for PWM generation.
- One 24-bit Timer/Counter type F (TCF) for frequency generation
- One 16-bit Real-Time Counter (RTC) that can run from an external crystal or internal oscillator

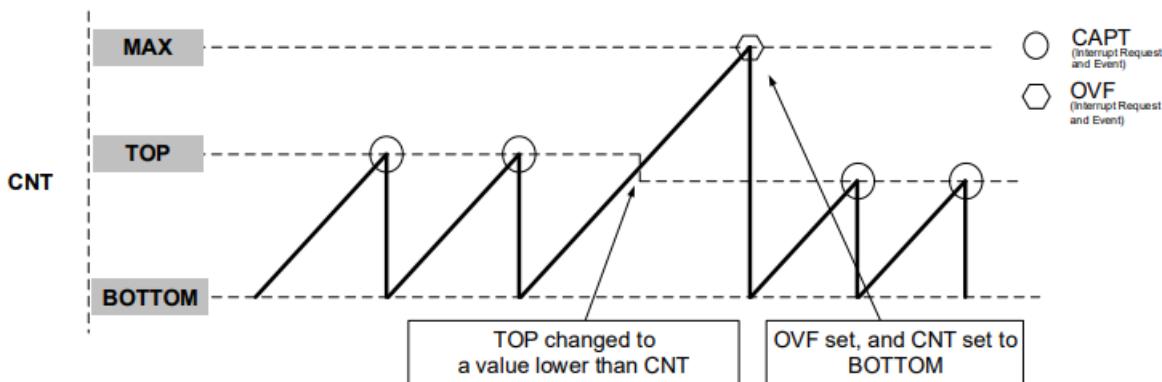
### 1.1 Timer/Counter Type B

The capabilities of the TCB include frequency-adjustable waveform generation and input capture on event with time and frequency measurement of digital signals. The TCB consists of a base counter and control logic that can be set in one of eight different modes, each mode providing unique functionality. The base counter is clocked by the peripheral clock with optional prescaling. The TCB features the following characteristics:

- 16-Bit Timer/Counter
- Operation Modes:
  - Periodic interrupt
  - Time-out check
  - Input capture:
    - On event
    - Frequency measurement
    - Pulse-width measurement
    - Frequency and pulse-width measurement
    - 32-Bit capture
  - Single-Shot
  - 8-Bit PWM
- Noise Canceler on Event Input
- Synchronized Operation with TCE

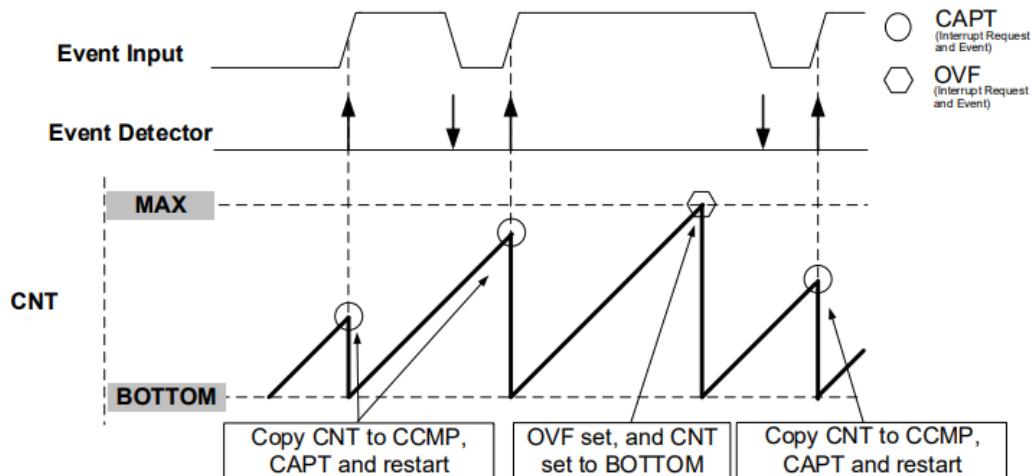
In the context of this technical brief, both TCB instances are used, and the focus is on the Periodic Interrupt mode and Input Capture Frequency Measurement mode.

In the Periodic Interrupt mode, the counter adds up to the capture value and restarts from BOTTOM. A Capture interrupt and event is generated when the counter value equals to TOP. If TOP is updated to a value lower than the counter value, upon reaching MAX (the maximum value in the count sequence), an Overflow interrupt and event is generated, and the counter restarts from BOTTOM.

**Figure 1-1.** TCB Periodic Interrupt Mode

In the Input Capture Frequency Measurement mode, the TCB captures the counter value and restarts on either a positive or negative edge of the event input signal, depending on the state of the Event Edge bit in the Event Control (TCBn.EVCTRL) register. The Count register value is transferred to the Compare/Capture register, and a Capture interrupt and event are generated. The Capture interrupt flag is cleared automatically after reading the low byte of the Compare/Capture register. An Overflow interrupt and event are generated when the counter value reaches MAX.

The Input Capture Frequency Measurement mode requires the TCB to be configured as an event user by writing 1 to the Capture Event Input Enable bit in the Event Control register and setting up the Event System (EVSYS) according to the application's requirements. The event must last at least one peripheral clock cycle to be recognized.

**Figure 1-2.** TCB Input Capture Frequency Measurement

If additional filtering of the input signal is desired, the Noise Canceler feature of the TCB can be used. When the Noise Filter bit in the Event Control register is enabled, the peripheral monitors the event channel and keeps a record of the last four observed samples. If the four consecutive samples are equal, the input is considered stable, and the signal is fed to the edge detector.

## 1.2

### Timer/Counter Type E

The TCE provides accurate program execution timing, frequency and waveform generation, and command execution. The TCE consists of a base counter and multiple compare channels. The base counter can be used to count clock cycles or events or let events control how it counts clock

cycles. The counting direction and period setting control are used for accurate timing. The compare channels can be used with the base counter for compare match control, frequency generation, and pulse-width waveform modulation. The TCE features the following characteristics:

- 16-Bit Timer/Counter
- Four Compare Channels
- Double-Buffered Timer Period Setting
- Double-Buffered Compare Channels
- Waveform Generation:
  - Frequency generation
  - Single-Slope PWM
  - Dual-Slope PWM
- Count on Event
- Timer Overflow Interrupts/Events
- One Compare Match per Compare Channel
- Increase Waveform Generator Resolution up to 8x (three bits)

Depending on the mode of operation, the counter is cleared, reloaded, incremented, or decremented at each timer/counter clock or event input. In the context of this technical brief, the focus is on the Normal operation mode.

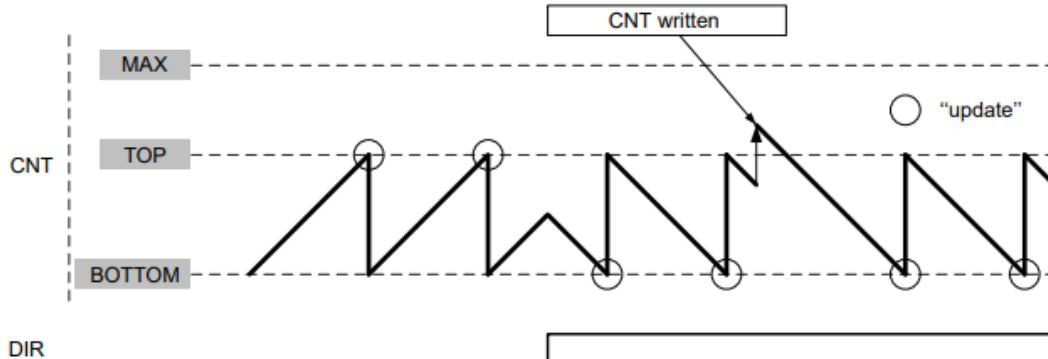
During operation, the counter counts clock ticks in the direction selected by the Direction bit in the Control E (TCEn.CTRLE) register. The clock ticks are given by the peripheral clock, prescaled according to the Clock Select bit field in the Control A (TCEn.CTRLA) register.

The counter value is compared continuously to zero and the Period register value to determine whether the counter has reached TOP (the highest value in the count sequence) or BOTTOM (zero). When reaching TOP while the counting direction is set to up, the counter will wrap to 0 at the next clock tick. When counting down, the counter is reloaded with the Period register value when the BOTTOM is reached.

The counter value in the Counter register can be changed during operation. The write access to the register has higher priority than the count, clear or reload operations and will be immediate. The direction of the counter can also be changed during normal operation by writing to the Direction bit.

An Overflow interrupt and event will be generated when the counter has reached either TOP or BOTTOM, depending on the counting direction.

**Figure 1-3. TCE Normal Operation**



## 1.3 Timer/Counter Type F

The TCF capabilities include frequency and waveform generation. The TCF consists of a base counter and a control logic, which can be set in different modes, each providing unique functionality. The base counter is clocked by a selectable clock source with optional prescaling. The TCF features the following characteristics:

- 24-Bit Timer/Counter
- Operation Modes:
  - Frequency Generation
  - Numerically Controlled Oscillator (NCO)
    - Pulse-Frequency
    - Fixed Duty Cycle
  - 8-Bit PWM
- 7-Bit Prescaler
- Timer Overflow and Two Compare Match Events/Interrupts
- Event Generation as Pulse or Waveform Output
- Multiple Clock Sources

Depending on the operation mode, the peripheral's registers functionality might be different. This chapter of the technical brief focuses on the NCO Fixed Duty Cycle mode.

In the NCO Fixed Duty Cycle Frequency Generation mode, the TCF operates by repeatedly adding at the input clock rate a fixed value (increment) defined by the Compare register to an accumulator (Counter register). The accumulator will overflow with a carry periodically, effectively reducing the input clock by the ratio of the added value to the maximum accumulator value.

The frequency ( $f_{FRQ}$ ) of the generated waveform is defined by the following equation:

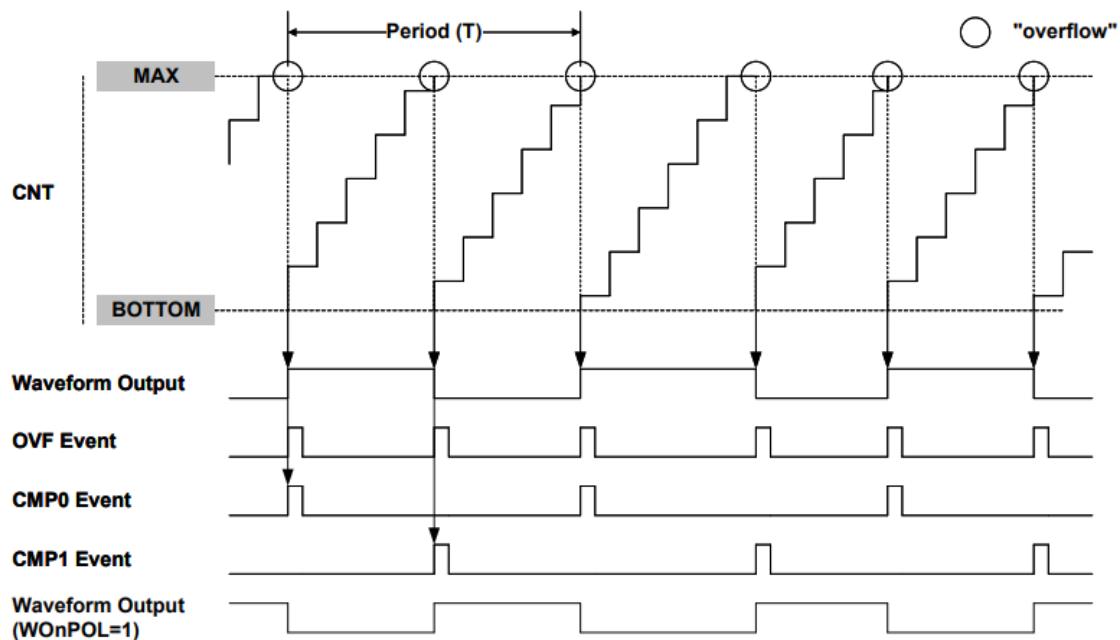
$$f_{FRQ} = (f_{CLK\_TCF} \times \text{Increment}) / 2^{\text{SIZE\_CNT} + 1}$$

This makes a linear relationship between the waveform frequency and the increment, effectively allowing for accurate frequency waveform generation. This linear advantage over divide-by-n timers comes at the cost of the output jitter. However, the jitter that periodically occurs is always plus or minus one clock period, depending on the division remainder.

The waveform output is toggled every time the accumulator overflows. Given that the increment value remains constant, the resulting waveform will have a 50% duty cycle.

The two Compare interrupts and events are generated on alternating overflows where one will match the rising edge of the waveform and the other the falling edge. An overflow interrupt/event is generated on all overflows.

Figure 1-4. TCF NCO Fixed Duty-Cycle Frequency Waveform Generation



## 2. Modulation Technique

The Universal Synchronous and Asynchronous Receiver and Transmitter (USART) peripheral receives the input data provided in the serial terminal. The modulation process starts when there are available data in the USART Receive Buffer.

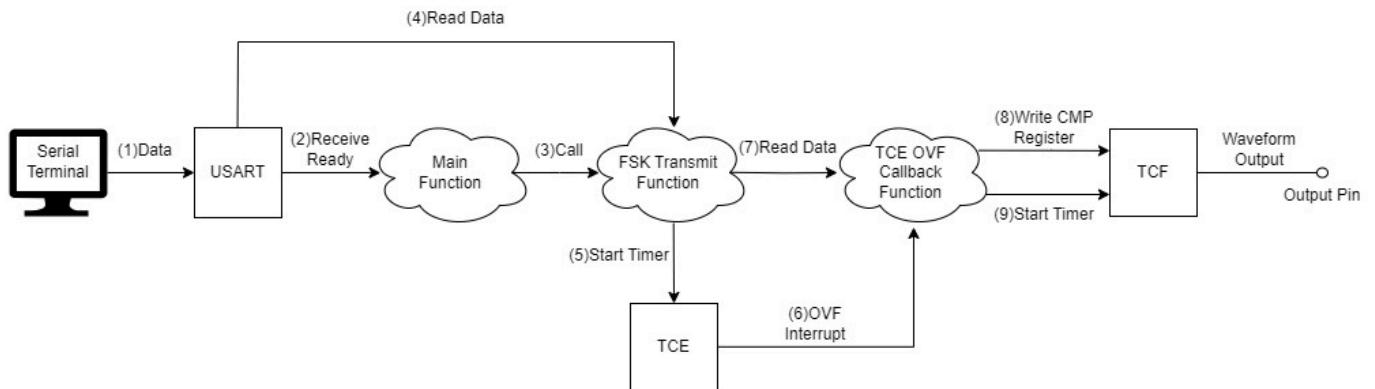
The TCF is configured in NCO Fixed Duty-Cycle mode and generates the modulated data signal. This operating mode offers great flexibility as the frequency of the generated signal is proportional to the increment value and, therefore, can be established precisely. Frequency shifting also happens without abrupt phase discontinuities of the output waveform.

The TCE is configured in Normal mode and generates an overflow interrupt once every millisecond. This periodic interrupt modulates the data byte by altering the increment value of the TCF and effectively switching the frequency of the output waveform to either the “mark” or the “space” corresponding value based on the state of each data bit.

The frame format of the modulated signal generated by the TCF is similar to the USART frame format. For every data byte, a total of 11 bits are modulated and transmitted. The output state of the TCF is initially logic low as the peripheral is disabled when there is no data to transmit.

As soon as the modulation process starts, the TCF is enabled, and a “mark” followed by a “space” are generated to emulate the Start bit. The data byte is modulated next, followed by another “mark” to emulate the Stop bit, before the TCF is disabled. The framing format will act as a synchronization method at the other end of the communication line, where the demodulation happens.

**Figure 2-1.** Modulation Process Diagram



**Figure 2-2.** Modulation of a Single Data Byte

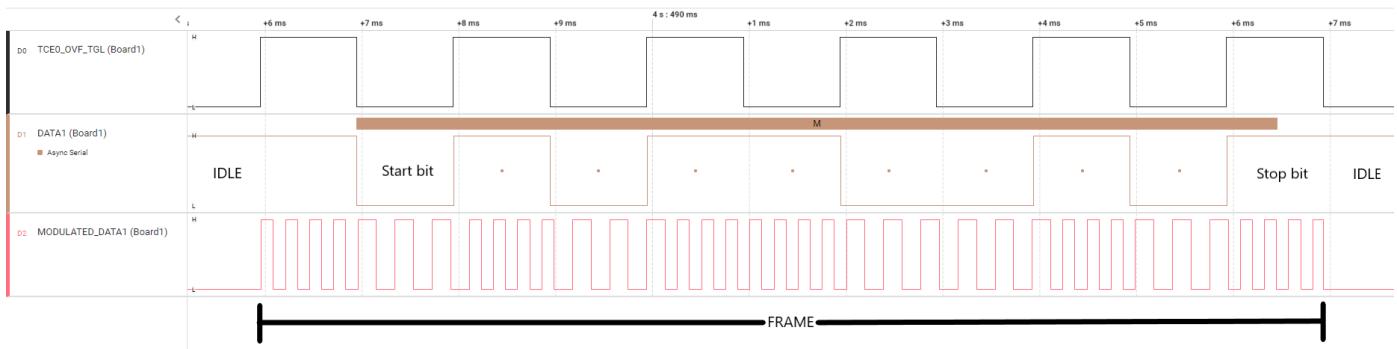
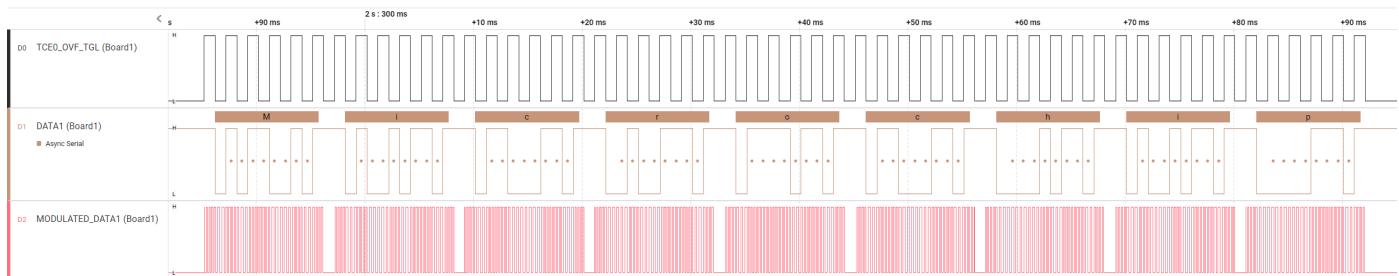


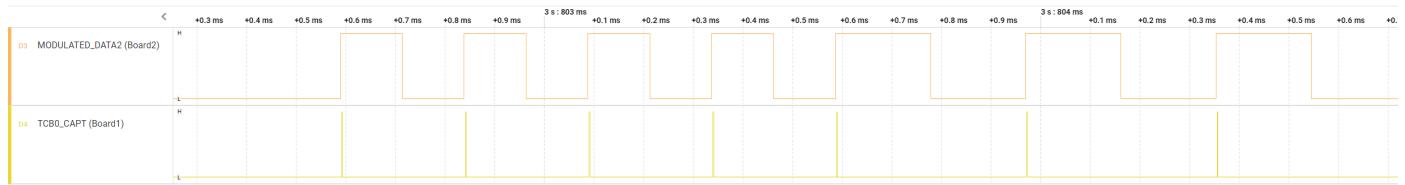
Figure 2-3. Modulation of Multiple Data Bytes



### 3. Demodulation Technique

The demodulation process is implemented using two instances of the TCB peripheral. The first instance operates in Input Capture Frequency Measurement mode and is used to distinguish between the two FSK frequencies. The received modulated signal is fed to the TCB input channel with the help of the EVSYS, and a capture interrupt is generated on each waveform period. Based on the captured value, the software determines if the measured frequency corresponds to a “mark” or a “space” and updates a state variable accordingly.

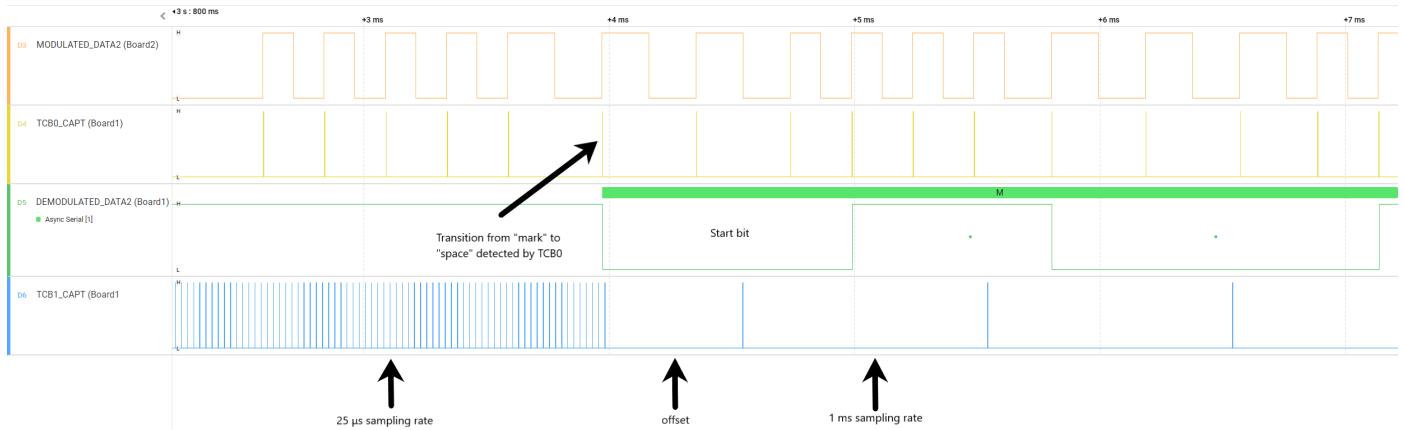
**Figure 3-1.** TCB Capture Interrupt Generation



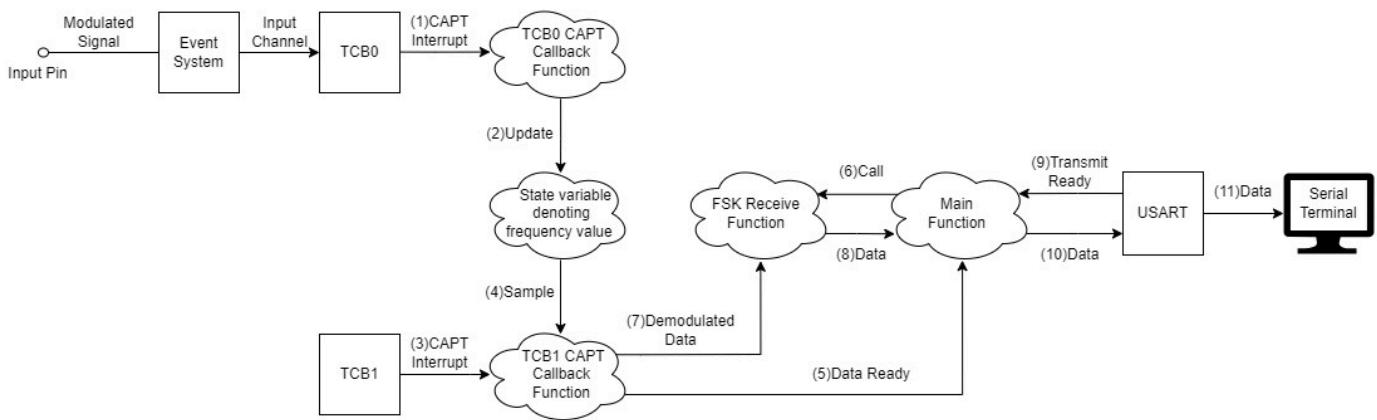
The second TCB instance, operating in the Periodic Interrupt mode, is used to sample the state variable. Initially, the interrupt is generated every 25  $\mu$ s and the current value of the state variable is compared with the previous one. When a “mark” to “space” transition of the state variable is detected (equivalent to the Start bit), the demodulation process starts. The sampling rate is changed to match the one used during the modulation process but not before introducing an additional time offset to ensure correct data interpretation.

The periodic interrupt is now generated once every 1 ms and the data byte is reconstructed bit by bit, according to the state variable. Once the data byte is successfully reconstructed and the value of the state variable indicates a “mark” (equivalent to the Stop bit), the sampling rate is set back to 25  $\mu$ s and the demodulated data byte is displayed in the serial terminal with the help of the USART peripheral.

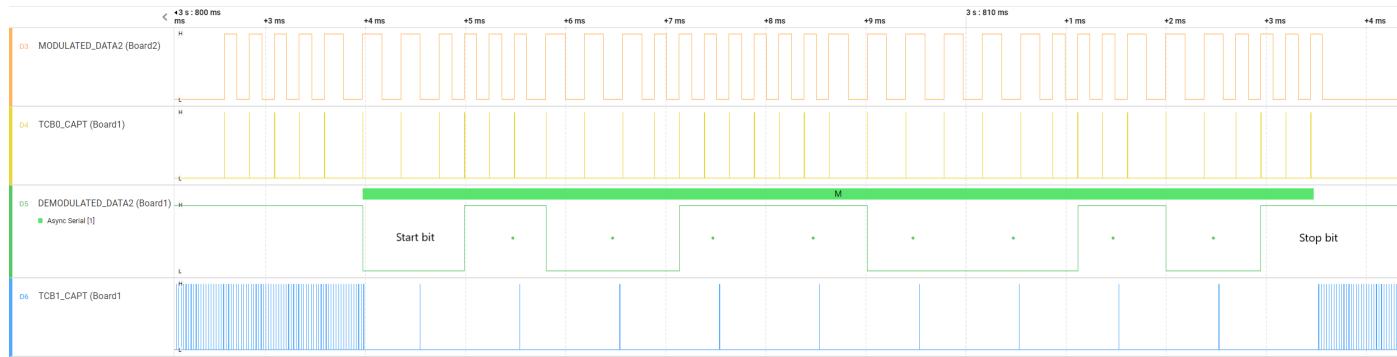
**Figure 3-2.** TCB Periodic Interrupt Generation



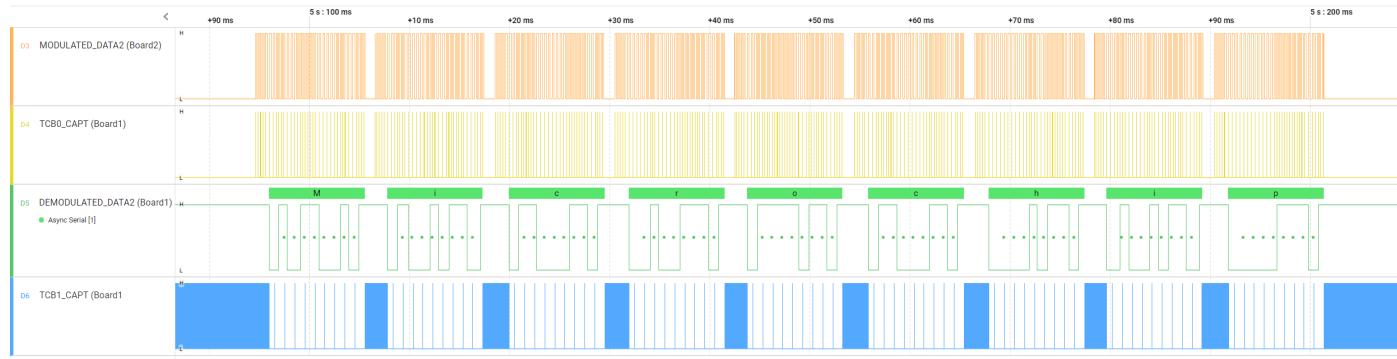
**Figure 3-3. Demodulation Process Diagram**



**Figure 3-4. Demodulation of a Single Data Byte**



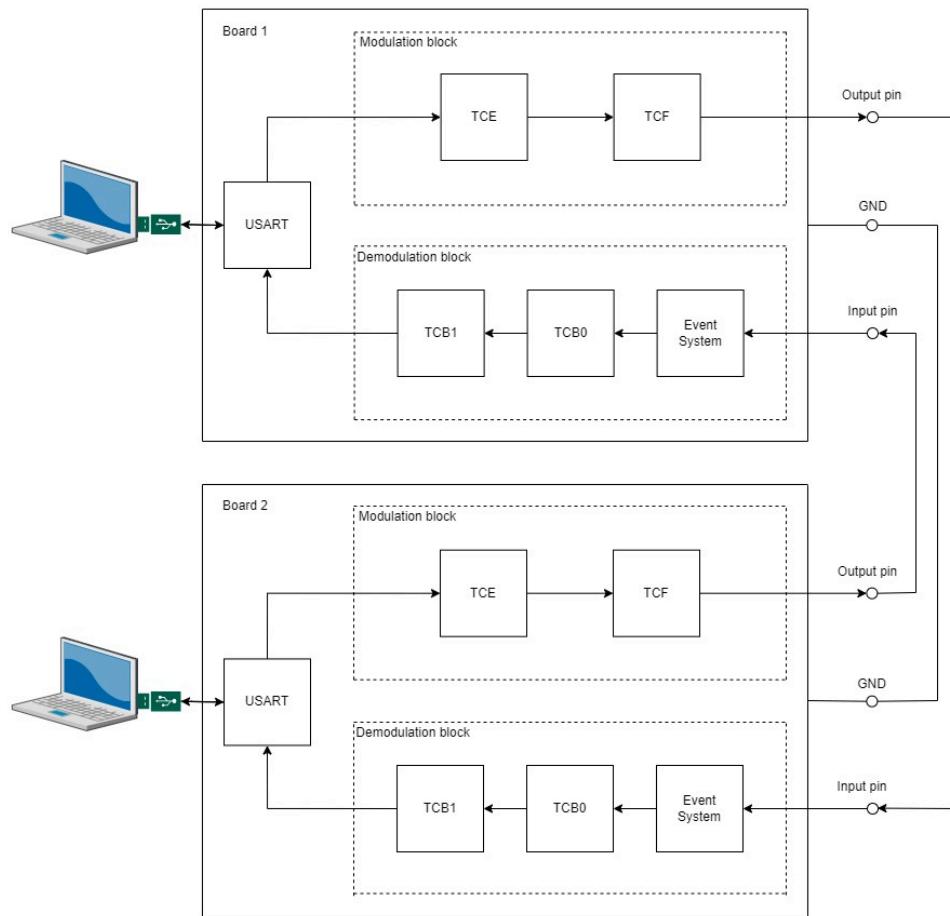
**Figure 3-5. Demodulation of Multiple Data Bytes**



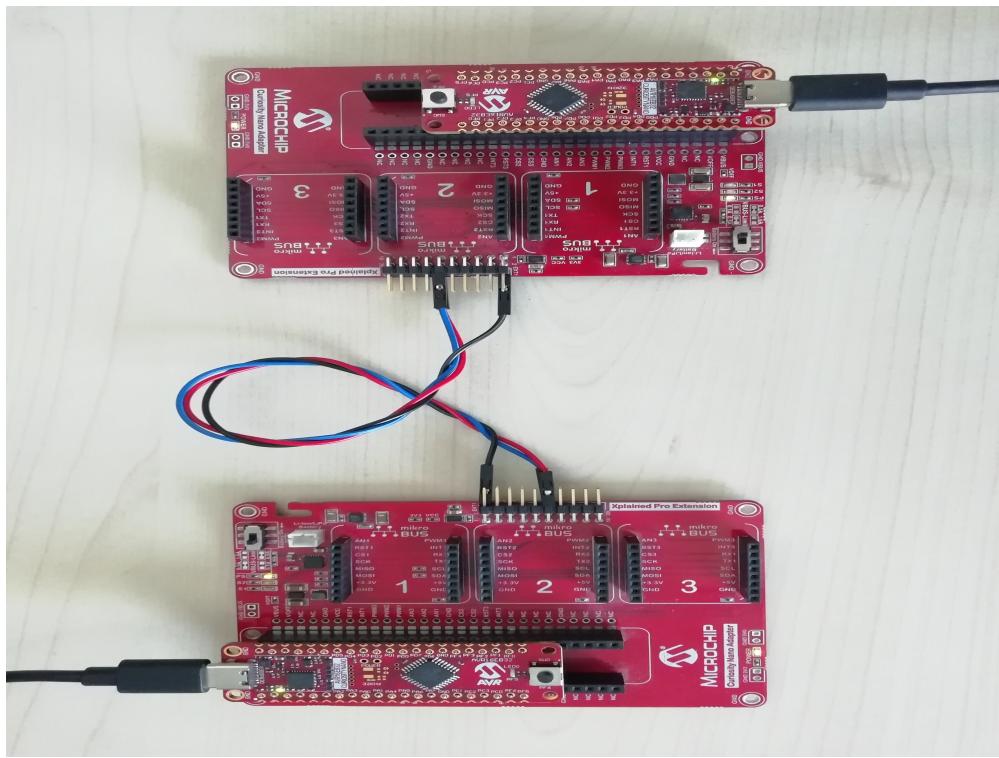
## 4. Results

The developed code example implements a full duplex communication between two AVR16EB32 CNANO boards using the previously described FSK modulation and demodulation techniques. If the two CNANO boards are connected to the same laptop/PC the communication between them uses only two wires. If each CNANO board is connected to a different PC, an additional wire for the ground is needed. The I/O1 Xplained Pro Extension header on the CNANO Base connects the two boards.

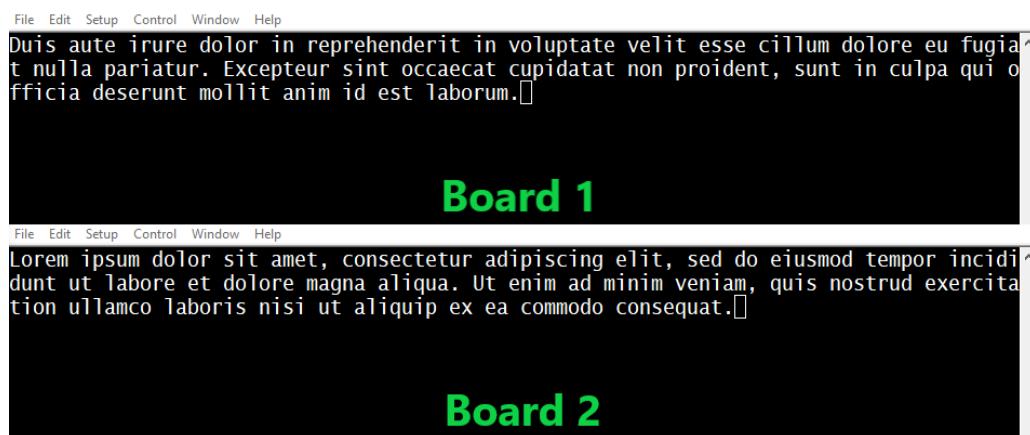
**Figure 4-1.** Block Diagram



**Figure 4-2.** Hardware Setup

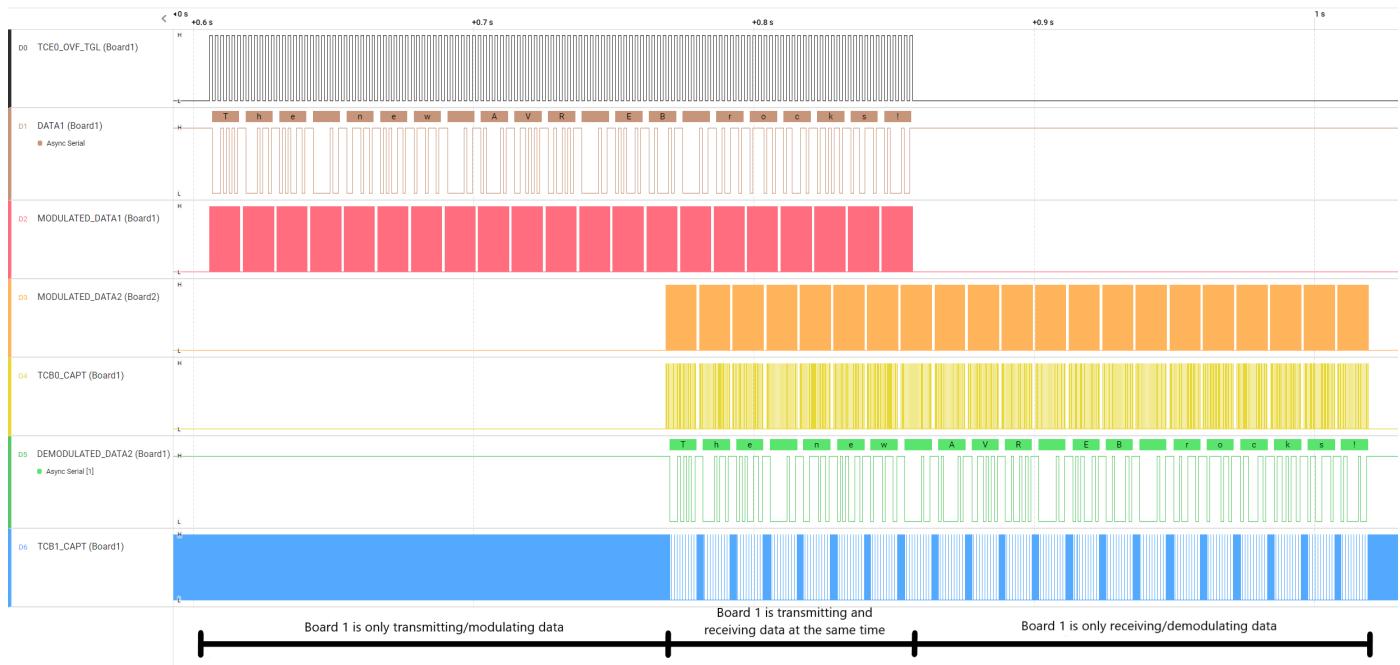


**Figure 4-3.** Serial Terminal Windows

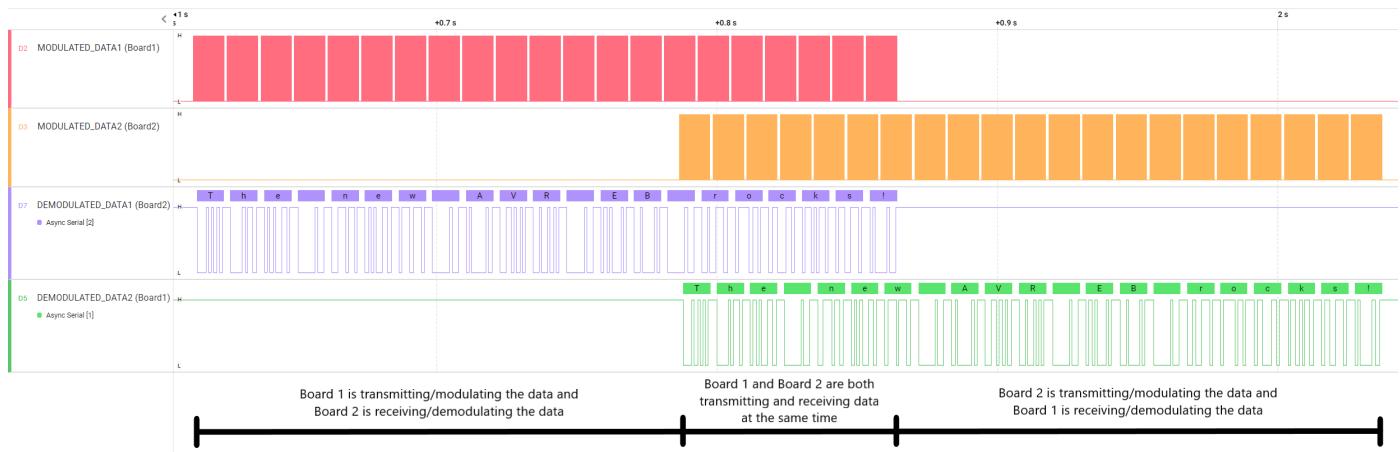


The communication between the two CNANO boards is illustrated in Figure 4-3<sup>Figure 4-3</sup>. The boards are connected to the same laptop/PC. The low-side window displays the text typed in the top-side window and vice versa.

**Figure 4-4. Modulation and Demodulation Processes Taking Place at the Same Time on a CNANO Board**



**Figure 4-5. Modulation and Demodulation Processes Taking Place at the Same Time on both CNANO Boards**



## 5. References

- ["AVR16EB14/20/28/32 Preliminary Data Sheet"](#) (DS40002522). Microchip Technology Inc.
- ["AVR16EB32 Curiosity Nano Pinout"](#). Microchip Technology Inc.
- ["Curiosity Nano Base for Click boards™ Hardware User Guide"](#) (DS50002839). Microchip Technology Inc.
- ["MPLAB® Code Configurator v3.xx User's Guide"](#) (DS40001829). Microchip Technology, Inc.
- [AVR16EB32 Curiosity Nano Evaluation Kit](#)

## 6. Revision History

Document Revision	Date	Comments
A	02/2024	Initial document release

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