

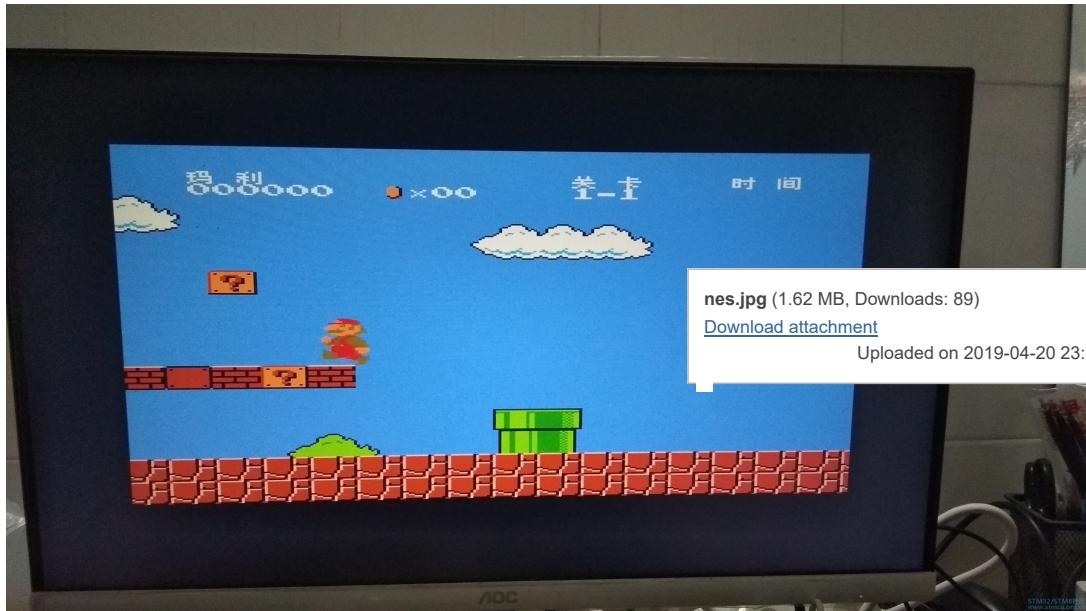


Published on 2019-04-21 00:30:50 | OP Direct elevator access



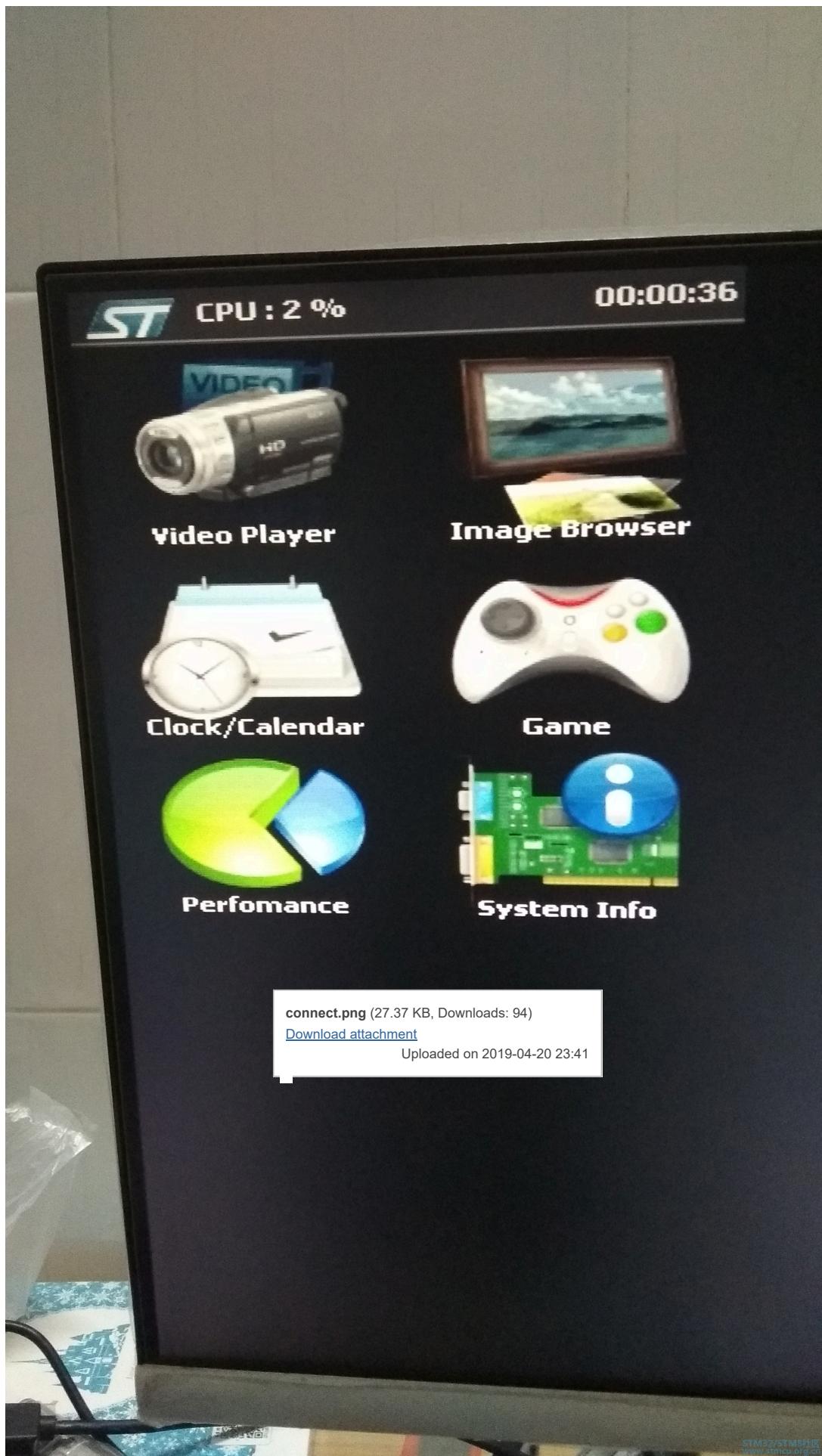
Here's a screenshot first.

The NES emulator, using code from Atomic, runs very smoothly (for USB overclocking to 192MHz). PS: The emulator from the forum is unwatchable, even overclocked to 260MHz.



This is a demo of the STM32F4Disco. It's overclocked to 800x600@60Hz, but 180MHz is too high. This configuration pushes it to 260MHz.



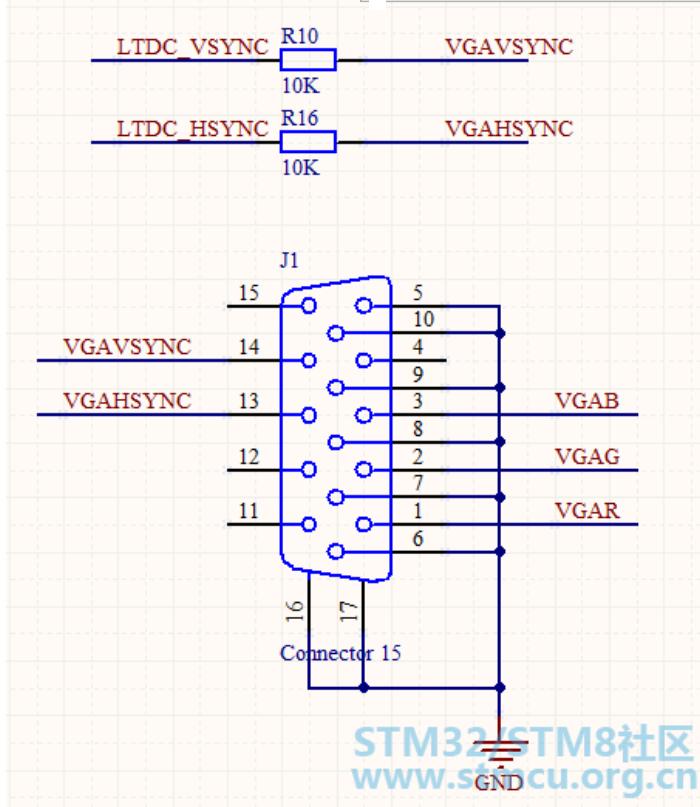


I was originally going to talk about the history, but I think I'll skip the preamble.

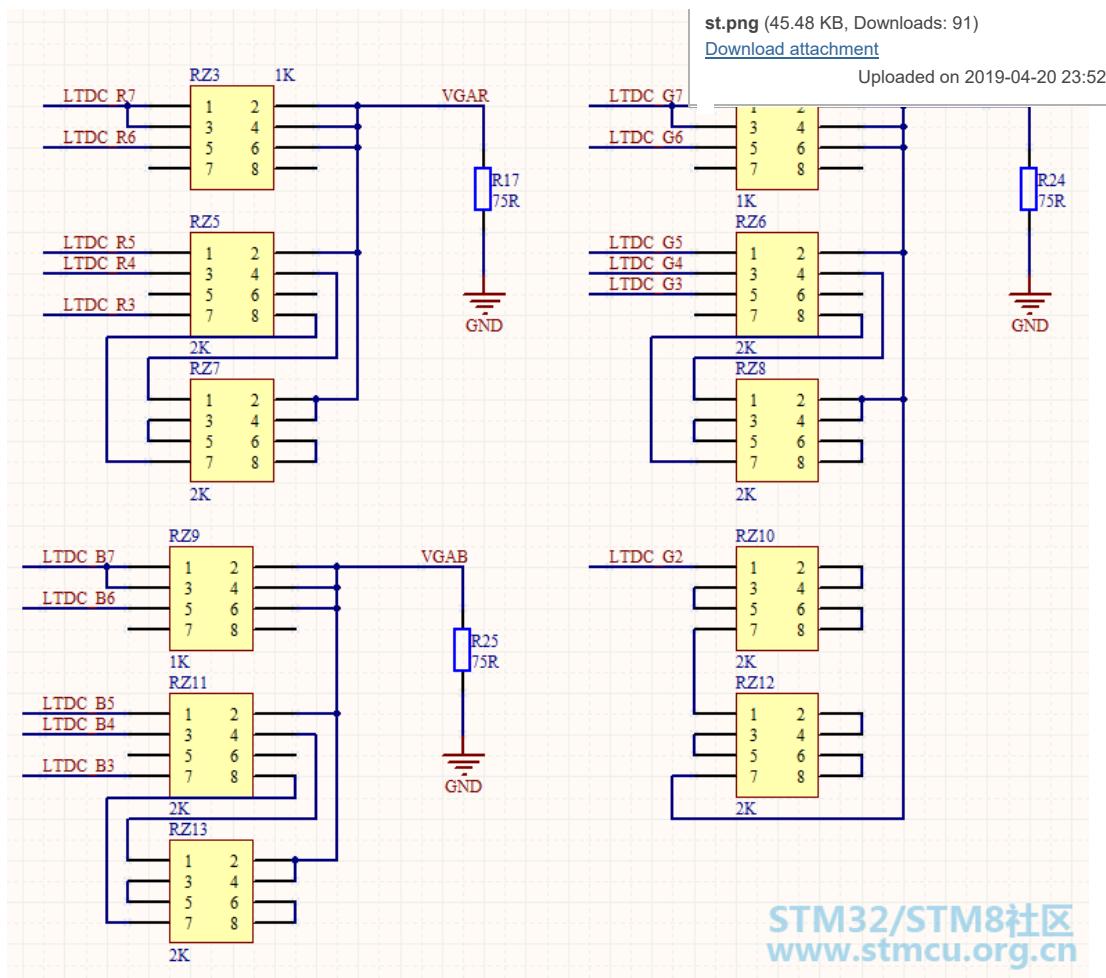
The horizontal and vertical sync of the LTDC interface corresponds to the horizontal and vertical sync of VGA, and the data is connected to the VGA data pins via a resistor **netv**

In the diagram, R10 and R16 should

dat.png (49 KB, Downloads: 83)
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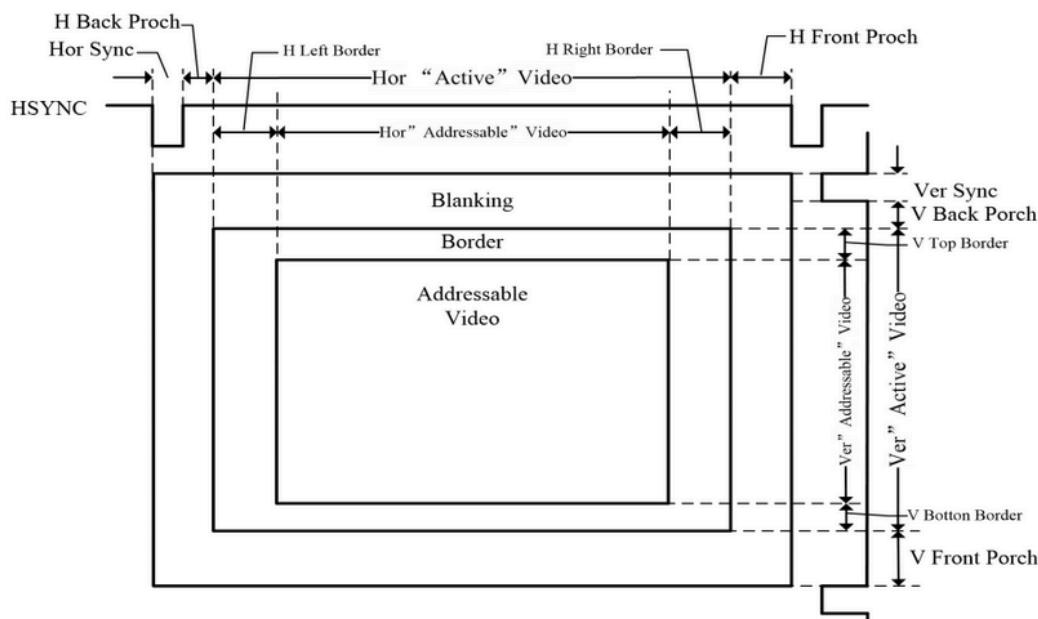


VGA.png (98.54 KB, Downloads: 85)
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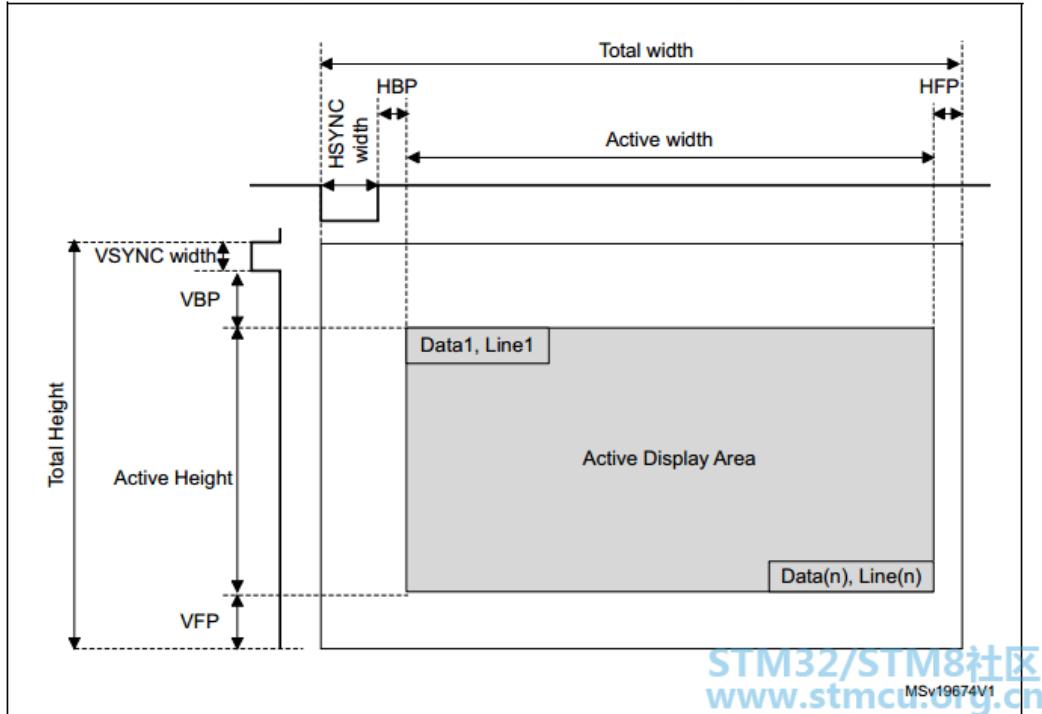


The VGA resistor network won't be discussed here; we'll only cover how to configure the VGA timings on the STM32.

The left side shows the VGA configuration, and the right side shows the RM documentation. The diagrams are the same, meaning that if the LTDC parameters are correct, the VGA will function correctly.



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Figure 82. LCD-TFT Synchronous timings

You can find the parameters required for VGA at <http://www.tinyvga.com/vga-timing>. The demo above is configured for 800x600@60Hz.

The required parameters are Pixel frequency and the two tables below. If you've read the RM documentation's LTDC section, you'll find the corresponding parameters there as well.

QQ screenshot 20190421001328.png (198.22

KB, Downloads: 77)

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SVGA Signal 800 x 600 @ 60 Hz timing

General timing

| | |
|---------------------|---------------------|
| Screen refresh rate | 60 Hz |
| Vertical refresh | 37.878787878788 kHz |
| Pixel freq. | 40.0 MHz |

Horizontal timing (line)

Polarity of horizontal sync pulse is positive.

| Scanline part | Pixels | Time [μs] |
|---------------|--------|-----------|
| Visible area | 800 | 20 |
| Front porch | 40 | 1 |
| Sync pulse | 128 | 3.2 |
| Back porch | 88 | 2.2 |
| Whole line | 1056 | 26.4 |

Vertical timing (frame)

Polarity of vertical sync pulse is positive.

| Frame part | Lines | Time [ms] |
|--------------|-------|-----------|
| Visible area | 600 | 15.84 |
| Front porch | 1 | 0.0264 |
| Sync pulse | 4 | 0.1056 |
| Back porch | 23 | 0.6072 |
| Whole frame | 628 | 16.5792 |

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Below is my configuration section. The parts in red are what need to be configured.

```
*****
*****
```

```
/* LTDC Configuration
*****
*/
/* Polarity configuration */
/* Initialize the horizontal synchronization polarity as active low */
LTDC_InitStruct.LTDC_HSPolarity = LTDC_HSPolarity_AH; // The
online diagram shows active low, but the monitors I've tested show
active high?
/* Initialize the vertical synchronization polarity as active low */
LTDC_InitStruct.LTDC_VSPolarity = LTDC_VSPolarity_AH; // The
online diagram shows active low, but the monitors I've tested show
active high?
/* Initialize the data enable polarity as active low */
LTDC_InitStruct.LTDC_DEPolarity = LTDC_DEPolarity_AL;
/* Initialize the pixel clock polarity as input pixel clock */
LTDC_InitStruct.LTDC_PCPolarity = LTDC_PCPolarity_IPC;

/* Configure R,G,B component values for LCD background color */

LTDC_InitStruct.LTDC_BackgroundRedValue = 0;
LTDC_InitStruct.LTDC_BackgroundGreenValue = 0;
LTDC_InitStruct.LTDC_BackgroundBlueValue = 0;
```

[PCB.jpg](#) (1.75 MB, Downloads: 89)

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```
/* Configure PLLSAI prescalers for LCD */
/* Enable Pixel Clock */
/* PLLSAI_VCO Input = HSE_VALUE/PLL_M = 1 Mhz */
/* PLLSAI_VCO Output = PLLSAI_VCO Input * PLLSAI_N = 192 Mhz
*/
/* PLLCDCLK = PLLSAI_VCO Output/PLLSAI_R = 192/4 = 48 Mhz
*/
/* LTDC clock frequency = PLLCDCLK / RCC_PLLSAIDivR = 48/8 =
6 Mhz */
RCC_PLLSAIConfig(160, 7, 2); // I am a 12M crystal oscillator
PLL_M=6
RCC_LTDCCLKDivConfig(RCC_PLLSAIDivR_Div4);

/* Enable PLLSAI Clock */
RCC_PLLSAICmd(ENABLE);
/* Wait for PLLSAI activation */
while(RCC_GetFlagStatus(RCC_FLAG_PLLSAIRDY) == RESET)
{
}

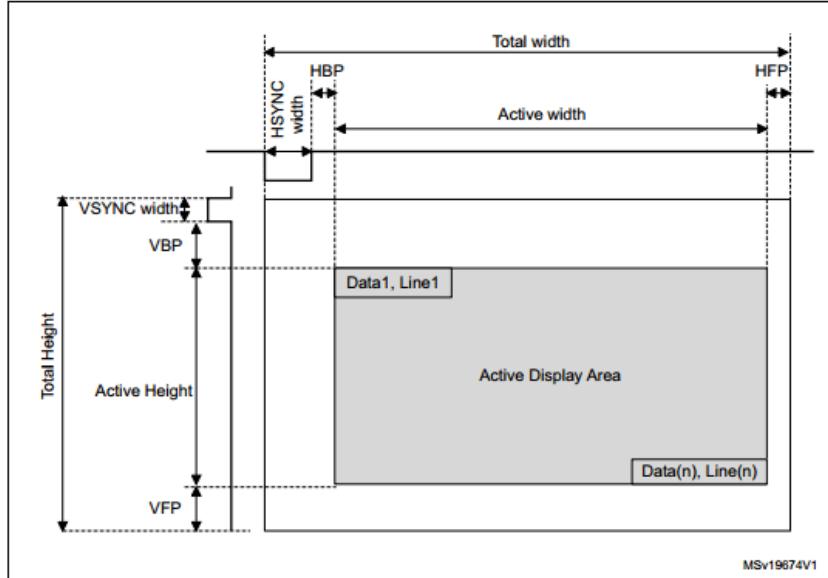
/* Timing configuration */
/* Configure horizontal synchronization width */
LTDC_InitStruct.LTDC_HorizontalSync = 127;
/* Configure vertical synchronization height */
LTDC_InitStruct.LTDC_VerticalSync = 3;
/* Configure accumulated horizontal back porch */
LTDC_InitStruct.LTDC_AccumulatedHBP = 215;
/* Configure accumulated vertical back porch */
LTDC_InitStruct.LTDC_AccumulatedVBP = 26;
/* Configure accumulated active width */
LTDC_InitStruct.LTDC_AccumulatedActiveW = 1015;
/* Configure accumulated active height */
LTDC_InitStruct.LTDC_AccumulatedActiveH = 626;
/* Configure total width */
LTDC_InitStruct.LTDC_TotalWidth = 1055;
/* Configure total height */
LTDC_InitStruct.LTDC_TotalHeight = 627;
```

For information on LTDC_Init(<DC_InitStruct>);
synchronizing the leading and trailing edges, please refer to page 483
of the RM documentation, which is shown in the screenshot below.

RM0090

LCD-TFT Controller (LTDC)

Figure 82. LCD-TFT Synchronous timings



Note: The HBP and HFP are respectively the Horizontal back porch and front porch period.

The VBP and the VFP are respectively the Vertical back porch and front porch period.

The LCD-TFT programmable synchronous timings are:

- HSYNC and VSYNC Width: Horizontal and Vertical Synchronization width configured by programming a value of **HSYNC Width - 1** and **VSYNC Width - 1** in the **LTDC_SSCR** register.
- HBP and VBP: Horizontal and Vertical Synchronization back porch width configured by programming the accumulated value **HSYNC Width + HBP - 1** and the accumulated value **VSYNC Width + VBP - 1** in the **LTDC_BPCR** register.
- Active Width and Active Height: The Active Width and Active Height are configured by programming the accumulated value **HSYNC Width + HBP + Active Width - 1** and the accumulated value **VSYNC Width + VBP + Active Height - 1** in the **LTDC_AWCR** register (only up to 1024x768 is supported).
- Total Width: The Total width is configured by programming the accumulated value **HSYNC Width + HBP + Active Width + HFP - 1** in the **LTDC_TWCR** register. The HFP is the Horizontal front porch period.
- Total Height: The Total Height is configured by programming the accumulated value **VSYNC Height + VBP + Active Height + VFP - 1** in the **LTDC_TWCR** register. The VFP is the Vertical front porch period.

Note: When the LTDC is enabled, the timings generated start with X/Y=0/0 position as the first horizontal synchronization pixel in the vertical synchronization area and following the back porch, active data display area and the front porch.

The pixel frequency error should be minimized; the simplest way is to configure it using a cube, without worrying about the calculation method.

Finally, here's a nice picture of the board.

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