ECE 485/585
Microprocessor System Design

Final Term Project

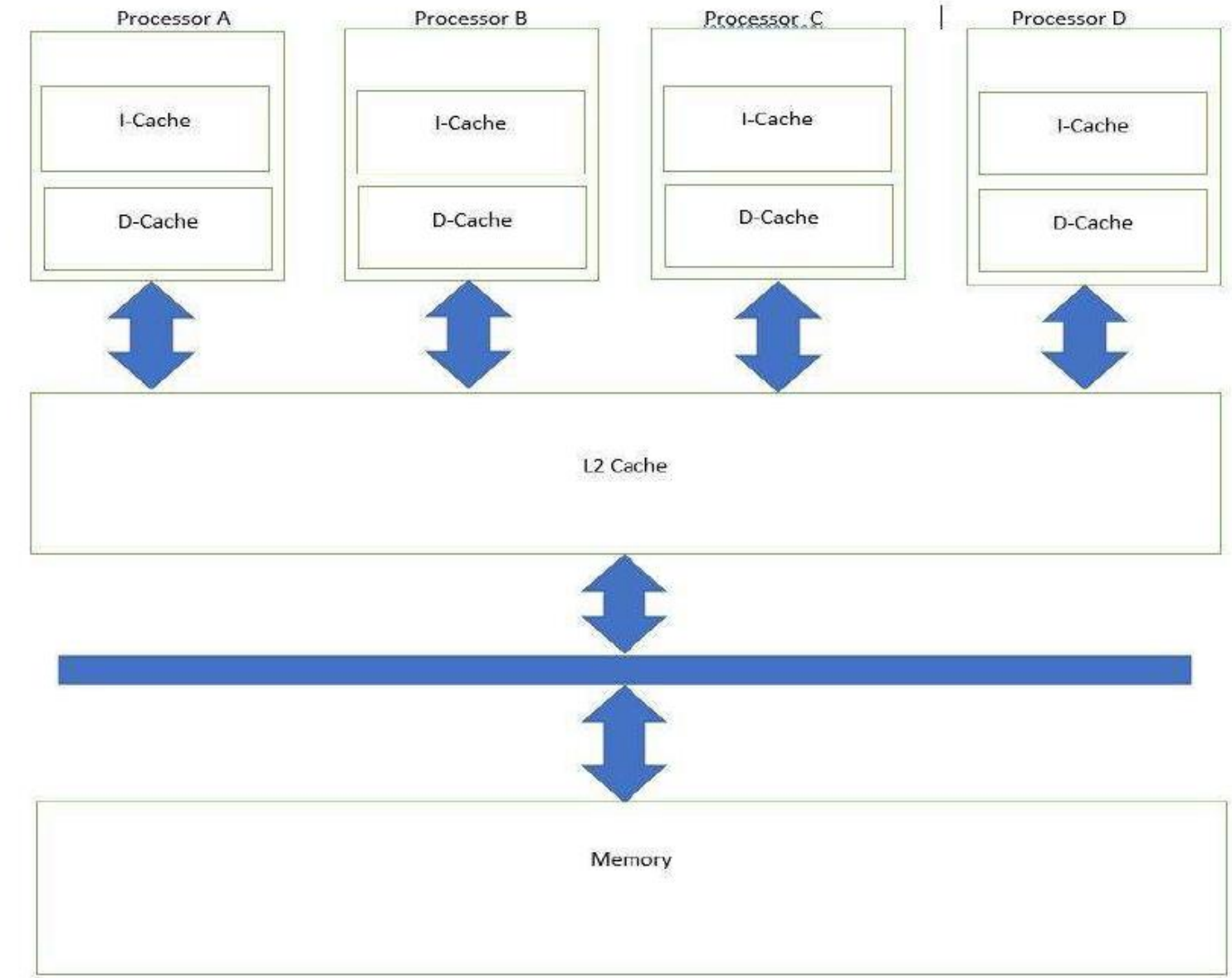
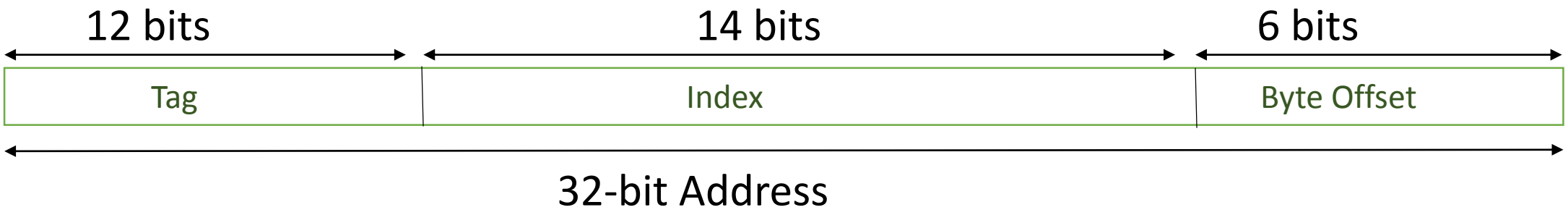


Figure 1: Block diagram

Split Cache

Specs:

- 8-way Set Associative Data Cache and 4-way Set Associative Instruction Cache
- 16K sets (14 bits for index)
- 64-byte Cache line (6 bits for byte offset)



Trace File Format

n address

Where n is

0	read data request to L1 data cache
1	write data request to L1 data cache
2	instruction fetch (a read request to L1 instruction cache)
3	invalidate command from L2
4	data request from L2 (in response to snoop)
8	clear the cache and reset all state (and statistics)
9	print contents and state of the cache (allow subsequent trace activity)

Trace File Example

Two scenarios have been explained in the following document

“Final_Project_Explanation.pdf”

The two scenarios are explained for the 8-way set Associative D-Cache to cover all the MESI states. LRU algorithm is used for eviction strategy which is also explained in the document.