实验五 Cache设计

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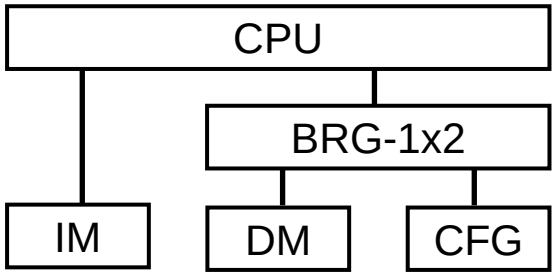
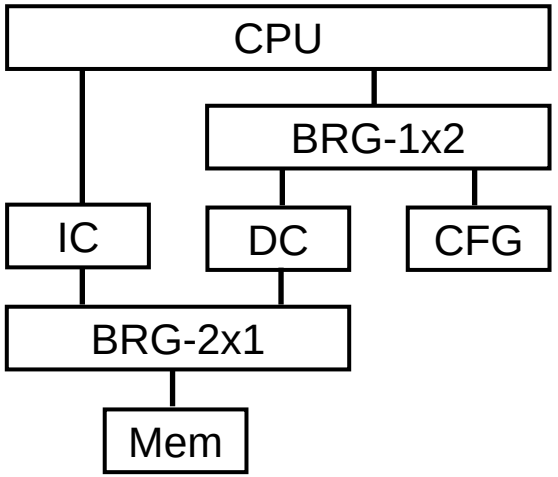
实验目标

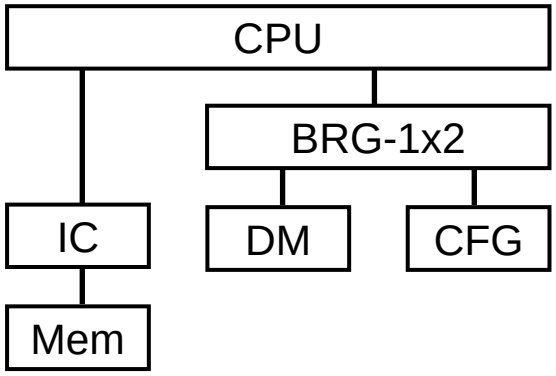
- **掌握Cache工作原理、基本结构、设计和调试方法**
- **熟练掌握数据通路和控制器的设计和描述方法**

实验内容

- **改造流水线LA32R CPU，增加指令cache**



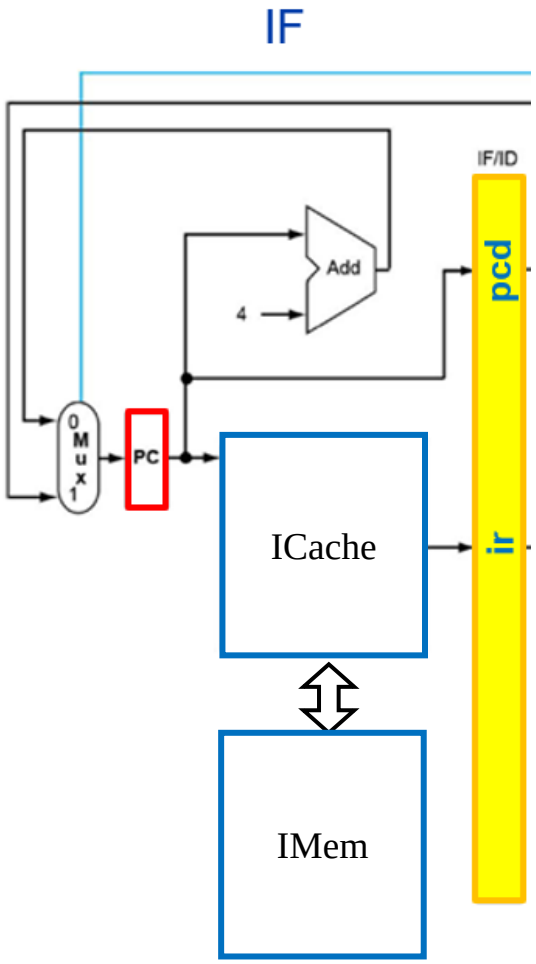




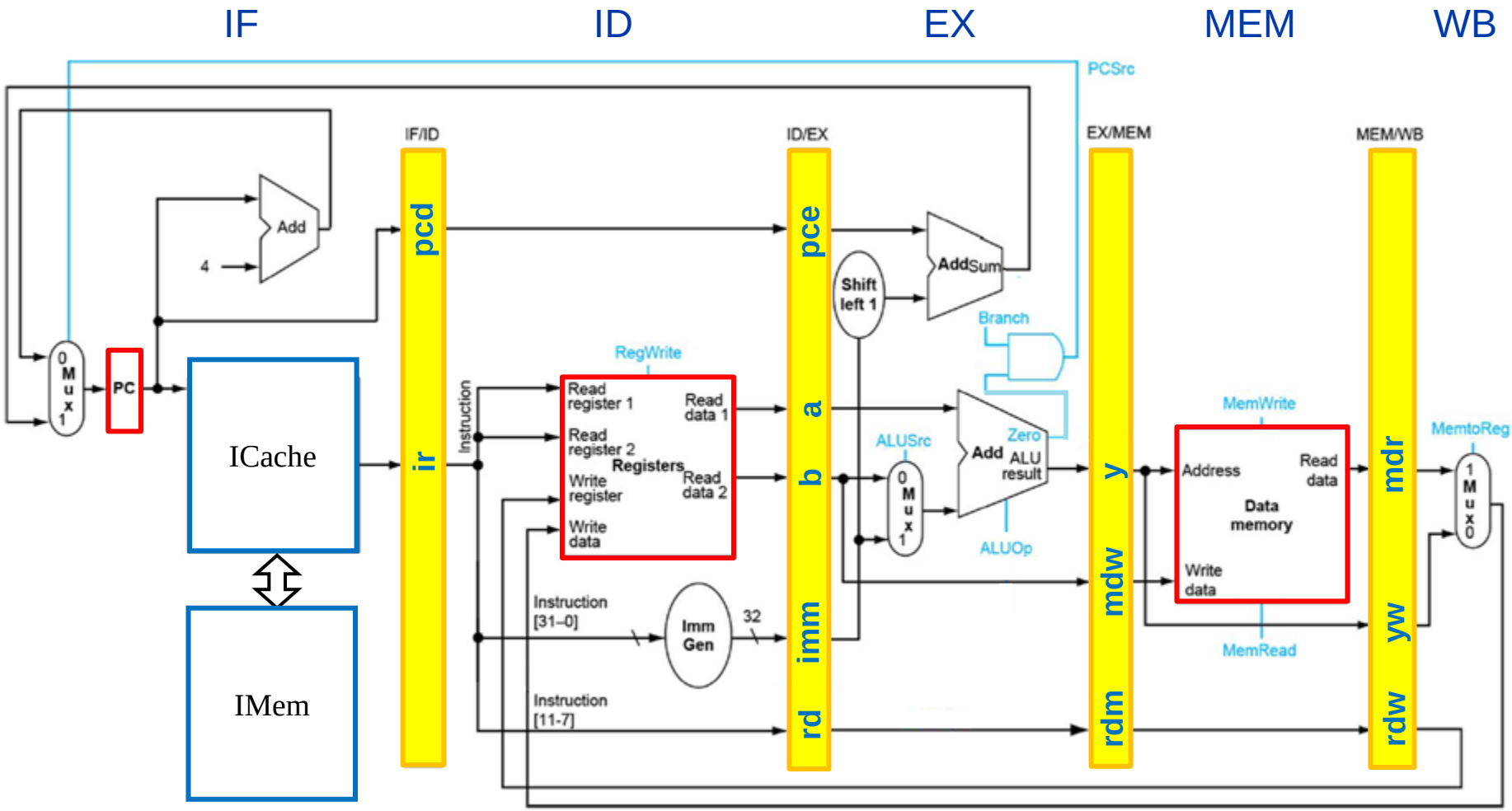
- IC：指令Cache
- DC：数据Cache
- BRG-2x1：仲裁桥

实验内容 (续)

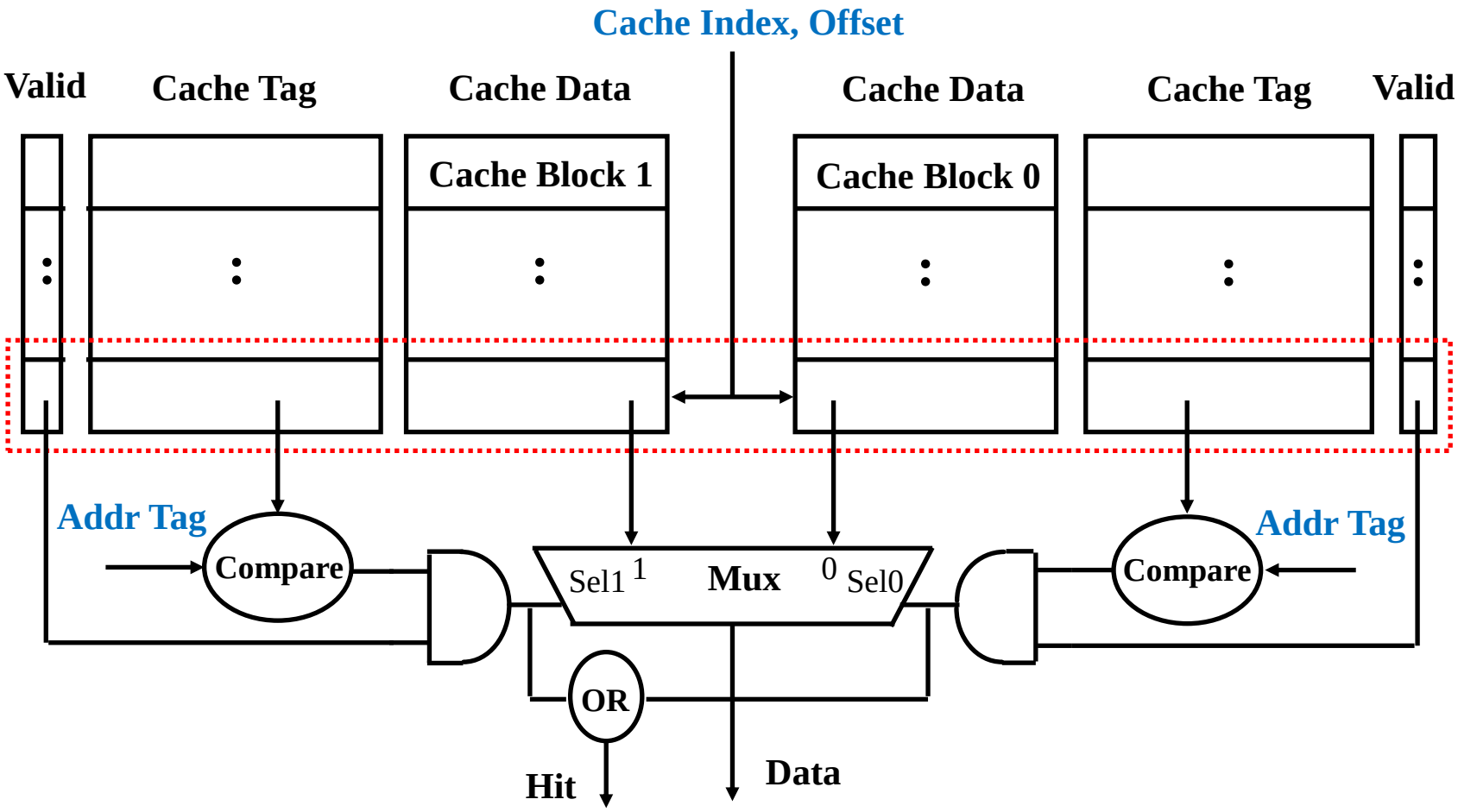
- **指令Cache (ICache) 配置**
  - 容量8KB，块式存储器
  - 块大小：1字（4字节）
  - 地址映射方式：2路组相联
  - 替换策略：LRU
- **指令存储器 (Imem) 配置**
  - 容量1MB，块式存储器
  - 按字访问，读取时间固定为4个时钟周期



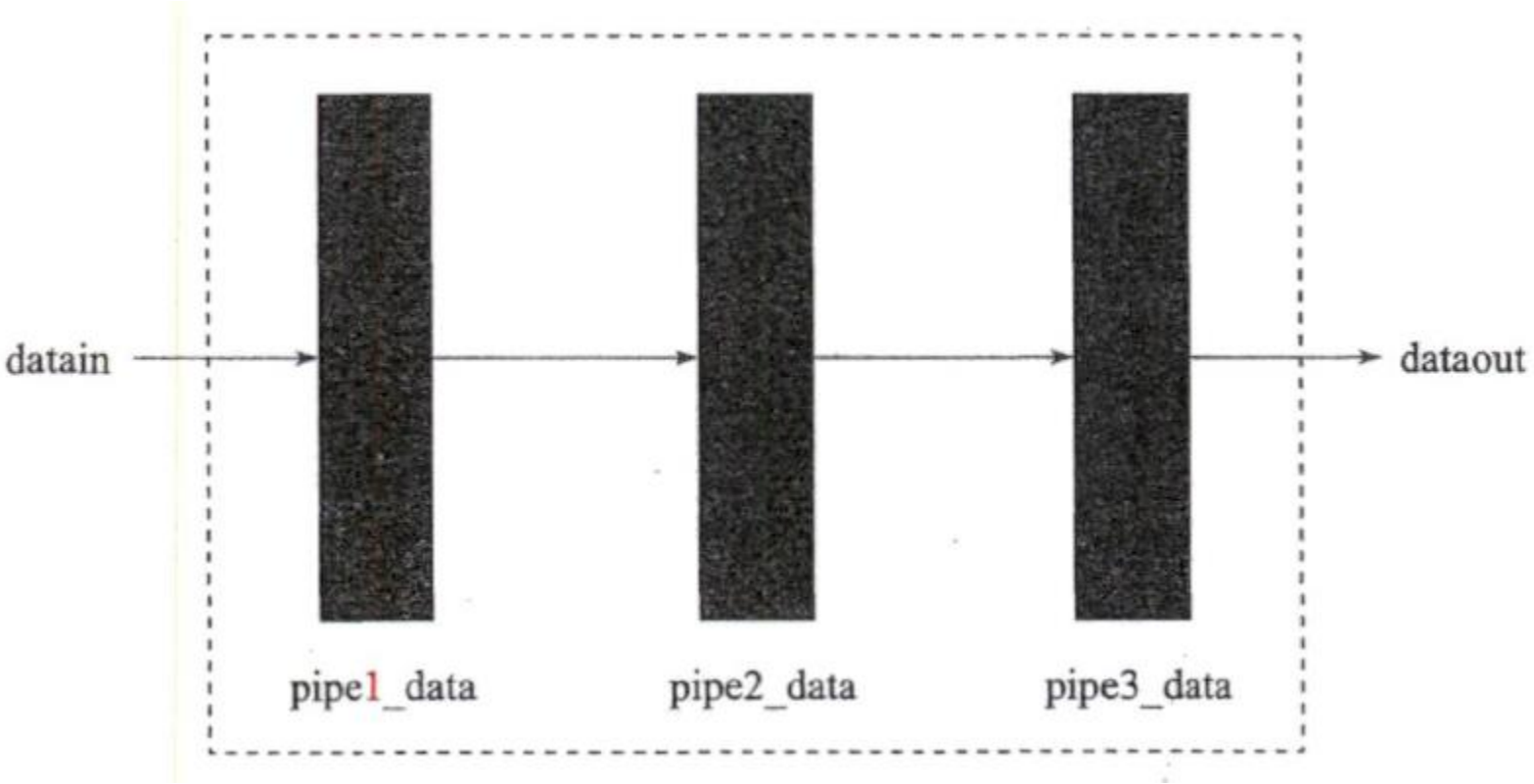
流水线CPU数据通路


IF
ID
EX
MEM
WB
PCSrc
IF/ID
ID/EX
EX/MEM
MEM/WB
Add
4
M u x
0
1
PC
ICache
IMem
pcd
ir
Instruction
RegWrite
Read register 1
Read register 2
Registers
Write register
Write data
Read data 1
Read data 2
pce
a
b
imm
rd
Shift left 1
AddSum
Branch
ALUSrc
Add
Zero
ALU result
ALUOp
Instruction [31–0]
Imm Gen
32
Instruction [11-7]
y
mdw
rdm
MemWrite
Address
Read data
Data memory
Write data
MemRead
mdr
yw
rdw
MemtoReg

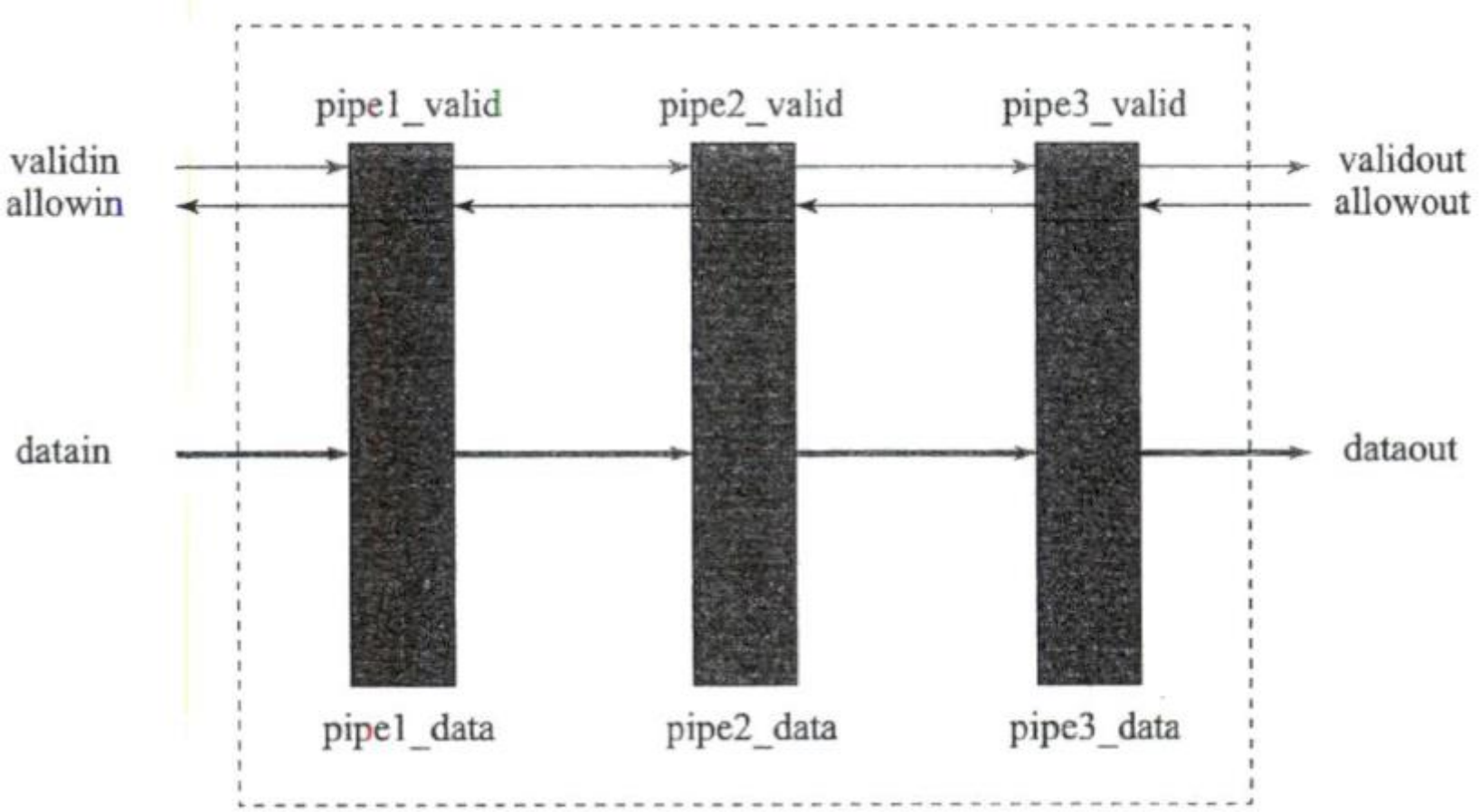
Cache组相联映射


Cache Index, Offset
Valid
Cache Tag
Cache Data
Cache Data
Cache Tag
Valid
Cache Block 1
Cache Block 0
Addr Tag
Compare
Sel1
1
Mux
0
Sel0
Compare
Addr Tag
OR
Hit
Data

无阻塞流水线结构



有阻塞流水线结构


pipe1_valid
pipe2_valid
pipe3_valid
validin
allowin
validout
allowout
datain
dataout
pipe1_data
pipe2_data
pipe3_data

流水线之间交互

```
reg             pipe1_valid;
reg [WIDTH-1:0] pipe1_data;

//pipeline stage1
wire            pipe1_allowin;
wire            pipe1_ready_go;
wire            pipe1_to_pipe2_valid;
assign pipe1_ready_go = ……
assign pipe1_allowin = !pipe1_valid || pipe1_ready_go && pipe2_allowin;
assign pipe1_to_pipe2_valid = pipe1_valid && pipe1_ready_go;
always @(posedge clk) begin
    if (rst) begin
        pipe1_valid <= 1'b0;
    end
    else if (pipe1_allowin) begin
        pipe1_valid <= validin;
    end
    if (validin && pipe1_allowin) begin
        pipe1_data <= datain;
    end
end
```

实验要求

- **设计包含指令Cache的流水线LA32R CPU，构建SoC并上板验证**
  - 运行指令测试程序
  - 查看电路资源和性能

The End