
Section 32. Configuration

HIGHLIGHTS

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32.1 INTRODUCTION

A PIC32MX family device includes several nonvolatile (programmable) Configuration Words that define the device's behavior.

Device Configuration features may vary according to PIC32MX family variants; however, the following configuration features are common:

- System Clock Oscillator mode and Phase-Locked Loop (PLL)
- Secondary oscillator (SOSC) enable/disable
- Watchdog Timer (WDT) enable/disable and postscaler
- Boot Flash and Program Flash write-protect regions
- User ID
- Debug mode

The PIC32MX Configuration Words are located in Boot Flash memory and are programmed when the PIC32MX Boot Flash region is programmed.

System clock oscillator and PLL bits provide a large selection of flexible clock source options and PLL prescalers/postscalers.

The secondary oscillator bit enables or disables a low-power secondary oscillator that can serve as a clock source for several peripherals, such as RTCC, Timer1 and CPU.

WDT and postscaler bits allow the user to permanently disable or enable the Watchdog timer. When enabled, a postscaler can be selected to provide a wide range of Watchdog Time-out periods. A Windowed mode Watchdog feature is also available.

Boot Flash and Program Flash write-protected bits provide write protection to all of Boot Flash memory and selected regions of Program Flash memory.

User ID bits are available for programming application-specific or product-specific identification information, such as product ID or serial numbers.

Debug mode bits provide a selection of debugging modes and channels.

32.2 CONFIGURATION WORDS

Following are the device Configuration Words:

- DEVCFGx: Device Configuration Words
- DEVID: Device ID

The following table summarizes the device Configuration Words. Corresponding Configuration Words appear after the summary, followed by a detailed description of each Configuration Word.

Note: Not all Configuration bits are present on all PIC32MX devices. Refer to the specific device data sheet for availability.

Table 32-1: Configuration Word Summary

Name	Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
DEVCFG3	31:24	FVBUSIO	FUSBIDIO	FSCM1IO	—	—	FCANIO	FETHIO	FMIEN
	23:16	—	—	—	—	—	FSRSSEL<2:0>		
	15:8	USERID<15:0>							
	7:0								
DEVCFG2	31:24	—	—	—	—	—	—	—	—
	23:16	—	—	—	—	—	FPLLODIV<2:0>		
	15:8	FUPLLEN	—	—	—	—	FUPLLDIV<2:0>		
	7:0	—	FPLLMULT<2:0>			—	FPLLDIV<2:0>		
DEVCFG1	31:24	—	—	—	—	—	—	—	—
	23:16	FWDTEN	WINDIS	—	WDTPS<4:0>				
	15:8	FCKSM<1:0>		FPBDIV<1:0>		—	OSCIOFNC	POSCMD<1:0>	
	7:0	IESO	—	FSOSCEN	—	—	FNOSC<2:0>		
DEVCFG0	31:24	SIGN	—	—	CP	—	—	—	BWP
	23:16	—	—	—	—	PWP<19:16>			
	15:8	PWP<15:12>				—	—	—	—
	7:0	—	—	—	—	ICESEL	—	DEBUG<1:0>	
DEVID	31:24	VER<11:4>							
	23:16	VER<3:0>				DEV<7:4>			
	15:8	DEV<3:0>				MANID<11:8>			
	7:0	MANID<7:0>							

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Register 32-1: DEVCFG0: Device Configuration Word 0

R/P-1	r-1	r-1	R/P-1	r-1	r-1	r-1	R/P-1
SIGN	—	—	CP	—	—	—	BWP
bit 31							bit 24

r-1	r-1	r-1	r-1	R/P-1	R/P-1	R/P-1	R/P-1
—	—	—	—	PWP<19:16>			
bit 23							bit 16

R/P-1	R/P-1	R/P-1	R/P-1	r-1	r-1	r-1	r-1
PWP<15:12>				—	—	—	—
bit 15							bit 8

r-1	r-1	r-1	r-1	R/P-1	r-1	R/P-1	R/P-1
—	—	—	—	ICESEL	—	DEBUG<1:0>	
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit P = Programmable bit r = Reserved bit
U = Unimplemented bit -n = Default unprogrammed bit value: ('0', '1', x = Unknown)

- bit 31 **SIGN:** Signature bit
This bit is automatically programmed to '0' following a bulk erase of the corresponding memory area. This bit is the Flash data signature value (it assures that at least one bit within the Configuration Word is a '0').
- bit 30-29 **Reserved:** Write '1'; ignore read
- bit 28 **CP:** Code-Protect bit
Prevents Boot and Program Flash memory from being read or modified by an external programming device.
1 = Protection disabled
0 = Protection enabled
Refer to **Section 32.3.2 “Device Code Protection”** for more information.
- bit 27-25 **Reserved:** Write '1'; ignore read
- bit 24 **BWP:** Boot Flash Write-Protect bit
Prevents Boot Flash memory from being modified during code execution.
1 = Boot Flash is writable
0 = Boot Flash is not writable
Refer to **Section 32.3.3 “Program Write Protection (PWP)”** for more information.
- bit 23-20 **Reserved:** Write '1'; ignore read
- bit 19-12 **PWP<19:12>:** Program Flash Write-Protect bits
Prevents selected Program Flash memory blocks from being modified during code execution. These bits represent the one's complement of write-protected Program Flash memory region.
Refer to **Section 32.3.3 “Program Write Protection (PWP)”**
- bit 11-4 **Reserved:** Write '1'; ignore read
- bit 3 **ICESEL:** In-Circuit Emulator/Debugger Communication Channel Select bit
1 = In-Circuit Emulator used EMUC2/EMUD2 pins; In-Circuit Debugger used PGC2/PGD2 pins
0 = In-Circuit Emulator used EMUC1/EMUD1 pins; In-Circuit Debugger used PGC1/PGD1 pins

Register 32-1: DEVCFG0: Device Configuration Word 0 (Continued)

bit 2 **Reserved:** Write '1'; ignore read

bit 1-0 **DEBUG<1:0>:** Background Debugger Enable bits (forced to '11' if code-protect is enabled)

11 = Debugger is disabled

10 = Debugger is enabled

01 = Reserved (same as '11' setting)

00 = Reserved (same as '11' setting)

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Register 32-2: DEVMCFG1: Device Configuration Word 1

r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
—	—	—	—	—	—	—	—
bit 31				bit 24			

R/P-1	R/P-1	r-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
FWDTEN	WINDIS	—	WDTPS<4:0>				
bit 23				bit 16			

R/P-1	R/P-1	R/P-1	R/P-1	r-1	R/P-1	R/P-1	R/P-1
FCKSM<1:0>		FPBDIV<1:0>		—	OSCIOFNC	POSCMD<1:0>	
bit 15				bit 8			

R/P-1	r-1	R/P-1	r-1	r-1	R/P-1	R/P-1	R/P-1
IESO	—	FSOSCEN	—	—	FNOSC<2:0>		
bit 7				bit 0			

Legend:

R = Readable bit W = Writable bit P = Programmable bit r = Reserved bit
 U = Unimplemented bit -n = Default unprogrammed bit value: ('0', '1', x = Unknown)

bit 31-24 **Reserved:** Write '1'; ignore read

bit 23 **FWDTEN:** WDT Enable bit
 1 = WDT is enabled and cannot be disabled by software
 0 = WDT is not enabled. It can be enabled in software

bit 22 **WINDIS:** Windowed Watchdog Timer Enable bit
 1 = Windowed Watchdog Timer is disabled
 0 = Windowed Watchdog Timer is enabled

bit 21 **Reserved:** Write '1'; ignore read

bit 20-16 **WDTPS<4:0>:** WDT Postscale Select bits

10100 = 1:1048576
 10011 = 1:524288
 10010 = 1:262144
 10001 = 1:131072
 10000 = 1:65536
 01111 = 1:32768
 01110 = 1:16384
 01101 = 1:8192
 01100 = 1:4096
 01011 = 1:2048
 01010 = 1:1024
 01001 = 1:512
 01000 = 1:256
 00111 = 1:128
 00110 = 1:64
 00101 = 1:32
 00100 = 1:16
 00011 = 1:8
 00010 = 1:4
 00001 = 1:2
 00000 = 1:1

All other combinations not shown result in operation = 10100

Register 32-2: DEVCFG1: Device Configuration Word 1 (Continued)

bit 15-14	FCKSM<1:0> : Clock Switching and Monitor Selection Configuration bits 1x = Clock switching is disabled, fail-safe clock monitor is disabled 01 = Clock switching is enabled, fail-safe clock monitor is disabled 00 = Clock switching is enabled, fail-safe clock monitor is enabled
bit 13-12	FPBDIV<1:0> : Peripheral Bus Clock Divisor Default Value bits 11 = PBCLK is SYSCLK divided by 8 10 = PBCLK is SYSCLK divided by 4 01 = PBCLK is SYSCLK divided by 2 00 = PBCLK is SYSCLK divided by 1
bit 11	Reserved : Write '1'; ignore read
bit 10	OSCIOFNC : CLKO Enable Configuration bit 1 = CLKO output signal active on the OSCO pin; primary oscillator must be disabled or configured for the External Clock mode (EC) for the CLKO to be active (POSCMD<1:0> = 11 OR = 00) 0 = CLKO output disabled
bit 9-8	POSCMD<1:0> : Primary Oscillator Configuration bits 11 = Primary oscillator disabled 10 = HS Oscillator mode selected 01 = XT Oscillator mode selected 00 = External Clock mode selected
bit 7	IESO : Internal External Switch Over bit 1 = Internal External Switch Over mode enabled (Two-Speed Start-up enabled) 0 = Internal External Switch Over mode disabled (Two-Speed Start-up disabled)
bit 6	Reserved : Write '1'; ignore read
bit 5	FSOSCEN : Secondary Oscillator Enable bit 1 = Enable Secondary Oscillator 0 = Disable Secondary Oscillator
bit 4-3	Reserved : Write '1'; ignore
bit 2-0	FNOSC<2:0> : Oscillator Selection bits 111 = Fast RC Oscillator with divide-by-N (FRCDIV) 110 = Reserved; do not use 101 = Low-Power RC (LPRC) Oscillator 100 = Secondary Oscillator (SOSC) 011 = Primary Oscillator (Posc) with PLL Module (XT + PLL, HS + PLL, EC + PLL) 010 = Primary Oscillator (XT, HS, EC) 001 = Fast RC Oscillator with divide-by-N with PLL Module (FRCDIV + PLL) 000 = Fast RC (FRC) Oscillator

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Register 32-3: DEVCFG2: Device Configuration Word 2

r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
—	—	—	—	—	—	—	—
bit 31						bit 24	

r-1	r-1	r-1	r-1	r-1	R/P-1	R/P-1	R/P-1
—	—	—	—	—	FPLLODIV<2:0>		
bit 23						bit 16	

R/P-1	r-1	r-1	r-1	r-1	R/P-1	R/P-1	R/P-1
FUPLLEN	—	—	—	—	FUPLLDIV<2:0>		
bit 15						bit 8	

r-1	R/P-1	R/P-1	R/P-1	r-1	R/P-1	R/P-1	R/P-1
—	FPLLMULT<2:0>			—	FPLLDIV<2:0>		
bit 7				bit 0			

Legend:

R = readable bit

W = writable bit

P = programmable

r = reserved bit

U = unimplemented bit, read as '0'

-n = bit value at POR: ('0', '1', x = unknown)

- bit 31-19 **Reserved:** Write '1'; ignore read
- bit 18-16 **FPLLODIV<2:0>:** Default postscaler for PLL
- 111 = PLL output divided by 256
 - 110 = PLL output divided by 64
 - 101 = PLL output divided by 32
 - 100 = PLL output divided by 16
 - 011 = PLL output divided by 8
 - 010 = PLL output divided by 4
 - 001 = PLL output divided by 2
 - 000 = PLL output divided by 1 (default setting)
- bit 15 **FUPLLEN:** USB PLL Enable bit
- 1 = Enable USB PLL
 - 0 = Disable and bypass USB PLL
- bit 14-11 **Reserved:** Write '1'; ignore read
- bit 10-8 **FUPLLDIV<2:0>:** USB PLL Input Divider bits
- 111 = 12x divider
 - 110 = 10x divider
 - 101 = 6x divider
 - 100 = 5x divider
 - 011 = 4x divider
 - 010 = 3x divider
 - 001 = 2x divider
 - 000 = 1x divider
- bit 7 **Reserved:** Write '1'; ignore read

Register 32-3: DEVCFG2: Device Configuration Word 2 (Continued)

bit 6-4 **FPLLMULT<2:0>**: Initial PLL Multiplier Value

111 = 24x Multiplier
110 = 21x Multiplier
101 = 20x Multiplier
100 = 19x Multiplier
011 = 18x Multiplier
010 = 17x Multiplier
001 = 16x Multiplier
000 = 15x Multiplier

bit 3 **Reserved**: Write '1'; ignore read

bit 2-0 **FPLLIDIV<2:0>**: PLL Input Divider Value

111 = Divide by 12
110 = Divide by 10
101 = Divide by 6
100 = Divide by 5
011 = Divide by 4
010 = Divide by 3
001 = Divide by 2
000 = Divide by 1

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Register 32-4: DEVCFG3: Device Configuration Word 3

R/P-1	R/P-1	R/P-1	r-1	r-1	R/P-1	R/P-1	R/P-1
FVBUSIO	FUSBIDIO	FSCM1IO	—	—	FCANIO	FETHIO	FMIEN
bit 31							bit 24

r-1	r-1	r-1	r-1	r-1	R/P-1	R/P-1	R/P-1
—	—	—	—	—	FSRSSEL<2:0>		
bit 23							bit 16

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
USERID<15:8>							
bit 15							bit 8

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
USERID<7:0>							
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit P = Programmable bit r = Reserved bit
U = Unimplemented bit -n = Default unprogrammed bit value: ('0', '1', x = Unknown)

- bit 31 **FVBUSIO:** USB VBUSON Selection bit
1 = VBUSON pin is controlled by the USB module
0 = VBUSON pin is controlled by the Port function
- bit 30 **FUSBIDIO:** USB USBID Selection bit
1 = USBID pin is controlled by the USB module
0 = USBID pin is controlled by the Port function
- bit 29 **FSCM1IO:** SCM1 Pin C Selection bit⁽¹⁾
1 = Default pin for SCM1C
0 = Alternate pin for SCM1C (for compatibility with 64-pin parts only)
- bit 28-27 **Reserved:** Write '1'; ignore read
- bit 26 **FCANIO:** CAN I/O Pin Selection bit
1 = Default CAN I/O Pins
0 = Alternate CAN I/O Pins
- bit 25 **FETHIO:** Ethernet I/O Pin Selection bit⁽²⁾
1 = Default Ethernet I/O Pins
0 = Alternate Ethernet I/O Pins
- bit 24 **FMIEN:** Ethernet MII Enable bit
1 = MII enabled
0 = RMII enabled
- bit 23-19 **Reserved:** Write '1'; ignore read
- bit 18-16 **FSRSSEL<2:0>:** SRS Select bits
This field assigns an interrupt priority to a Shadow Register Set.
- bit 15-0 **USERID<15:0>:** A 16-bit value that is user-defined and is readable via ICSP™ and JTAG

Register 32-5: DEVID: Device ID

R	R	R	R	R-0	R-0	R-0	R-0
VER<11:4>							
bit 31				bit 24			

R-1	R-0	R-0	R-1	R	R	R	R
VER<3:0>				DEV<7:4>			
bit 23				bit 16			

R	R	R	R	R-0	R-0	R-0	R-0
DEV<3:0>				MANID<11:8>			
bit 15				bit 8			

R-0	R-1	R-0	R-1	R-0	R-0	R-1	R-1
MANID<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit W = Writable bit P = Programmable bit r = Reserved bit
U = Unimplemented bit -n = Bit Value at POR: ('0', '1', x = Unknown)

- bit 31-20 **VER<11:0>**: Device Variant Revision bits
- bit 19-12 **DEV<7:0>**: Device ID bits
Refer to the specific device data sheet for variant device ID definitions.
- bit 11-0 **MANID<11:0>**: JEDEC manufacturer's identification code for Microchip Technology Inc.

32.3 MODES OF OPERATION

32.3.1 Configuration Bits

In PIC32MX family devices, the Configuration Words select various device Configurations. These Configuration Words are implemented as volatile memory registers and are automatically loaded from the nonvolatile programmed Configuration data mapped in the last four Words (32-bit x 4 Words) of Boot Flash memory, DEVCFG0-DEVCFG3. These are the four locations an external programming device programs with the appropriate Configuration data (see Table 32-2).

Table 32-2: Boot Flash Configuration Locations

Configuration Word	Virtual Address
DEVCFG0	0xBFC0_2FFC
DEVCFG1	0xBFC0_2FF8
DEVCFG2	0xBFC0_2FF4
DEVCFG3	0xBFC0_2FF0

On Power-on Reset (POR) or any Reset, the Configuration Words are copied from Boot Flash memory to their corresponding Configuration registers. A Configuration bit can only be programmed = 0, (an erased state = 1).

During programming, a Configuration Word can be programmed a maximum of two times before a page erase must be performed. For example, during device programming, a user can program the Configuration Word DEVCFG1 with desired data, and perform a verification or other integrity check; then, program DEVCFG1 again—this time programming any remaining unprogrammed bits = 0.

Note: Configuration Word DEVCFG0 can only be programmed a single time before a page erase must be performed. Each time the Boot Flash memory region is erased, bit DEVCFG0<31> is automatically programmed = 0 leaving only one additional programming operation available DEVCFG0.

After programming the Configuration Words, the user should reset the device to ensure the Configuration registers are reloaded with the new programmed data.

32.3.1.1 CONFIGURATION REGISTER PROTECTION

To ensure the 128-bit data integrity of each Configuration Word, a comparison is continuously made between each Configuration bit and its stored complement. If a mismatch is detected, a Configuration Mismatch Reset is generated causing a device Reset.

32.3.2 Device Code Protection

The PIC32MX family features a single device code protection bit (DEVCFG0<28>), that when programmed to '0', protects Boot Flash and Program Flash from being read or modified by an external programming device. When code protection is enabled, only the device ID word locations are available to be read by an external programmer.

Boot Flash and Program Flash memory are not protected from self-programming during program execution when code protection is enabled. **Section 32.3.3 “Program Write Protection (PWP)”** provides more information.

32.3.3 Program Write Protection (PWP)

In addition to a device code protection bit, the PIC32MX family also features write protection bits to prevent Boot Flash and Program Flash memory regions from being written during code execution.

Boot Flash memory is write-protected with a single Configuration bit, BWP (DEVCFG0<24>), when programmed to '0'.

Using Configuration bits PWP<19:12> (DEVCFG0<19:12>), Program Flash memory can be write-protected entirely, or in blocks of memory starting from address 0xBD00_0000. The PWP bits represent the one's complement of a protected Flash memory region. For example, programming the PWP bits to 0xFF selects a region of size '0' to be write-protected, effectively disabling the Program Flash write protection. Programming the PWP bits to 0xFE selects the first block of Flash memory to be write-protected. When enabled, the selected memory range is inclusive starting from the beginning of Program Flash memory (0xBD00_0000).

The following table, Table 32-3, illustrates selectable write-protected memory regions for a device variant supporting a 4096 Byte (1024 Word) block size. Depending on the PIC32MX family variant, this memory block size may vary. Refer to the specific PIC32MX family variant data sheet for more information.

Table 32-3: Flash Program Memory Write-Protect Ranges (4096 Byte/Block)

PWP Bit Value	Range Size (K-bytes)	Write-Protected Memory Ranges ⁽¹⁾
0xFF	0	disabled
0xFE	4	0xBD00_0FFF
0xFD	8	0xBD00_1FFF
0xFC	12	0xBD00_2FFF
0xFB	16	0xBD00_3FFF
0xFA	20	0xBD00_4FFF
0xF9	24	0xBD00_5FFF
0xF8	28	0xBD00_6FFF
0xF7	32	0xBD00_7FFF
0xF6	36	0xBD00_8FFF
0xF5	40	0xBD00_9FFF
0xF4	44	0xBD00_AFFF
0xF3	48	0xBD00_BFFF
0xF2	52	0xBD00_CFFF
0xF1	56	0xBD00_DFFF
0xF0	60	0xBD00_EFFF
0xEF	64	0xBD00_FFFF
•		
•		
•		
0x7F	512	0xBD07_FFFF

Note 1: Write-protected memory range is inclusive from 0xBD00_0000.

32.4 EFFECTS OF VARIOUS RESETS

On POR (Power-on Reset), BOR (Brown-out Reset), $\overline{\text{MCLR}}$ (External Reset), CM (Configuration-Mismatch Reset), WDTR (Watchdog Timer Reset) or SWR (Software Reset), the Configuration Words are reloaded from their corresponding Boot Flash memory Configuration Words.

32.5 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC32MX device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to Configuration Words are:

Title	Application Note #
No related application notes at this time.	N/A

Note: Please visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the PIC32MX family of devices.

32.6 REVISION HISTORY

Revision A (August 2007)

This is the initial released version of this document.

Revision B (October 2007)

Updated document to remove Confidential status.

Revision C (April 2008)

Revised status to Preliminary; Revised U-0 to r-x; Revised Section 32.3.2; Revised Table 32-1; Revised Configuration Word DEVID Register; Revised Configuration Word DEVCFG2 Register.

Revision D (June 2008)

Revised Register 31-1 (DEVCFG0); Change Reserved bits from “Maintain as” to “Write”.

Revision E (July 2009)

This revision includes the following updates:

- Minor updates to the text and formatting have been incorporated throughout the document.
- Added a note regarding Configuration Word availability in PIC32MX devices to **Section 32.2 “Configuration Words”**.
- Added the following bits to Table 32-1: Configuration Word Summary and to the related registers:
 - SIGN (see Register 32-1)
 - WINDIS (Register 32-2)
 - FVBUSIO (Register 32-4)
 - FUSBIDIO (Register 32-4)
 - FSCM1IO (Register 32-4)
 - FCANIO (Register 32-4)
 - FETHIO (Register 32-4)
 - FMIIEN (Register 32-4)
 - FSRSEL (Register 32-4)