Section 20. Comparator Voltage Reference

HIGHLIGHTS

This section of the manual contains the following topics:

20.1 INTRODUCTION

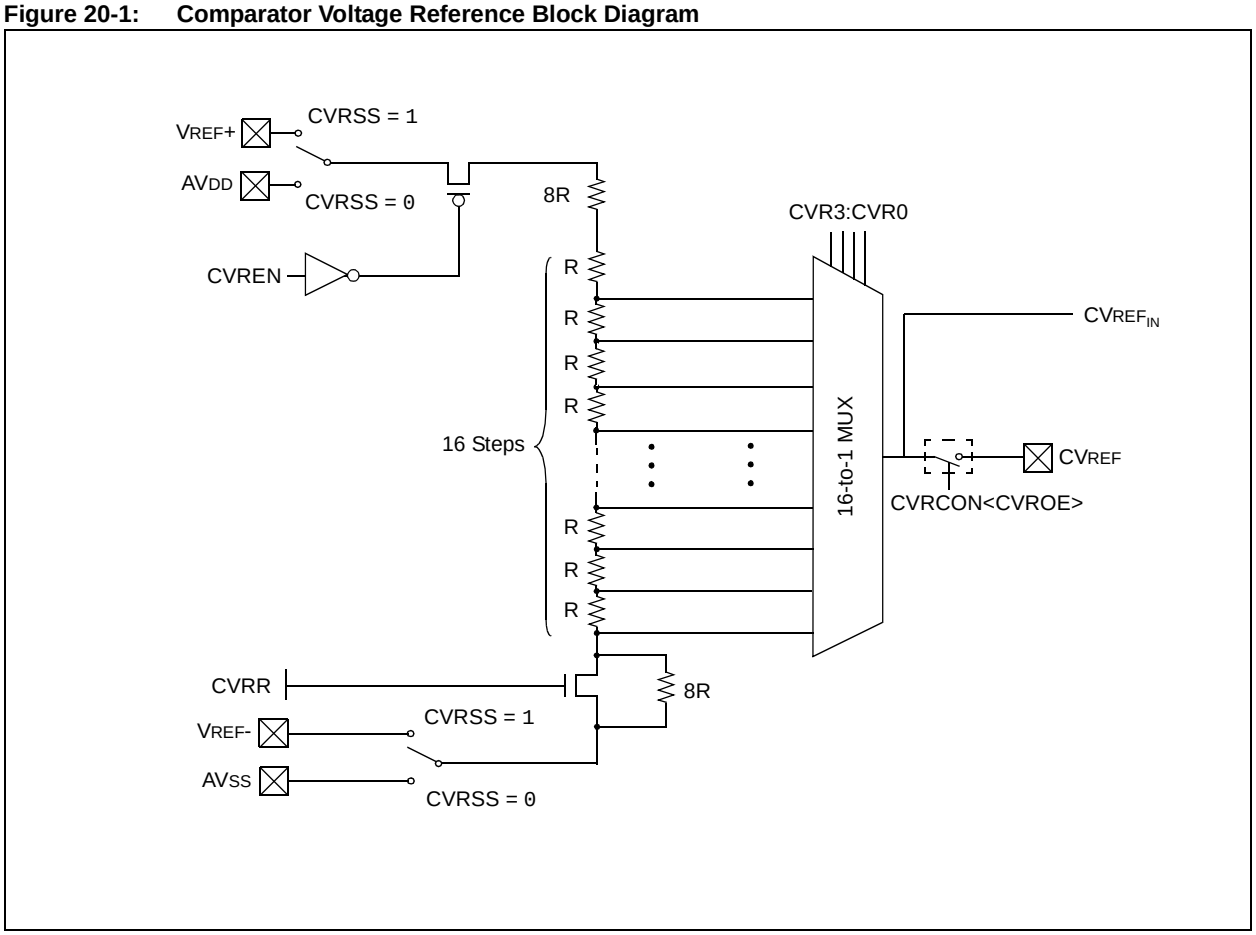
The Comparator Voltage Reference (CVREF) is a 16-tap, resistor ladder network that provides a selectable reference voltage. Although its primary purpose is to provide a reference for the analog comparators, it also may be used independently of them.

A block diagram of the module is shown in Figure 20-1. The resistor ladder is segmented to provide two ranges of voltage reference values and has a power-down function to conserve power when the reference is not being used. The module's supply reference can be provided from either device VDD/VSS or an external voltage reference. The CVREF output is available for the comparators and typically available for pin output. Please see the specific device data sheet for more information.

The Comparator Voltage Reference has the following features:

- High and low range selection
- Sixteen output levels available for each range
- Internally connected to comparators to conserve device pins
- Output can be connected to a pin

Figure 20-1: Comparator Voltage Reference Block Diagram



20.2 COMPARATOR VOLTAGE REFERENCE CONTROL REGISTERS

The CVREF module consists of the following Special Function Registers (SFR):

- CVRCON: Control Register for the module

  CVRCONCLR, CVRCONSET, CVRCONINV: Atomic Bit Manipulation Registers for CVRCON

The following table provides a brief summary of all CVREF-module-related registers. Corresponding registers appear after the summary, followed by a detailed description of each register.

Table 20-1: Comparator Voltage Reference SFR Summary

Name		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
CVRCON	31:24	—	—	—	—	—	—	—	—
	23:16	—	—	—	—	—	—	—	—
	15:8	ON	—	—	—	—	—	—	—
	7:0	—	CVROE	CVRR	CVRSS	CVR<3:0>			
CVRCONCLR	31:0	Write clears selected bits in CVRCON, read yields undefined							
CVRCONSET	31:0	Write sets selected bits in CVRCON, read yields undefined							
CVRCONINV	31:0	Write inverts selected bits in CVRCON, read yields undefined							

Register 20-1: CVRCON: Comparator Voltage Reference Control Register

r-x	r-x	r-x	r-x	r-x	r-x	r-x	r-x
—	—	—	—	—	—	—	—
bit 31							bit 24

r-x	r-x	r-x	r-x	r-x	r-x	r-x	r-x
—	—	—	—	—	—	—	—
bit 23							bit 16

R/W-0	r-x	r-x	r-x	r-x	r-x	r-x	r-x
ON	—	—	—	—	—	—	—
bit 15							bit 8

r-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	CVROE	CVRR	CVRSS	CVR<3:0>			
bit 7							bit 0

Legend:			
R = readable bit	W = writable bit	P = programmable	r = reserved bit
U = unimplemented bit, read as '0'		-n = bit value at POR: ('0', '1', x = unknown)	

bit 31-16 **Reserved:** Write '0'; ignore read

bit 15 **ON:** CVREF Peripheral On bit

1 = Module is enabled, setting this bit does not affect the other bits in the register.
0 = Module is disabled and does not consume current. Clearing this bit does not affect the other bits in the register.

Note: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

bit 14-7 **Reserved:** Write '0'; ignore read

bit 6 **CVROE:** CVREF Output Enable bit

1 = Voltage level is output on CVREF pin
0 = Voltage level is disconnected from CVREF pin
Note: CVROE overrides the TRIS bit setting, see **Section 12. "I/O Ports"** for more information.

bit 5 **CVRR:** CVREF Range Selection bit

1 = 0 to 0.67 CVRSRC, with CVRSRC/24 step size
0 = 0.25 CVRSRC to 0.75 CVRSRC, with CVRSRC/32 step size

bit 4 **CVRSS:** CVREF Source Selection bit

1 = Comparator voltage reference source, CVRSRC = (VREF+) – (VREF-)
0 = Comparator voltage reference source, CVRSRC = AVDD – AVSS

bit 3-0 **CVR<3:0>:** CVREF Value Selection 0 ≤ CVR3:CVR0 ≤ 15 bits

When CVRR = 1:
CVREF = (CVR<3:0>/24) • (CVRSRC)

When CVRR = 0:
CVREF = 1/4 • (CVRSRC) + (CVR<3:0>/32) • (CVRSRC)

Register 20-2: CVRCONCLR: CVREF Control Clear Register

Write clears selected bits in CVRCON, read yields undefined
bit 31 bit 0

bit 31-0 **Clear selected bits in CVRCON**

A write of '1' in one or more bit positions clears the corresponding bit(s) in CVRCON register, a write of '0' will not affect the register.(1)

The read operation returns an undefined value and is not recommended.

Example:
`CVRCONCLR = 0x00008001` clears bits 15 and 0 in CVRCON register.

Note 1: This operation will not affect unimplemented or read-only bits.

Register 20-3: CVRCONSET: CVREF Control Set Register

Write sets selected bits in CVRCON, read yields undefined
bit 31 bit 0

bit 31-0 **Set selected bits in CVRCON**

A write of '1' in one or more bit positions sets the corresponding bit(s) in CVRCON register, a write of '0' will not affect the register.(1)

The read operation returns an undefined value and is not recommended.

Example:
`CVRCONSET = 0x00008001` sets bits 15 and 0 in CVRCON register.

Note 1: This operation will not affect unimplemented or read-only bits.

Register 20-4: CVRCONINV: CVREF Control Invert Register

Write inverts selected bits in CVRCON, read yields undefined
bit 31 bit 0

bit 31-0 **Inverts selected bits in CVRCON**

A write of '1' in one or more bit positions inverts the corresponding bit(s) in CVRCON register, a write of '0' will not affect the register.(1)

The read operation returns an undefined value and is not recommended.

Example:
`CVRCONINV = 0x00008001` inverts bits 15 and 0 in CVRCON register.

Note 1: This operation will not affect unimplemented or read-only bits.

20.3 OPERATION

The CVREF module is controlled through the CVRCON register (Register 20-1). The CVREF provides two ranges of output voltage, each with 16 distinct levels. The range to be used is selected by the CVRR bit (CVRCON<5>). The primary difference between the ranges is the size of the steps selected by the CVREF value selection bits, CVR3:CVR0, with one range offering finer resolution and the other offering a wider range of output voltage. The typical output voltages are listed in Table 20-2.

The equations used to calculate the CVREF output are as follows:

If CVRR = 1:
Voltage Reference = ((CVR3:CVR0)/24) x (CVRSRC)

If CVRR = 0:
Voltage Reference = (CVRSRC/4) + ((CVR3:CVR0)/32) x (CVRSRC)

The CVREF Source Voltage (CVRSRC) can come from either VDD and VSS, or the external VREF+ and VREF- pins that are multiplexed with I/O pins. The voltage source is selected by the CVRSS bit (CVRCON<4>). The voltage reference is output to the CVREF pin by setting the CVROE (CVRCON<6>) bit; this will override the corresponding TRIS bit setting.

The settling time of the CVREF must be considered when changing the CVREF output (Refer to the device data sheet).

Table 20-2: Typical Voltage Reference with CVRSRC = 3.3

CVR<3:0>	Voltage Reference	
	CVRR = 0 (CVRCON <5>)	CVRR = 1 (CVRCON <5>
0	0.83V	0.00V
1	0.93V	0.14V
2	1.03V	0.28V
3	1.13V	0.41V
4	1.24V	0.55V
5	1.34V	0.69V
6	1.44V	0.83V
7	1.55V	0.96V
8	1.65V	1.10V
9	1.75V	1.24V
10	1.86V	1.38V
11	1.96V	1.51V
12	2.06V	1.65V
13	2.17V	1.79V
14	2.27V	1.93V
15	2.37V	2.06V

20.3.1 CVREF Output Considerations

The full range of voltage reference cannot be realized due to the construction of the module. The transistors on the top and bottom of the resistor ladder network (Figure 20-1) keep the voltage reference from approaching the reference source rails. The voltage reference is derived from the reference source; therefore, the voltage reference output changes with fluctuations in that source. Refer to the product data sheet for the electrical specifications. Table 20-3 contains the typical output impedances for the CVREF module.

Table 20-3: Typical CVREF Output Impedance in Ohms

CVR<3:0>	Voltage Reference	
	CVRR = 0 (CVRCON <5>)	CVRR = 1 (CVRCON <5>
0	12k	500
1	13k	1.9k
2	13.8k	3.7k
3	14.4k	5.3k
4	15k	6.7k
5	15.4k	7.9k
6	15.8k	9k
7	15.9k	9.9k
8	16k	10.7k
9	15.9k	11.3k
10	15.8k	11.7k
11	15.4k	11.9k
12	15k	12k
13	14.4k	11.9k
14	13.8k	11.7k
15	12.9k	11.3k

20.3.2 Initialization

This initialization sequence shown in Example 20-1 configures the CVREF module for: module enabled, output enabled, high range, and set output for maximum (2.37V).

Example 20-1: Voltage Reference Configuration

```
CVRCON = 0x804F;   //Initialize Voltage Reference Module
                   //enable module, enable output, set
                   // range to high, set output to maximum
```

20.4 INTERRUPTS

There are no Interrupt configuration registers or bits for the CVREF module. The CVREF module does not generate interrupts.

20.5 I/O PIN CONTROL

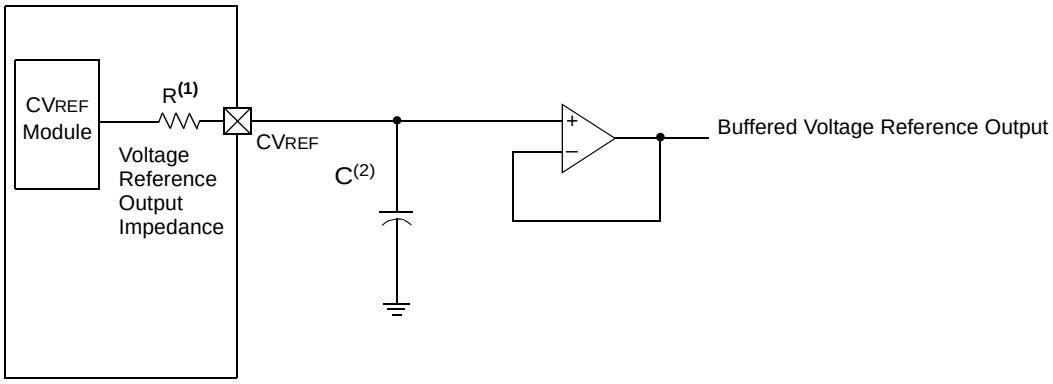
The CVREF module has the ability to output to a pin. When the CVREF module is enabled and CVROE (CVRCON<6>) is '1', the output driver for the CVREF pin is disabled and the CVREF voltage is available at the pin. For proper operation, the TRIS bit corresponding to the CVREF pin must be a '1' when CVREF is to be output to a pin. This disables the digital Input mode for the pin and prevents undesired current draw resulting from applying an analog voltage to a digital input pin. The output buffer has very limited drive capability. An external buffer amplifier is recommended for any application that uses the CVREF voltage externally. An output capacitor may be used to reduce output noise. Use of an output capacitor will increase settling time (see Figure 20-2).

Table 20-4: Pins Associated with a Comparator

Pin Name	Module Control	Controlling Bit Field	Required TRIS bit Setting	Pin Type	Buffer Type	Description
CVREF	ON	CVROE	Input	A, O	—	CVREF Output

Legend: ST = Schmitt Trigger input with CMOS levels, I = Input, O = Output, A = Analog, D = Digital

Figure 20-2: Comparator Voltage Reference Output Buffer Example



Note 1: R is dependent on the comparator voltage reference control bits CVRR (CVRCON<5>) and CVR<3:0> (CVRCON<3:0 Refer to Table 20-3

2: Use of an output capacitor will increase settling time. Capacitor value selection is dependent on the CVR<3:0> and CVRR settings, as well as the frequency to be attenuated.

20.6 OPERATION IN POWER-SAVING AND DEBUG MODES

Note:	In this manual, a distinction is made between a power mode as it is used in a specific module, and a power mode as it is used by the device, e.g., Sleep mode of the Comparator and SLEEP mode of the CPU. To indicate which type of power mode is intended, uppercase and lowercase letters (Sleep, Idle, Debug) signify a module power mode, and all uppercase letters (SLEEP, IDLE, DEBUG) signify a device power mode.

20.6.1 CVREF Operation in SLEEP Mode

The CVREF module continues to operate in SLEEP mode. The CVRCON register is not affected when the device enters or wakes from SLEEP mode. If the CVREF voltage is not used in SLEEP, the module can be disabled by clearing the ON bit CVRCON<15> prior to entering SLEEP to save power.

20.6.2 IDLE

The CVREF module continues to operate in IDLE mode. The CVRCON register is not affected when the device enters or exits IDLE mode. There is no provision to automatically disable the module in IDLE mode. If the CVREF voltage is not used in IDLE, the module can be disabled by clearing the ON bit CVRCON<15> prior to entering IDLE to save power.

20.6.3 DEBUG

The CVREF module continues to operate while the device is in DEBUG mode. The module doesn't support Freeze mode.

Note:	There is no FRZ mode for this module.

20.7 EFFECTS OF RESETS

All Resets disable the voltage reference by forcing all bits in CVRCON to a '0'.

20.8 DESIGN TIPS

Question 1: ***My voltage reference is not what I expect.***

Answer: Any variation of the voltage reference source will translate directly onto the CVREF pin. Also, ensure that you have correctly calculated (specified) the voltage divider which generates the voltage reference. Ensure the TRIS bit for the CVREF pin is a '1' to disable the digital output circuitry, as well.

Question 2: ***I am connecting CVREF into a low-impedance circuit and the voltage reference is not at the expected level.***

Answer: The voltage reference module is not intended to drive large loads. A buffer must be used between the CVREF pin and the load (see Figure 20-2).

20.9 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC32MX device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Comparator Voltage Reference module are:

Title	Application Note #
No related application notes at this time.	N/A

Note: Please visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the PIC32MX family of devices.

20.10 REVISION HISTORY

Revision A (October 2007)

This is the initial released version of this document.

Revision B (October 2007)

Updated document to remove Confidential status.

Revision C (April 2008)

Revised status to Preliminary; Revised U-0 to r-x.

Revision D (June 2008)

Revised Figure 20-1; Change Reserved bits from “Maintain as” to “Write”; Added Note to ON bit (CVRCON Register).

NOTES:

