

Microprocessor-

The Microprocessor is the Central Unit of a Computer system that performs arithmetic and logic ops which generally include adding, subtracting, transferring numbers from one area to another, and comparing two Numbers. It's often known simply as a processor or a CPU or a logic chip.

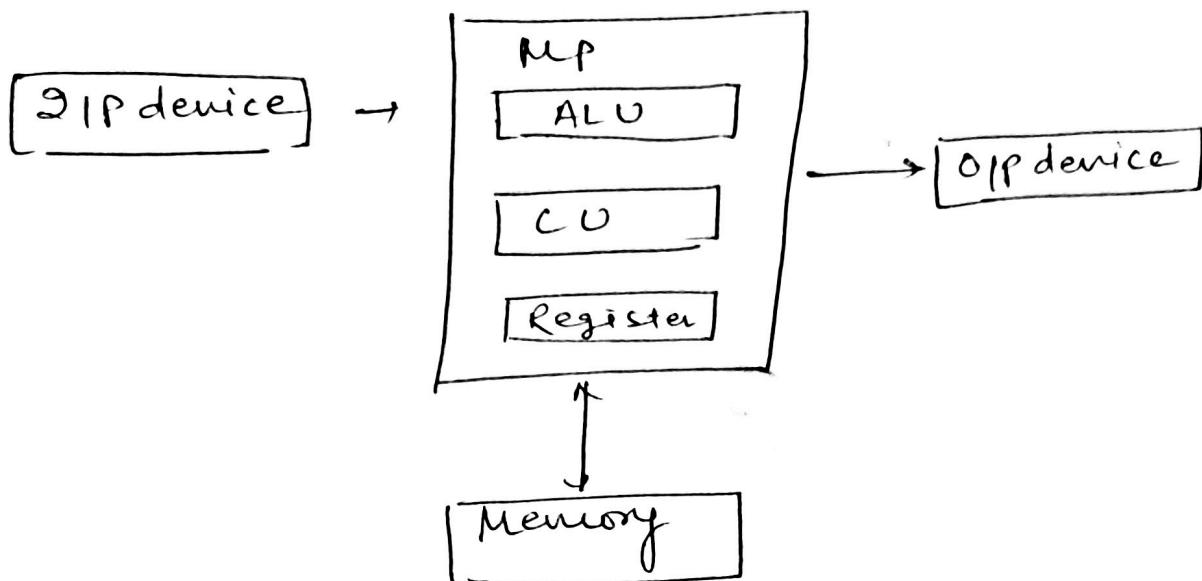
- " A Microprocessor is a computer processor where the data processing logic and control is included on a single integrated circuit or a small no of Integrated circuit "
- " Microprocessor is an electronic circuit that functions as the CPU of a computer providing computational control."

- * The MP or CPU is the brain of the Computer.
- * MP is the core of the system.
- * A digital Computer with one MP which acts as a CPU is called Microcomputer.

How Does a Microprocessor Work.

A MP accepts binary data as input, processes that data and then provides op based on the instructions stored in the memory. The data is processed using the

Mp ALU, CU, and a register.



Block diagram of a Microcomputer.

Evolution of Microprocessor.

Transistor was invented in 1948 (23 Dec 1947 in Bell Lab). IC was invented in 1958 (Fairchild Semiconductors) By Texas Instruments J Kilby. first microprocessor was invented by INTEL (Integrated electronics)

Size of Mp - 4 bit

Name	Year of Invention	Clock Speed	No of Transistors	Inst ⁿ per second
INTEL 4004/4040	1971 by Ted Hoff and Stanley Mazor	740 KHz	2300	60,000

(3)

size of Mp - 8 bit

Name	Year of Invention	Clock Speed	No of Transistors	Inst ⁿ per sec
8008	1972	500 KHz	50,000	
8080	1974	2 MHz	60,000	10 times faster than 8008.
8085	1976 (16 bit address bus)	3 MHz	6500	769230

size of Mp - 16 bit

8086	1978 (Multiply & divide Inst ⁿ , 16 bit data Bus, 20 bit address bus)	4.77 MHz, 8 MHz, 10 MHz	29000	2.5 million
8080	1979			2.5 million
8086 / 8088	1982	6 MHz		
80286	1982	8 MHz	134000	4 million

size of Mp - 32 bit

Intel 80386	1986	16 MHz	275000	
INTEL 80486	1986	16 MHz - 100 MHz	1.2 million	8 KB of Cache Memory

PENTIUM

1993

66MHz

Cache Memory
8 bit for
instr. & 8 bit for
data.

size of MP - 64 bit

Intel Core 2	2006	1.2 GHz to 3 GHz	291 Million
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i3, i5, i7	2007, 2009, 2010	2.2 GHz - 3.3 GHz 2.4 GHz - 3.64 GHz 2.93 GHz - 3.33 GHz
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Generation of MP -

1. 1st generation - from 1971 to 1972 the era of the 1st generation came which brought microprocessor like Intel 4004
2. 2nd generation - The 2nd generation marked the development of 8 bit MP from 1973 to 1978. Processor like INTEL 8085, Motorola 6800 and 6801 etc came into existence.
3. 3rd generation - The Third generation brought forward the 16 bit MP like INTEL 8086 / 80186 / 80286 from 1979 to 1980 this generation used to HMOS Technology

4th generation - It came into existence from 1981 to 1995.
32 bit processor introduced.

5th generation - from 1995 till now 64 bit processor
like Pentium dual, Octa core.

Types of MP -

- ① Complex Instⁿ set MP - The processor are designed to minimize the no of Instⁿ per program and ignore the no of cycle per instruction.
- * The compiler is used to translate a High level language to Assembly Level language.
 - * because the length of code is relatively short and an extra RAM is used to store the instruction.
 - * These processor can do tasks like downloading, uploading & recalling data from Memory.
 - * Apart from these tasks these MP can perform complex Mathematical Calculation in a single command.
- ex- IBM 370 / 168.

② Reduced Instⁿ set MP-

These type of processor are made according to the function in which the MP can carry out small things in specific commands. In this way these processor complete

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more commands at a faster rate.

③ Super Scalar MP - These processor can perform many tasks at a time. They can be used for ALUs and multiplier like array. They have multiple opⁿ unit and perform to task

④ Application specific IC - These processor are application specific like for personal digital Assistant computers. They are designed according to proper specification.

⑤ Digital signal MP - These processor are used to convert signal like analog to digital or digital to analog. The chips of these processor are used in many device such as home theatres, mobile phone etc.

Advantage of MP

- ① High processing speed.
- ② Compact size
- ③ Easy Maintenance
- ④ flexible
- ⑤ Can be modified improved according to requirement.

Disadvantage

- ① Performance depends on the size of data.
- ② Overheating occurs due to overuse.
- ③ Most MP do not support floating point opⁿ.

Microprocessor Architecture.

The MP is the CPU of a computer. It is the heart of computer. Here we will describe Intel 8085 as it is one of the most popular 8 bit microprocessor.

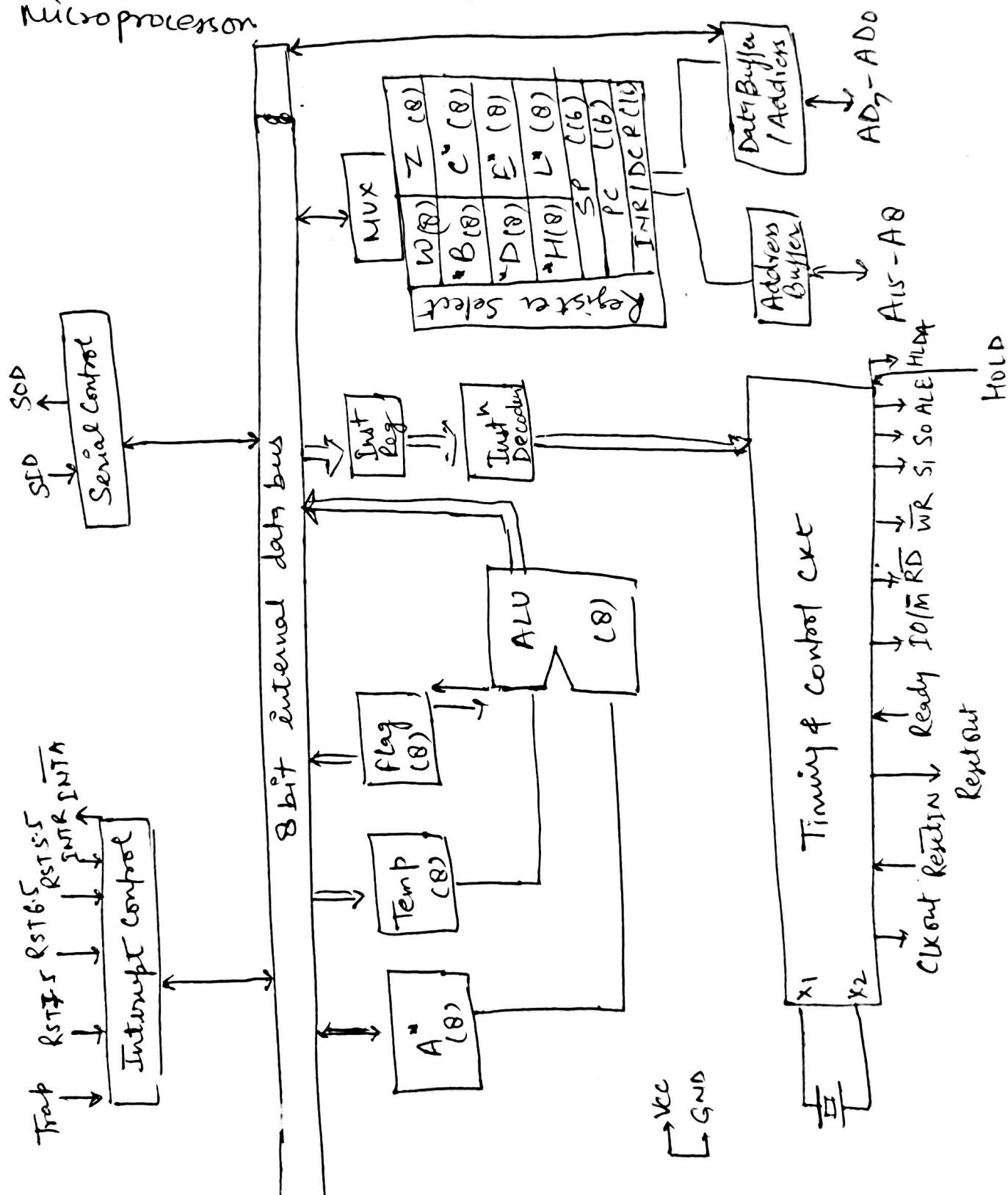


fig - 8085 Architecture.

8085 Microprocessor - functional Units.

Accumulator

It is an 8 bit register used to perform arithmetic, logical, L1O & Load / STORE opⁿ. It is connected to internal data bus of ALU.

Arithmetic & Logic Unit

It performs ALU opⁿ like addition, Subtraction, AND, OR, etc. on 8-bit data.

General Purpose Register

There are 6 general purpose register in 8085 processor, i.e., B, C, D, E, H & L. Each register can hold 8-bit data.

These register can work in pair to hold 16 bit data and their pairing combination is like B-C, D-E & H-L.

Program Counter

It is a 16-bit register used to store the memory address location of the next instruction to be executed.

Stack Pointer

It is also 16 bit register works like stack which is always inc/dec by during push & pop opⁿ.

TR-

It is an 8 bit register, which holds the temporary data of ALU opⁿ.

(a)

Flag Register-

It is an 8 bit register having five 1 bit flip-flops which holds either 0 or 1 depending upon the result stored in the Accumulator. These are the set of flags.

- 1- Sign (S)
- 2- Zero (Z)
- 3- Auxiliary Carry (AC)
- 4- Parity (P)
- 5- Carry (C)

Instruction Reg & Decoder-

It is an 8 bit register. When an instruction is fetched from memory then it is stored in the Instruction Reg. Decoder decodes the information present in the IR.

Timing & Control Unit-

It provides timing and control signals to microprocessor to perform opn.

Interrupt Control -

It controls the interrupts during a process. When MP is executing a main program and whenever interrupt occurs, the MP shifts the control from the main program to process the incoming Request.

Serial I/P & O/P Control -

It controls the serial data communication by using 2 instructions (SIN) and (SOD) (Serial I/P data)

Address Bus and Data Bus -

Data Bus carries the data to be stored.

It is bidirectional.

Address Buffer & ADB -

The content stored in the SP and PC is loaded into the Address Buffer and Address data Buffer to communicate with the CPU.

→ Assembly Language (How you access (use) the data in the instruction)

Addressing Modes -

The way of specifying data to be operated by an instruction is called addressing mode.

Types of 8085 AM -

1. Immediate Addressing Mode -

In IAM the source operand is always data. If the data is 8 bit, then the instruction will be of 2 bytes. If the data is of 16 bit then the instruction will be of 3 bytes.

example -

• MVI B 45 (move the data 45H immediately to Reg B)

• LXI H 3050 (load the HL Pair with the operand 3050H immediately)

• JMP address (Jump to operand address immediately)

② Reg A M - In R.A.M the data to be operated is available inside the register(s) and register(s) is (are) operands. Therefore the opⁿ is performed within various Reg of the microprocessor.

ex -

MOV A, B (move the content of B to reg A)
ADD B (The add of content B to reg A)
INR A (& store a result in A
Increment of Register A by one)

③ Direct A M -

The data to be operated is available inside a Memory location and that Memory location is directly specified as an operand. The operand is directly available in the instruction itself.

ex -

LDA 2050 (load the contents of Memory location into Accumulator A)

LH LD Address (load contents of 16 bit Memory location into H-L Reg pair)

IN 35 (Read the data from port whose address is 35)

④

Reg Indirect A M - In Reg Indirect A M , the data to be operated is available inside a memory location and that Memory location is indirectly specified by a Register pair.

ex - MOV A,M (move the contents of the Memory location pointed by the H-L pair to accumulator)

LDAXB (move content of B-C Reg to Accum)

⑤ Implied / Implicit AM-

The operand is hidden and

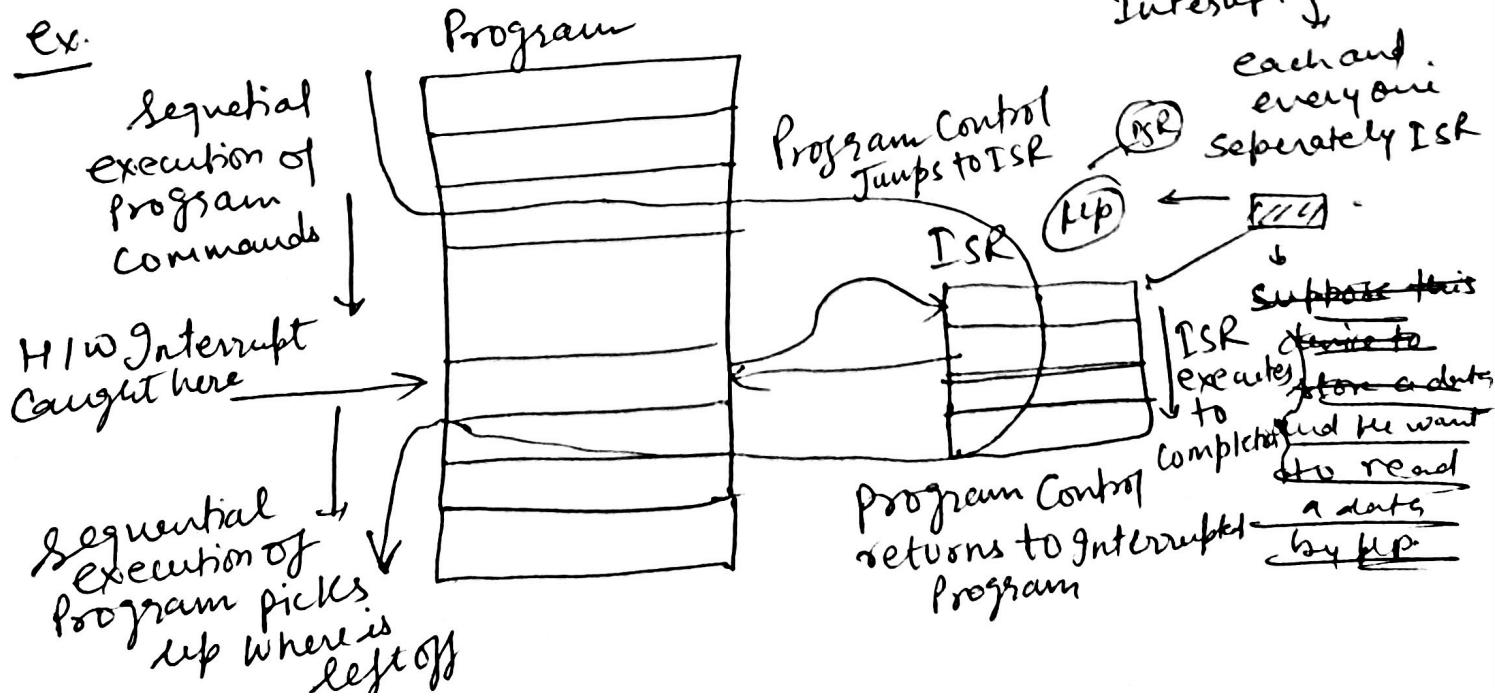
the data to be operated is available in the instru
itself

ex- RRC (rotate AC A right by one bit)
RLC (rotate AC A left by one bit)

Interrupt

An external I/O signal or an instruction
can suspend normal flow of execution and
go to Interrupt Service Routine. Once serviced,
program resumes.

ISR- A small program or a routine that
when executed service the corresponding
interrupting source is called as an ISR.



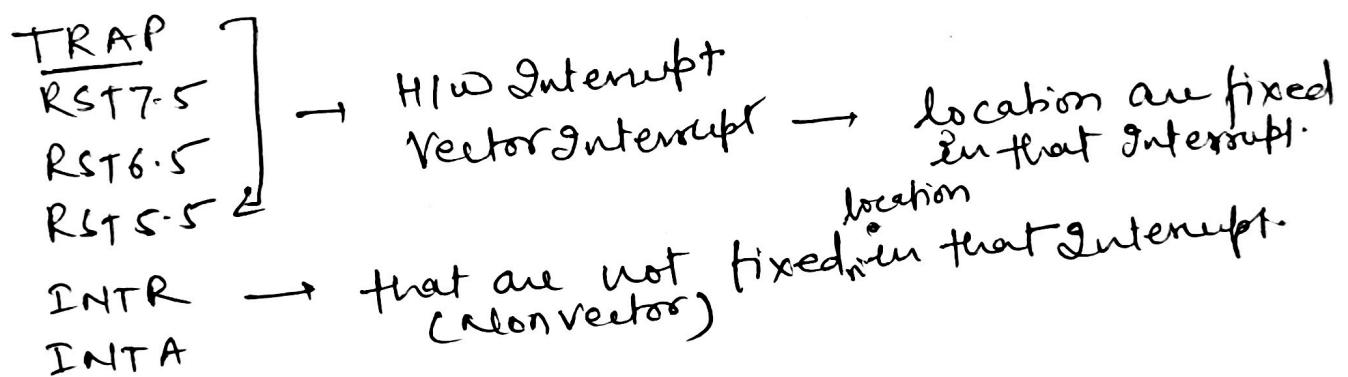
Maskable / Non Maskable Interrupt

↓
Mask means
HIDE / Ignore / Disable

Maskable - It can be disabled, ignored.
Non maskable - that is not ignored like Trap
this is not ignored but this interrupt
are used of HOLD.

There are 6 pins are available in 8085 for
interrupt

INTA → Interrupt Acknowledge (Up to Response to INTA).



what happens when interrupt comes

- INTA (ACTIVE LOW) Signal to Peripheral.
- Vectored Address of Particular interrupt is stored in PC.
- The Processor executes an interrupt service Routine (ISR).

There are 2 types of Interrupts used in 8085P/C

- ① H/W Interrupts
- ② S/W Interrupts.

S/W Interrupts - due to instruction inserts
total 8 S/W interrupts.

- ① RST 0
- ② RST 1
- ③ RST 2
- ④ RST 3
- ⑤ RST 4
- ⑥ RST 5
- ⑦ RST 6
- ⑧ RST 7

Vector address = $\text{Interrupt No}^* 8$

ex: $\text{RST 1} = 1^* 8 = 08 = 0008H$

$\text{RST 2} = 2^* 8 = 16 = 0010H$

$\text{RST 3} = 3^* 8 = 24$

Interrupt

RST 0

RST 1

RST 2

RST 3

Vector Address

0000H

0008H

0010H

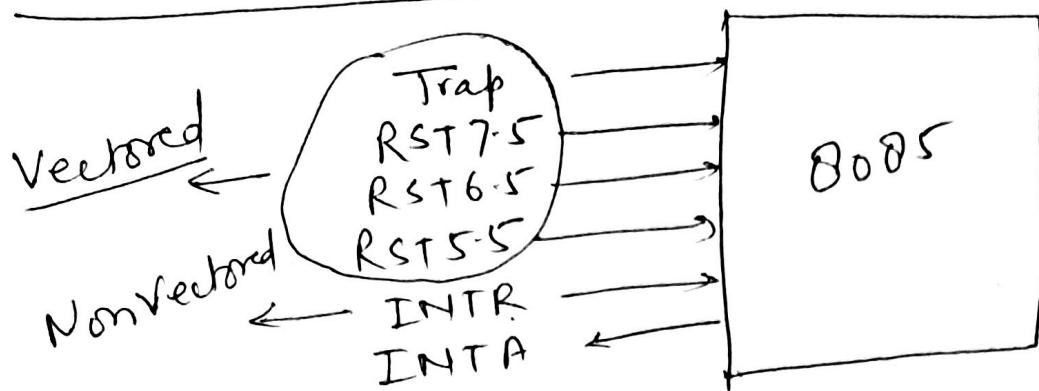
0018H

write to LSR
in this
location

↓
that is
interrupt
to write in
a program
and this
is go to fixed vector address.

HW interrupt

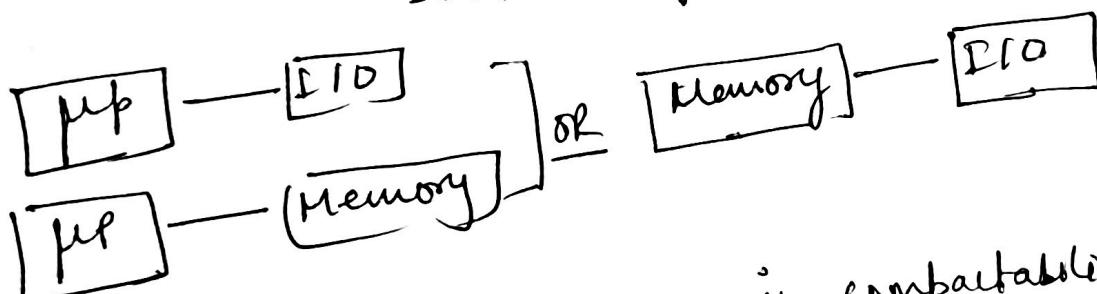
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- = 5 interrupt input
- = Trap, RST 7.5, RST 6.5, RST 5.5 are vector interrupt.
- = Trap is Non Maskable Interrupt
- = INTA is acknowledgement signal.

Data Transfer Scheme

Data Transfer scheme b/w 2 devices.



generally μP is memory is compatibility with μP .
 because both are the ~~manufacture by~~ ^{use of semiconductor} of same Technique and Manufacture

μP } semiconductor
 Memory } \rightarrow interfacing - less problem

I/O - having a different speed &
 different characteristics are available.
 and different-different technology are used to
 a manufacture.

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different Manufacturing Technology
such as - electronic
electrical
Mechanical etc

μP Based System to be included different types
of speed device

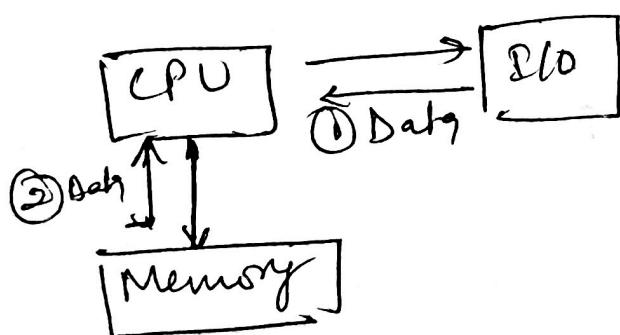
Data Transfer scheme are classified

in two categories.

- ① Programmed data Transfer
- ② ~~data~~ DMA data Transfer Scheme

Programmed data Transfer.

- ① Controlled by CPU



- ② Data Transfer control by
the Memory

+ Memory to be stored a program
and program to be executed by the μP
when data to be transferred by I/O.

⇒ It is used for small amount of data
... to be transferred.

Programmed data Transfer

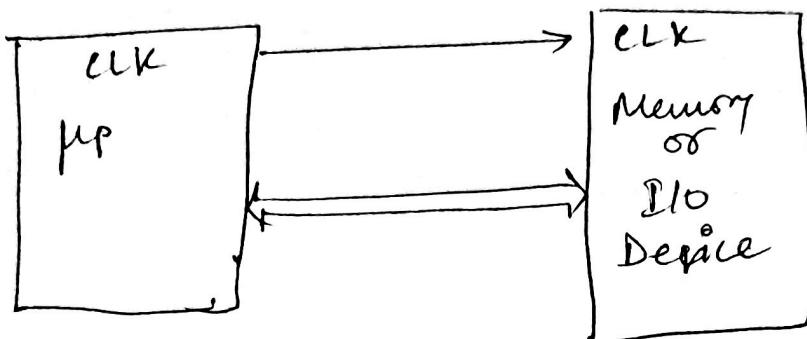
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↓
Synchronous
data
Transfer

↓
Asynchronous
data
Transfer

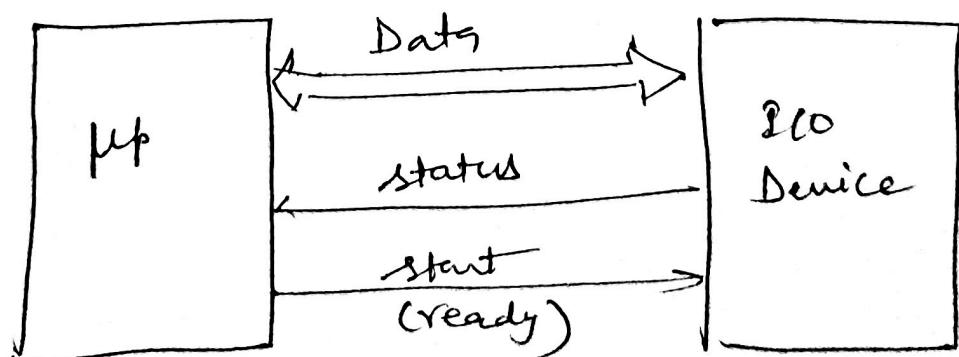
↓
Interrupt
driven
data
Transfer

① Synchronous data Transfer-



- ① at the same time and same clock to be used for the transfer of data when the CPU and I/O device which is matched in the speed.

Asynchronous data Transfer

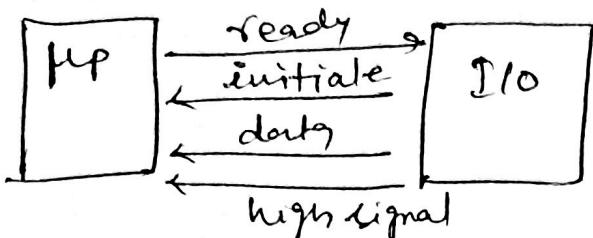


This scheme will be used for not match of μP speed of any device so that it is use at irregular intervals.

Interrupt driven data Transfer



when its main program to be execute

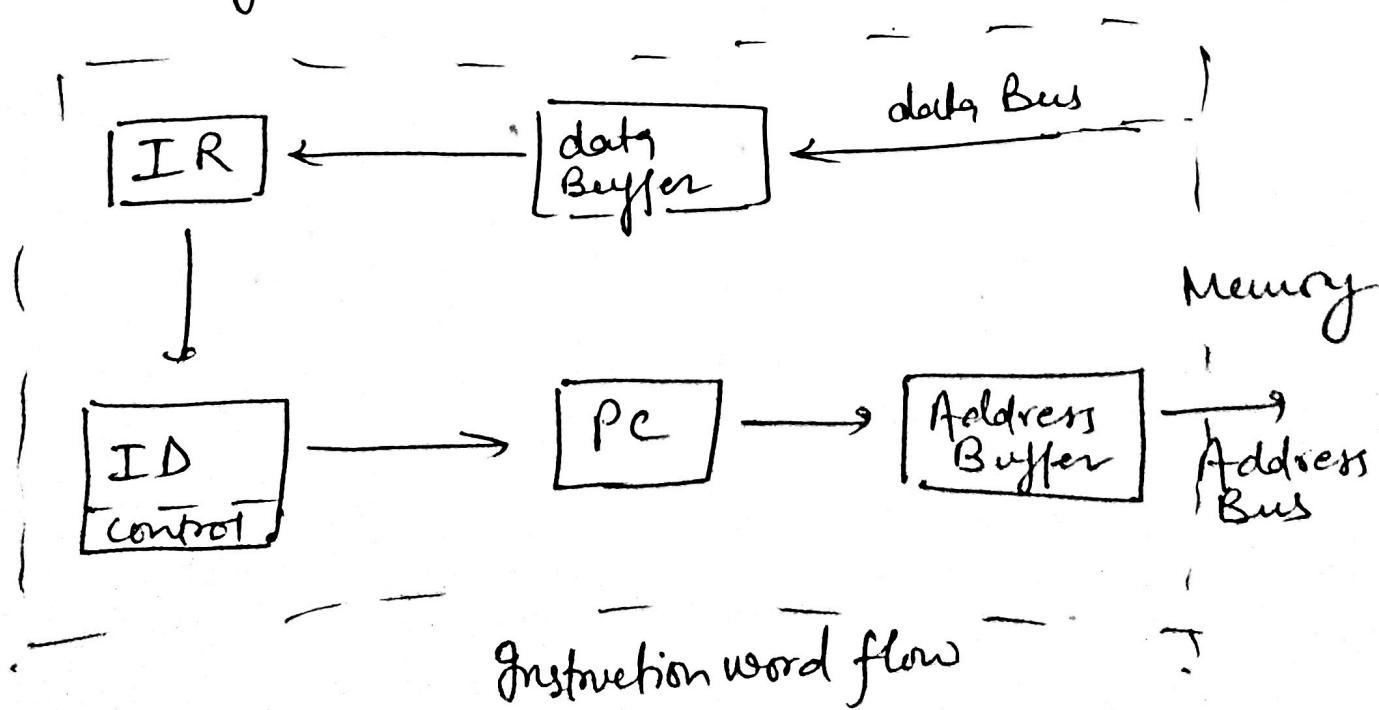


① when I/O device (ready) to transfer data

② I/O sends a high signal to μP that high signal also called interrupt.

Instruction and data flow-

- At the starting of fetch cycle the content of Program Counter is transferred in Memory Address register or Address Buffer.



Then the content of Address buffer is transferred to Memory through address bus. It send some control signal to Memory. It indicate that data has to be read or write.

- * Then the Memory send the opcode to the PU through data bus.

- Opcode firstly comes in data buffer. Then opcode is placed to IR and it decodes by the ID.
- The data word is transferred to the PU through the data bus or store in AC or some other general purpose Reg depends on the instruction.
- After the execution the result is send to Memory or OP device.

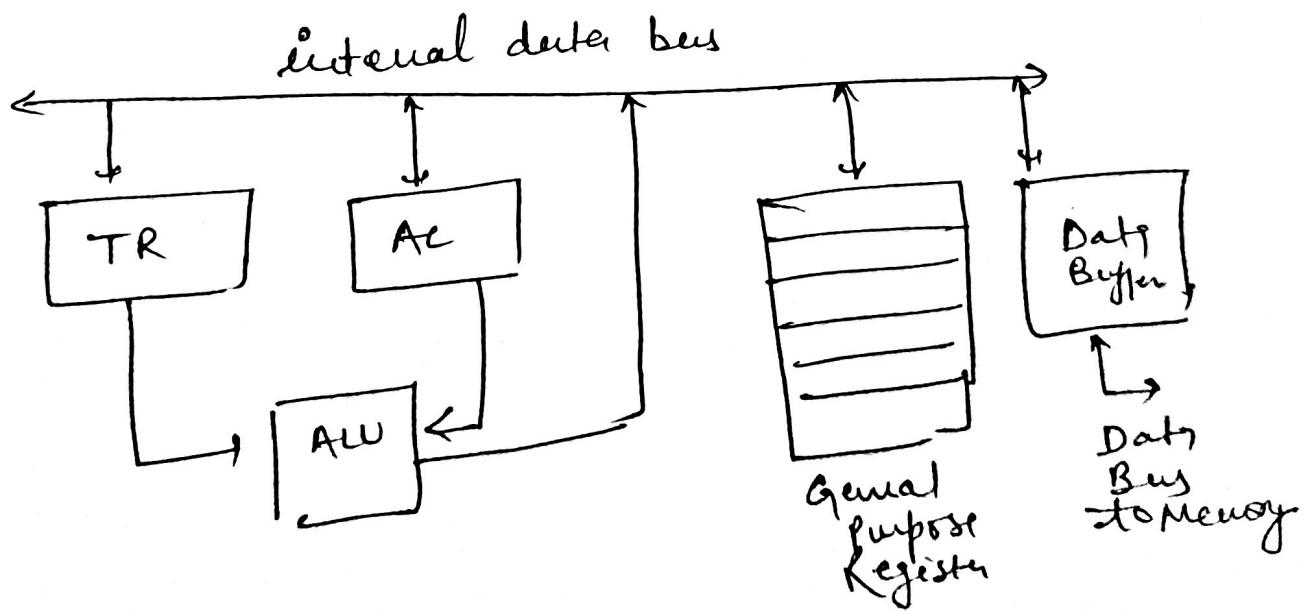


fig. Data word flow

Timing diagram

ex:-

Program :- Hexa code

. MOV CA.

4FH

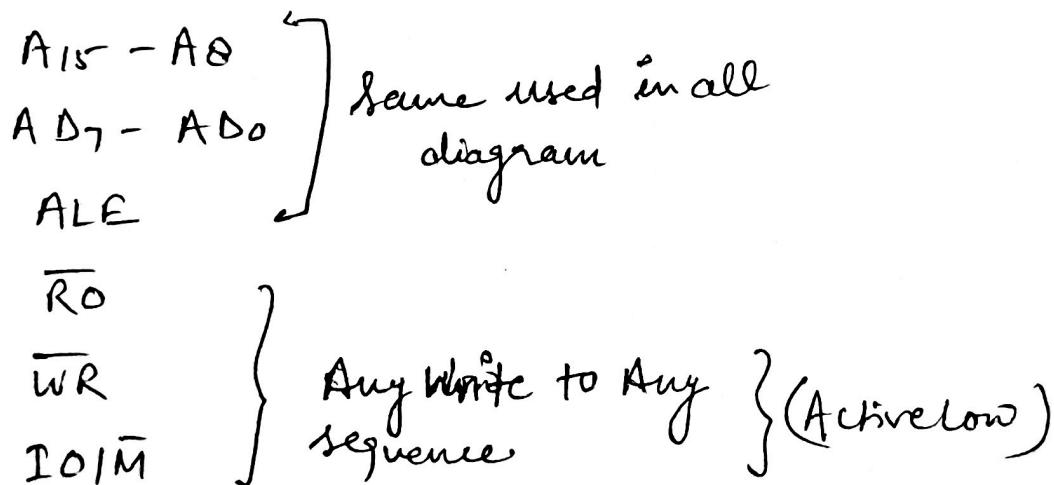
address
2008

* Data Transfer Group-

- 1) MOV R₁, R₂ → Move data :- Move the content of the one register to another.

$$[R_1] \leftarrow [R_2]$$

sequence -



use of 3 element for Timing diagram.

OF → 4T (4 Timing clock)

MR → 3T

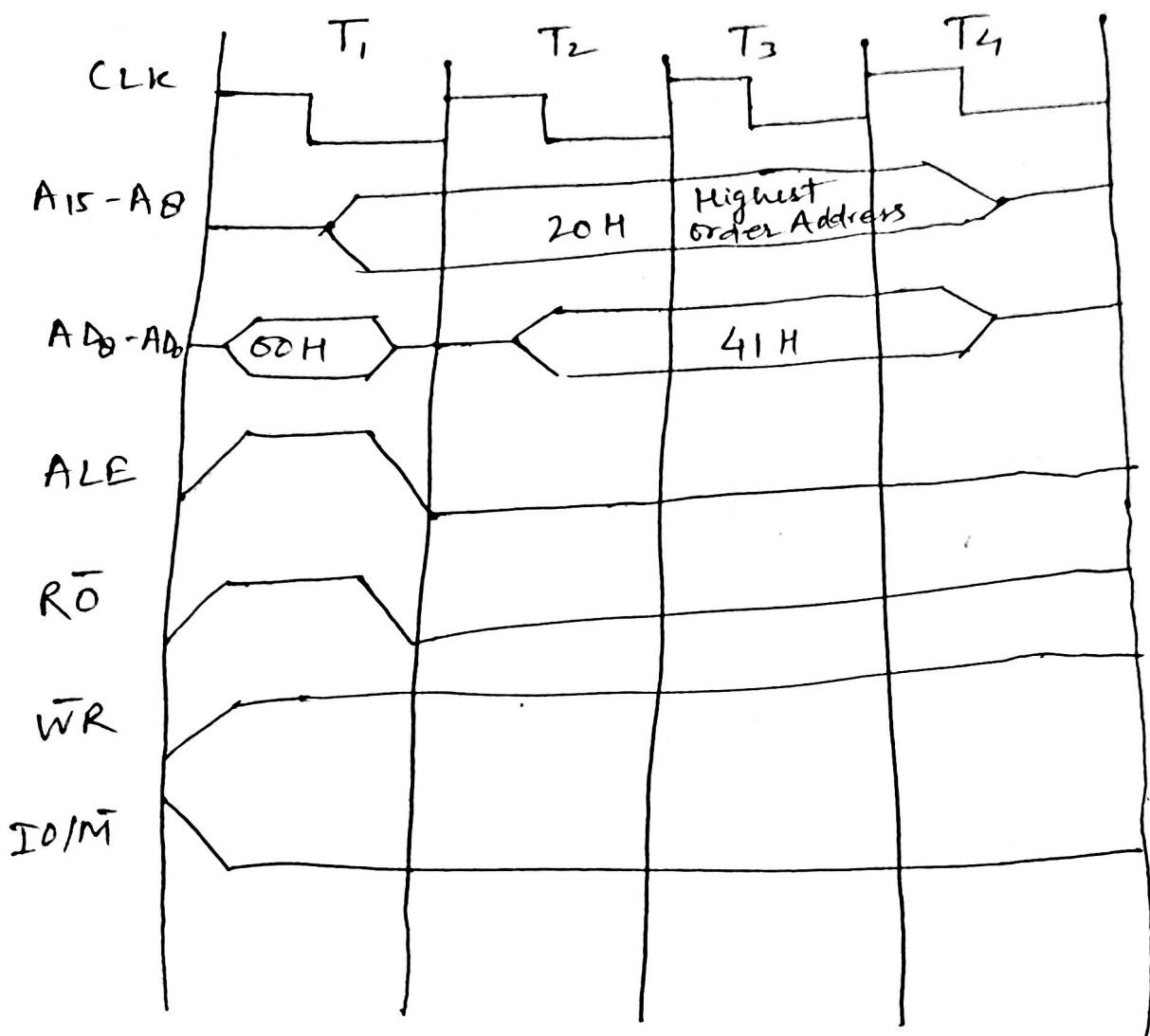
MW → 3T

OF → OPCODE fetch are used any instruction of Timing diagram.

MOV R1, R2

ex. MOV B, C

(opcode fetch - 4 T)



MOV BC
20 00 41 11
↓ + ↓ Data
↓ lowest highest
(T₂-T₄)

- Note-
- (1) Lower address contain only A_{D8}-A_{D0}
 - (2) Highest address contain only A_B-A₁₅
 - (3) ALE is always high on T_1 and rest of down each of every instruction.
 - (4) T_2, T_3, T_4 store only data.

Q2) MOV M, RS → Move the content of Reg to Memory.

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$$M \leftarrow \{R_S\}$$

This instruction MOV M R_s will copy 8 bit value from the register R_s to the memory location as pointed by the Register pair.

Example: MOU M, E

OF, MR, MW

Hex code change

<u>for Memory write cycle</u>	Before
E	ABH
HL	4050H
4050H	CDH

Affee

ABH

4050H

ABH

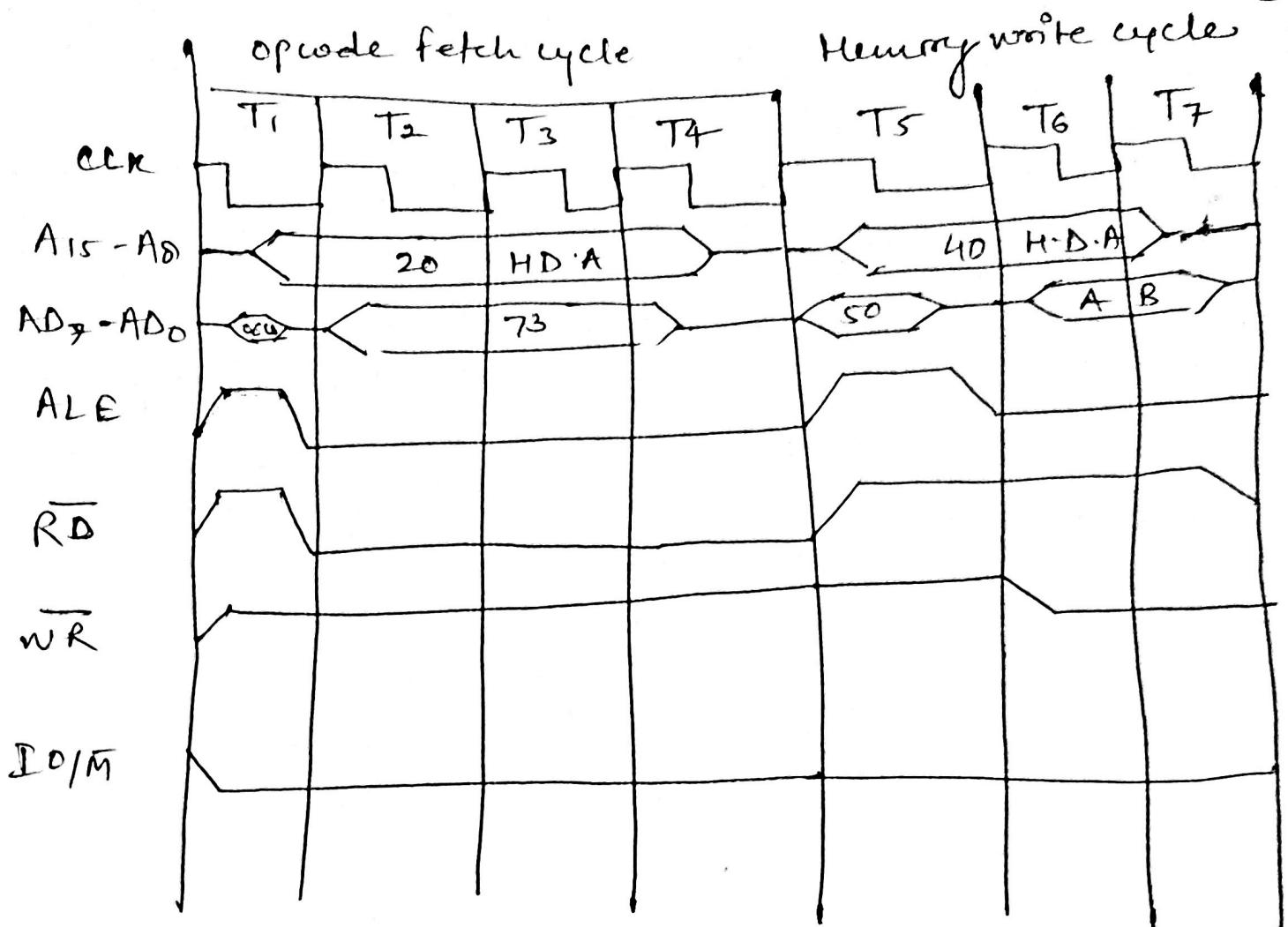
Mnemonic

MOR M, E

Address
2006
High Low

flex code
73

Timing diagram



HL → 4050H

4050 → CDM ABH

③ MOV R, M → Mov the content of Memory Register

R ← [M]

example MOV E, M

Hexcode \rightarrow 5E

(cont)

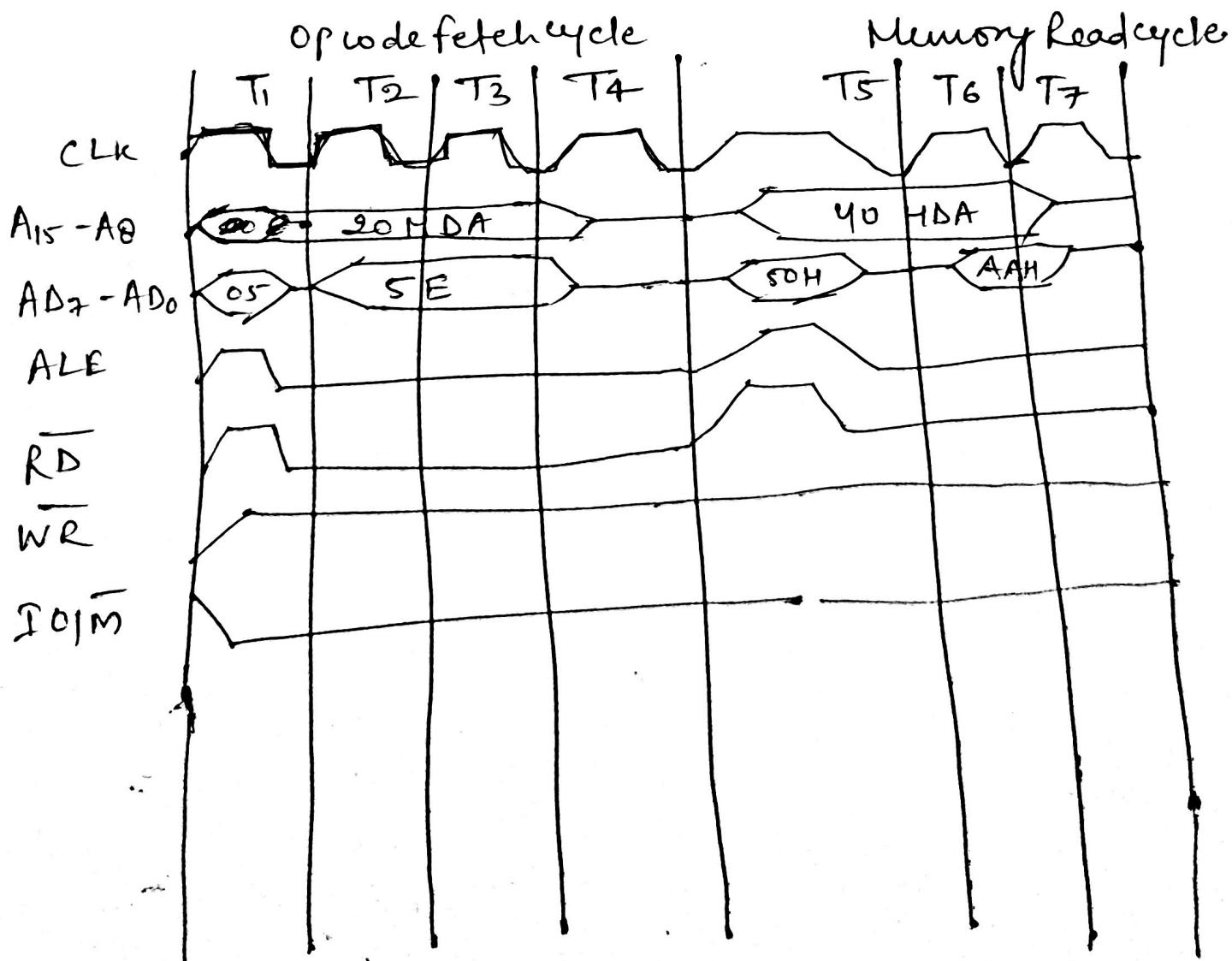
for Memory Read cycle

	Before	After
E	DBH	AAH
HL	40SDH	40SDH
40SDH	AAH	AAH

for opcode fetch cycle

Address	Hex code	Mnemonic
2005	5E	MOVE,M

TT-

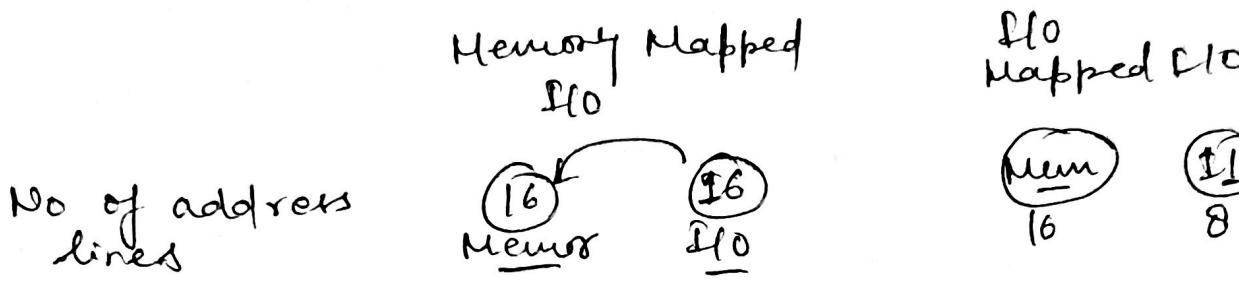


Interfacing devices -

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Peripherals are connected to CPU by two modes.

- ① Memory Mapped I/O — I/O devices are treated as memory I/O.
- ② I/O Mapped I/O mode



No of peripherals 64 KB $2^8 = 256$ I/O device

Advantage

① $I/O/M$ is not required

so no separate instruction needed

① Interfacing is less complex

② Maximum capacity of MP will be utilized.

② ALU opⁿ directly Operated can be perform of I/O data.

Disadvantage

① Interfacing is complex.

② Memory required is high

① I/O device required separate instⁿ.

② 4 control signal.