Jiajun Hu

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Education

Arizona State University (ASU) Tempe, AZ
Ph.D. in Computer Engineering 08/2024 - Present

Carnegie Mellon University (CMU) Pittsburgh, PA
Master of Science in Electrical and Computer Engineering 02/2022 – 12/2024

University of Nottingham, Ningbo, China (UNNC) Ningbo, China
Bachelor of Engineering in Electrical and Electronics Engineering 09/2017-07/2021

Skills

Programming: C/C++, Python, SystemVerilog, CUDA

Research Projects

***ReAcc-PIM*: Reuse-Aware LLMs Acceleration with Bit-Serial DRAM-PIM (under review)**

- Designed and implemented an in-DRAM bit-serial analytical performance simulator supporting end-to-end large language model (LLM) workloads with various sizes of GEMM/GEMV kernels.
- Extended the simulator to enable flexible GEMM/GEMV mapping schemes optimized for DRAM architectures, determining the optimal data layout for each LLM kernel to enhance DRAM-PIM efficiency.
- Conducted detailed area estimations for additional peripheral units integrated into DRAM using *Synopsys Design Compiler*.

***PATH-AI*: Pathfinding and Architecture Optimization for Heterogeneous AI Systems (under review)**

- Designed and implemented a comprehensive multi-systolic array modeling framework including interconnect traffic analysis, fair workload partitioning and assignment, and performance simulation.
- Developed energy and latency models for 2D, 2.5D, and 3D chiplet architectures across different integration and memory configurations.
- Integrated a simulated annealing-based cost optimization front-end to efficiently prune the large system design space under various application scenarios.

***CarbonSet*: A Dataset to Analyze Trends and Benchmark the Sustainability of CPUs and GPUs (published)**

- Compiled a comprehensive dataset of flagship CPU and GPU manufacturing and performance metrics to support sustainability and efficiency analysis.
- Extended the ECO-CHIP framework by integrating probabilistic modeling and conducting Monte Carlo simulations to estimate the carbon footprint of individual processors.
- Conducted benchmarking and trend analysis to evaluate performance-to-carbon efficiency and derive insights into processor manufacturing sustainability.

Exploring Accelerator-Level Parallelism in Sensor-Fusion applications, *CMU* Pittsburgh, PA
Supervisor: *James Hoe, Professor* 07/2023-12/2023

- Fused SYCL C++ and verified RTL modules to boost kernel performance.
- Employed CNN for camera-lidar sensor fusion feature extraction in SYCL environment.
- Benchmarked NVIDIA BEVFusion Orin SoC platform with our FPGA integrated platform for end-to-end performance and efficiency evaluation.

Selected Publication

- **Jiajun Hu**, Chetan Choppali Sudarshan, Maxwell Clifford, Vidya Chhabria, and Aman Arora. 2025. *CarbonSet: A Dataset to Analyze Trends and Benchmark the Sustainability of CPUs and GPUs*. In Proceedings of the Great Lakes Symposium on VLSI 2025 (GLSVLSI '25). Association for Computing Machinery, New York, NY, USA, 177–184. https://doi.org/10.1145/3716368.3735235