Jiajun Hu

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Education

Arizona State University (ASU) Tempe, AZ
Ph.D. in Computer Engineering 08/2024 - Present

Carnegie Mellon University (CMU) Pittsburgh, PA
Master of Science in Electrical and Computer Engineering *0*2/2022 – 12/2024

- **Courses**: Parallel Programming, Advanced Computer Architecture, Reconfigurable Computing.

University of Nottingham, Ningbo, China (UNNC) Ningbo, China
Bachelor of Engineering in Electrical and Electronics Engineering 09/2017-07/2021

Skills

Programming / Hardware Design Languages: C/C++, Python, SystemVerilog, SYCL/DPC++, CUDA
Software & Tools: Linux, git, Xilinx Vivado, Verilog, Verilator, oneAPI

Research Experiences

Exploring Accelerator-Level Parallelism in Sensor-Fusion applications, *CMU* Pittsburgh, PA
Supervisor: *James Hoe, Professor* 07/2023-12/2023

- Fused SYCL C++ and verified RTL modules to boost kernel performance.
- Employed CNN for camera-lidar sensor fusion feature extraction in SYCL environment.
- Benchmarked NVIDIA BEVFusion Orin SoC platform with our FPGA integrated platform for end-to-end performance and efficiency evaluation.

Empirical-Mode-Decomposition (EMD) enhanced Audio Denoising, *Capstone Project- UNNC* Ningbo, China
Supervisor: *Bai Shun, Assistant Professor* 06/2020-04/2021

- Developed EMD enhanced denoising signal processing algorithms for human audio under gaussian distribution background noise environment in Python.
- Applied signal framing & windowing techniques for fast signal reconstruction and information preservation.
- Compared conventional digital signal processing filter (FIR, IIR, FFT) effects in under gaussian noise distribution, in-door constant noise distribution and out-door changing noise distribution scenarios.

Selected Projects

CUDA Accelerated mmWave Radar moving object detection, *CMU* 02/2023-05/2023

- Utilized OpenMP to benchmark radar processing algorithms, achieving 2x speedup.
- Conducted CUDA version benchmarking in both single stream and multi-stream, achieved 5x speedup.
- Transferred final algorithms to FPGA through Intel OneAPI and ongoing optimization of board resource utilization and application performance.

Sparse Matrix Vector Multiplication (SpMV) FPGA Acceleration, *CMU* 02/2023-05/2023

- Applying data-streaming interfaces for fast data accessing and operation decoupling.
- Deploying multiple streaming-compute kernels for parallel processing by reducing the FIFO port requirements of CSR format.
- Quantitating the significance performance factors in terms of memory access pattern, loop unrolling/pipeline dependencies and logic resources mapping utilization.

Modern Out-of-Order processor techniques implementation, *CMU* 09/2022-12/2022

- Developed C implementations of traditional branch predictor algorithms, encompassing the 2-level branch predictor (utilizing global and local history), the perceptron branch predictor, and a hybrid branch predictor.
- Designed a 64-entry issue queue and a 128-entry reorder buffer (ROB) in SystemVerilog.
- Employed McPAT and Gem5 open-source simulation tools to assess implementation performance and power consumption across various benchmarks.