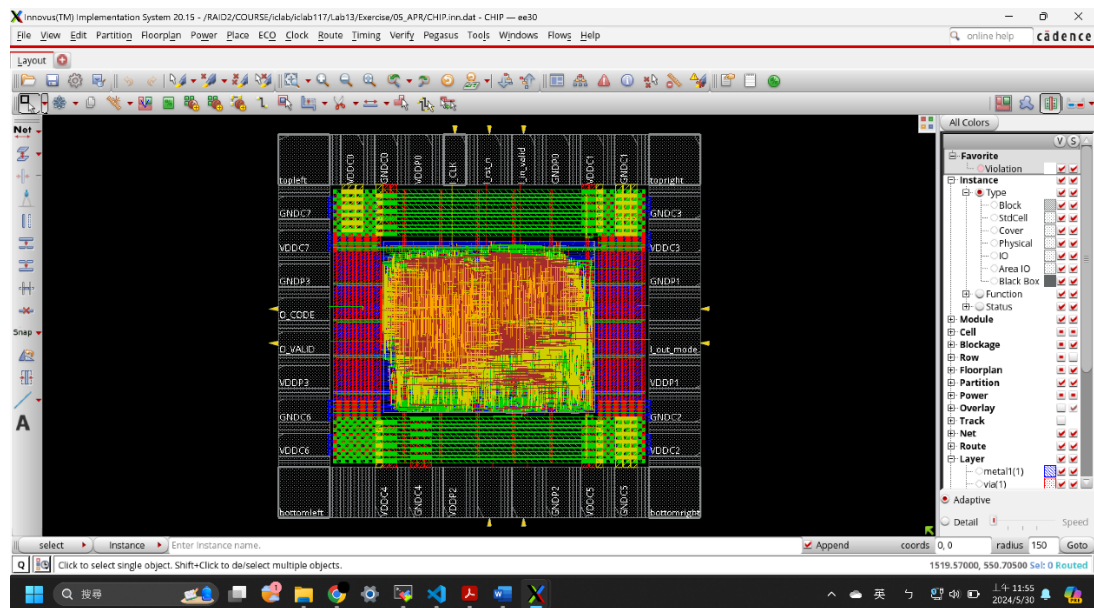
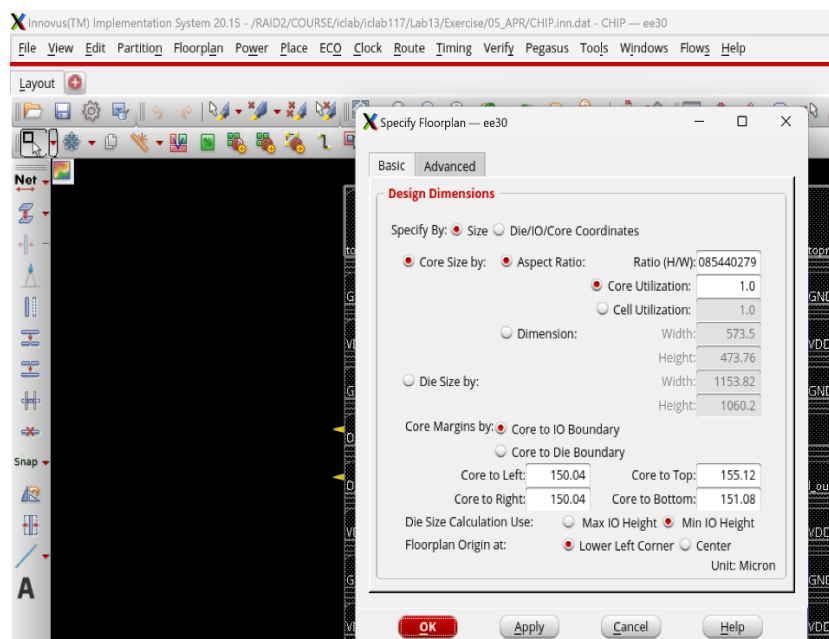


Report

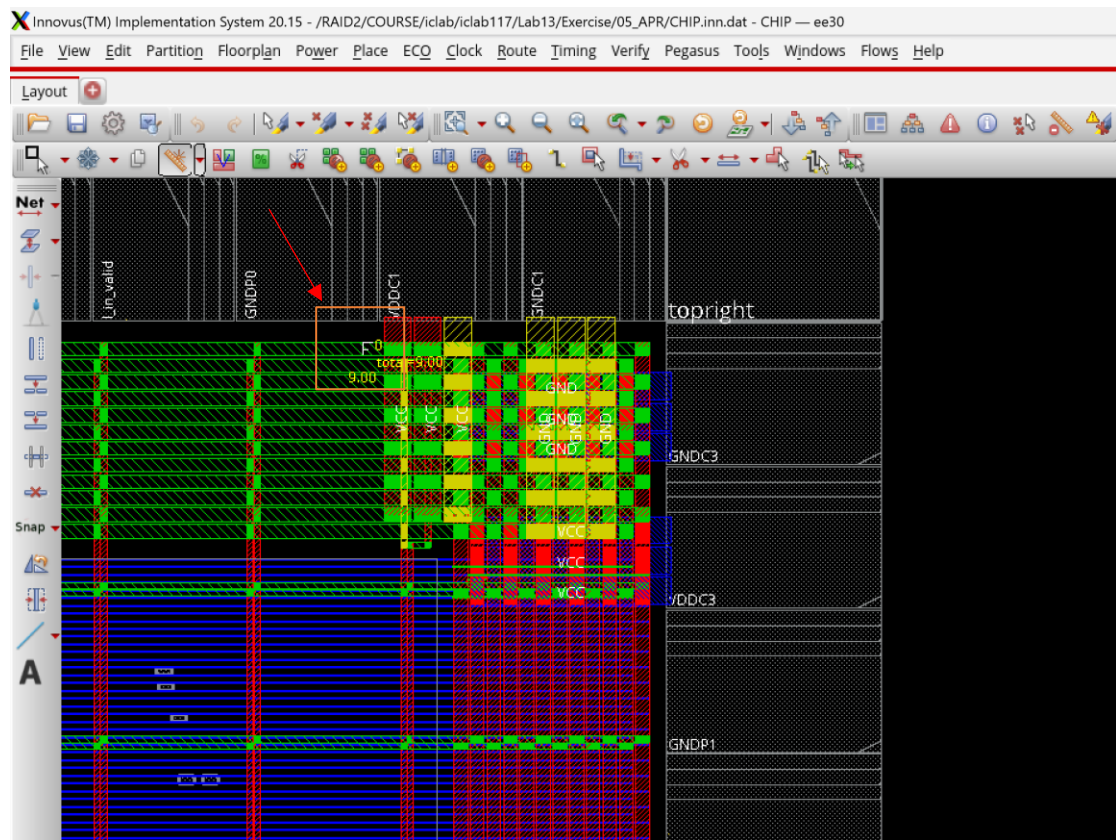
1. Chip Layout View :



2. Core to IO boundary :



3. Core Ring :



4. Post-Route setup time analysis :

ck connect...

2. ee30.jee.nycu.edu.tw (iclab117)

RAID2/COURSE/iclab/iclab117/Lab13/Exercise/05_APR/CHIP.inn.dat - CHIP — ee30

File View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify Pegasus Tools Windows Flows Help

Layout

Net

Snap

A

timeDesign Summary

Setup views included:
av_func_mode_max

Setup mode	all	reg2reg	default
WNS (ns):	0.489	0.489	3.502
TNS (ns):	0.000	0.000	0.000
Violating Paths:	0	0	0
All Paths:	371	281	370

DRVs	Real		Total
	Nr nets(terms)	Worst Vio	Nr nets(terms)
max_cap	0 (0)	0.000	0 (0)
max_tran	0 (0)	0.000	0 (0)
max_fanout	0 (0)	0	0 (0)
max_length	0 (0)	0	0 (0)

Density: 68.851%

Total number of glitch violations: 0

Reported timing to dir timingReports

Total CPU time: 22.05 sec

Total Real time: 24.0 sec

Total Memory Usage: 2636.78125 Mbytes

Reset AAE Options

*** timeDesign #4 [finish] : cpu/real = 0:00:22.1/0:00:24.3 (0.9), totSession cpu/real = 0:04:33.2/0:25

innovus 10>

5. Post-Route hold time analysis :

```
ck connect...
/RAID2/COURSE/iclab/iclab117/Lab13/Exer...

Name
  CHIP_floorplan.inn.dat
  CeltIC
  .cadence
  rc_model.bin
  pegasus_ui_gui.log
  makefile
  innovus.logv1
  innovus.logv
  innovus.log1
  innovus.log
  innovus.cmd1
  innovus.cmd
  HT_TOP_SYN.v
  CHIP_SYN.v
  CHIP_SHELL.v
  CHIP_mmmc.view
  CHIP_floorplan.inn
  CHIP_cts.sdc
  CHIP.sdc
  CHIP.io
  CHIP_globals
  CHIP.drc.rpt.old
  CHIP.drc.rpt
  CHIP.conn.rpt.old
  CHIP.conn.rpt
  CHIP.CCOPT.spec
  09_clean_up
  00_combine

Remote monitoring
Follow terminal folder

End delay calculation (fullDC). (MEM=2837.95 CPU=0:00:02.4 REAL=0:00:02.0)
Loading CTE timing window with TwFlowType 0...(CPU = 0:00:00.0, REAL = 0:00:00.0, MEM = 2838.0M)
Add other clocks and setupCteToAAEClockMapping during iter 1
Loading CTE timing window is completed (CPU = 0:00:00.0, REAL = 0:00:00.0, MEM = 2838.0M)
Starting SI iteration 2
Start delay calculation (fullDC) (1 T). (MEM=2801.07)
Glitch Analysis: View av_func_mode_min -- Total Number of Nets Skipped = 0.
Glitch Analysis: View av_func_mode_min -- Total Number of Nets Analyzed = 8897.
Total number of fetched objects 8897
AAE_INFO: Total number of nets for which stage creation was skipped for all views 0
AAE_INFO-618: Total number of nets in the design is 8876, 0.0 percent of the nets selected for SI analysis
End delay calculation. (MEM=2839.23 CPU=0:00:00.1 REAL=0:00:01.0)
End delay calculation (fullDC). (MEM=2839.23 CPU=0:00:00.1 REAL=0:00:01.0)
*** Done Building Timing Graph (cpu=0:00:03.0 real=0:00:03.0 totSessionCpu=0:04:43 mem=2839.2M)

-----
timeDesign Summary
-----

Hold views included:
av_func_mode_min

+-----+-----+-----+-----+
| Hold mode | all | reg2reg | default |
+-----+-----+-----+-----+
| WNS (ns) | 0.227 | 0.227 | 9.768 |
| TNS (ns) | 0.000 | 0.000 | 0.000 |
| Violating Paths | 0 | 0 | 0 |
| All Paths | 371 | 281 | 370 |
+-----+-----+-----+-----+

Density: 68.851%

Reported timing to dir timingReports
Total CPU time: 3.6 sec
Total Real time: 4.0 sec
Total Memory Usage: 2772.492188 Mbytes
Reset AAE Options
*** timeDesign #5 [finish] : cpu/real = 0:00:03.6/0:00:03.9 (0.9), totSession cpu/real = 0:04:43.5/0:29:29.6 (0.2), m
innovus 10>
```

6. DRC result :

```
ck connect...
/RAID2/COURSE/iclab/iclab117/Lab13/Exer...

Name
  CHIP_floorplan.inn.dat
  CeltIC
  .cadence
  rc_model.bin
  pegasus_ui_gui.log
  makefile
  innovus.logv1
  innovus.logv
  innovus.log1
  innovus.log
  innovus.cmd1
  innovus.cmd
  HT_TOP_SYN.v
  CHIP_SYN.v
  CHIP_SHELL.v
  CHIP_mmmc.view
  CHIP_floorplan.inn
  CHIP_cts.sdc
  CHIP.sdc
  CHIP.io
  CHIP_globals
  CHIP.drc.rpt.old
  CHIP.drc.rpt
  CHIP.conn.rpt.old
  CHIP.conn.rpt
  CHIP.CCOPT.spec
  09_clean_up
  00_combine

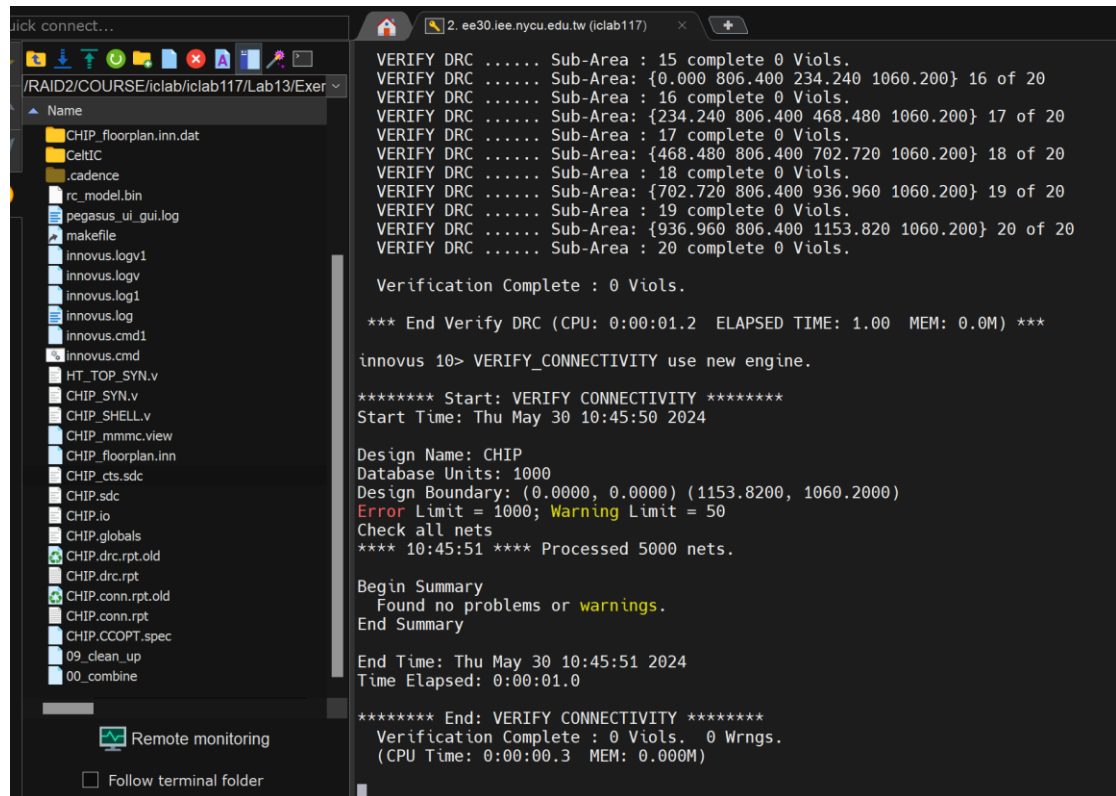
Remote monitoring
Follow terminal folder

VERIFY DRC ..... Sub-Area: {702.720 0.000 936.960 268.800} 4 of 20
VERIFY DRC ..... Sub-Area: 4 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {936.960 0.000 1153.820 268.800} 5 of 20
VERIFY DRC ..... Sub-Area: 5 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 268.800 234.240 537.600} 6 of 20
VERIFY DRC ..... Sub-Area: 6 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {234.240 268.800 468.480 537.600} 7 of 20
VERIFY DRC ..... Sub-Area: 7 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {468.480 268.800 702.720 537.600} 8 of 20
VERIFY DRC ..... Sub-Area: 8 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {702.720 268.800 936.960 537.600} 9 of 20
VERIFY DRC ..... Sub-Area: 9 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {936.960 268.800 1153.820 537.600} 10 of 20
VERIFY DRC ..... Sub-Area: 10 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 537.600 234.240 806.400} 11 of 20
VERIFY DRC ..... Sub-Area: 11 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {234.240 537.600 468.480 806.400} 12 of 20
VERIFY DRC ..... Sub-Area: 12 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {468.480 537.600 702.720 806.400} 13 of 20
VERIFY DRC ..... Sub-Area: 13 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {702.720 537.600 936.960 806.400} 14 of 20
VERIFY DRC ..... Sub-Area: 14 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {936.960 537.600 1153.820 806.400} 15 of 20
VERIFY DRC ..... Sub-Area: 15 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 806.400 234.240 1060.200} 16 of 20
VERIFY DRC ..... Sub-Area: 16 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {234.240 806.400 468.480 1060.200} 17 of 20
VERIFY DRC ..... Sub-Area: 17 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {468.480 806.400 702.720 1060.200} 18 of 20
VERIFY DRC ..... Sub-Area: 18 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {702.720 806.400 936.960 1060.200} 19 of 20
VERIFY DRC ..... Sub-Area: 19 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {936.960 806.400 1153.820 1060.200} 20 of 20
VERIFY DRC ..... Sub-Area: 20 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:01.2 ELAPSED TIME: 1.00 MEM: 0.0M) ***
innovus 10>
```

7. LVS result :



```
VERIFY DRC ..... Sub-Area : 15 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 806.400 234.240 1060.200} 16 of 20
VERIFY DRC ..... Sub-Area : 16 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {234.240 806.400 468.480 1060.200} 17 of 20
VERIFY DRC ..... Sub-Area : 17 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {468.480 806.400 702.720 1060.200} 18 of 20
VERIFY DRC ..... Sub-Area : 18 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {702.720 806.400 936.960 1060.200} 19 of 20
VERIFY DRC ..... Sub-Area : 19 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {936.960 806.400 1153.820 1060.200} 20 of 20
VERIFY DRC ..... Sub-Area : 20 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:01.2 ELAPSED TIME: 1.00 MEM: 0.0M) ***

innovus 10> VERIFY_CONNECTIVITY use new engine.

***** Start: VERIFY CONNECTIVITY *****
Start Time: Thu May 30 10:45:50 2024

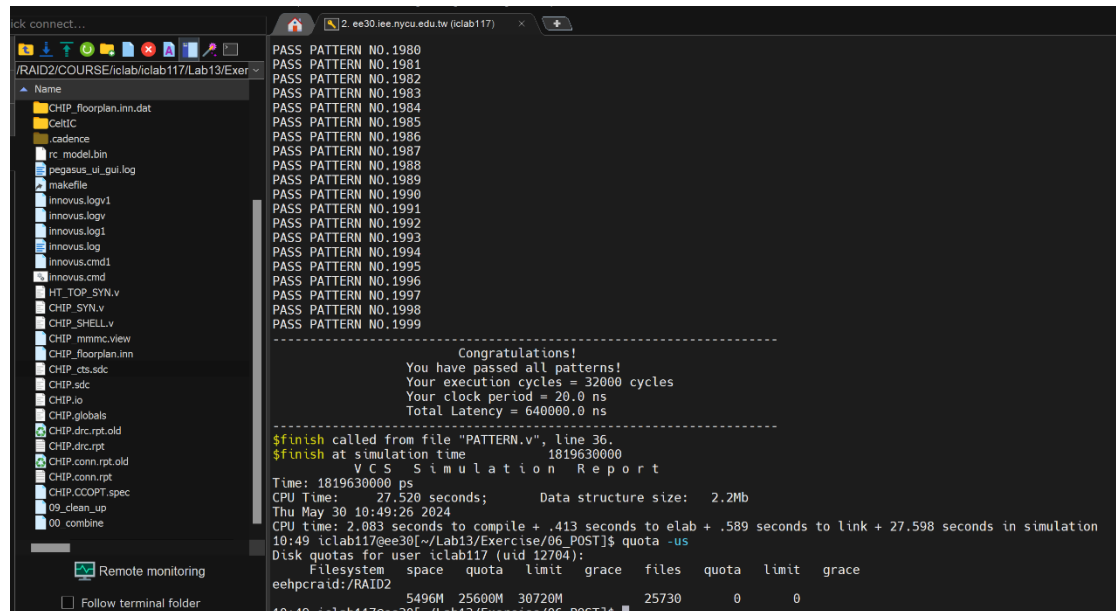
Design Name: CHIP
Database Units: 1000
Design Boundary: (0.0000, 0.0000) (1153.8200, 1060.2000)
Error Limit = 1000; Warning Limit = 50
Check all nets
**** 10:45:51 **** Processed 5000 nets.

Begin Summary
Found no problems or warnings.
End Summary

End Time: Thu May 30 10:45:51 2024
Time Elapsed: 0:00:01.0

***** End: VERIFY CONNECTIVITY *****
Verification Complete : 0 Viols. 0 Wrngs.
(CPU Time: 0:00:00.3 MEM: 0.000M)
```

8. Post Layout simulation result :



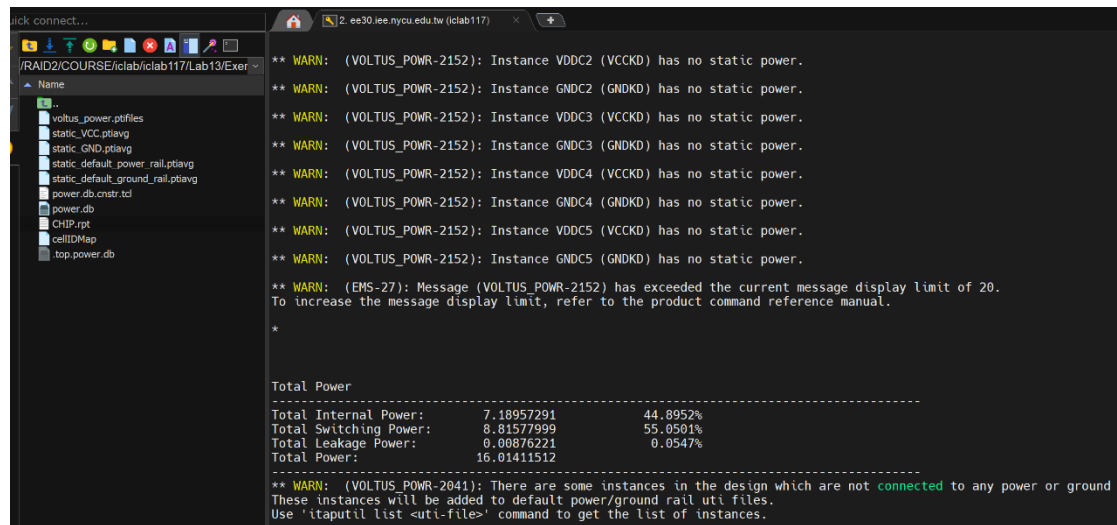
```
PASS PATTERN NO. 1980
PASS PATTERN NO. 1981
PASS PATTERN NO. 1982
PASS PATTERN NO. 1983
PASS PATTERN NO. 1984
PASS PATTERN NO. 1985
PASS PATTERN NO. 1986
PASS PATTERN NO. 1987
PASS PATTERN NO. 1988
PASS PATTERN NO. 1989
PASS PATTERN NO. 1990
PASS PATTERN NO. 1991
PASS PATTERN NO. 1992
PASS PATTERN NO. 1993
PASS PATTERN NO. 1994
PASS PATTERN NO. 1995
PASS PATTERN NO. 1996
PASS PATTERN NO. 1997
PASS PATTERN NO. 1998
PASS PATTERN NO. 1999

-----
Congratulations!
You have passed all patterns!
Your execution cycles = 32000 cycles
Your clock period = 20.0 ns
Total Latency = 640000.0 ns
-----

$finish called from file "PATTERN.v", line 36.
$finish at simulation time 1819630000
VCS Simulation Report

Time: 1819630000 ns
CPU Time: 27.520 seconds; Data structure size: 2.2Mb
Thu May 30 10:49:26 2024
CPU time: 2.083 seconds to compile + .413 seconds to elab + .589 seconds to link + 27.598 seconds in simulation
10:49 iclab117@ee30[~/Lab13/Exercise/06_POST] $ quota -us
Disk quotas for user iclab117 (uid 12704):
Filesystem space quota limit grace files quota limit grace
eehpcraid:/RAID2 5496M 25600M 30720M 25730 0 0
10:49 iclab117@ee30[~/Lab13/Exercise/06_POST] $
```


9. Power result :



10. IR Drop Results :

Ways to mitigate IR drop: More core power pad, increasing width & numbers of power strip

