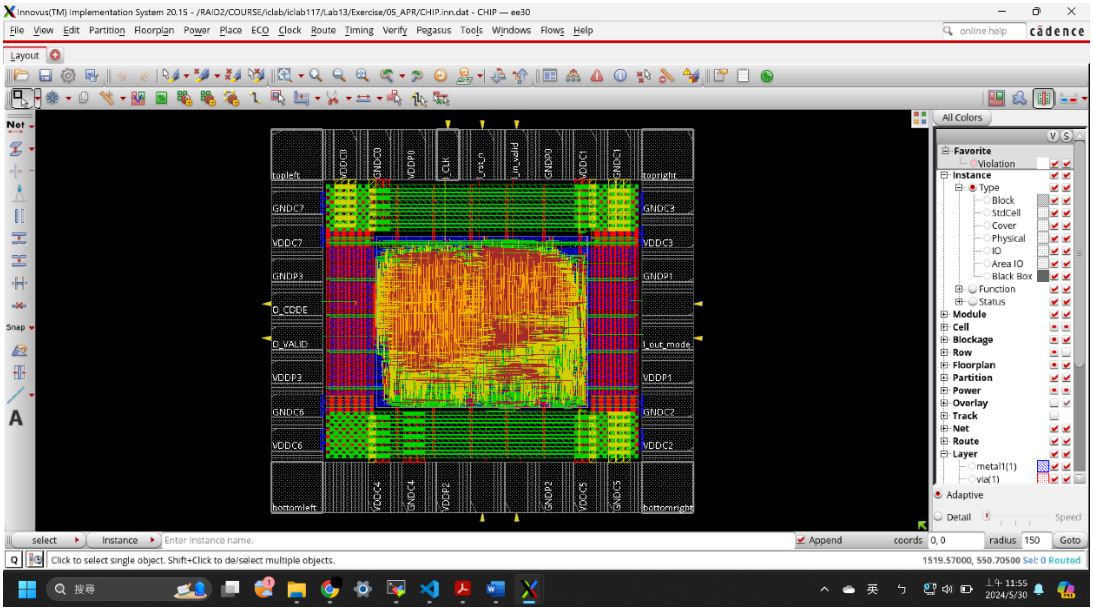
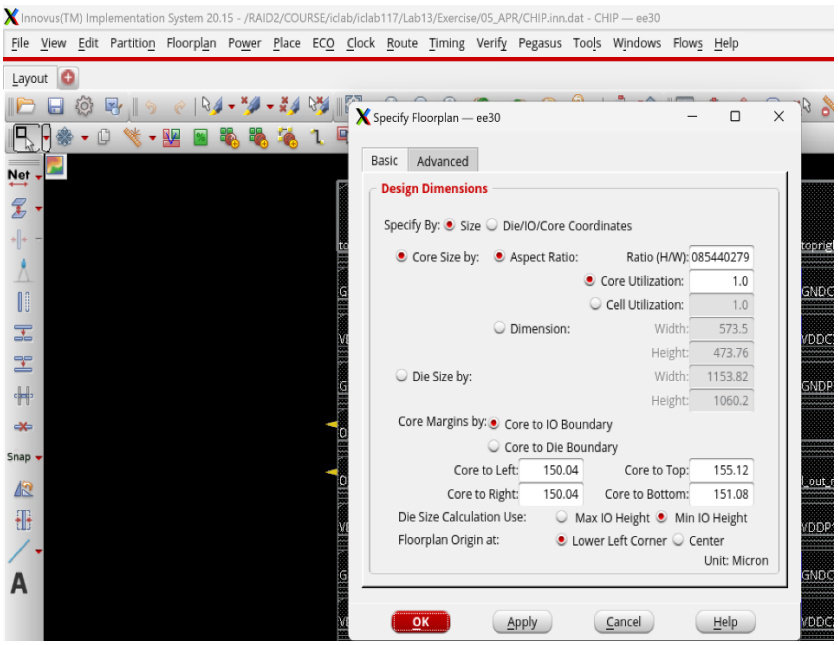
Report

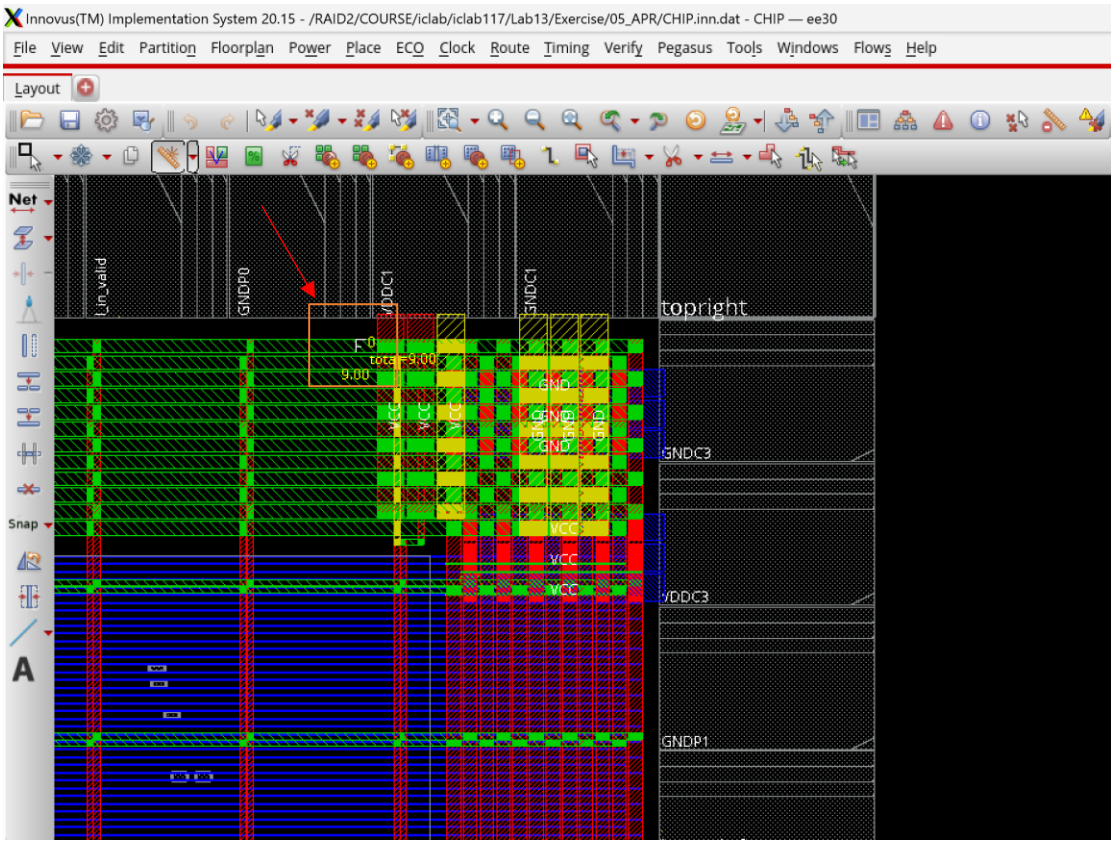
1. Chip Layout View :



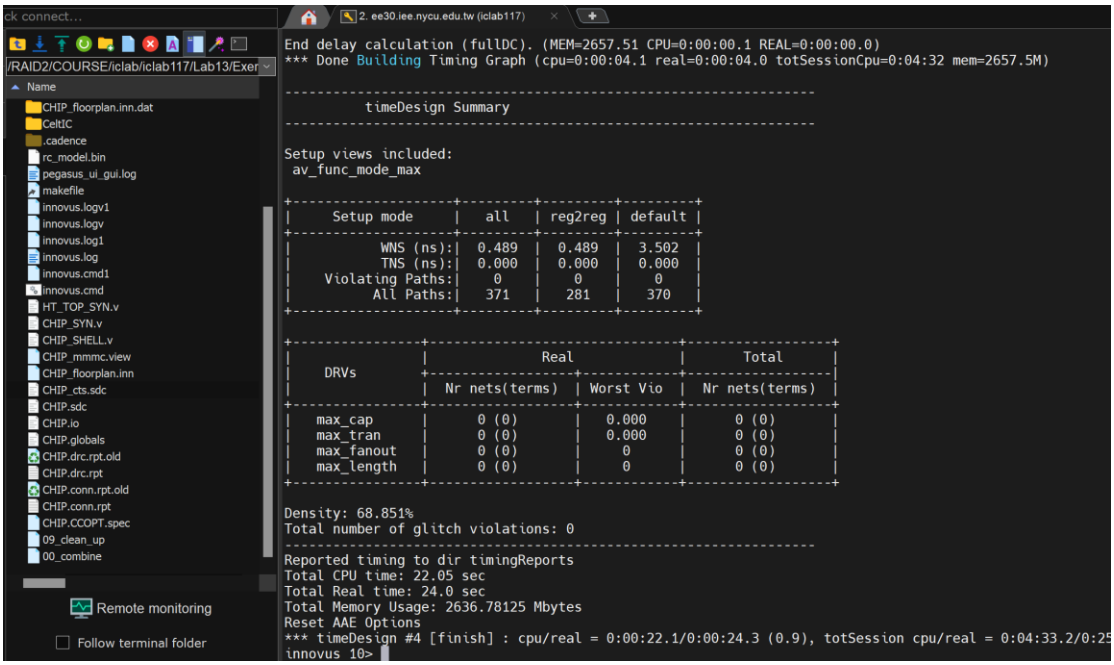
2. Core to IO boundary :



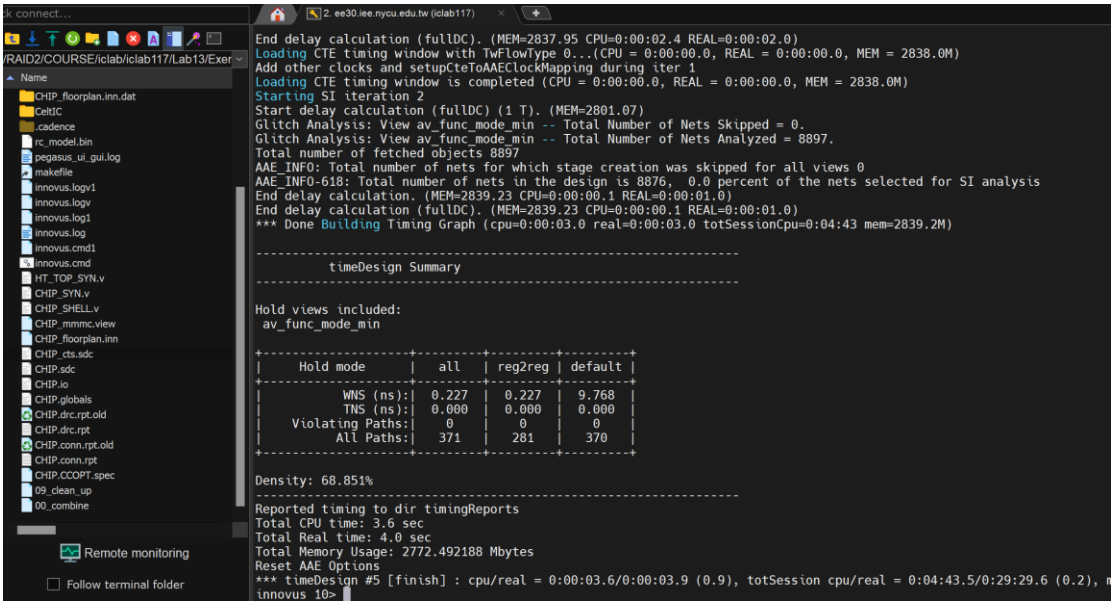
3. Core Ring :



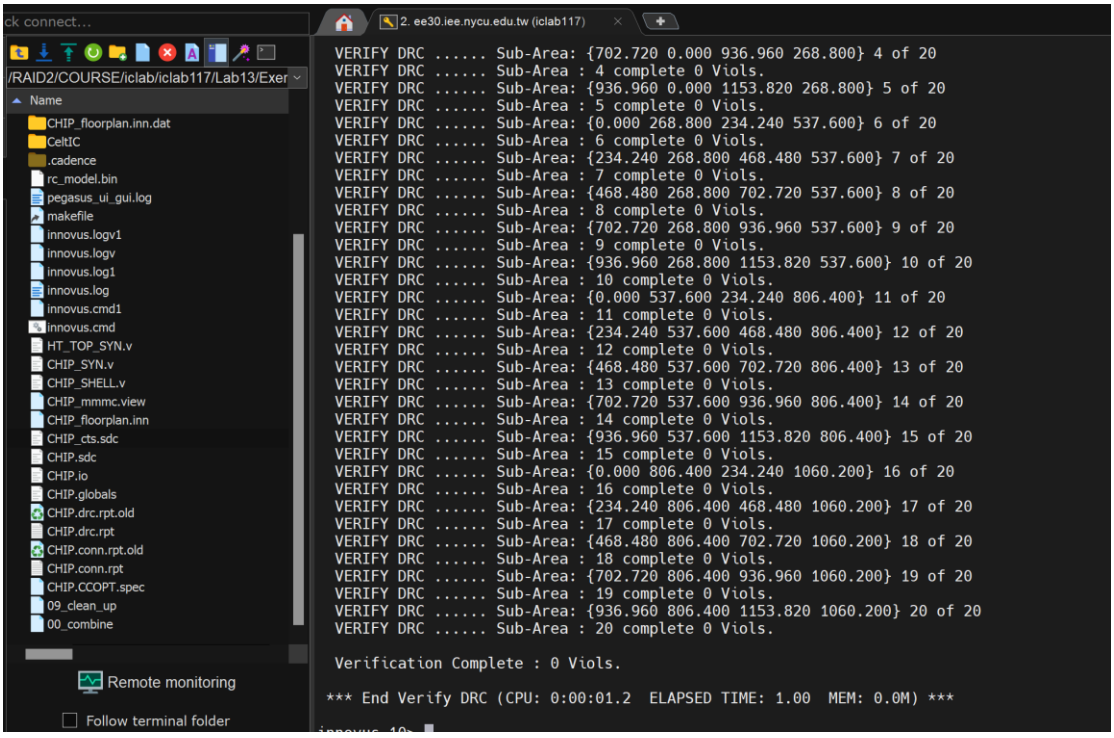
4. Post-Route setup time analysis :



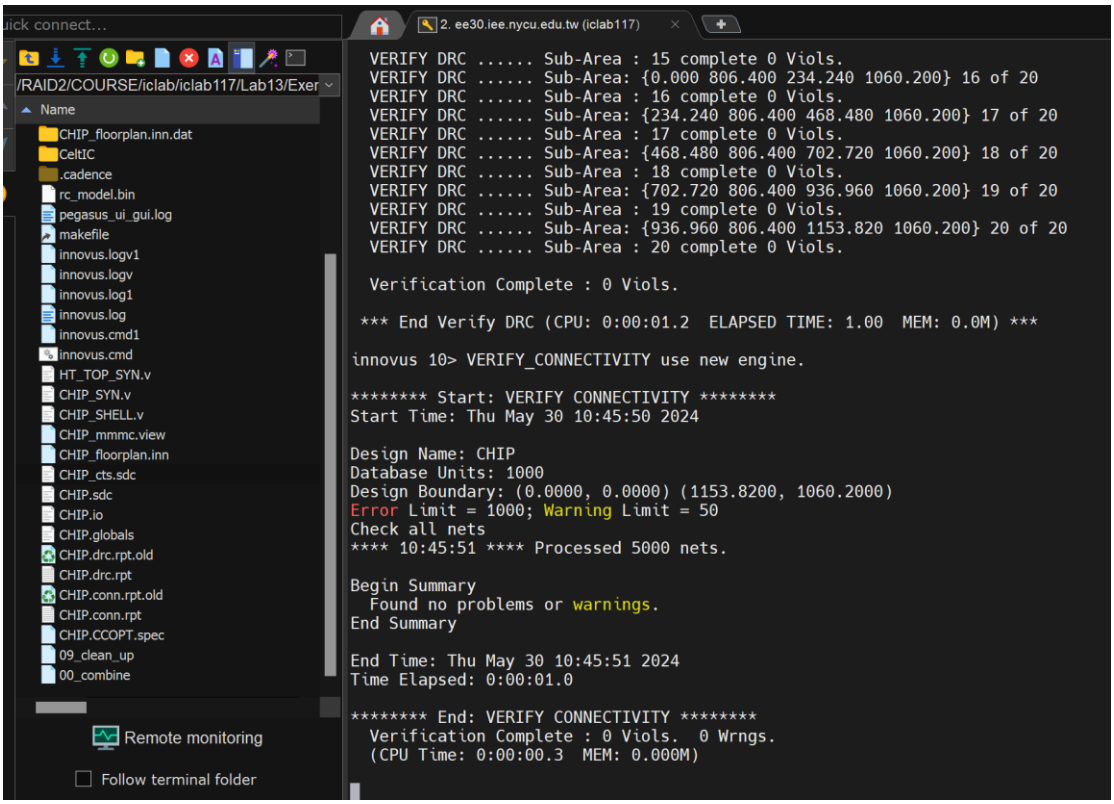
5. Post-Route hold time analysis :



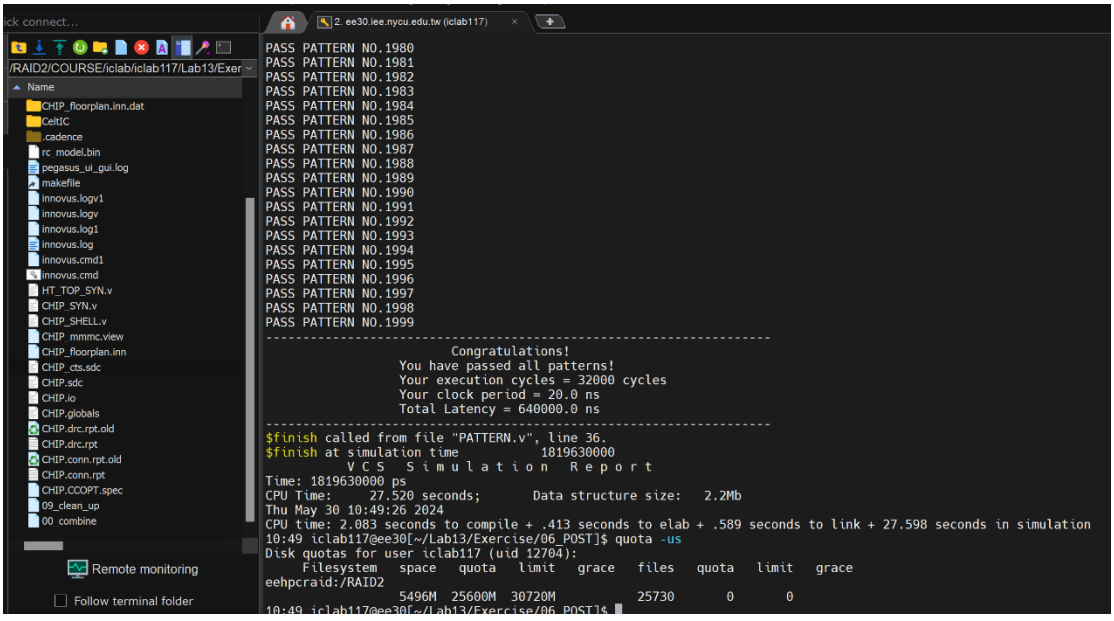
6. DRC result :



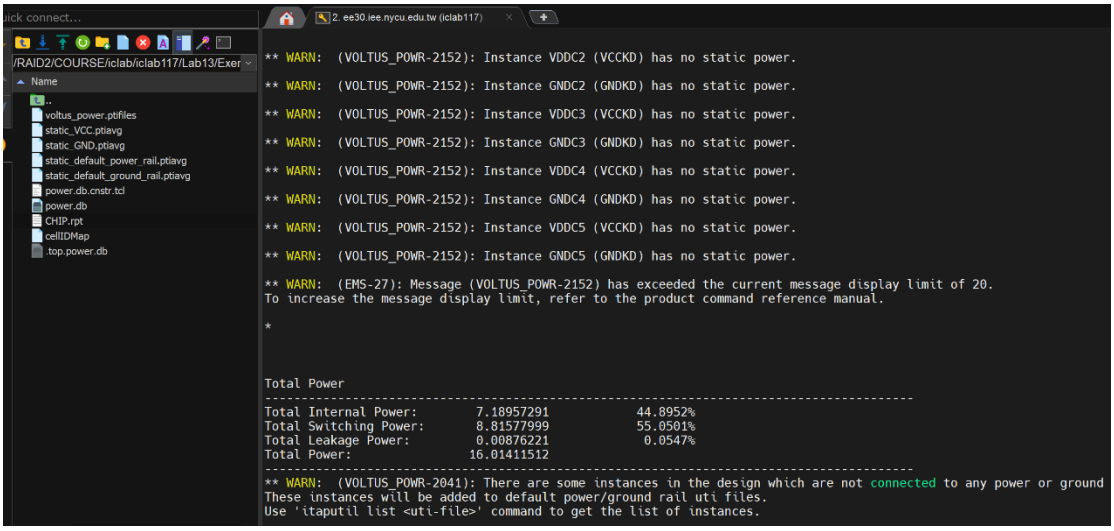
7. LVS result :



8. Post Layout simulation result :



9. Power result :



10. IR Drop Results :

Ways to mitigate IR drop: More core power pad, increasing width & numbers of power strip