第09次實習課

學生：林培瑋

2024 Advanced Mixed-Operation System (AMOS) Lab.

Tamkang University
Department of Electrical and Computer Engineering
No.151, Yingzhuan Rd., Tamsui Dist., New Taipei City 25137, Taiwan (R.O.C.)

第一次作業

2024 Advanced Mixed-Operation System (AMOS) Lab.

Tamkang University
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評分標準

- 第一部分(60%)：
  - 第1題(20%)：輸出正確，並包含F5、F10、F11執行結果&心得。
  - 第2題(20%)：輸出正確反向字串，並包含F5、F10、F11執行結果(&心得)。
  - 第3題(20%)：UART0視窗顯示大約9600 baud。
- 第二部分(40%)：
  - 加入Receive(20%)： (F5、)F10、F11執行結果&心得。
  - 加入三種錯誤偵測(20%)：(F5、)F10、F11執行結果(&心得)。

➢ 不計分：截圖中**看不到學號、姓名**。
➢ 一半分數：截圖不完整、心得不完整。
➢ 以最後繳交的版本為準。
➢ 遲交者分數 = 原始分數*0.5

第一次作業-UART初始化

2024 Advanced Mixed-Operation System (AMOS) Lab.

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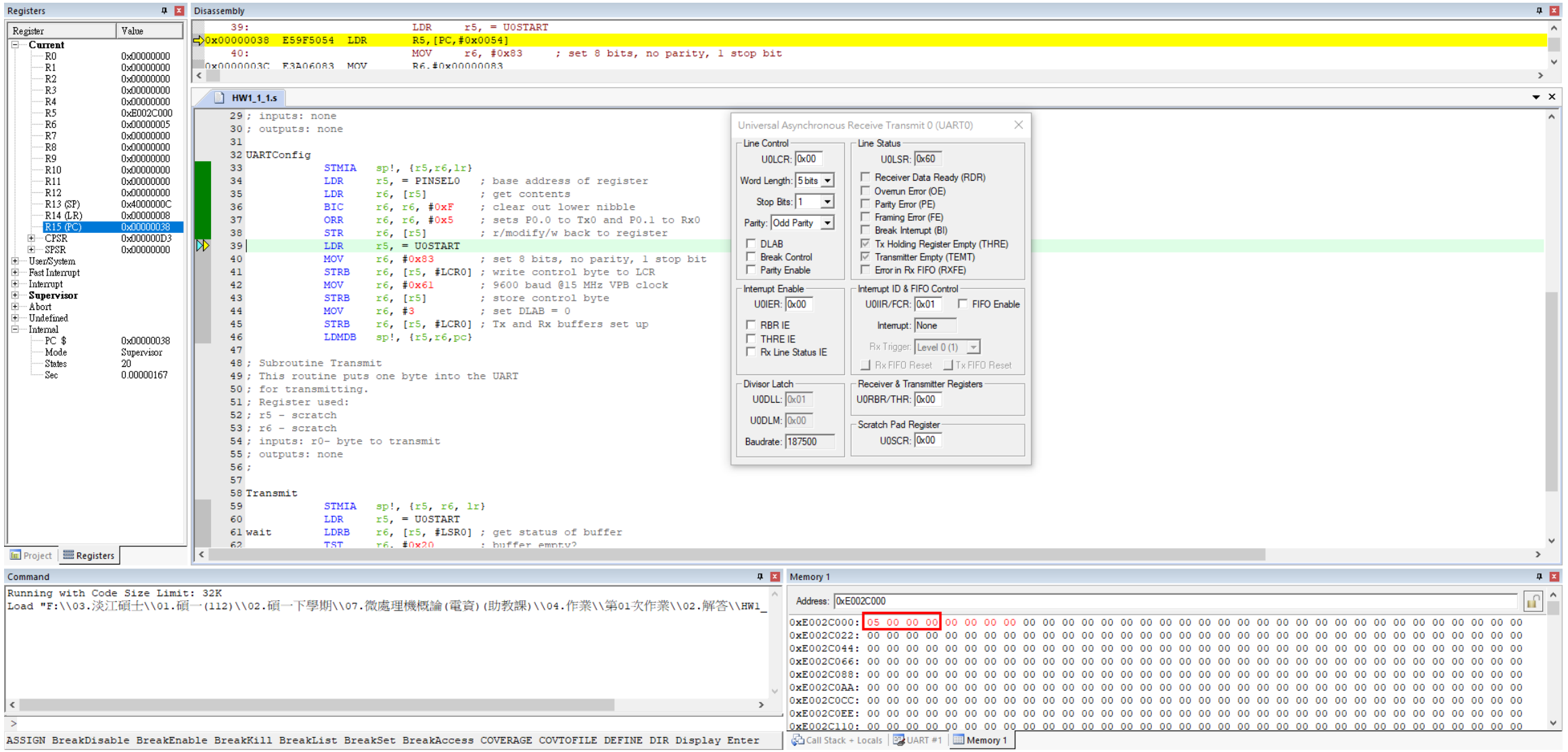
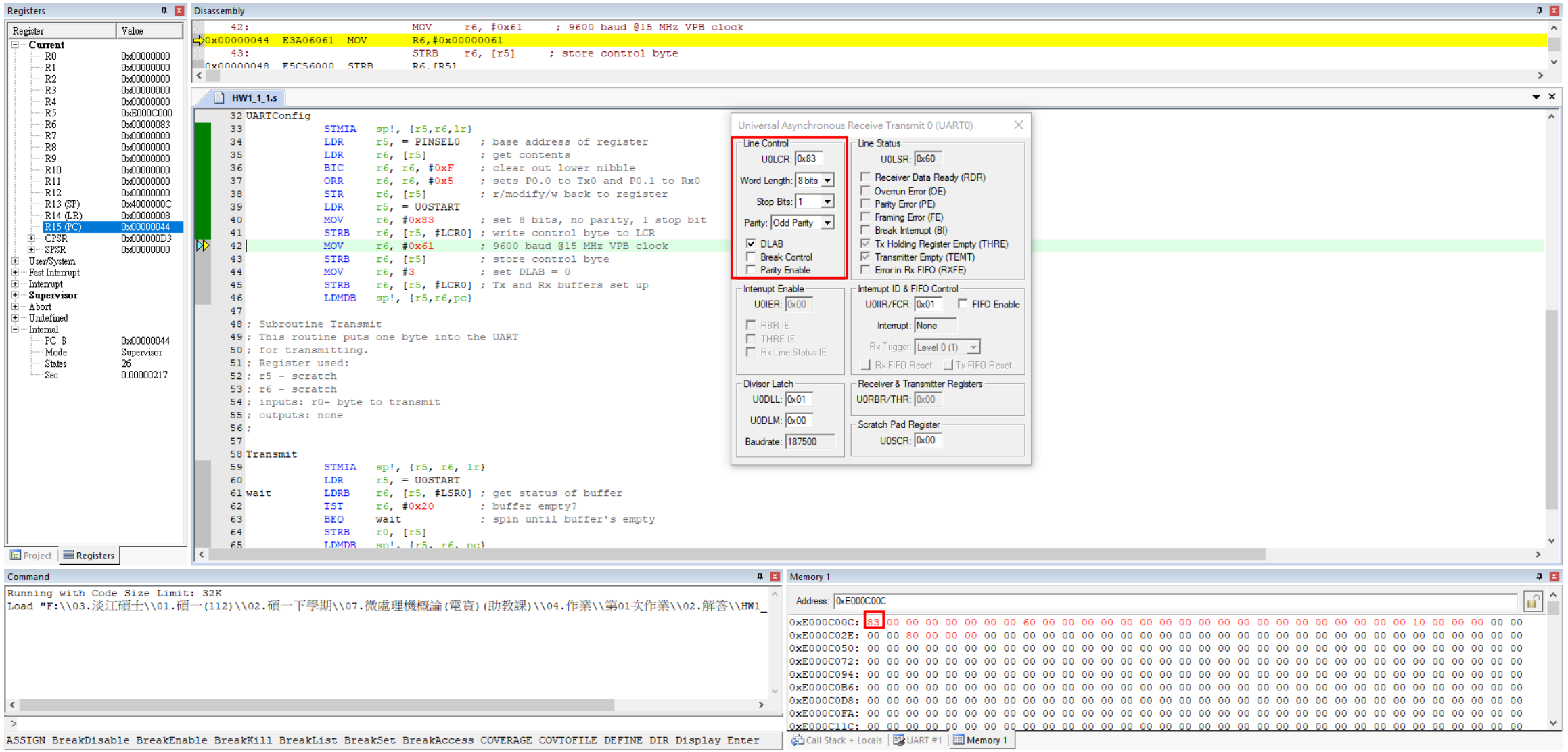
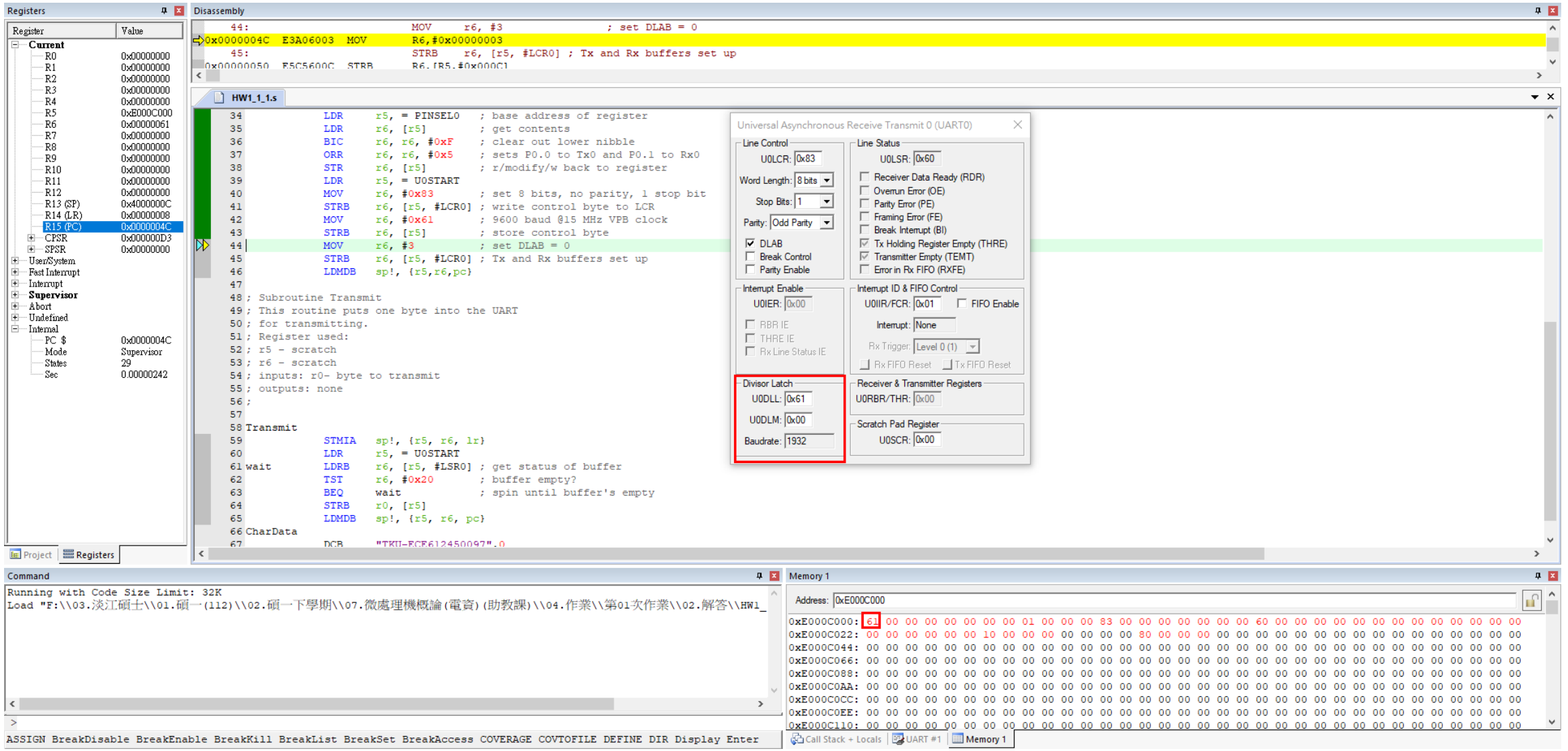
設定Tx、Rx腳位


Registers
Register
Value
Current
R0 0x00000000
R1 0x00000000
R2 0x00000000
R3 0x00000000
R4 0x00000000
R5 0xE002C000
R6 0x00000005
R7 0x00000000
R8 0x00000000
R9 0x00000000
R10 0x00000000
R11 0x00000000
R12 0x00000000
R13 (SP) 0x4000000C
R14 (LR) 0x00000008
R15 (PC) 0x00000038
CPSR 0x000000D3
SPSR 0x00000000
User/System
Fast Interrupt
Interrupt
Supervisor
Abort
Undefined
Internal
PC $ 0x00000038
Mode Supervisor
States 20
Sec 0.00000167
Project
Registers
Disassembly
39: LDR r5, = U0START
0x00000038 E59F5054 LDR R5,[PC,#0x0054]
40: MOV r6, #0x83 ; set 8 bits, no parity, 1 stop bit
0x0000003C E3A06083 MOV R6,#0x00000083
HW1_1_1.s
29 ; inputs: none
30 ; outputs: none
31
32 UARTConfig
33 STMIA sp!, {r5,r6,lr}
34 LDR r5, = PINSEL0 ; base address of register
35 LDR r6, [r5] ; get contents
36 BIC r6, r6, #0xF ; clear out lower nibble
37 ORR r6, r6, #0x5 ; sets P0.0 to Tx0 and P0.1 to Rx0
38 STR r6, [r5] ; r/modify/w back to register
39 LDR r5, = U0START
40 MOV r6, #0x83 ; set 8 bits, no parity, 1 stop bit
41 STRB r6, [r5, #LCR0] ; write control byte to LCR
42 MOV r6, #0x61 ; 9600 baud @15 MHz VPB clock
43 STRB r6, [r5] ; store control byte
44 MOV r6, #3 ; set DLAB = 0
45 STRB r6, [r5, #LCR0] ; Tx and Rx buffers set up
46 LDMDB sp!, {r5,r6,pc}
47
48 ; Subroutine Transmit
49 ; This routine puts one byte into the UART
50 ; for transmitting.
51 ; Register used:
52 ; r5 - scratch
53 ; r6 - scratch
54 ; inputs: r0- byte to transmit
55 ; outputs: none
56 ;
57
58 Transmit
59 STMIA sp!, {r5, r6, lr}
60 LDR r5, = U0START
61 wait LDRB r6, [r5, #LSR0] ; get status of buffer
62 TST r6, #0x20 ; buffer empty?
Universal Asynchronous Receive Transmit 0 (UART0)
Line Control
U0LCR: 0x00
Word Length: 5 bits
Stop Bits: 1
Parity: Odd Parity
DLAB
Break Control
Parity Enable
Line Status
U0LSR: 0x60
Receiver Data Ready (RDR)
Overrun Error (OE)
Parity Error (PE)
Framing Error (FE)
Break Interrupt (BI)
Tx Holding Register Empty (THRE)
Transmitter Empty (TEMT)
Error in Rx FIFO (RXFE)
Interrupt Enable
U0IER: 0x00
RBR IE
THRE IE
Rx Line Status IE
Interrupt ID & FIFO Control
U0IIR/FCR: 0x01
FIFO Enable
Interrupt: None
Rx Trigger: Level 0 (1)
Rx FIFO Reset
Tx FIFO Reset
Divisor Latch
U0DLL: 0x01
U0DLM: 0x00
Baudrate: 187500
Receiver & Transmitter Registers
U0RBR/THR: 0x00
Scratch Pad Register
U0SCR: 0x00
Command
Running with Code Size Limit: 32K
Load "F:\\03.淡江碩士\\01.碩一(112)\\02.碩一下學期\\07.微處理機概論(電資)(助教課)\\04.作業\\第01次作業\\02.解答\\HW1_
ASSIGN BreakDisable BreakEnable BreakKill BreakList BreakSet BreakAccess COVERAGE COVTOFILE DEFINE DIR Display Enter
Memory 1
Address: 0xE002C000
0xE002C000: 05 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0xE002C022: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0xE002C044: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0xE002C066: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0xE002C088: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0xE002C0AA: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0xE002C0CC: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0xE002C0EE: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0xE002C110: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
Call Stack + Locals
UART #1
Memory 1

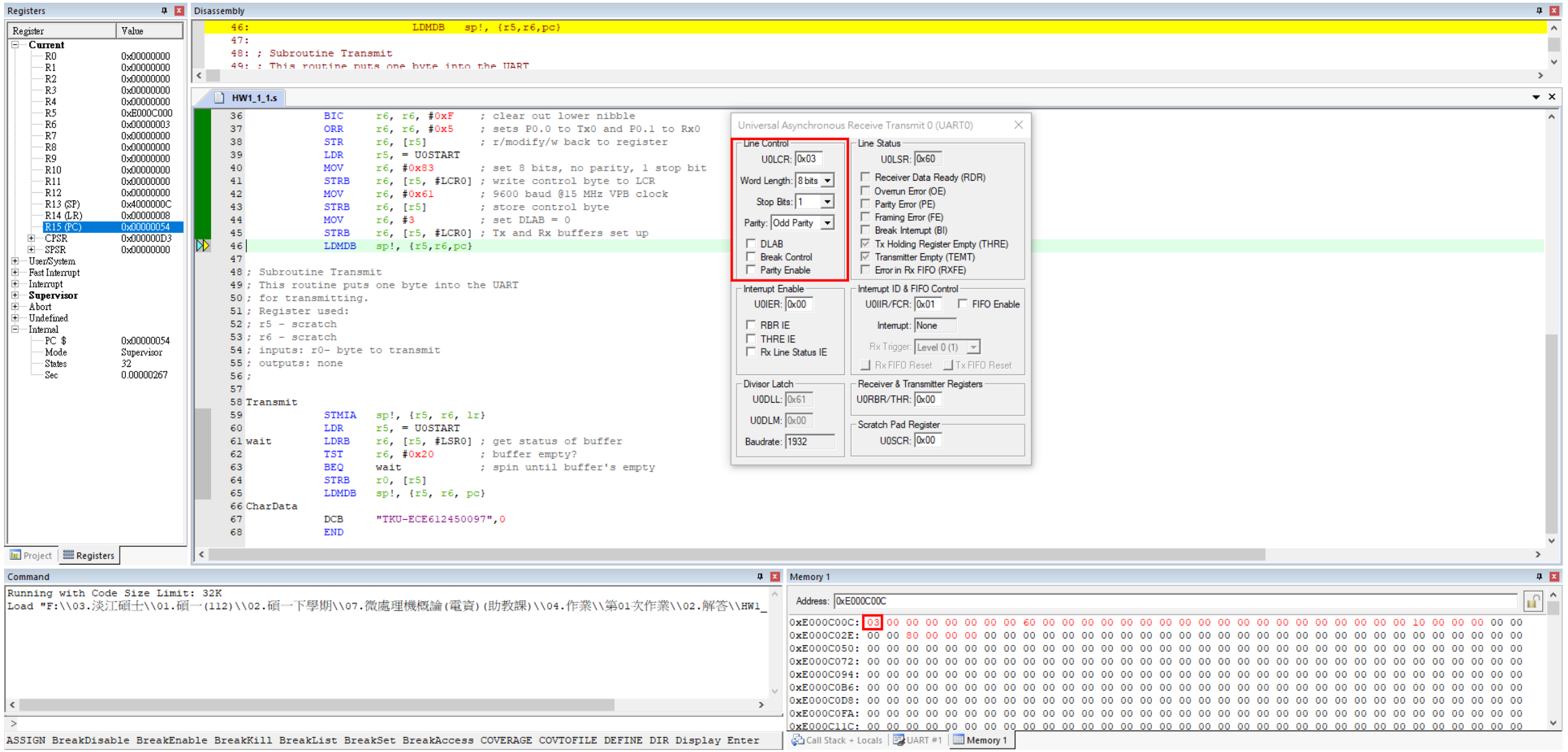
設定資料傳輸格式(DLAB=1)



設定速率


Registers
Register
Value
Current
R0 0x00000000
R1 0x00000000
R2 0x00000000
R3 0x00000000
R4 0x00000000
R5 0xE000C000
R6 0x00000061
R7 0x00000000
R8 0x00000000
R9 0x00000000
R10 0x00000000
R11 0x00000000
R12 0x00000000
R13 (SP) 0x4000000C
R14 (LR) 0x00000008
R15 (PC) 0x0000004C
CPSR 0x000000D3
SPSR 0x00000000
UserSystem
Fast Interrupt
Interrupt
Supervisor
Abort
Undefined
Internal
PC $ 0x0000004C
Mode Supervisor
States 29
Sec 0.00000242
Project
Registers
Disassembly
44: MOV r6, #3 ; set DLAB = 0
0x0000004C E3A06003 MOV R6,#0x00000003
45: STRB r6, [r5, #LCR0] ; Tx and Rx buffers set up
0x00000050 E5C5600C STRB R6,[R5,#0x000C]
HW1_1_1.s
34 LDR r5, = PINSEL0 ; base address of register
35 LDR r6, [r5] ; get contents
36 BIC r6, r6, #0xF ; clear out lower nibble
37 ORR r6, r6, #0x5 ; sets P0.0 to Tx0 and P0.1 to Rx0
38 STR r6, [r5] ; r/modify/w back to register
39 LDR r5, = U0START
40 MOV r6, #0x83 ; set 8 bits, no parity, 1 stop bit
41 STRB r6, [r5, #LCR0] ; write control byte to LCR
42 MOV r6, #0x61 ; 9600 baud @15 MHz VPB clock
43 STRB r6, [r5] ; store control byte
44 MOV r6, #3 ; set DLAB = 0
45 STRB r6, [r5, #LCR0] ; Tx and Rx buffers set up
46 LDMDB sp!, {r5,r6,pc}
47
48 ; Subroutine Transmit
49 ; This routine puts one byte into the UART
50 ; for transmitting.
51 ; Register used:
52 ; r5 - scratch
53 ; r6 - scratch
54 ; inputs: r0- byte to transmit
55 ; outputs: none
56 ;
57
58 Transmit
59 STMIA sp!, {r5, r6, lr}
60 LDR r5, = U0START
61 wait LDRB r6, [r5, #LSR0] ; get status of buffer
62 TST r6, #0x20 ; buffer empty?
63 BEQ wait ; spin until buffer's empty
64 STRB r0, [r5]
65 LDMDB sp!, {r5, r6, pc}
66 CharData
67 DCB "TKU-ECE612450097",0
Universal Asynchronous Receive Transmit 0 (UART0)
Line Control
U0LCR: 0x83
Word Length: 8 bits
Stop Bits: 1
Parity: Odd Parity
DLAB
Break Control
Parity Enable
Line Status
U0LSR: 0x60
Receiver Data Ready (RDR)
Overrun Error (OE)
Parity Error (PE)
Framing Error (FE)
Break Interrupt (BI)
Tx Holding Register Empty (THRE)
Transmitter Empty (TEMT)
Error in Rx FIFO (RXFE)
Interrupt Enable
U0IER: 0x00
RBR IE
THRE IE
Rx Line Status IE
Interrupt ID & FIFO Control
U0IIR/FCR: 0x01
FIFO Enable
Interrupt: None
Rx Trigger: Level 0 (1)
Rx FIFO Reset
Tx FIFO Reset
Divisor Latch
U0DLL: 0x61
U0DLM: 0x00
Baudrate: 1932
Receiver & Transmitter Registers
U0RBR/THR: 0x00
Scratch Pad Register
U0SCR: 0x00
Command
Running with Code Size Limit: 32K
Load "F:\\03.淡江碩士\\01.碩一(112)\\02.碩一下學期\\07.微處理機概論(電資)(助教課)\\04.作業\\第01次作業\\02.解答\\HW1_
ASSIGN BreakDisable BreakEnable BreakKill BreakList BreakSet BreakAccess COVERAGE COVTOFILE DEFINE DIR Display Enter
Memory 1
Address: 0xE000C000
0xE000C000: 61 00 00 00 00 00 00 00 01 00 00 00 83 00 00 00 00 00 00 00 60 00 00 00 00 00 00 00 00 00 00 00 00 00
0xE000C022: 00 00 00 00 00 00 10 00 00 00 00 00 00 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0xE000C044: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0xE000C066: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0xE000C088: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0xE000C0AA: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0xE000C0CC: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0xE000C0EE: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0xE000C110: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
Call Stack + Locals
UART #1
Memory 1

設為Receive/Transmit功能(DLAB=0)



第一次作業-第一部分

2024 Advanced Mixed-Operation System (AMOS) Lab.

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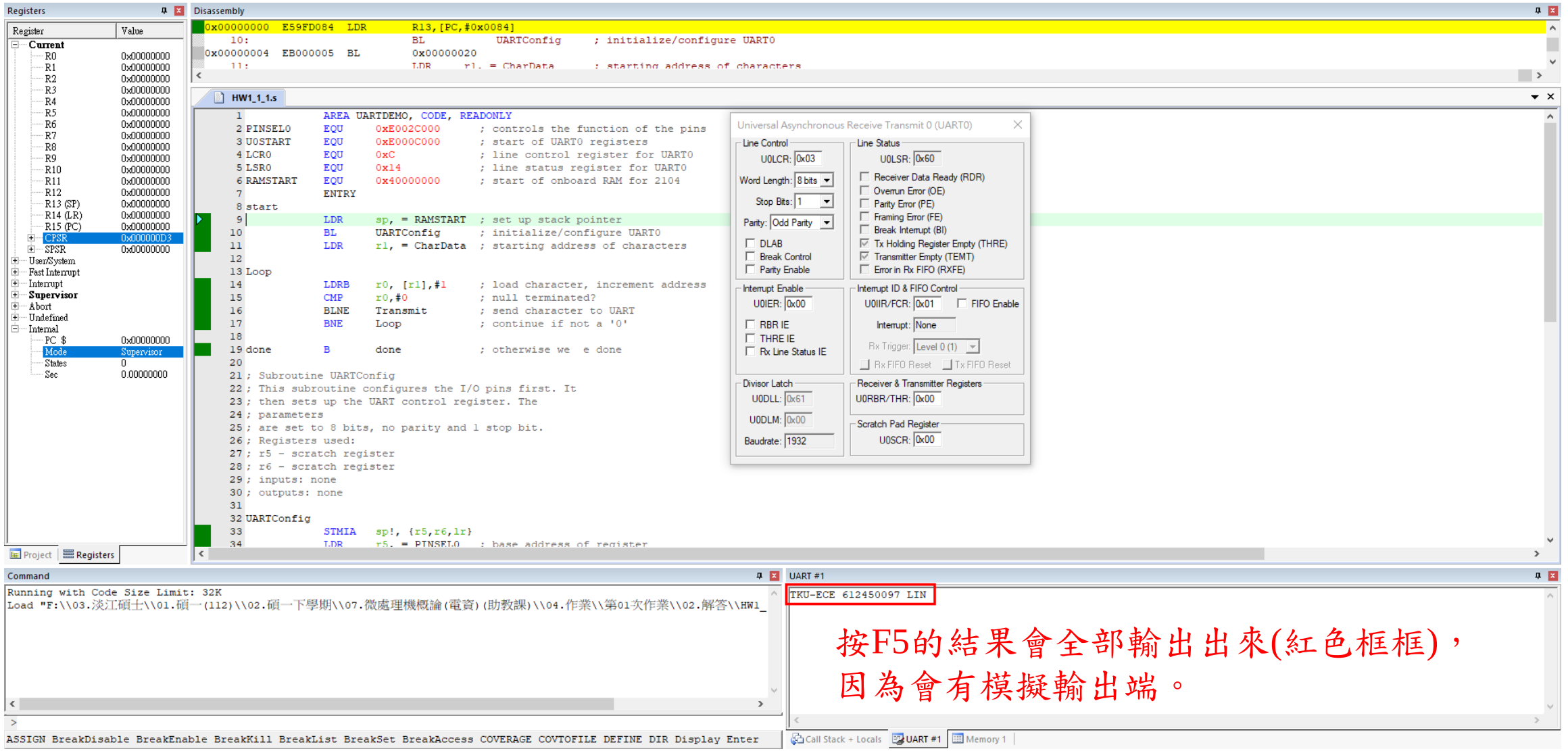
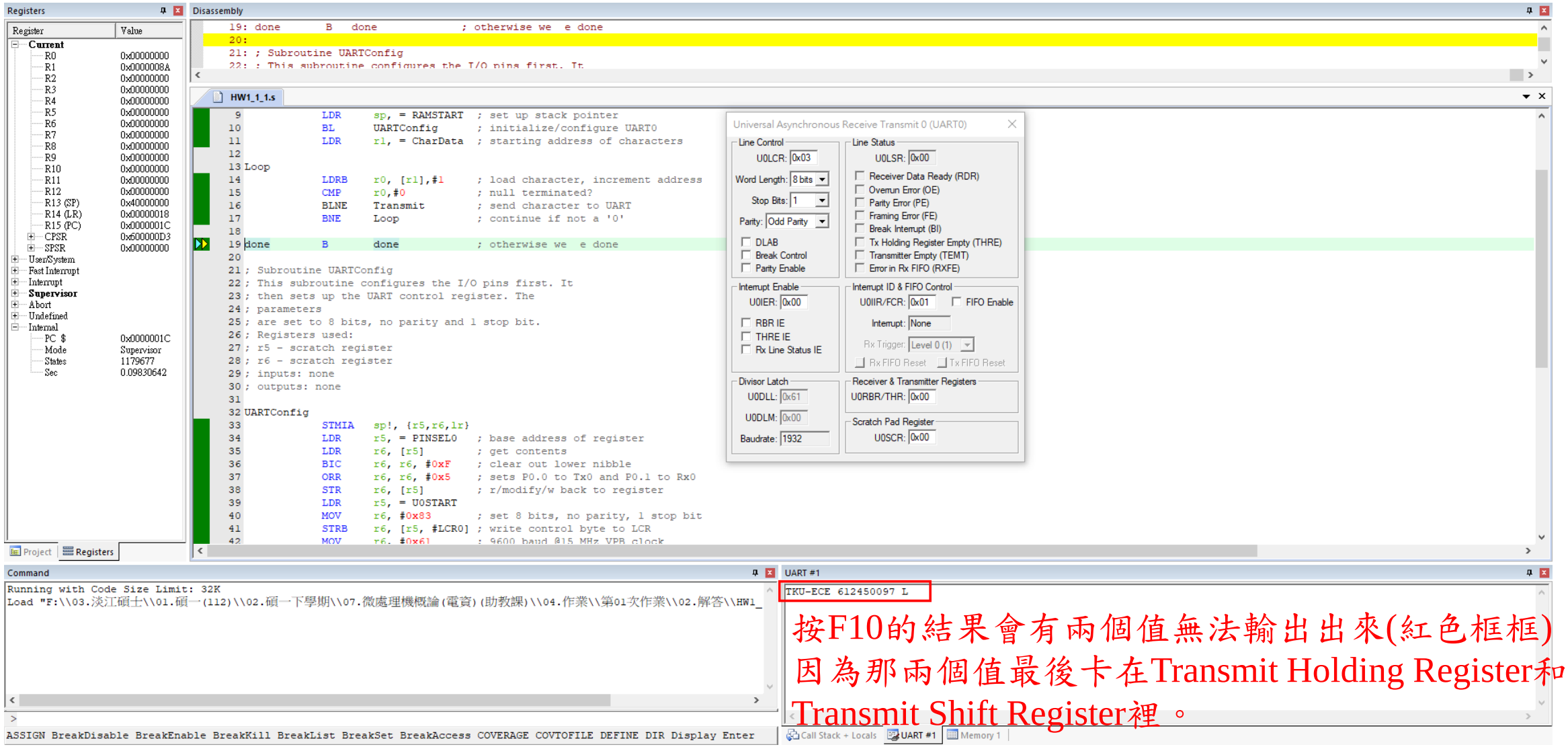
執行心得-1(F5)



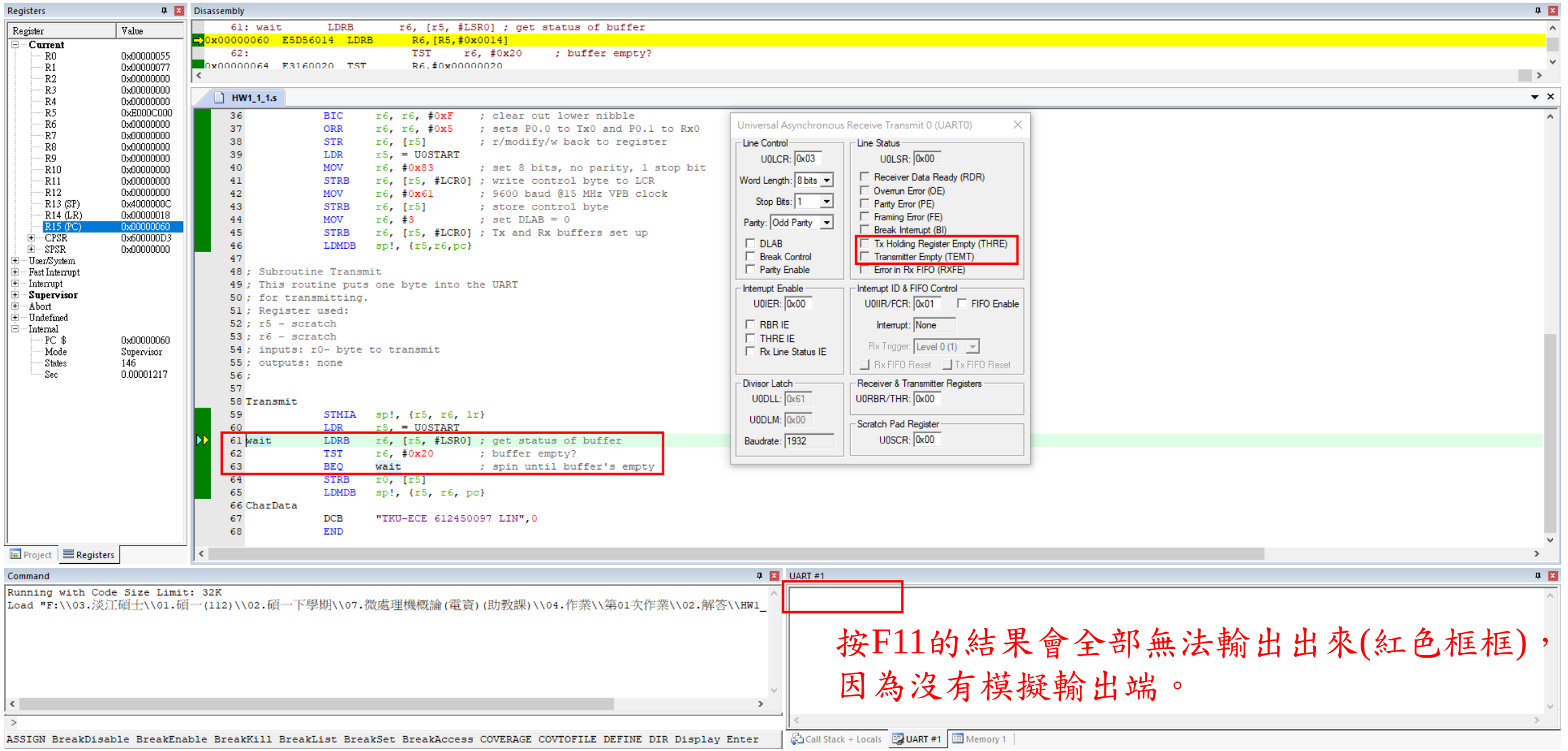
按F5的結果會全部輸出出來(紅色框框)，
因為會有模擬輸出端。

執行心得-1(F10)

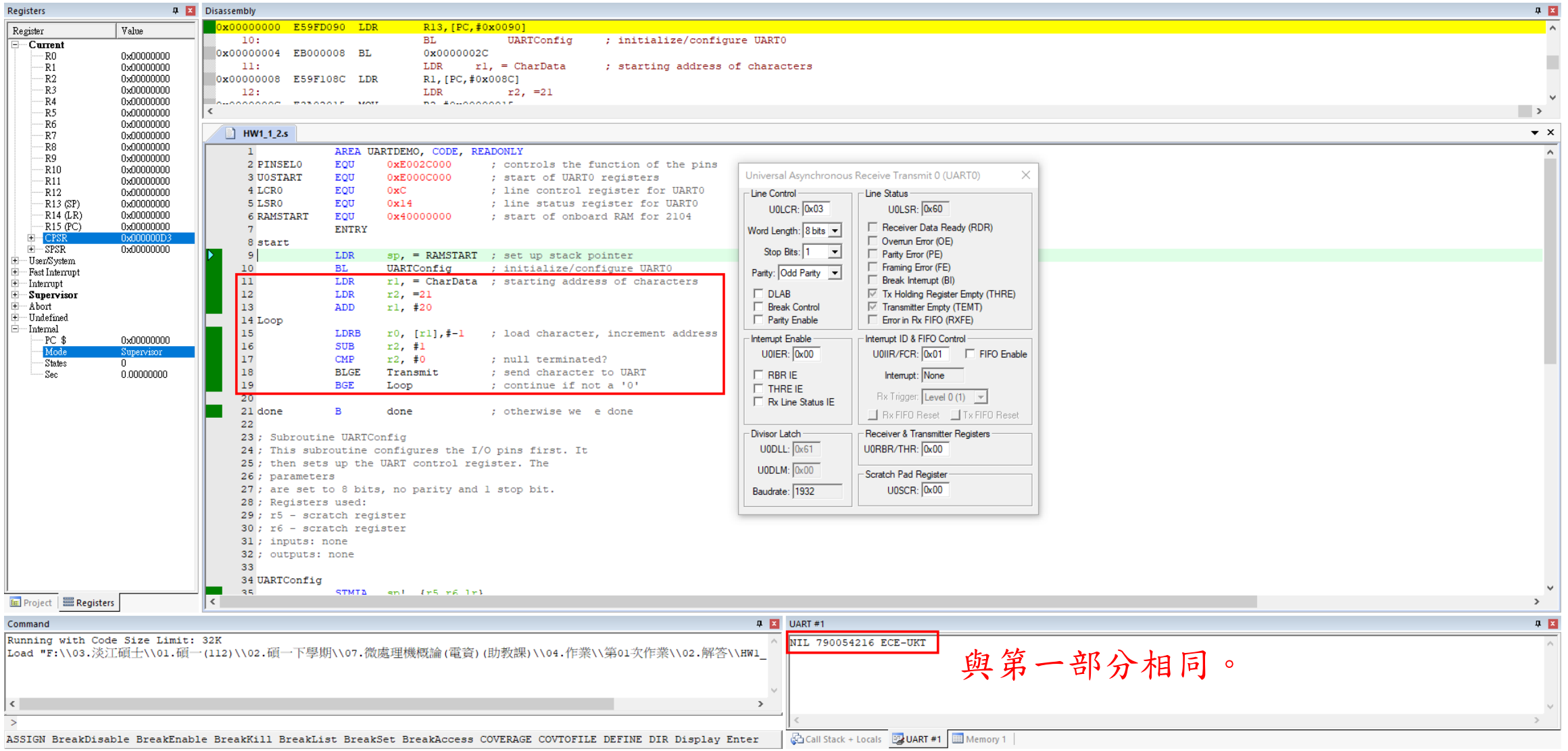


按F10的結果會有兩個值無法輸出出來(紅色框框)，因為那兩個值最後卡在Transmit Holding Register和Transmit Shift Register裡。

執行心得-1(F11)

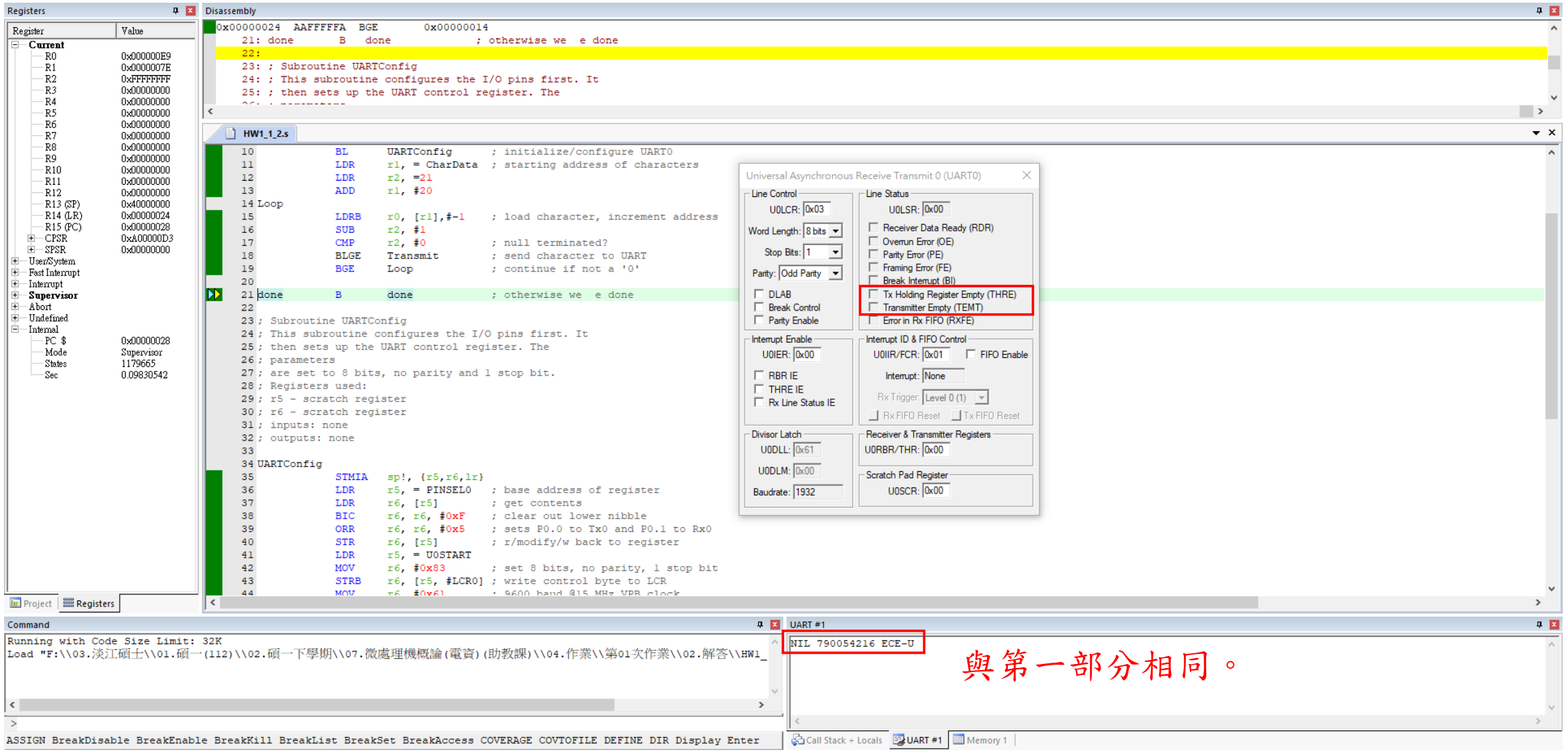

Registers
Register
Value
Current
R0 0x00000055
R1 0x00000077
R2 0x00000000
R3 0x00000000
R4 0x00000000
R5 0xE000C000
R6 0x00000000
R7 0x00000000
R8 0x00000000
R9 0x00000000
R10 0x00000000
R11 0x00000000
R12 0x00000000
R13 (SP) 0x4000000C
R14 (LR) 0x00000018
R15 (PC) 0x00000060
CPSR 0x600000D3
SPSR 0x00000000
User/System
Fast Interrupt
Interrupt
Supervisor
Abort
Undefined
Internal
PC $ 0x00000060
Mode Supervisor
States 146
Sec 0.00001217
Project
Registers
Disassembly
61: wait LDRB r6, [r5, #LSR0] ; get status of buffer
0x00000060 E5D56014 LDRB R6,[R5,#0x0014]
62: TST r6, #0x20 ; buffer empty?
0x00000064 E3160020 TST R6,#0x00000020
HW1_1_1.s
36 BIC r6, r6, #0xF ; clear out lower nibble
37 ORR r6, r6, #0x5 ; sets P0.0 to Tx0 and P0.1 to Rx0
38 STR r6, [r5] ; r/modify/w back to register
39 LDR r5, = U0START
40 MOV r6, #0x83 ; set 8 bits, no parity, 1 stop bit
41 STRB r6, [r5, #LCR0] ; write control byte to LCR
42 MOV r6, #0x61 ; 9600 baud @15 MHz VPB clock
43 STRB r6, [r5] ; store control byte
44 MOV r6, #3 ; set DLAB = 0
45 STRB r6, [r5, #LCR0] ; Tx and Rx buffers set up
46 LDMDB sp!, {r5,r6,pc}
47
48 ; Subroutine Transmit
49 ; This routine puts one byte into the UART
50 ; for transmitting.
51 ; Register used:
52 ; r5 - scratch
53 ; r6 - scratch
54 ; inputs: r0- byte to transmit
55 ; outputs: none
56 ;
57
58 Transmit
59 STMIA sp!, {r5, r6, lr}
60 LDR r5, = U0START
61 wait LDRB r6, [r5, #LSR0] ; get status of buffer
62 TST r6, #0x20 ; buffer empty?
63 BEQ wait ; spin until buffer's empty
64 STRB r0, [r5]
65 LDMDB sp!, {r5, r6, pc}
66 CharData
67 DCB "TKU-ECE 612450097 LIN",0
68 END
Universal Asynchronous Receive Transmit 0 (UART0)
Line Control
U0LCR: 0x03
Word Length: 8 bits
Stop Bits: 1
Parity: Odd Parity
DLAB
Break Control
Parity Enable
Line Status
U0LSR: 0x00
Receiver Data Ready (RDR)
Overrun Error (OE)
Parity Error (PE)
Framing Error (FE)
Break Interrupt (BI)
Tx Holding Register Empty (THRE)
Transmitter Empty (TEMT)
Error in Rx FIFO (RXFE)
Interrupt Enable
U0IER: 0x00
RBR IE
THRE IE
Rx Line Status IE
Interrupt ID & FIFO Control
U0IIR/FCR: 0x01
FIFO Enable
Interrupt: None
Rx Trigger: Level 0 (1)
Rx FIFO Reset
Tx FIFO Reset
Divisor Latch
U0DLL: 0x61
U0DLM: 0x00
Baudrate: 1932
Receiver & Transmitter Registers
U0RBR/THR: 0x00
Scratch Pad Register
U0SCR: 0x00
Command
Running with Code Size Limit: 32K
Load "F:\\03.淡江碩士\\01.碩一(112)\\02.碩一下學期\\07.微處理機概論(電資)(助教課)\\04.作業\\第01次作業\\02.解答\\HW1_
ASSIGN BreakDisable BreakEnable BreakKill BreakList BreakSet BreakAccess COVERAGE COVTOFILE DEFINE DIR Display Enter
UART #1
Call Stack + Locals
UART #1
Memory 1
按F11的結果會全部無法輸出出來(紅色框框)，
因為沒有模擬輸出端。

2(F5)


Registers
Register
Value
Current
R0 0x00000000
R1 0x00000000
R2 0x00000000
R3 0x00000000
R4 0x00000000
R5 0x00000000
R6 0x00000000
R7 0x00000000
R8 0x00000000
R9 0x00000000
R10 0x00000000
R11 0x00000000
R12 0x00000000
R13 (SP) 0x00000000
R14 (LR) 0x00000000
R15 (PC) 0x00000000
CPSR 0x000000D3
SPSR 0x00000000
User/System
Fast Interrupt
Interrupt
Supervisor
Abort
Undefined
Internal
PC $ 0x00000000
Mode Supervisor
States 0
Sec 0.00000000
Project
Registers
Disassembly
0x00000000 E59FD090 LDR R13,[PC,#0x0090]
10: BL UARTConfig ; initialize/configure UART0
0x00000004 EB000008 BL 0x0000002C
11: LDR r1, = CharData ; starting address of characters
0x00000008 E59F108C LDR R1,[PC,#0x008C]
12: LDR r2, =21
HW1_1_2.s
1 AREA UARTDEMO, CODE, READONLY
2 PINSEL0 EQU 0xE002C000 ; controls the function of the pins
3 U0START EQU 0xE000C000 ; start of UART0 registers
4 LCR0 EQU 0xC ; line control register for UART0
5 LSR0 EQU 0x14 ; line status register for UART0
6 RAMSTART EQU 0x40000000 ; start of onboard RAM for 2104
7 ENTRY
8 start
9 LDR sp, = RAMSTART ; set up stack pointer
10 BL UARTConfig ; initialize/configure UART0
11 LDR r1, = CharData ; starting address of characters
12 LDR r2, =21
13 ADD r1, #20
14 Loop
15 LDRB r0, [r1],#-1 ; load character, increment address
16 SUB r2, #1
17 CMP r2, #0 ; null terminated?
18 BLGE Transmit ; send character to UART
19 BGE Loop ; continue if not a '0'
20
21 done B done ; otherwise we e done
22
23 ; Subroutine UARTConfig
24 ; This subroutine configures the I/O pins first. It
25 ; then sets up the UART control register. The
26 ; parameters
27 ; are set to 8 bits, no parity and 1 stop bit.
28 ; Registers used:
29 ; r5 - scratch register
30 ; r6 - scratch register
31 ; inputs: none
32 ; outputs: none
33
34 UARTConfig
Universal Asynchronous Receive Transmit 0 (UART0)
Line Control
U0LCR: 0x03
Word Length: 8 bits
Stop Bits: 1
Parity: Odd Parity
DLAB
Break Control
Parity Enable
Line Status
U0LSR: 0x60
Receiver Data Ready (RDR)
Overrun Error (OE)
Parity Error (PE)
Framing Error (FE)
Break Interrupt (BI)
Tx Holding Register Empty (THRE)
Transmitter Empty (TEMT)
Error in Rx FIFO (RXFE)
Interrupt Enable
U0IER: 0x00
RBR IE
THRE IE
Rx Line Status IE
Interrupt ID & FIFO Control
U0IIR/FCR: 0x01
FIFO Enable
Interrupt: None
Rx Trigger: Level 0 (1)
Rx FIFO Reset
Tx FIFO Reset
Divisor Latch
U0DLL: 0x61
U0DLM: 0x00
Baudrate: 1932
Receiver & Transmitter Registers
U0RBR/THR: 0x00
Scratch Pad Register
U0SCR: 0x00
Command
Running with Code Size Limit: 32K
Load "F:\\03.淡江碩士\\01.碩一(112)\\02.碩一下學期\\07.微處理機概論(電資)(助教課)\\04.作業\\第01次作業\\02.解答\\HW1_
ASSIGN BreakDisable BreakEnable BreakKill BreakList BreakSet BreakAccess COVERAGE COVTOFILE DEFINE DIR Display Enter
UART #1
NIL 790054216 ECE-UKT
Call Stack + Locals
UART #1
Memory 1

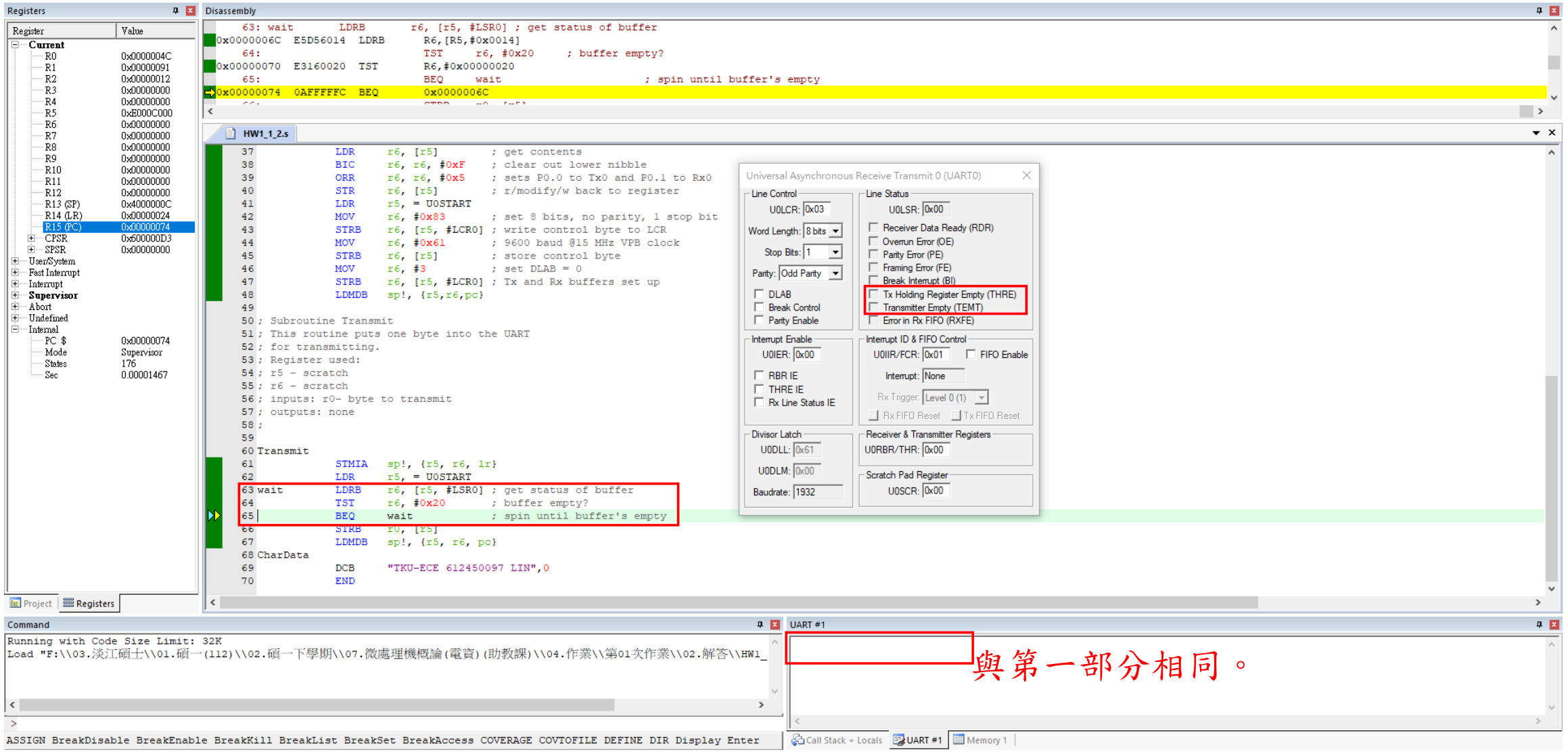
與第一部分相同。

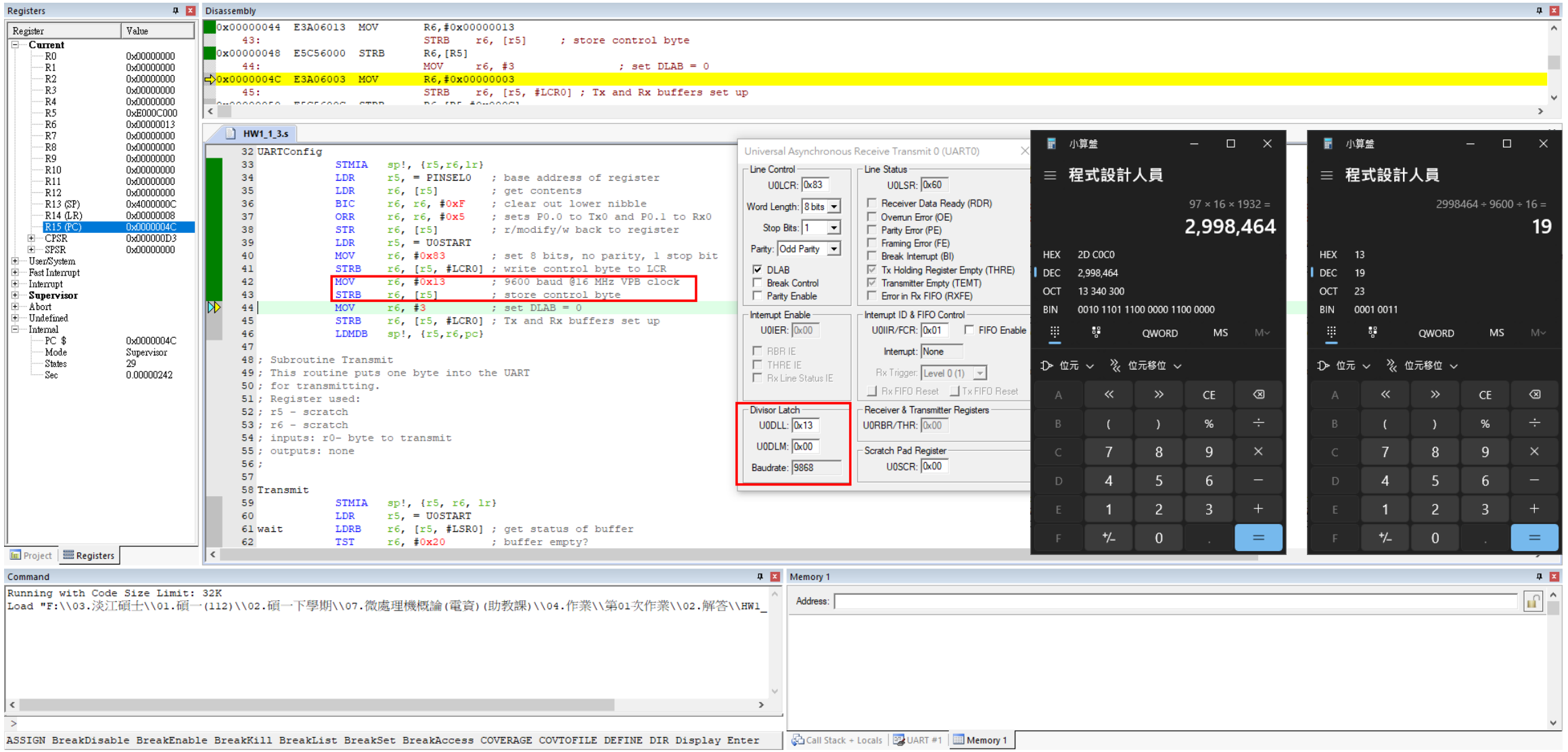
2(F10)



與第一部分相同。

2(F11)


Registers
Register
Value
Current
R0 0x0000004C
R1 0x00000091
R2 0x00000012
R3 0x00000000
R4 0x00000000
R5 0xE000C000
R6 0x00000000
R7 0x00000000
R8 0x00000000
R9 0x00000000
R10 0x00000000
R11 0x00000000
R12 0x00000000
R13 (SP) 0x4000000C
R14 (LR) 0x00000024
R15 (PC) 0x00000074
CPSR 0x600000D3
SPSR 0x00000000
User/System
Fast Interrupt
Interrupt
Supervisor
Abort
Undefined
Internal
PC $ 0x00000074
Mode Supervisor
States 176
Sec 0.00001467
Project
Registers
Disassembly
63: wait LDRB r6, [r5, #LSR0] ; get status of buffer
0x0000006C E5D56014 LDRB R6,[R5,#0x0014]
64: TST r6, #0x20 ; buffer empty?
0x00000070 E3160020 TST R6,#0x00000020
65: BEQ wait ; spin until buffer's empty
0x00000074 0AFFFFFC BEQ 0x0000006C
HW1_1_2.s
37 LDR r6, [r5] ; get contents
38 BIC r6, r6, #0xF ; clear out lower nibble
39 ORR r6, r6, #0x5 ; sets P0.0 to Tx0 and P0.1 to Rx0
40 STR r6, [r5] ; r/modify/w back to register
41 LDR r5, = U0START
42 MOV r6, #0x83 ; set 8 bits, no parity, 1 stop bit
43 STRB r6, [r5, #LCR0] ; write control byte to LCR
44 MOV r6, #0x61 ; 9600 baud @15 MHz VPB clock
45 STRB r6, [r5] ; store control byte
46 MOV r6, #3 ; set DLAB = 0
47 STRB r6, [r5, #LCR0] ; Tx and Rx buffers set up
48 LDMDB sp!, {r5,r6,pc}
49
50 ; Subroutine Transmit
51 ; This routine puts one byte into the UART
52 ; for transmitting.
53 ; Register used:
54 ; r5 - scratch
55 ; r6 - scratch
56 ; inputs: r0- byte to transmit
57 ; outputs: none
58 ;
59
60 Transmit
61 STMIA sp!, {r5, r6, lr}
62 LDR r5, = U0START
63 wait LDRB r6, [r5, #LSR0] ; get status of buffer
64 TST r6, #0x20 ; buffer empty?
65 BEQ wait ; spin until buffer's empty
66 STRB r0, [r5]
67 LDMDB sp!, {r5, r6, pc}
68 CharData
69 DCB "TKU-ECE 612450097 LIN",0
70 END
Universal Asynchronous Receive Transmit 0 (UART0)
Line Control
U0LCR: 0x03
Word Length: 8 bits
Stop Bits: 1
Parity: Odd Parity
DLAB
Break Control
Parity Enable
Line Status
U0LSR: 0x00
Receiver Data Ready (RDR)
Overrun Error (OE)
Parity Error (PE)
Framing Error (FE)
Break Interrupt (BI)
Tx Holding Register Empty (THRE)
Transmitter Empty (TEMT)
Error in Rx FIFO (RXFE)
Interrupt Enable
U0IER: 0x00
RBR IE
THRE IE
Rx Line Status IE
Interrupt ID & FIFO Control
U0IIR/FCR: 0x01
FIFO Enable
Interrupt: None
Rx Trigger: Level 0 (1)
Rx FIFO Reset
Tx FIFO Reset
Divisor Latch
U0DLL: 0x61
U0DLM: 0x00
Baudrate: 1932
Receiver & Transmitter Registers
U0RBR/THR: 0x00
Scratch Pad Register
U0SCR: 0x00
Command
Running with Code Size Limit: 32K
Load "F:\\03.淡江碩士\\01.碩一(112)\\02.碩一下學期\\07.微處理機概論(電資)(助教課)\\04.作業\\第01次作業\\02.解答\\HW1_
ASSIGN BreakDisable BreakEnable BreakKill BreakList BreakSet BreakAccess COVERAGE COVTOFILE DEFINE DIR Display Enter
UART #1
Call Stack + Locals
UART #1
Memory 1
與第一部分相同。

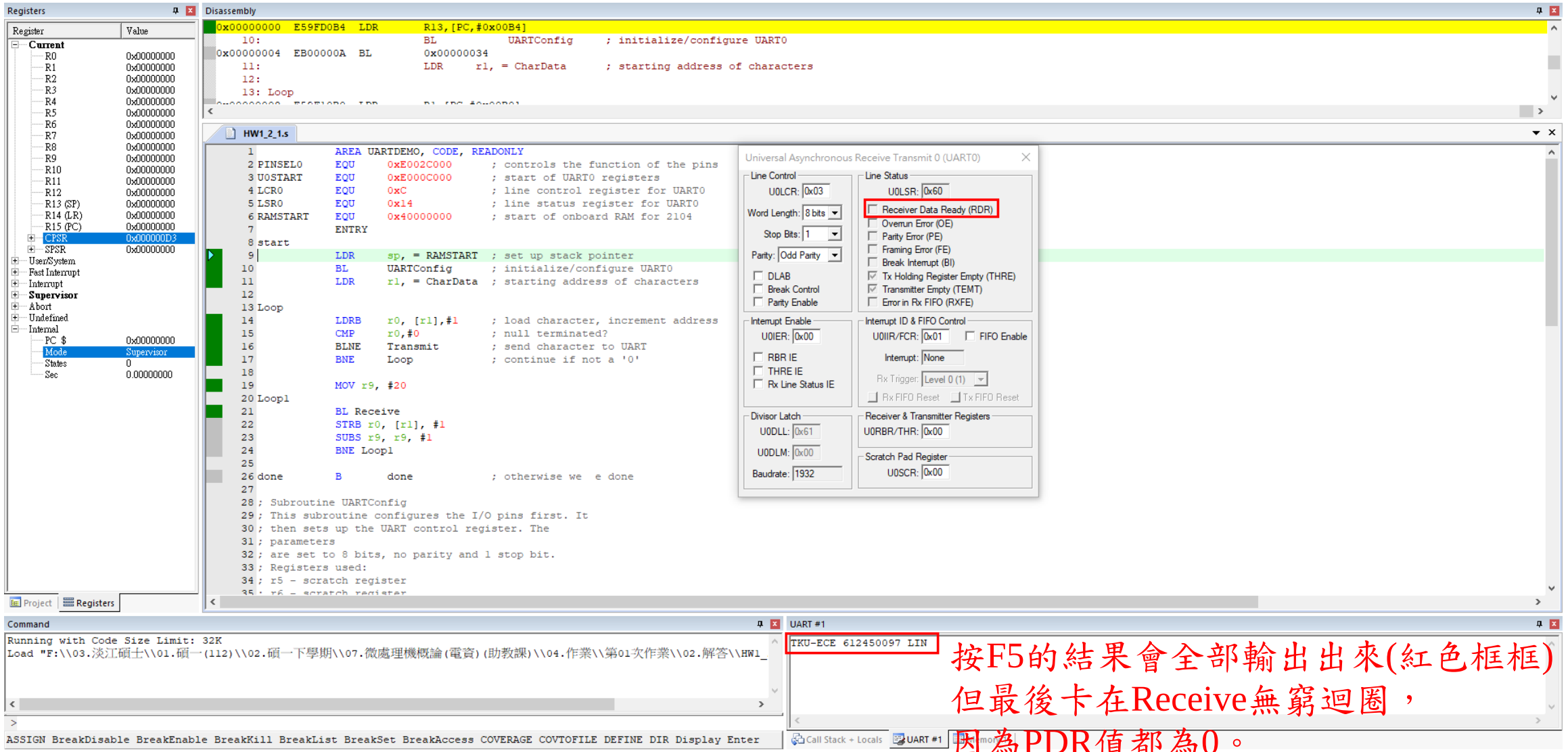

Registers
Register
Value
Current
R0 0x00000000
R1 0x00000000
R2 0x00000000
R3 0x00000000
R4 0x00000000
R5 0xE000C000
R6 0x00000013
R7 0x00000000
R8 0x00000000
R9 0x00000000
R10 0x00000000
R11 0x00000000
R12 0x00000000
R13 (SP) 0x4000000C
R14 (LR) 0x00000008
R15 (PC) 0x0000004C
CPSR 0x000000D3
SPSR 0x00000000
User/System
Fast Interrupt
Interrupt
Supervisor
Abort
Undefined
Internal
PC $ 0x0000004C
Mode Supervisor
States 29
Sec 0.00000242
Project
Registers
Disassembly
0x00000044 E3A06013 MOV R6,#0x00000013
43: STRB r6, [r5] ; store control byte
0x00000048 E5C56000 STRB R6,[R5]
44: MOV r6, #3 ; set DLAB = 0
0x0000004C E3A06003 MOV R6,#0x00000003
45: STRB r6, [r5, #LCR0] ; Tx and Rx buffers set up
HW1_1_3.s
32 UARTConfig
33 STMIA sp!, {r5,r6,lr}
34 LDR r5, = PINSEL0 ; base address of register
35 LDR r6, [r5] ; get contents
36 BIC r6, r6, #0xF ; clear out lower nibble
37 ORR r6, r6, #0x5 ; sets P0.0 to Tx0 and P0.1 to Rx0
38 STR r6, [r5] ; r/modify/w back to register
39 LDR r5, = U0START
40 MOV r6, #0x83 ; set 8 bits, no parity, 1 stop bit
41 STRB r6, [r5, #LCR0] ; write control byte to LCR
42 MOV r6, #0x13 ; 9600 baud @16 MHz VPB clock
43 STRB r6, [r5] ; store control byte
44 MOV r6, #3 ; set DLAB = 0
45 STRB r6, [r5, #LCR0] ; Tx and Rx buffers set up
46 LDMDB sp!, {r5,r6,pc}
47
48 ; Subroutine Transmit
49 ; This routine puts one byte into the UART
50 ; for transmitting.
51 ; Register used:
52 ; r5 - scratch
53 ; r6 - scratch
54 ; inputs: r0- byte to transmit
55 ; outputs: none
56 ;
57
58 Transmit
59 STMIA sp!, {r5, r6, lr}
60 LDR r5, = U0START
61 wait LDRB r6, [r5, #LSR0] ; get status of buffer
62 TST r6, #0x20 ; buffer empty?
Universal Asynchronous Receive Transmit 0 (UART0)
Line Control
U0LCR: 0x83
Word Length: 8 bits
Stop Bits: 1
Parity: Odd Parity
DLAB
Break Control
Parity Enable
Line Status
U0LSR: 0x60
Receiver Data Ready (RDR)
Overrun Error (OE)
Parity Error (PE)
Framing Error (FE)
Break Interrupt (BI)
Tx Holding Register Empty (THRE)
Transmitter Empty (TEMT)
Error in Rx FIFO (RXFE)
Interrupt Enable
U0IER: 0x00
RBR IE
THRE IE
Rx Line Status IE
Interrupt ID & FIFO Control
U0IIR/FCR: 0x01
FIFO Enable
Interrupt: None
Rx Trigger: Level 0 (1)
Rx FIFO Reset
Tx FIFO Reset
Divisor Latch
U0DLL: 0x13
U0DLM: 0x00
Baudrate: 9868
Receiver & Transmitter Registers
U0RBR/THR: 0x00
Scratch Pad Register
U0SCR: 0x00
小算盤
程式設計人員
97 × 16 × 1932 =
2,998,464
HEX 2D C0C0
DEC 2,998,464
OCT 13 340 300
BIN 0010 1101 1100 0000 1100 0000
QWORD MS
小算盤
程式設計人員
2998464 ÷ 9600 ÷ 16 =
19
HEX 13
DEC 19
OCT 23
BIN 0001 0011
QWORD MS
Command
Running with Code Size Limit: 32K
Load "F:\\03.淡江碩士\\01.碩一(112)\\02.碩一下學期\\07.微處理機概論(電資)(助教課)\\04.作業\\第01次作業\\02.解答\\HW1_
ASSIGN BreakDisable BreakEnable BreakKill BreakList BreakSet BreakAccess COVERAGE COVTOFILE DEFINE DIR Display Enter
Memory 1
Address:
Call Stack + Locals
UART #1
Memory 1

第一次作業-第二部分

2024 Advanced Mixed-Operation System (AMOS) Lab.

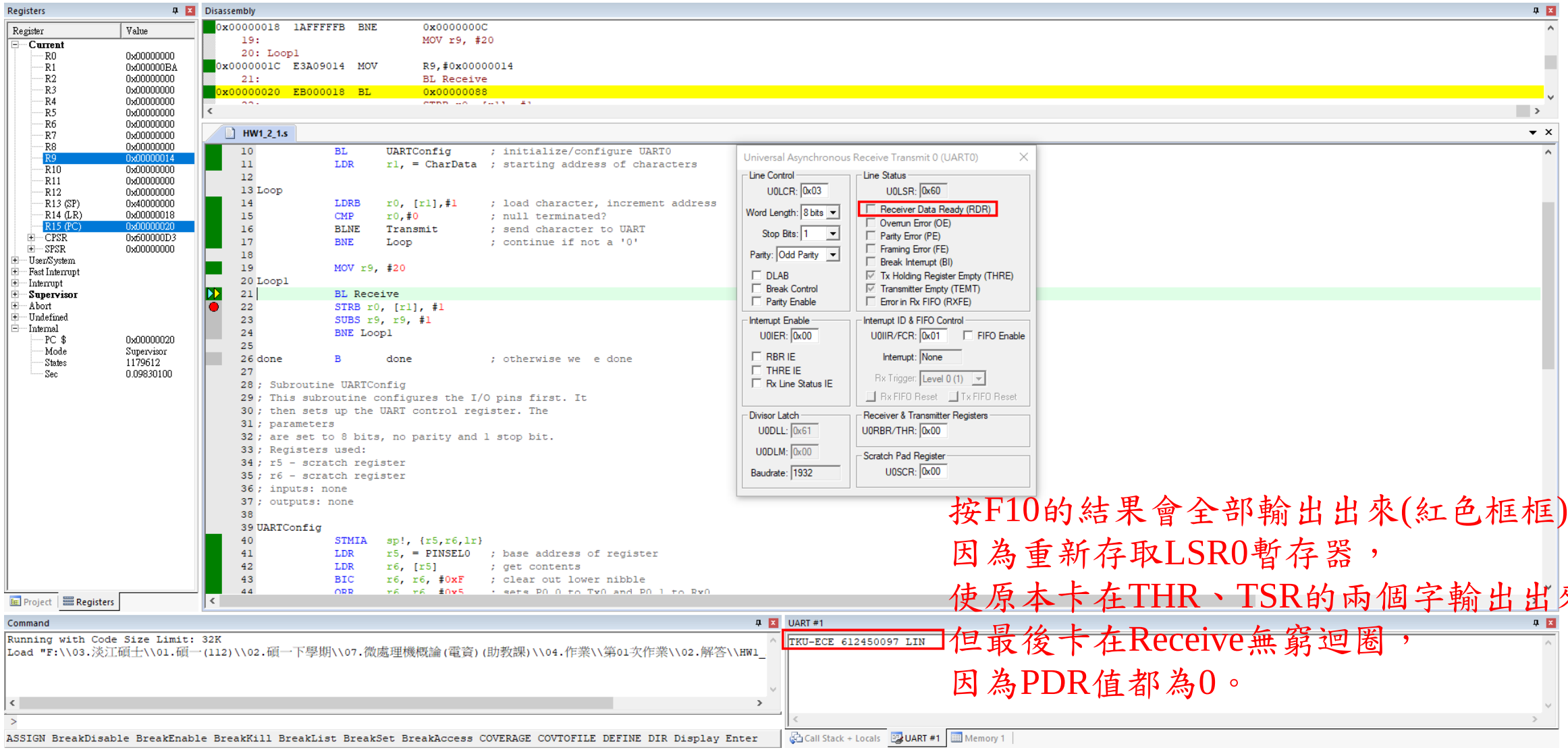
Tamkang University
Department of Electrical and Computer Engineering
No.151, Yingzhuan Rd., Tamsui Dist., New Taipei City 25137, Taiwan (R.O.C.)

執行心得-加入Receive(F5)



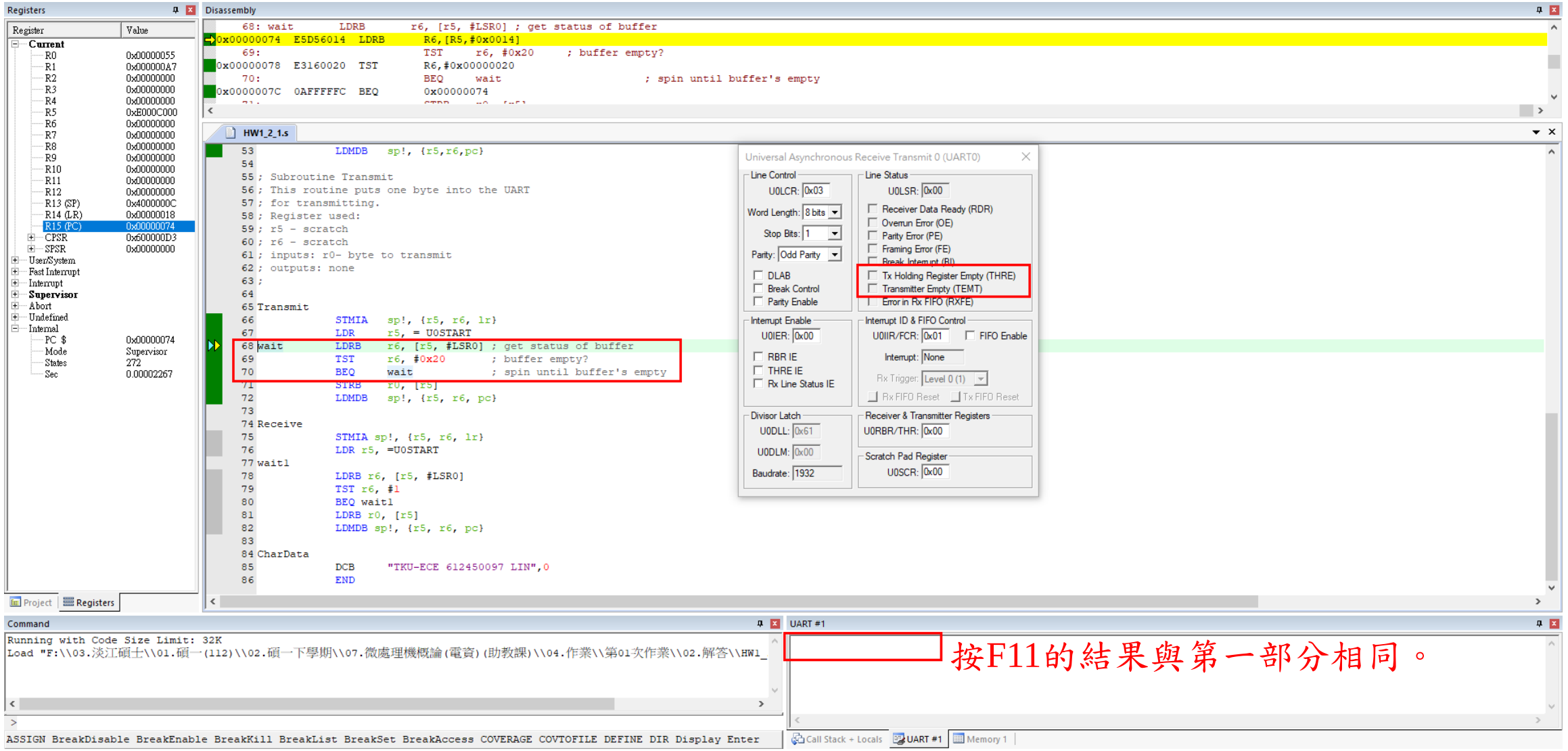
按F5的結果會全部輸出出來(紅色框框)，
但最後卡在Receive無窮迴圈，
因為PDR值都為0。

執行心得-加入Receive(F10)



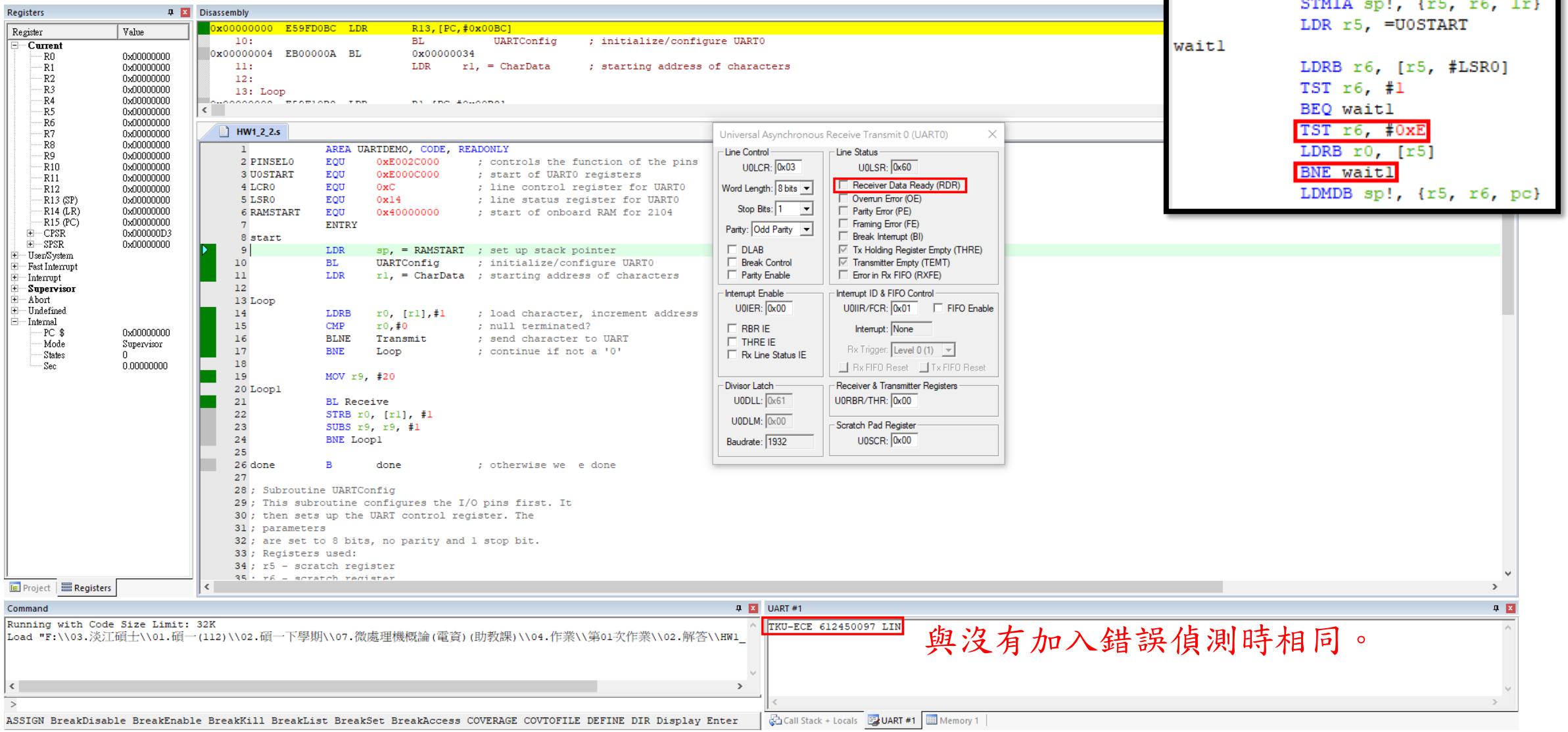
按F10的結果會全部輸出出來(紅色框框)，
因為重新存取LSR0暫存器，
使原本卡在THR、TSR的兩個字輸出出來。
但最後卡在Receive無窮迴圈，
因為PDR值都為0。

執行心得-加入Receive(F11)



按F11的結果與第一部分相同。

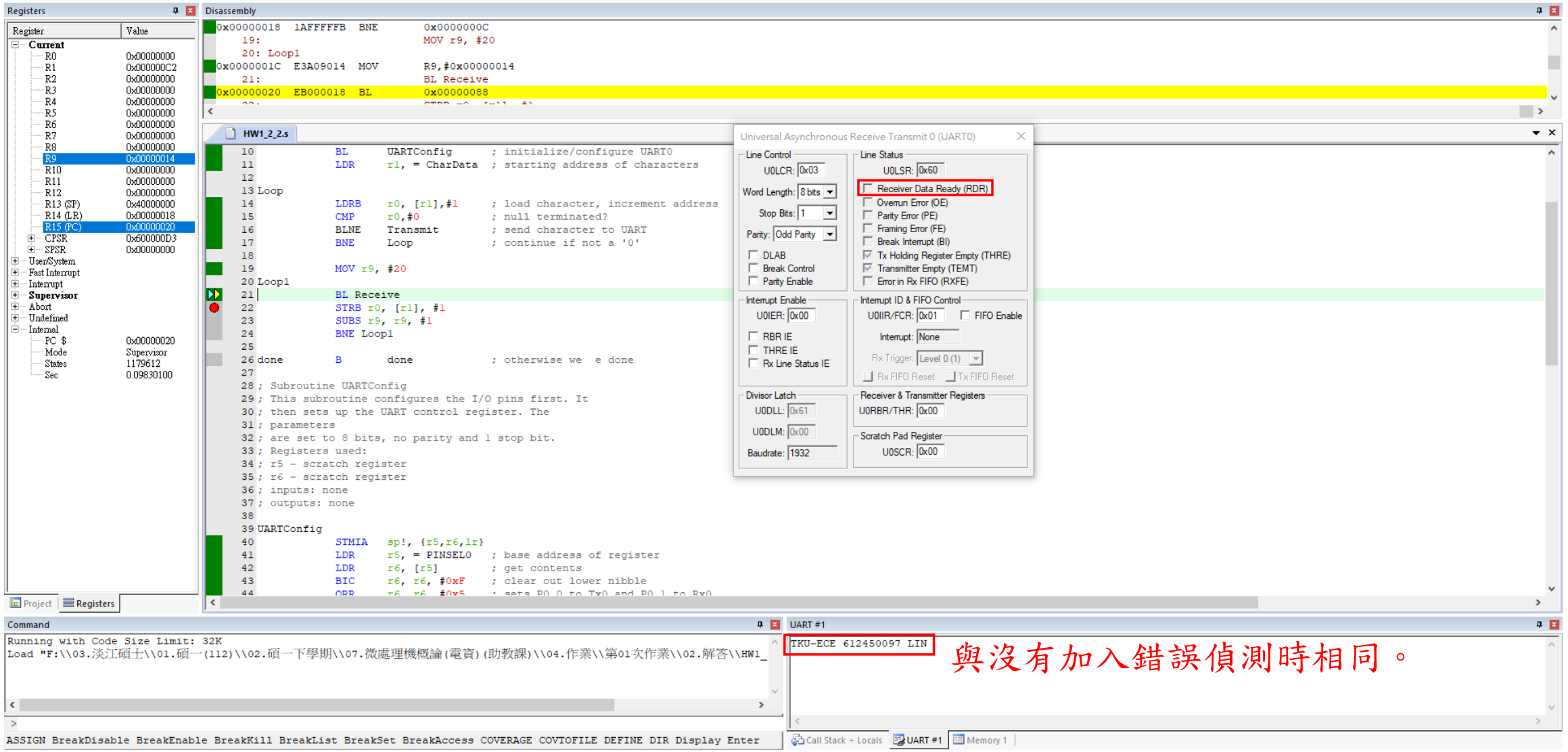
執行心得-加入三種錯誤偵測(F5)




```
Receive
        STMIA sp!, {r5, r6, lr}
        LDR r5, =U0START
wait1
        LDRB r6, [r5, #LSR0]
        TST r6, #1
        BEQ wait1
        TST r6, #0xE
        LDRB r0, [r5]
        BNE wait1
        LDMDB sp!, {r5, r6, pc}
```

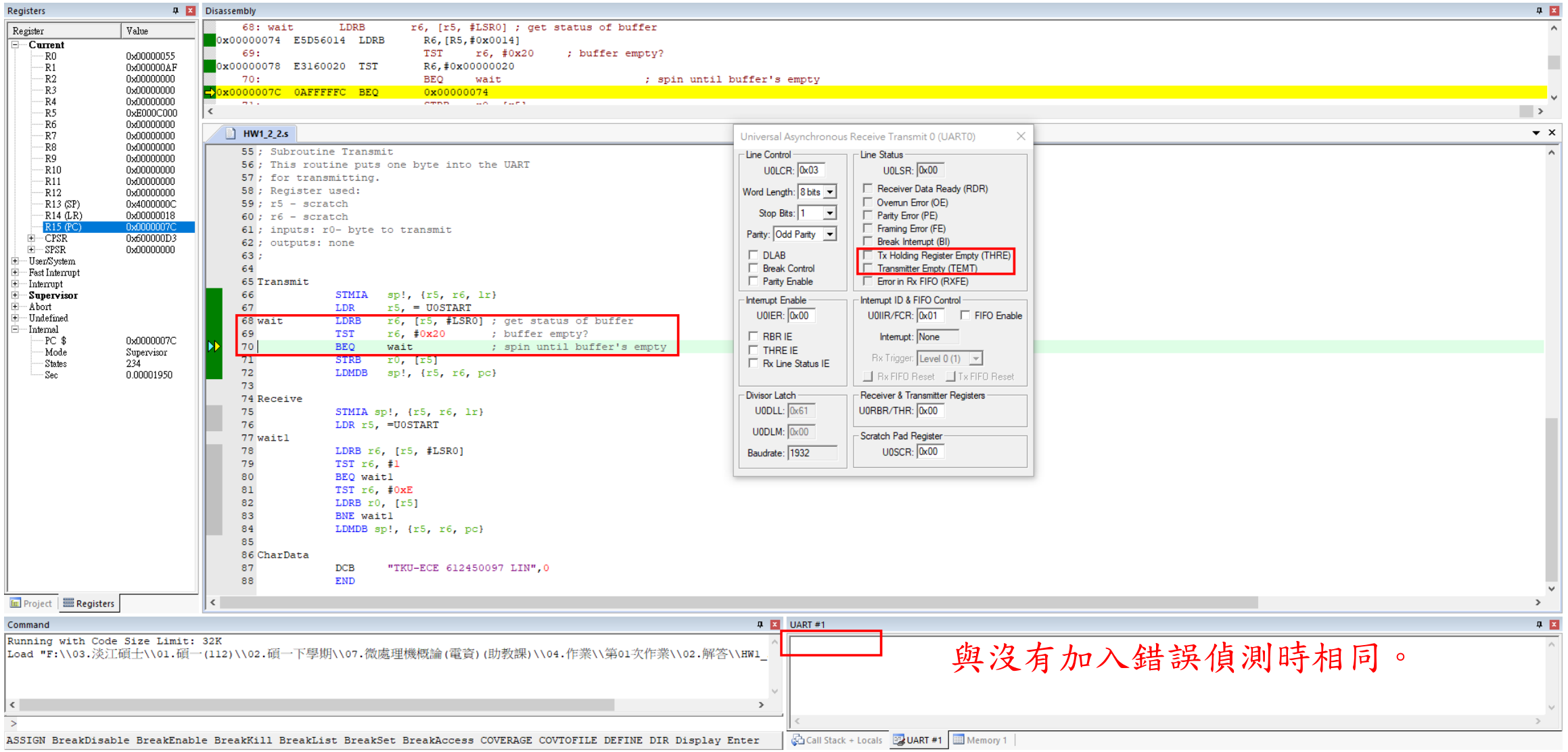
與沒有加入錯誤偵測時相同。

執行心得-加入三種錯誤偵測(F10)



與沒有加入錯誤偵測時相同。

執行心得-加入三種錯誤偵測(F11)



與沒有加入錯誤偵測時相同。

Q&A

Thanks for your attention !!