第13次組語實習課

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2023 Advanced Mixed-Operation System (AMOS) Lab.

Tamkang University
Department of Electrical and Computer Engineering
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期末上機考

2023 Advanced Mixed-Operation System (AMOS) Lab.

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Department of Electrical and Computer Engineering
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評分標準

- 第1題(28%)：共3小題，
  - 1.(1)(2)各佔9%，
  - 1.(3)佔10%。
- 第2題(48%)：共6小題，一題佔8%。
- 第3題(24%)：共8小題，一題佔3% 。

不計分
程式碼沒有學號、姓名
暫存器模糊不清楚
暫存器視窗沒拉開
暫存器數值不正確

➢ **以最後繳交的版本為準**

第1大題

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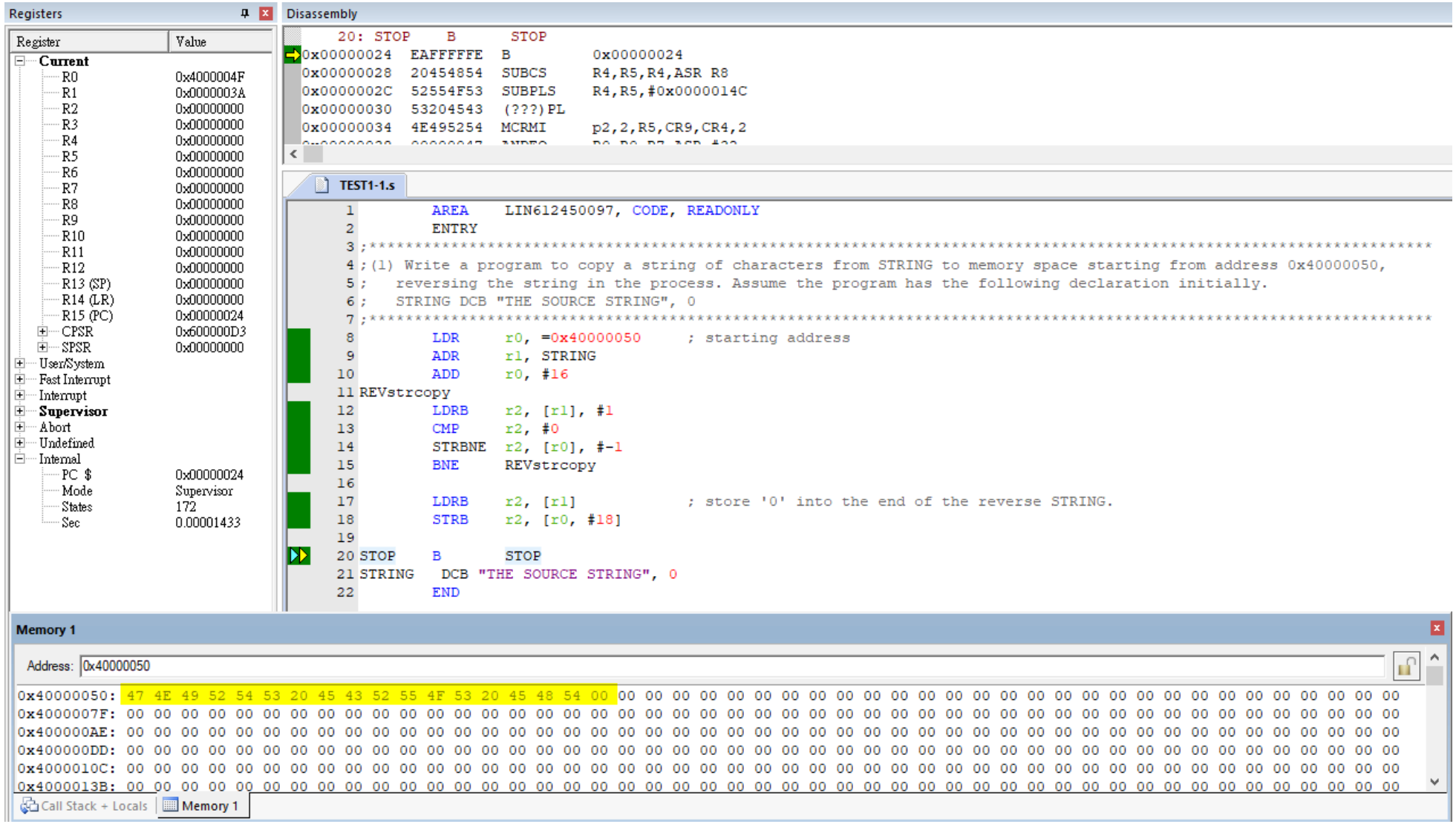
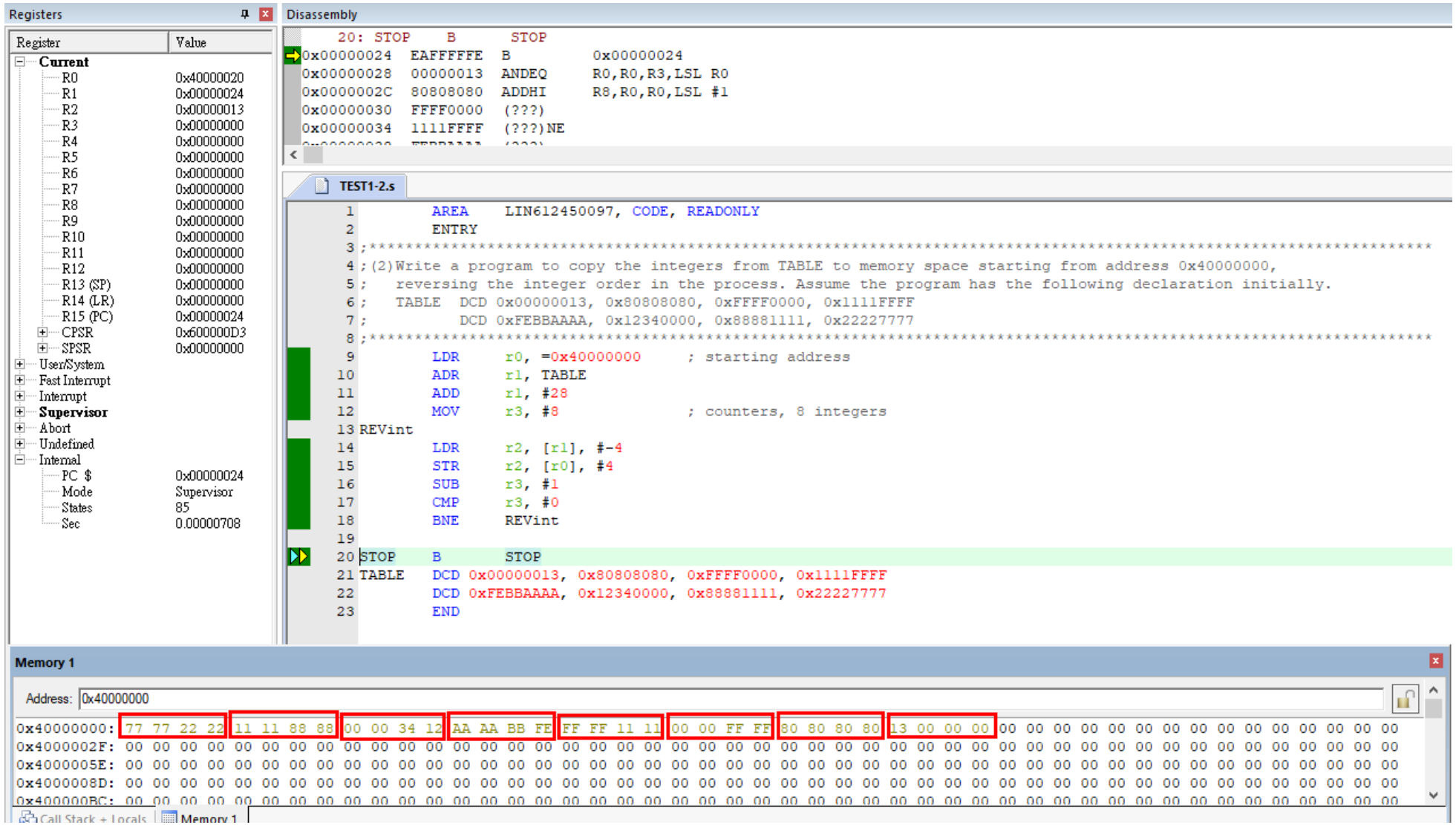
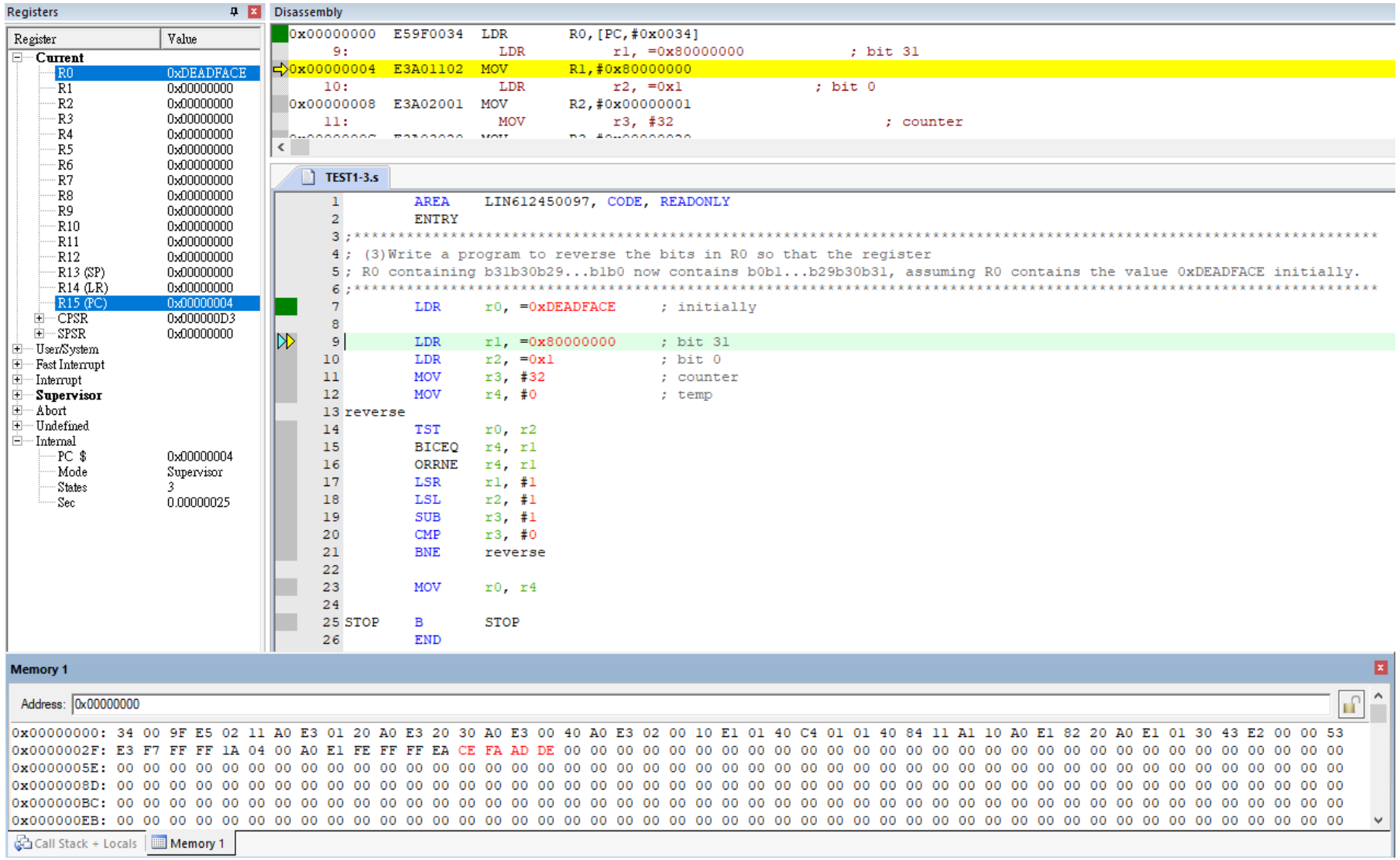
1.(1)


Registers
Register
Value
Current
R0 0x4000004F
R1 0x0000003A
R2 0x00000000
R3 0x00000000
R4 0x00000000
R5 0x00000000
R6 0x00000000
R7 0x00000000
R8 0x00000000
R9 0x00000000
R10 0x00000000
R11 0x00000000
R12 0x00000000
R13 (SP) 0x00000000
R14 (LR) 0x00000000
R15 (PC) 0x00000024
CPSR 0x600000D3
SPSR 0x00000000
User/System
Fast Interrupt
Interrupt
Supervisor
Abort
Undefined
Internal
PC $ 0x00000024
Mode Supervisor
States 172
Sec 0.00001433
Disassembly
20: STOP B STOP
0x00000024 EAFFFFFE B 0x00000024
0x00000028 20454854 SUBCS R4,R5,R4,ASR R8
0x0000002C 52554F53 SUBPLS R4,R5,#0x0000014C
0x00000030 53204543 (???)PL
0x00000034 4E495254 MCRMI p2,2,R5,CR9,CR4,2
TEST1-1.s
1 AREA LIN612450097, CODE, READONLY
2 ENTRY
3 ;*****
4 ;(1) Write a program to copy a string of characters from STRING to memory space starting from address 0x40000050,
5 ; reversing the string in the process. Assume the program has the following declaration initially.
6 ; STRING DCB "THE SOURCE STRING", 0
7 ;*****
8 LDR r0, =0x40000050 ; starting address
9 ADR r1, STRING
10 ADD r0, #16
11 REVstrcopy
12 LDRB r2, [r1], #1
13 CMP r2, #0
14 STRBNE r2, [r0], #-1
15 BNE REVstrcopy
16
17 LDRB r2, [r1] ; store '0' into the end of the reverse STRING.
18 STRB r2, [r0, #18]
19
20 STOP B STOP
21 STRING DCB "THE SOURCE STRING", 0
22 END
Memory 1
Address: 0x40000050
0x40000050: 47 4E 49 52 54 53 20 45 43 52 55 4F 53 20 45 48 54 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x4000007F: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x400000AE: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x400000DD: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x4000010C: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x4000013B: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
Call Stack + Locals
Memory 1

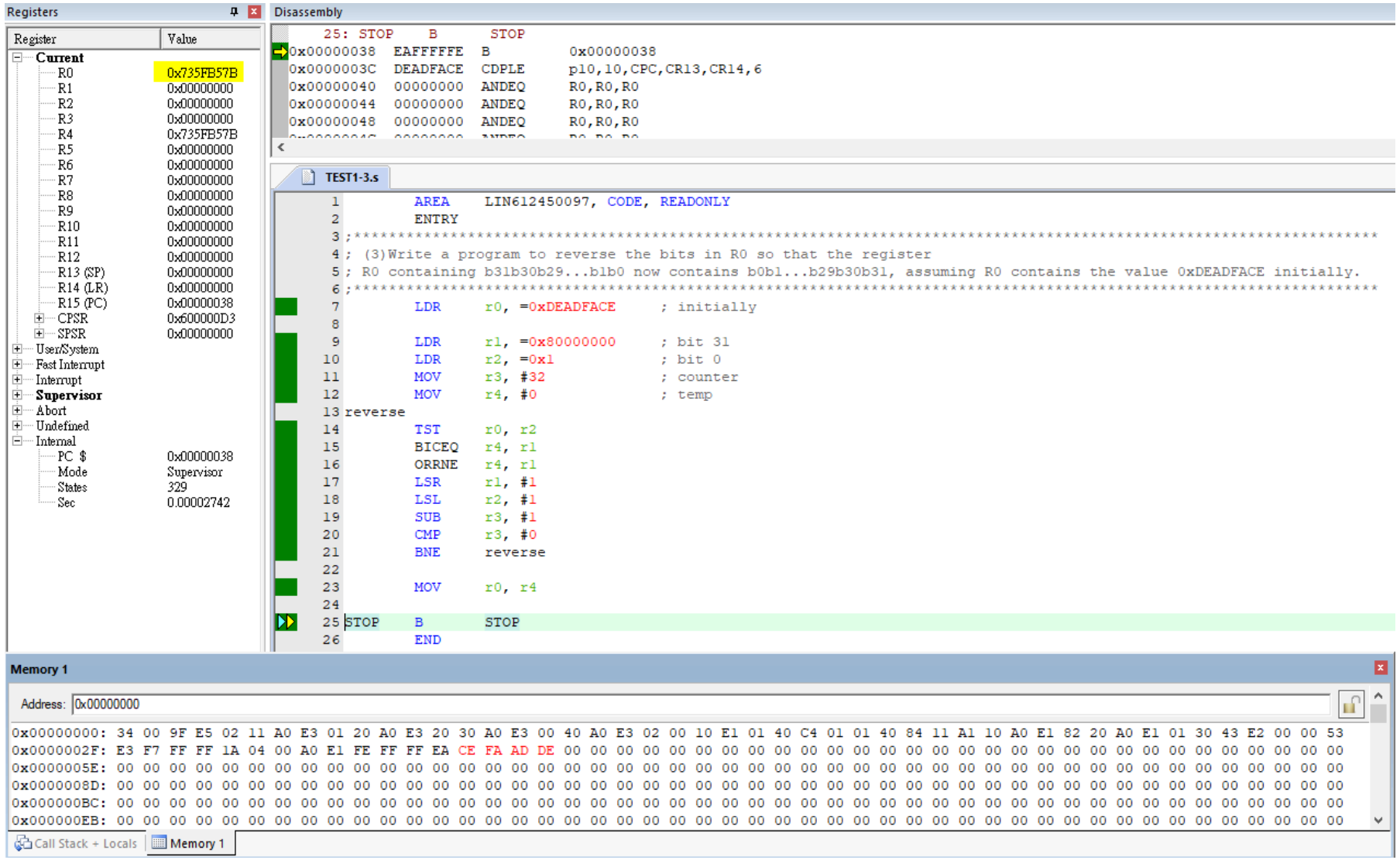
1.(2)


Registers
Register
Value
Current
R0 0x40000020
R1 0x00000024
R2 0x00000013
R3 0x00000000
R4 0x00000000
R5 0x00000000
R6 0x00000000
R7 0x00000000
R8 0x00000000
R9 0x00000000
R10 0x00000000
R11 0x00000000
R12 0x00000000
R13 (SP) 0x00000000
R14 (LR) 0x00000000
R15 (PC) 0x00000024
CPSR 0x600000D3
SPSR 0x00000000
User/System
Fast Interrupt
Interrupt
Supervisor
Abort
Undefined
Internal
PC $ 0x00000024
Mode Supervisor
States 85
Sec 0.00000708
Disassembly
20: STOP B STOP
0x00000024 EAFFFFFE B 0x00000024
0x00000028 00000013 ANDEQ R0,R0,R3,LSL R0
0x0000002C 80808080 ADDHI R8,R0,R0,LSL #1
0x00000030 FFFF0000 (???)
0x00000034 1111FFFF (???)NE
TEST1-2.s
1 AREA LIN612450097, CODE, READONLY
2 ENTRY
3 ;**********
4 ;(2)Write a program to copy the integers from TABLE to memory space starting from address 0x40000000,
5 ; reversing the integer order in the process. Assume the program has the following declaration initially.
6 ; TABLE DCD 0x00000013, 0x80808080, 0xFFFF0000, 0x1111FFFF
7 ; DCD 0xFEBBAAAA, 0x12340000, 0x88881111, 0x22227777
8 ;**********
9 LDR r0, =0x40000000 ; starting address
10 ADR r1, TABLE
11 ADD r1, #28
12 MOV r3, #8 ; counters, 8 integers
13 REVint
14 LDR r2, [r1], #-4
15 STR r2, [r0], #4
16 SUB r3, #1
17 CMP r3, #0
18 BNE REVint
19
20 STOP B STOP
21 TABLE DCD 0x00000013, 0x80808080, 0xFFFF0000, 0x1111FFFF
22 DCD 0xFEBBAAAA, 0x12340000, 0x88881111, 0x22227777
23 END
Memory 1
Address: 0x40000000
0x40000000: 77 77 22 22 11 11 88 88 00 00 34 12 AA AA BB FE FF FF 11 11 00 00 FF FF 80 80 80 80 13 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x4000002F: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x4000005E: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x4000008D: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x400000BC: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
Call Stack + Locals
Memory 1

1.(3) Initially



1.(3)


Registers
Register
Value
Current
R0 0x735FB57B
R1 0x00000000
R2 0x00000000
R3 0x00000000
R4 0x735FB57B
R5 0x00000000
R6 0x00000000
R7 0x00000000
R8 0x00000000
R9 0x00000000
R10 0x00000000
R11 0x00000000
R12 0x00000000
R13 (SP) 0x00000000
R14 (LR) 0x00000000
R15 (PC) 0x00000038
CPSR 0x600000D3
SPSR 0x00000000
User/System
Fast Interrupt
Interrupt
Supervisor
Abort
Undefined
Internal
PC $ 0x00000038
Mode Supervisor
States 329
Sec 0.00002742
Disassembly
25: STOP B STOP
0x00000038 EAFFFFFE B 0x00000038
0x0000003C DEADFACE CDPLE p10,10,CPC,CR13,CR14,6
0x00000040 00000000 ANDEQ R0,R0,R0
0x00000044 00000000 ANDEQ R0,R0,R0
0x00000048 00000000 ANDEQ R0,R0,R0
TEST1-3.s
1 AREA LIN612450097, CODE, READONLY
2 ENTRY
3 ;*****
4 ; (3)Write a program to reverse the bits in R0 so that the register
5 ; R0 containing b31b30b29...b1b0 now contains b0b1...b29b30b31, assuming R0 contains the value 0xDEADFACE initially.
6 ;*****
7 LDR r0, =0xDEADFACE ; initially
8
9 LDR r1, =0x80000000 ; bit 31
10 LDR r2, =0x1 ; bit 0
11 MOV r3, #32 ; counter
12 MOV r4, #0 ; temp
13 reverse
14 TST r0, r2
15 BICEQ r4, r1
16 ORRNE r4, r1
17 LSR r1, #1
18 LSL r2, #1
19 SUB r3, #1
20 CMP r3, #0
21 BNE reverse
22
23 MOV r0, r4
24
25 STOP B STOP
26 END
Memory 1
Address: 0x00000000
0x00000000: 34 00 9F E5 02 11 A0 E3 01 20 A0 E3 20 30 A0 E3 00 40 A0 E3 02 00 10 E1 01 40 C4 01 01 40 84 11 A1 10 A0 E1 82 20 A0 E1 01 30 43 E2 00 00 53
0x0000002F: E3 F7 FF FF 1A 04 00 A0 E1 FE FF FF EA CE FA AD DE 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x0000005E: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x0000008D: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x000000BC: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x000000EB: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
Call Stack + Locals
Memory 1

第2大題

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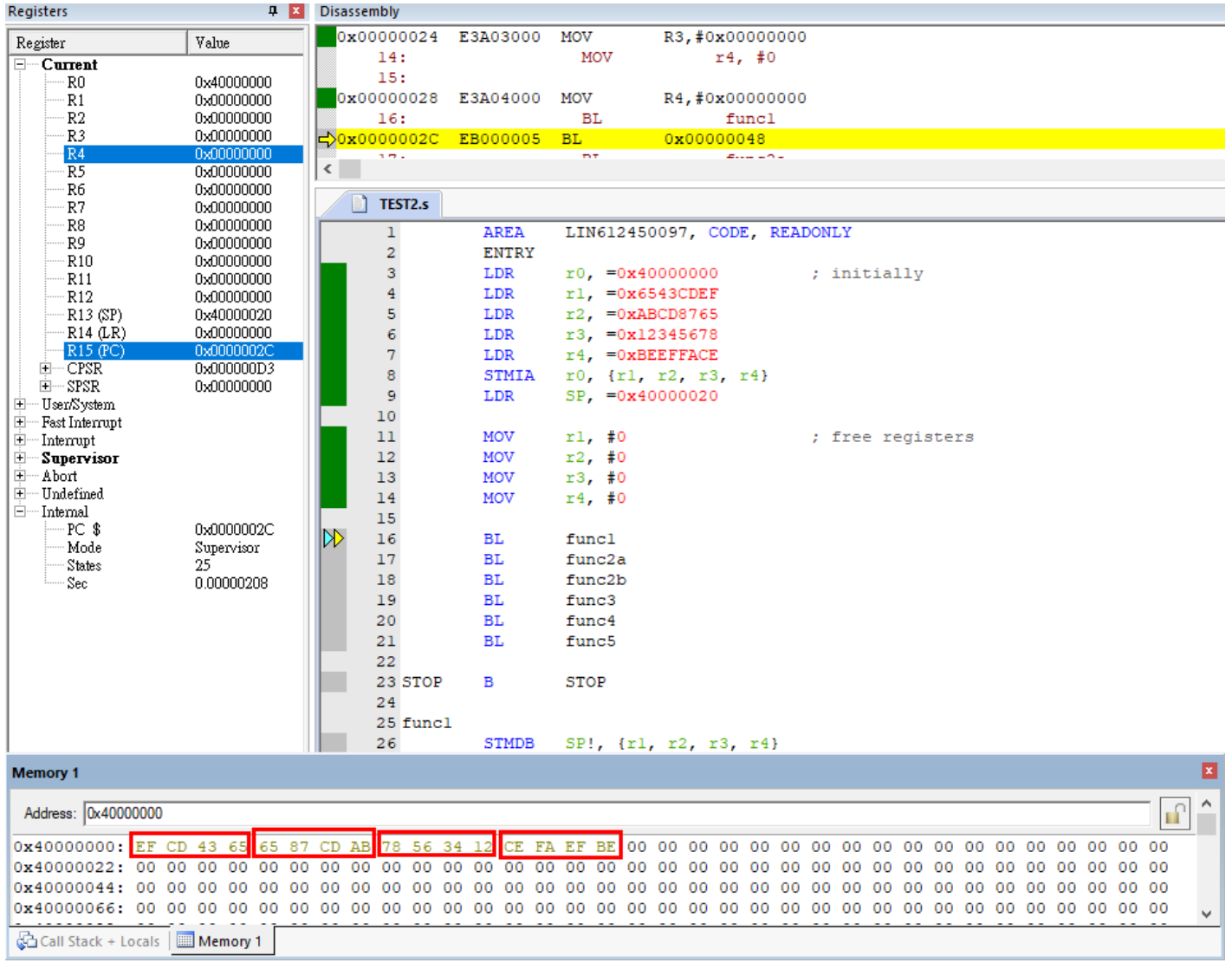
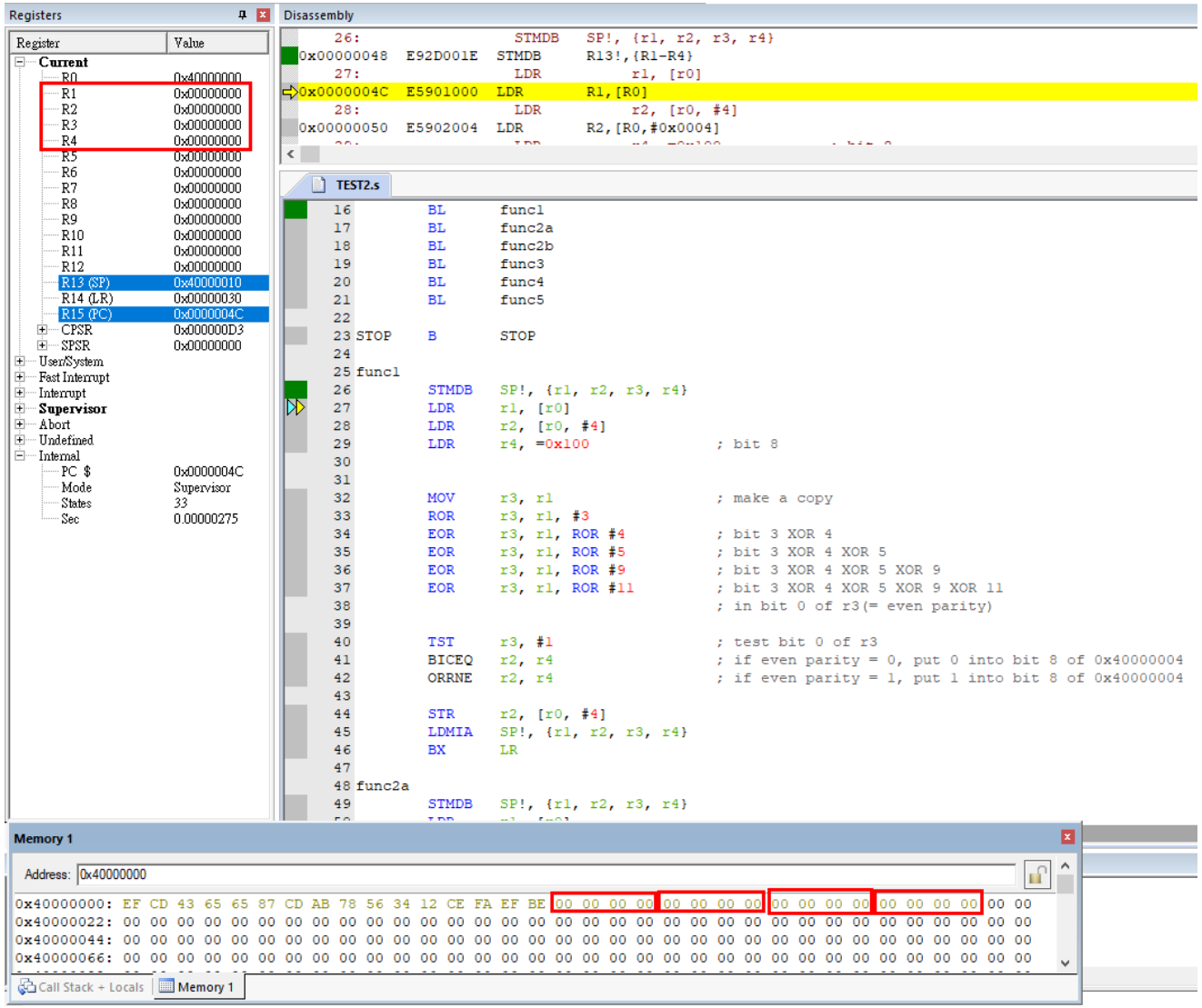
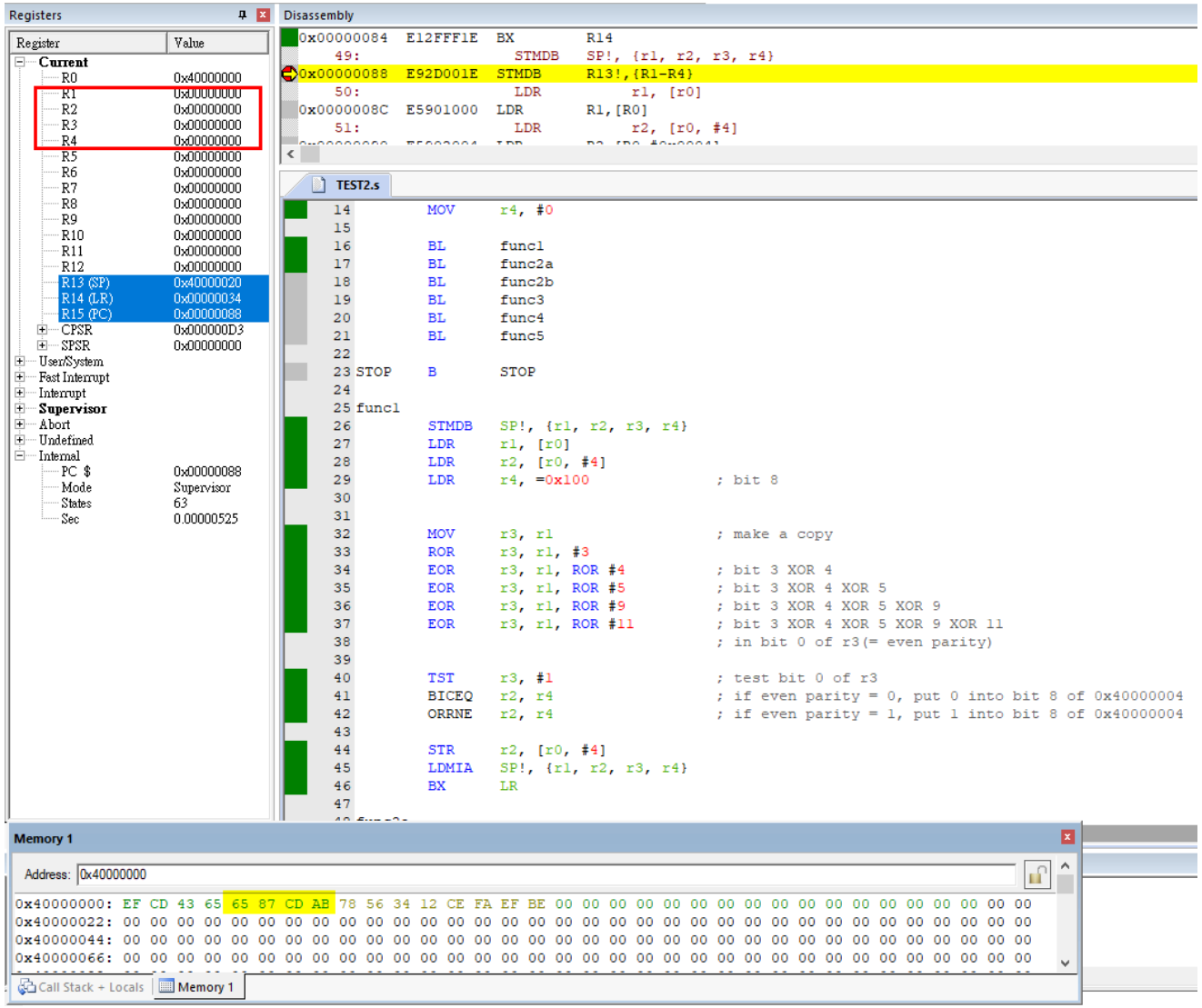
2. Initially


Registers
Register
Value
Current
R0 0x40000000
R1 0x00000000
R2 0x00000000
R3 0x00000000
R4 0x00000000
R5 0x00000000
R6 0x00000000
R7 0x00000000
R8 0x00000000
R9 0x00000000
R10 0x00000000
R11 0x00000000
R12 0x00000000
R13 (SP) 0x40000020
R14 (LR) 0x00000000
R15 (PC) 0x0000002C
CPSR 0x000000D3
SPSR 0x00000000
User/System
Fast Interrupt
Interrupt
Supervisor
Abort
Undefined
Internal
PC $ 0x0000002C
Mode Supervisor
States 25
Sec 0.00000208
Disassembly
0x00000024 E3A03000 MOV R3,#0x00000000
14: MOV r4, #0
15:
0x00000028 E3A04000 MOV R4,#0x00000000
16: BL func1
0x0000002C EB000005 BL 0x00000048
TEST2.s
1 AREA LIN612450097, CODE, READONLY
2 ENTRY
3 LDR r0, =0x40000000 ; initially
4 LDR r1, =0x6543CDEF
5 LDR r2, =0xABCD8765
6 LDR r3, =0x12345678
7 LDR r4, =0xBEEFFACE
8 STMIA r0, {r1, r2, r3, r4}
9 LDR SP, =0x40000020
10
11 MOV r1, #0 ; free registers
12 MOV r2, #0
13 MOV r3, #0
14 MOV r4, #0
15
16 BL func1
17 BL func2a
18 BL func2b
19 BL func3
20 BL func4
21 BL func5
22
23 STOP B STOP
24
25 func1
26 STMDB SP!, {r1, r2, r3, r4}
Memory 1
Address: 0x40000000
0x40000000: EF CD 43 65 65 87 CD AB 78 56 34 12 CE FA EF BE 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x40000022: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x40000044: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x40000066: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
Call Stack + Locals
Memory 1

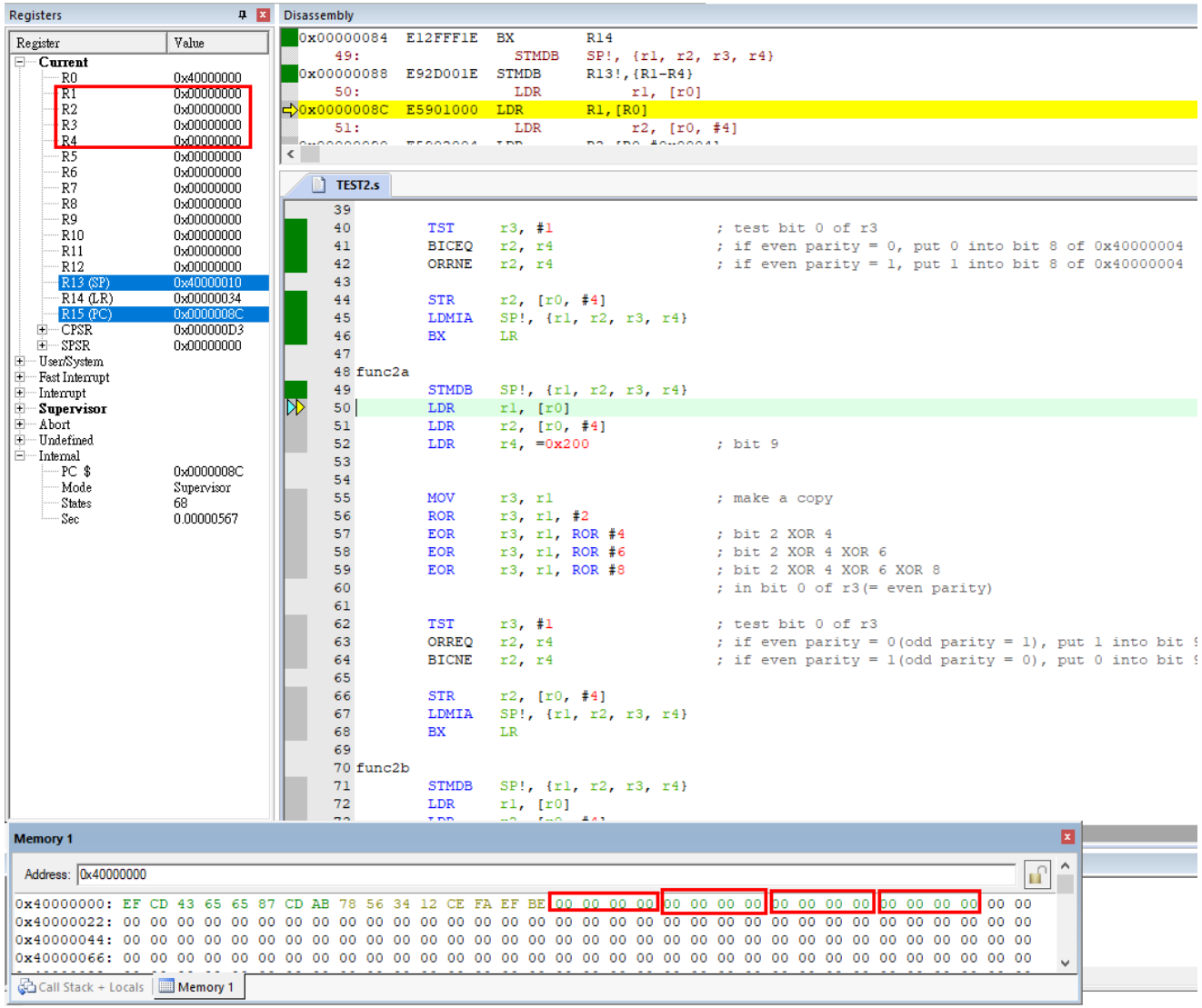
2.(1) func1(STMDB SP!, {r1, r2, r3, r4})



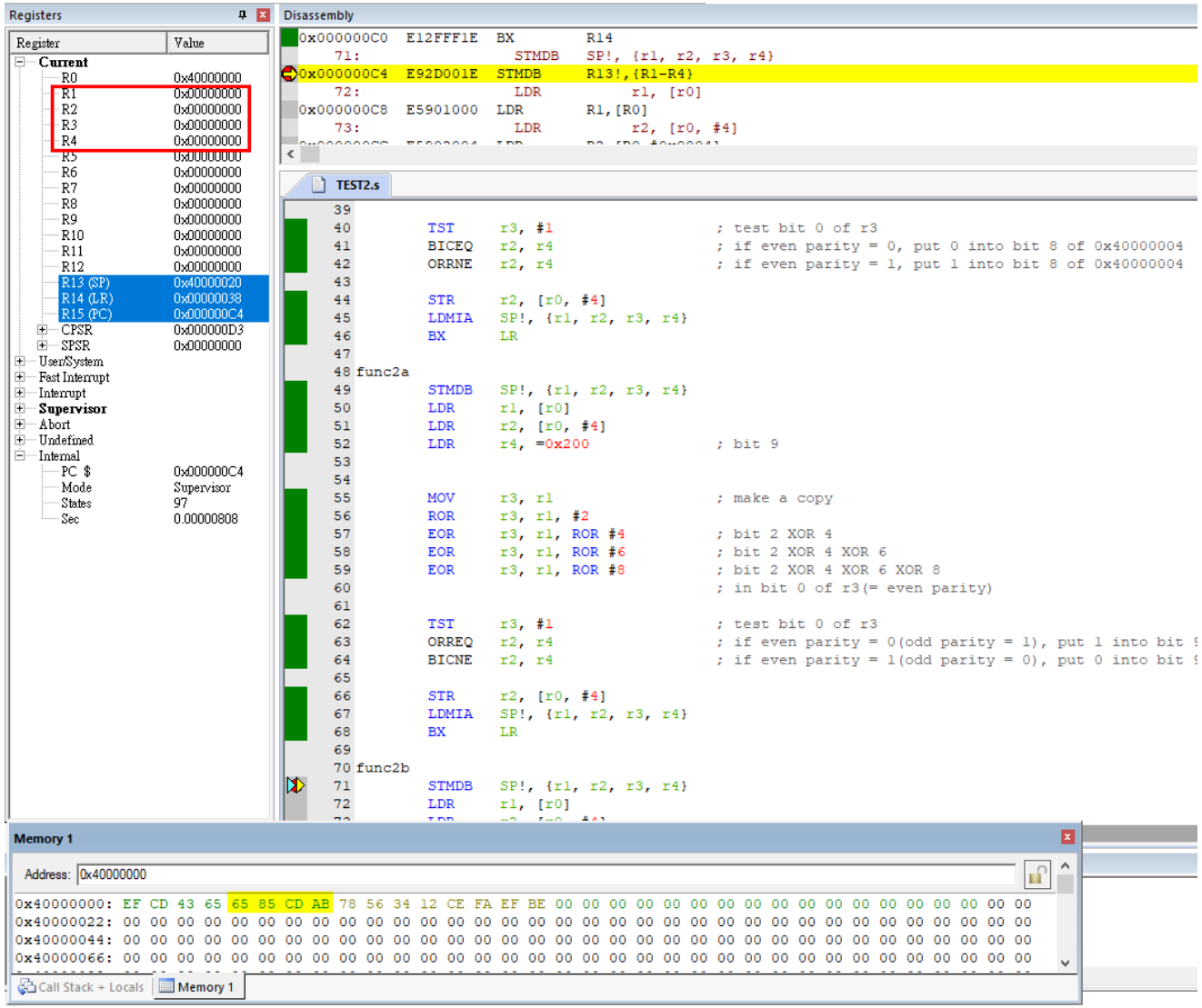
2.(1) func1


Registers
Register
Value
Current
R0 0x40000000
R1 0x00000000
R2 0x00000000
R3 0x00000000
R4 0x00000000
R5 0x00000000
R6 0x00000000
R7 0x00000000
R8 0x00000000
R9 0x00000000
R10 0x00000000
R11 0x00000000
R12 0x00000000
R13 (SP) 0x40000020
R14 (LR) 0x00000034
R15 (PC) 0x00000088
CPSR 0x000000D3
SPSR 0x00000000
User/System
Fast Interrupt
Interrupt
Supervisor
Abort
Undefined
Internal
PC $ 0x00000088
Mode Supervisor
States 63
Sec 0.00000525
Disassembly
0x00000084 E12FFF1E BX R14
49: STMDB SP!, {r1, r2, r3, r4}
0x00000088 E92D001E STMDB R13!,{R1-R4}
50: LDR r1, [r0]
0x0000008C E5901000 LDR R1,[R0]
51: LDR r2, [r0, #4]
TEST2.s
14 MOV r4, #0
15
16 BL func1
17 BL func2a
18 BL func2b
19 BL func3
20 BL func4
21 BL func5
22
23 STOP B STOP
24
25 func1
26 STMDB SP!, {r1, r2, r3, r4}
27 LDR r1, [r0]
28 LDR r2, [r0, #4]
29 LDR r4, =0x100 ; bit 8
30
31
32 MOV r3, r1 ; make a copy
33 ROR r3, r1, #3
34 EOR r3, r1, ROR #4 ; bit 3 XOR 4
35 EOR r3, r1, ROR #5 ; bit 3 XOR 4 XOR 5
36 EOR r3, r1, ROR #9 ; bit 3 XOR 4 XOR 5 XOR 9
37 EOR r3, r1, ROR #11 ; bit 3 XOR 4 XOR 5 XOR 9 XOR 11
38 ; in bit 0 of r3(= even parity)
39
40 TST r3, #1 ; test bit 0 of r3
41 BICEQ r2, r4 ; if even parity = 0, put 0 into bit 8 of 0x40000004
42 ORRNE r2, r4 ; if even parity = 1, put 1 into bit 8 of 0x40000004
43
44 STR r2, [r0, #4]
45 LDMIA SP!, {r1, r2, r3, r4}
46 BX LR
47
Memory 1
Address: 0x40000000
0x40000000: EF CD 43 65 65 87 CD AB 78 56 34 12 CE FA EF BE 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x40000022: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x40000044: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x40000066: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
Call Stack + Locals
Memory 1

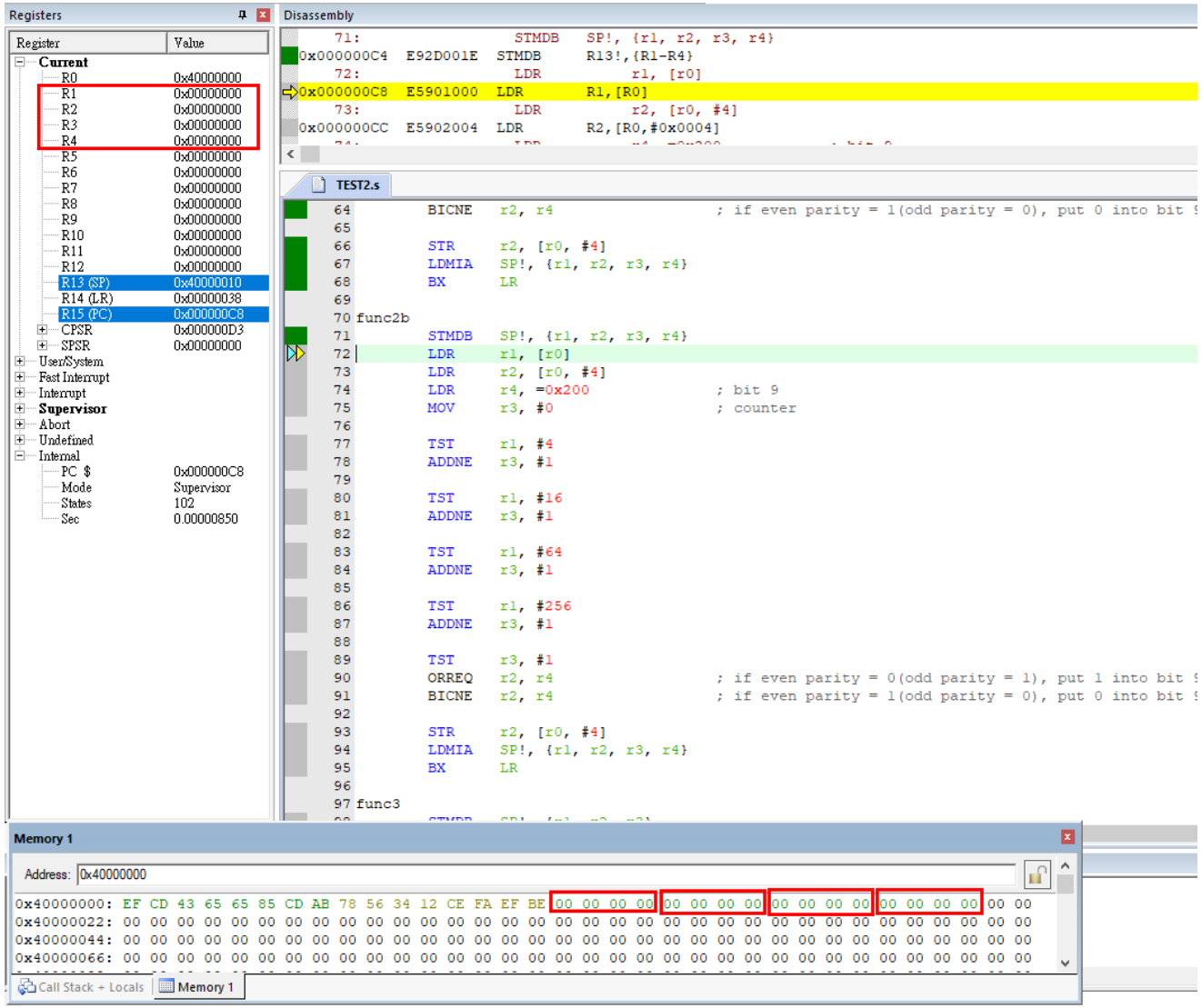
2.(2)(a) func2a (STMDB SP!, {r1, r2, r3, r4})



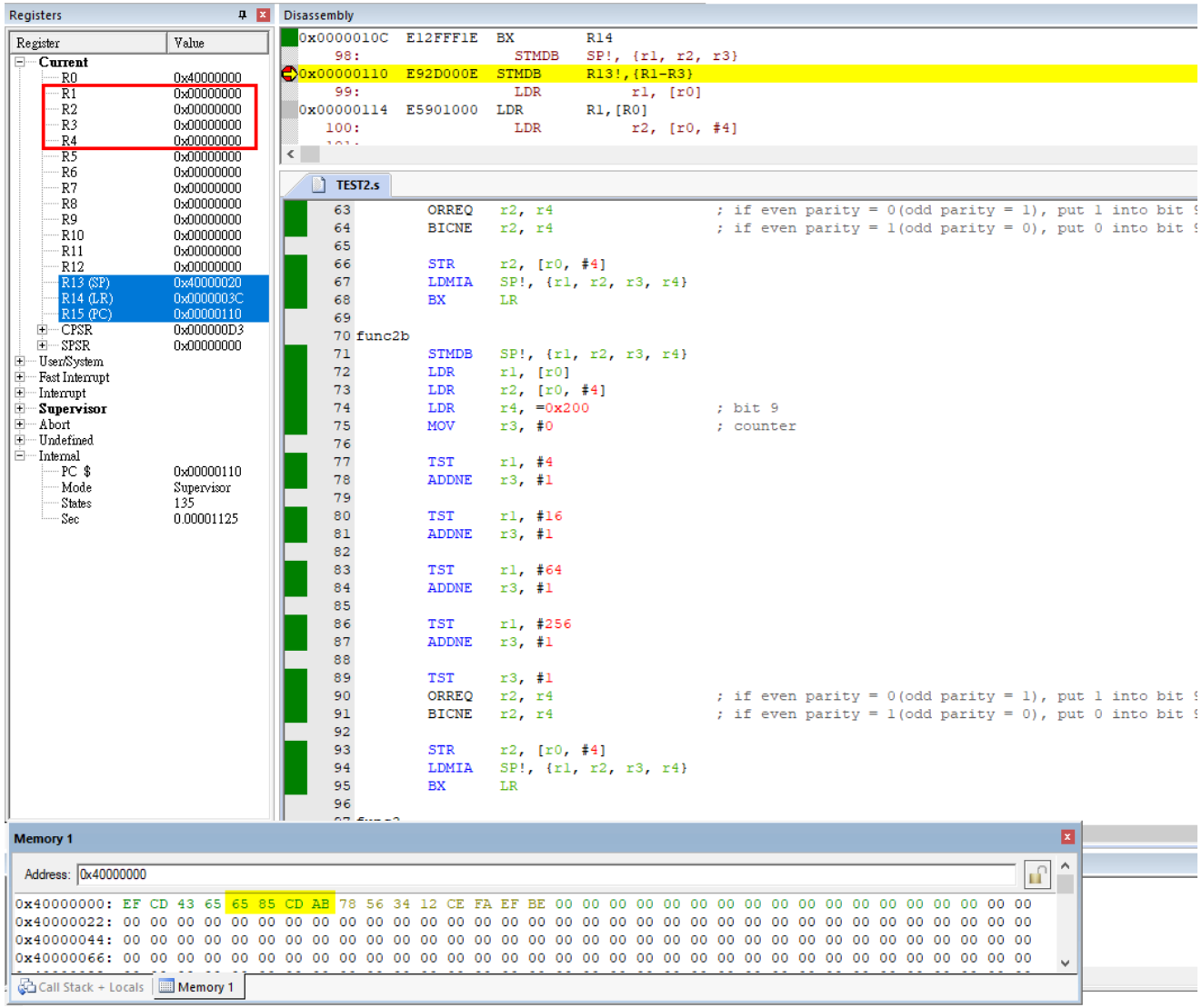
2.(2)(a) func2a


Registers
Register
Value
Current
R0 0x40000000
R1 0x00000000
R2 0x00000000
R3 0x00000000
R4 0x00000000
R5 0x00000000
R6 0x00000000
R7 0x00000000
R8 0x00000000
R9 0x00000000
R10 0x00000000
R11 0x00000000
R12 0x00000000
R13 (SP) 0x40000020
R14 (LR) 0x00000038
R15 (PC) 0x000000C4
CPSR 0x000000D3
SPSR 0x00000000
User/System
Fast Interrupt
Interrupt
Supervisor
Abort
Undefined
Internal
PC $ 0x000000C4
Mode Supervisor
States 97
Sec 0.00000808
Disassembly
0x000000C0 E12FFF1E BX R14
71: STMDB SP!, {r1, r2, r3, r4}
0x000000C4 E92D001E STMDB R13!,{R1-R4}
72: LDR r1, [r0]
0x000000C8 E5901000 LDR R1,[R0]
73: LDR r2, [r0, #4]
TEST2.s
39
40 TST r3, #1 ; test bit 0 of r3
41 BICEQ r2, r4 ; if even parity = 0, put 0 into bit 8 of 0x40000004
42 ORRNE r2, r4 ; if even parity = 1, put 1 into bit 8 of 0x40000004
43
44 STR r2, [r0, #4]
45 LDMIA SP!, {r1, r2, r3, r4}
46 BX LR
47
48 func2a
49 STMDB SP!, {r1, r2, r3, r4}
50 LDR r1, [r0]
51 LDR r2, [r0, #4]
52 LDR r4, =0x200 ; bit 9
53
54
55 MOV r3, r1 ; make a copy
56 ROR r3, r1, #2
57 EOR r3, r1, ROR #4 ; bit 2 XOR 4
58 EOR r3, r1, ROR #6 ; bit 2 XOR 4 XOR 6
59 EOR r3, r1, ROR #8 ; bit 2 XOR 4 XOR 6 XOR 8
60 ; in bit 0 of r3(= even parity)
61
62 TST r3, #1 ; test bit 0 of r3
63 ORREQ r2, r4 ; if even parity = 0(odd parity = 1), put 1 into bit
64 BICNE r2, r4 ; if even parity = 1(odd parity = 0), put 0 into bit
65
66 STR r2, [r0, #4]
67 LDMIA SP!, {r1, r2, r3, r4}
68 BX LR
69
70 func2b
71 STMDB SP!, {r1, r2, r3, r4}
72 LDR r1, [r0]
Memory 1
Address: 0x40000000
0x40000000: EF CD 43 65 65 85 CD AB 78 56 34 12 CE FA EF BE 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x40000022: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x40000044: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x40000066: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
Call Stack + Locals
Memory 1

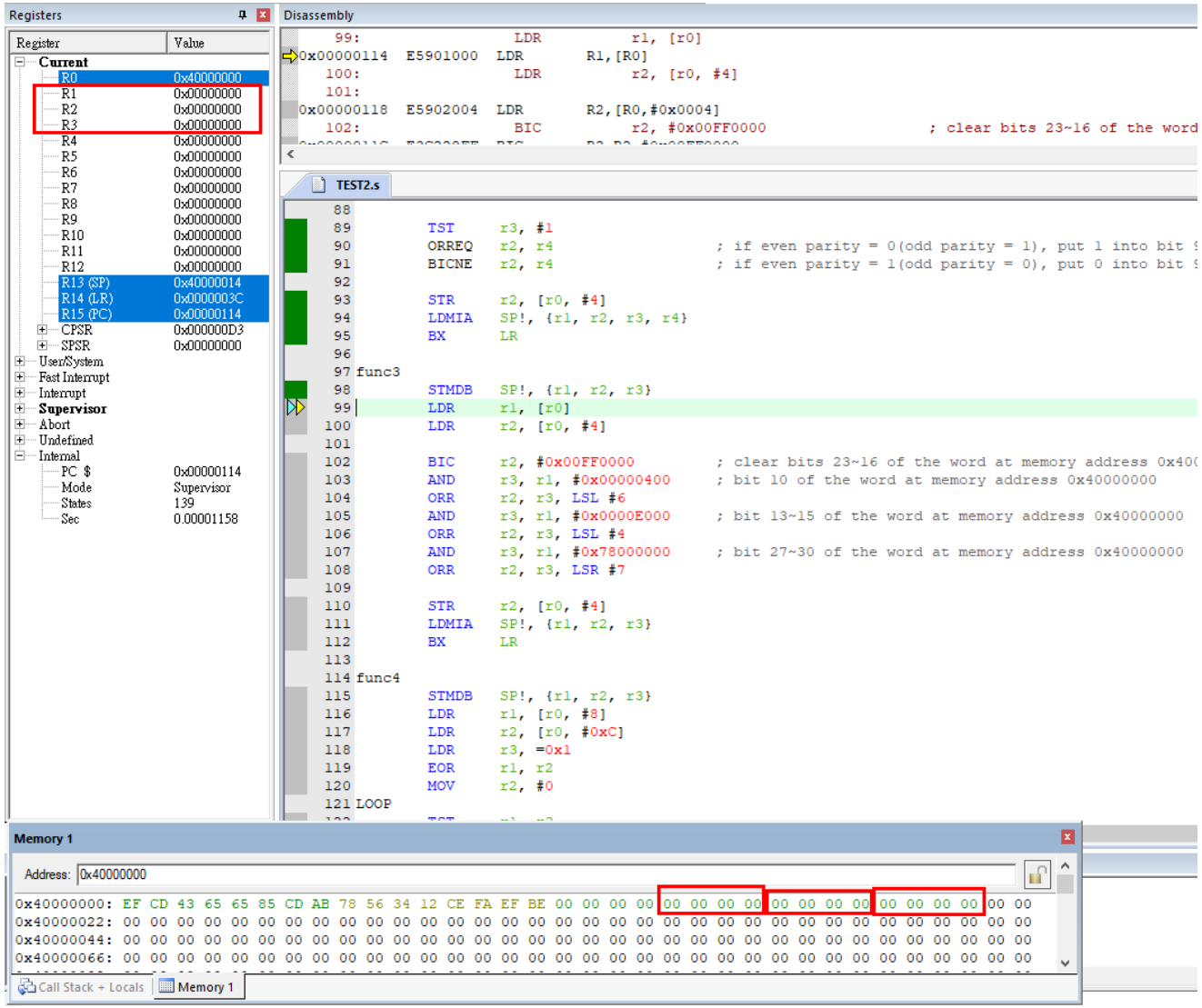
2.(2)(b) func2b (STMDB SP!, {r1, r2, r3, r4})



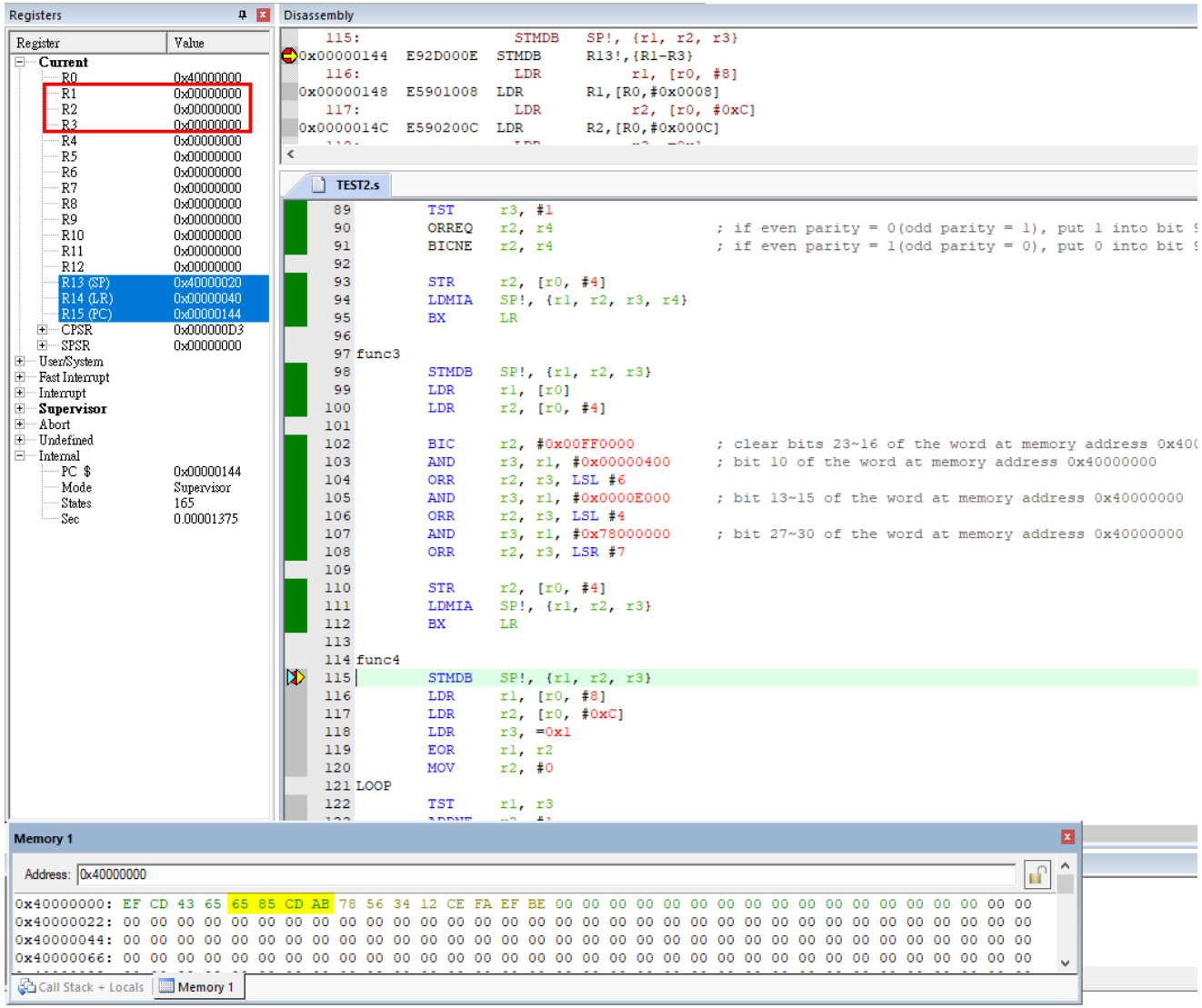
2.(2)(b) func2b


Registers
Register
Value
Current
R0 0x40000000
R1 0x00000000
R2 0x00000000
R3 0x00000000
R4 0x00000000
R5 0x00000000
R6 0x00000000
R7 0x00000000
R8 0x00000000
R9 0x00000000
R10 0x00000000
R11 0x00000000
R12 0x00000000
R13 (SP) 0x40000020
R14 (LR) 0x0000003C
R15 (PC) 0x00000110
CPSR 0x000000D3
SPSR 0x00000000
User/System
Fast Interrupt
Interrupt
Supervisor
Abort
Undefined
Internal
PC $ 0x00000110
Mode Supervisor
States 135
Sec 0.00001125
Disassembly
0x0000010C E12FFF1E BX R14
98: STMDB SP!, {r1, r2, r3}
0x00000110 E92D000E STMDB R13!,{R1-R3}
99: LDR r1, [r0]
0x00000114 E5901000 LDR R1,[R0]
100: LDR r2, [r0, #4]
TEST2.s
63 ORREQ r2, r4 ; if even parity = 0(odd parity = 1), put 1 into bit 9
64 BICNE r2, r4 ; if even parity = 1(odd parity = 0), put 0 into bit 9
65
66 STR r2, [r0, #4]
67 LDMIA SP!, {r1, r2, r3, r4}
68 BX LR
69
70 func2b
71 STMDB SP!, {r1, r2, r3, r4}
72 LDR r1, [r0]
73 LDR r2, [r0, #4]
74 LDR r4, =0x200 ; bit 9
75 MOV r3, #0 ; counter
76
77 TST r1, #4
78 ADDNE r3, #1
79
80 TST r1, #16
81 ADDNE r3, #1
82
83 TST r1, #64
84 ADDNE r3, #1
85
86 TST r1, #256
87 ADDNE r3, #1
88
89 TST r3, #1
90 ORREQ r2, r4 ; if even parity = 0(odd parity = 1), put 1 into bit 9
91 BICNE r2, r4 ; if even parity = 1(odd parity = 0), put 0 into bit 9
92
93 STR r2, [r0, #4]
94 LDMIA SP!, {r1, r2, r3, r4}
95 BX LR
96
Memory 1
Address: 0x40000000
0x40000000: EF CD 43 65 65 85 CD AB 78 56 34 12 CE FA EF BE 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x40000022: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x40000044: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x40000066: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
Call Stack + Locals
Memory 1

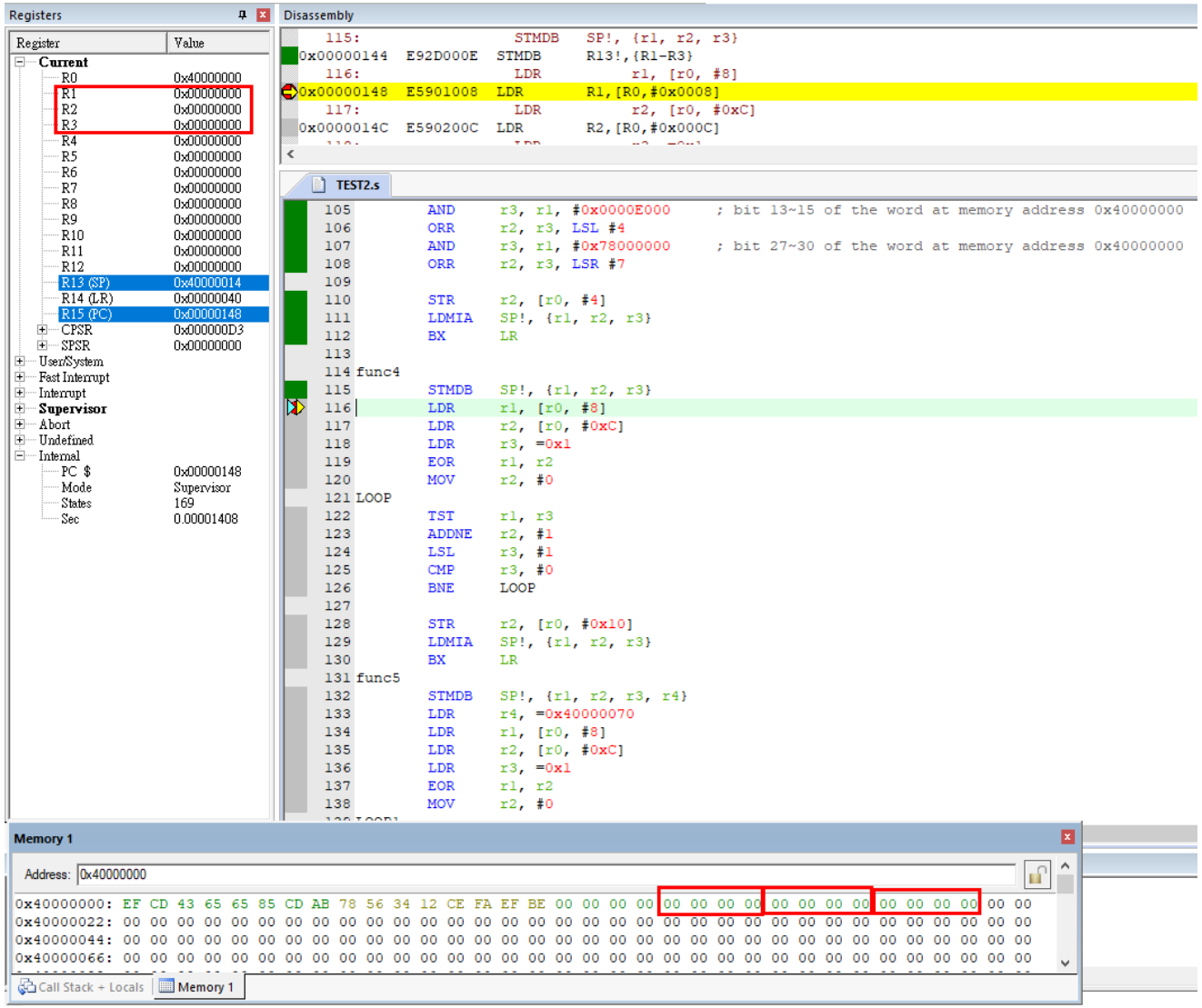
2.(3) func3 (STMDB SP!, {r1, r2, r3})



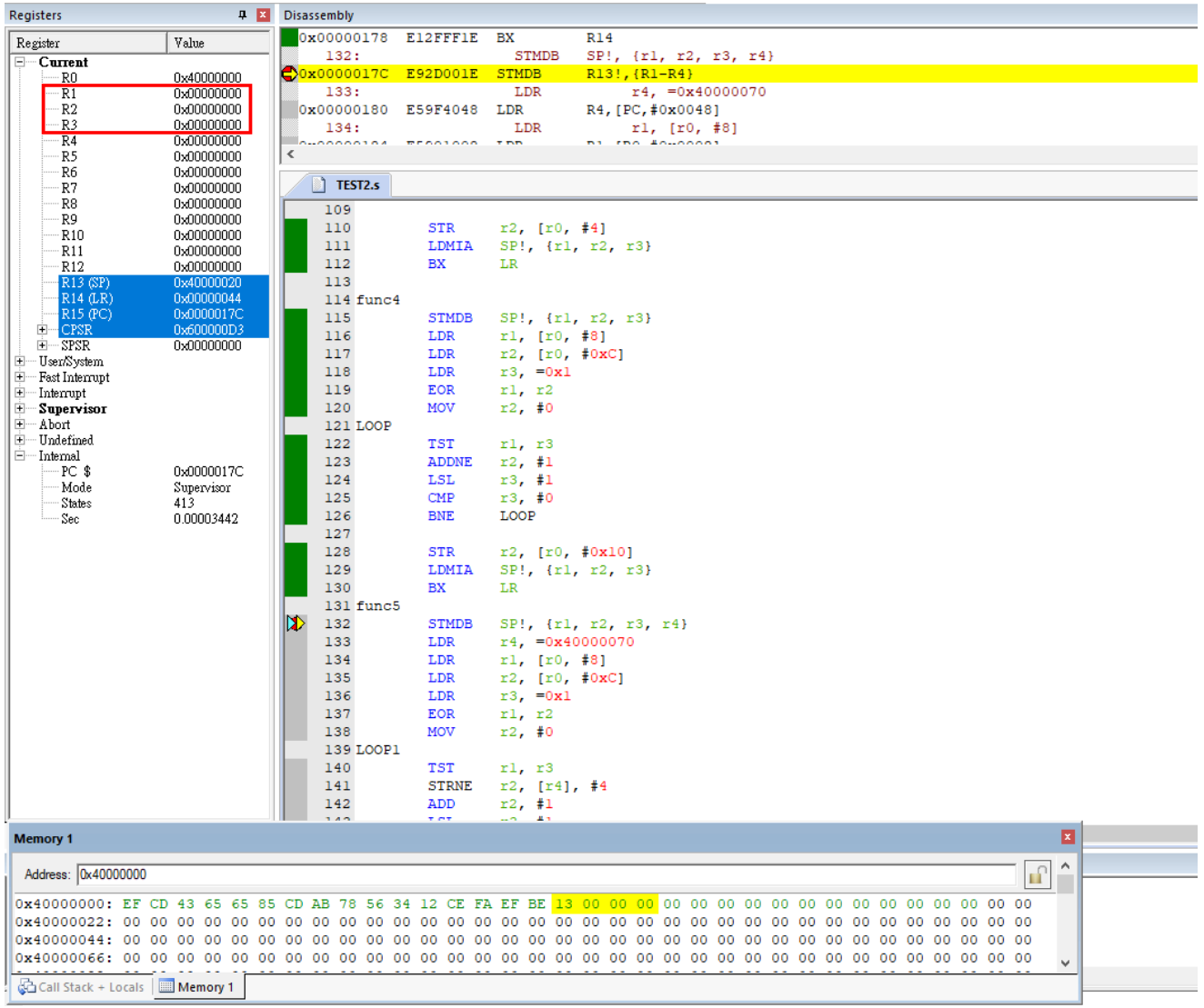
2.(3) func3


Registers
Register
Value
Current
R0 0x40000000
R1 0x00000000
R2 0x00000000
R3 0x00000000
R4 0x00000000
R5 0x00000000
R6 0x00000000
R7 0x00000000
R8 0x00000000
R9 0x00000000
R10 0x00000000
R11 0x00000000
R12 0x00000000
R13 (SP) 0x40000020
R14 (LR) 0x00000040
R15 (PC) 0x00000144
CPSR 0x000000D3
SPSR 0x00000000
User/System
Fast Interrupt
Interrupt
Supervisor
Abort
Undefined
Internal
PC $ 0x00000144
Mode Supervisor
States 165
Sec 0.00001375
Disassembly
115: STMDB SP!, {r1, r2, r3}
0x00000144 E92D000E STMDB R13!,{R1-R3}
116: LDR r1, [r0, #8]
0x00000148 E5901008 LDR R1,[R0,#0x0008]
117: LDR r2, [r0, #0xC]
0x0000014C E590200C LDR R2,[R0,#0x000C]
TEST2.s
89 TST r3, #1
90 ORREQ r2, r4 ; if even parity = 0(odd parity = 1), put 1 into bit
91 BICNE r2, r4 ; if even parity = 1(odd parity = 0), put 0 into bit
92
93 STR r2, [r0, #4]
94 LDMIA SP!, {r1, r2, r3, r4}
95 BX LR
96
97 func3
98 STMDB SP!, {r1, r2, r3}
99 LDR r1, [r0]
100 LDR r2, [r0, #4]
101
102 BIC r2, #0x00FF0000 ; clear bits 23~16 of the word at memory address 0x40
103 AND r3, r1, #0x00000400 ; bit 10 of the word at memory address 0x40000000
104 ORR r2, r3, LSL #6
105 AND r3, r1, #0x0000E000 ; bit 13~15 of the word at memory address 0x40000000
106 ORR r2, r3, LSL #4
107 AND r3, r1, #0x78000000 ; bit 27~30 of the word at memory address 0x40000000
108 ORR r2, r3, LSR #7
109
110 STR r2, [r0, #4]
111 LDMIA SP!, {r1, r2, r3}
112 BX LR
113
114 func4
115 STMDB SP!, {r1, r2, r3}
116 LDR r1, [r0, #8]
117 LDR r2, [r0, #0xC]
118 LDR r3, =0x1
119 EOR r1, r2
120 MOV r2, #0
121 LOOP
122 TST r1, r3
Memory 1
Address: 0x40000000
0x40000000: EF CD 43 65 65 85 CD AB 78 56 34 12 CE FA EF BE 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x40000022: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x40000044: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x40000066: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
Call Stack + Locals
Memory 1

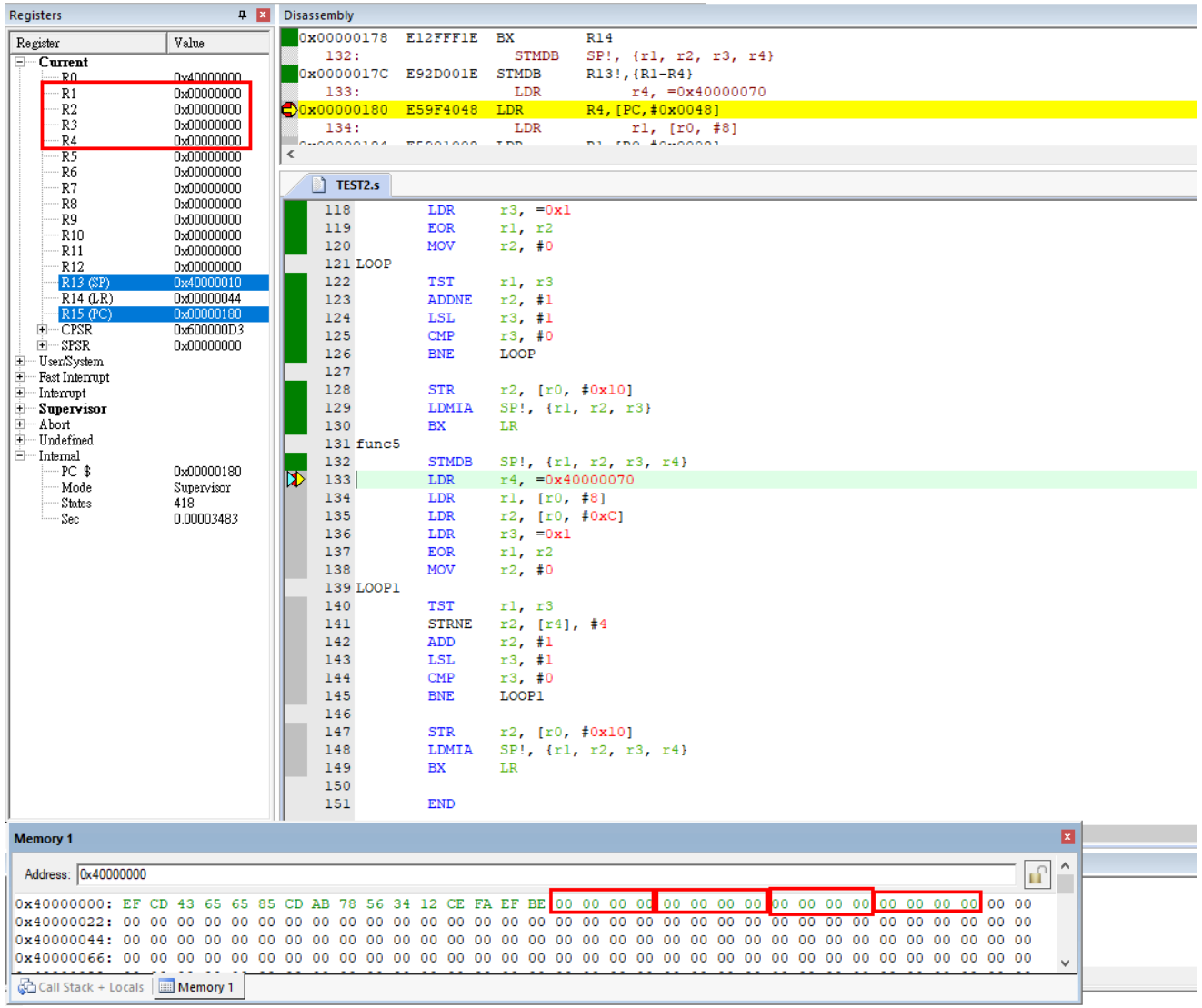
2.(4) func4 (STMDB SP!, {r1, r2, r3})



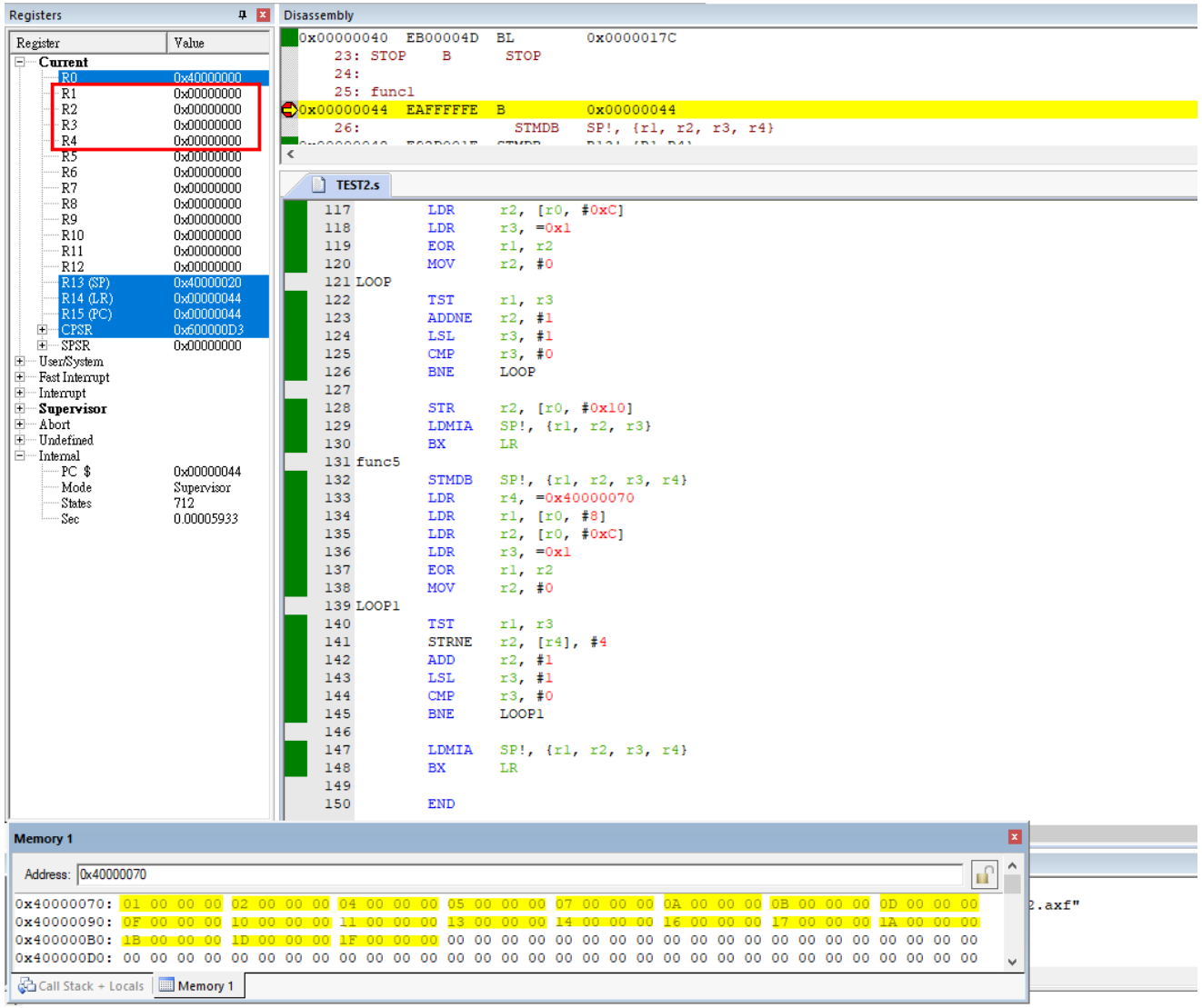
2.(4) func4


Registers
Register
Value
Current
R0 0x40000000
R1 0x00000000
R2 0x00000000
R3 0x00000000
R4 0x00000000
R5 0x00000000
R6 0x00000000
R7 0x00000000
R8 0x00000000
R9 0x00000000
R10 0x00000000
R11 0x00000000
R12 0x00000000
R13 (SP) 0x40000020
R14 (LR) 0x00000044
R15 (PC) 0x0000017C
CPSR 0x600000D3
SPSR 0x00000000
User/System
Fast Interrupt
Interrupt
Supervisor
Abort
Undefined
Internal
PC $ 0x0000017C
Mode Supervisor
States 413
Sec 0.00003442
Disassembly
0x00000178 E12FFF1E BX R14
132: STMDB SP!, {r1, r2, r3, r4}
0x0000017C E92D001E STMDB R13!,{R1-R4}
133: LDR r4, =0x40000070
0x00000180 E59F4048 LDR R4,[PC,#0x0048]
134: LDR r1, [r0, #8]
TEST2.s
109
110 STR r2, [r0, #4]
111 LDMIA SP!, {r1, r2, r3}
112 BX LR
113
114 func4
115 STMDB SP!, {r1, r2, r3}
116 LDR r1, [r0, #8]
117 LDR r2, [r0, #0xC]
118 LDR r3, =0x1
119 EOR r1, r2
120 MOV r2, #0
121 LOOP
122 TST r1, r3
123 ADDNE r2, #1
124 LSL r3, #1
125 CMP r3, #0
126 BNE LOOP
127
128 STR r2, [r0, #0x10]
129 LDMIA SP!, {r1, r2, r3}
130 BX LR
131 func5
132 STMDB SP!, {r1, r2, r3, r4}
133 LDR r4, =0x40000070
134 LDR r1, [r0, #8]
135 LDR r2, [r0, #0xC]
136 LDR r3, =0x1
137 EOR r1, r2
138 MOV r2, #0
139 LOOP1
140 TST r1, r3
141 STRNE r2, [r4], #4
142 ADD r2, #1
Memory 1
Address: 0x40000000
0x40000000: EF CD 43 65 65 85 CD AB 78 56 34 12 CE FA EF BE 13 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x40000022: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x40000044: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x40000066: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
Call Stack + Locals
Memory 1

2.(5) func5 (STMDB SP!, {r1, r2, r3, r4})



2.(5) func5


Registers
Register
Value
Current
R0 0x40000000
R1 0x00000000
R2 0x00000000
R3 0x00000000
R4 0x00000000
R5 0x00000000
R6 0x00000000
R7 0x00000000
R8 0x00000000
R9 0x00000000
R10 0x00000000
R11 0x00000000
R12 0x00000000
R13 (SP) 0x40000020
R14 (LR) 0x00000044
R15 (PC) 0x00000044
CPSR 0x600000D3
SPSR 0x00000000
User/System
Fast Interrupt
Interrupt
Supervisor
Abort
Undefined
Internal
PC $ 0x00000044
Mode Supervisor
States 712
Sec 0.00005933
Disassembly
0x00000040 EB00004D BL 0x0000017C
23: STOP B STOP
24:
25: func1
0x00000044 EAFFFFFE B 0x00000044
26: STMDB SP!, {r1, r2, r3, r4}
TEST2.s
117 LDR r2, [r0, #0xC]
118 LDR r3, =0x1
119 EOR r1, r2
120 MOV r2, #0
121 LOOP
122 TST r1, r3
123 ADDNE r2, #1
124 LSL r3, #1
125 CMP r3, #0
126 BNE LOOP
127
128 STR r2, [r0, #0x10]
129 LDMIA SP!, {r1, r2, r3}
130 BX LR
131 func5
132 STMDB SP!, {r1, r2, r3, r4}
133 LDR r4, =0x40000070
134 LDR r1, [r0, #8]
135 LDR r2, [r0, #0xC]
136 LDR r3, =0x1
137 EOR r1, r2
138 MOV r2, #0
139 LOOP1
140 TST r1, r3
141 STRNE r2, [r4], #4
142 ADD r2, #1
143 LSL r3, #1
144 CMP r3, #0
145 BNE LOOP1
146
147 LDMIA SP!, {r1, r2, r3, r4}
148 BX LR
149
150 END
Memory 1
Address: 0x40000070
0x40000070: 01 00 00 00 02 00 00 00 04 00 00 00 05 00 00 00 07 00 00 00 0A 00 00 00 0B 00 00 00 0D 00 00 00
0x40000090: 0F 00 00 00 10 00 00 00 11 00 00 00 13 00 00 00 14 00 00 00 16 00 00 00 17 00 00 00 1A 00 00 00
0x400000B0: 1B 00 00 00 1D 00 00 00 1F 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x400000D0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
Call Stack + Locals
Memory 1

第3大題

2023 Advanced Mixed-Operation System (AMOS) Lab.

Tamkang University
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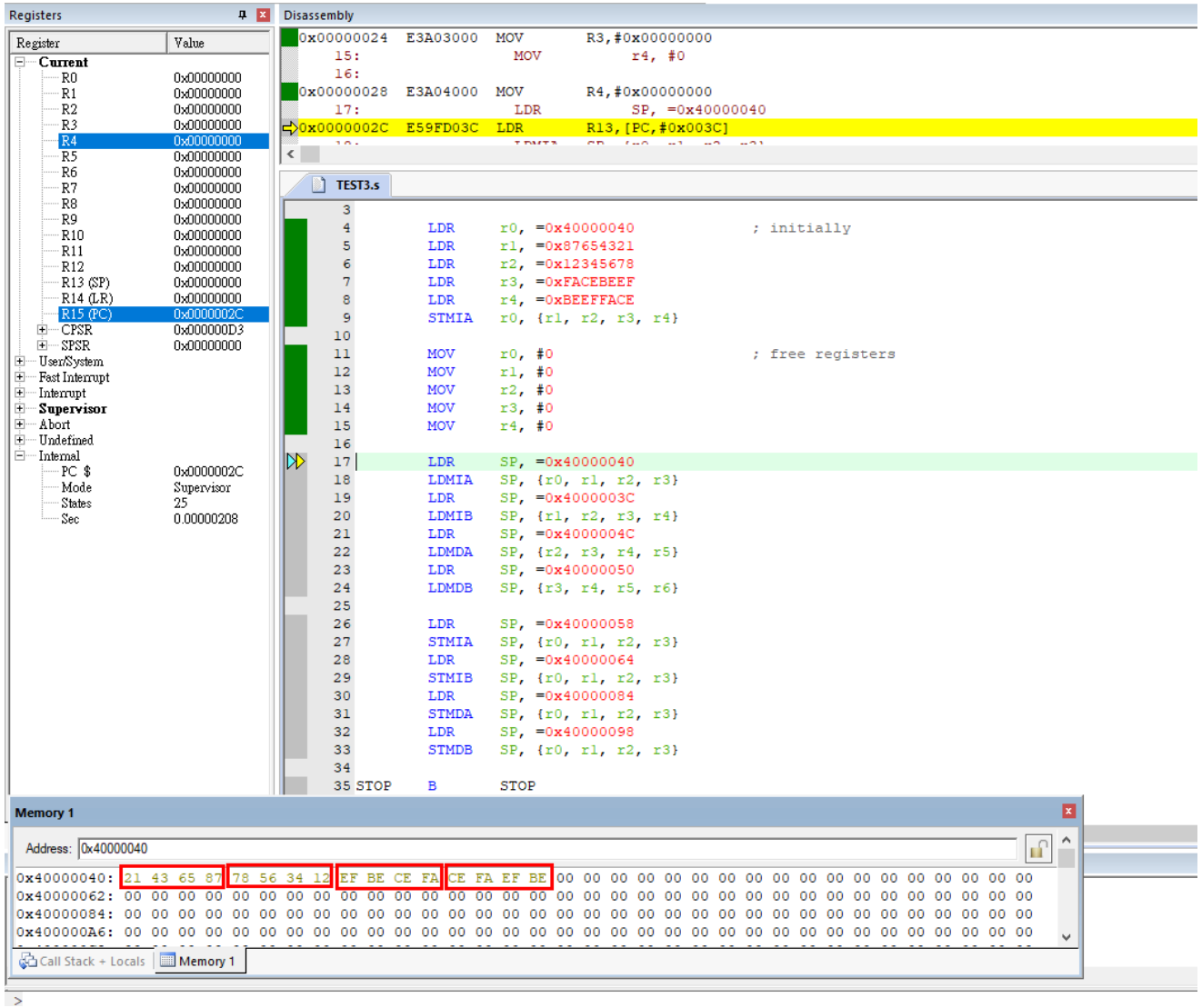
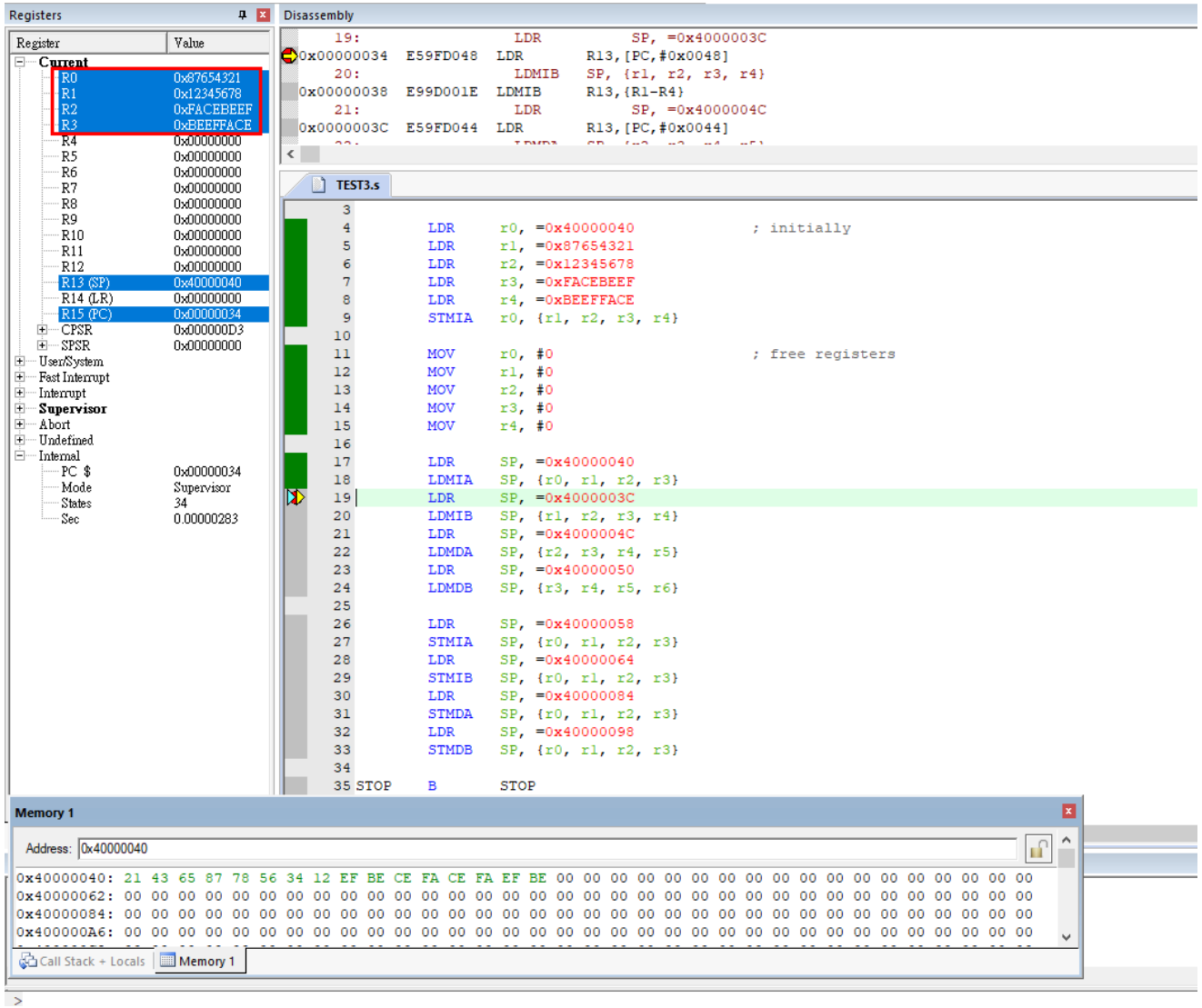
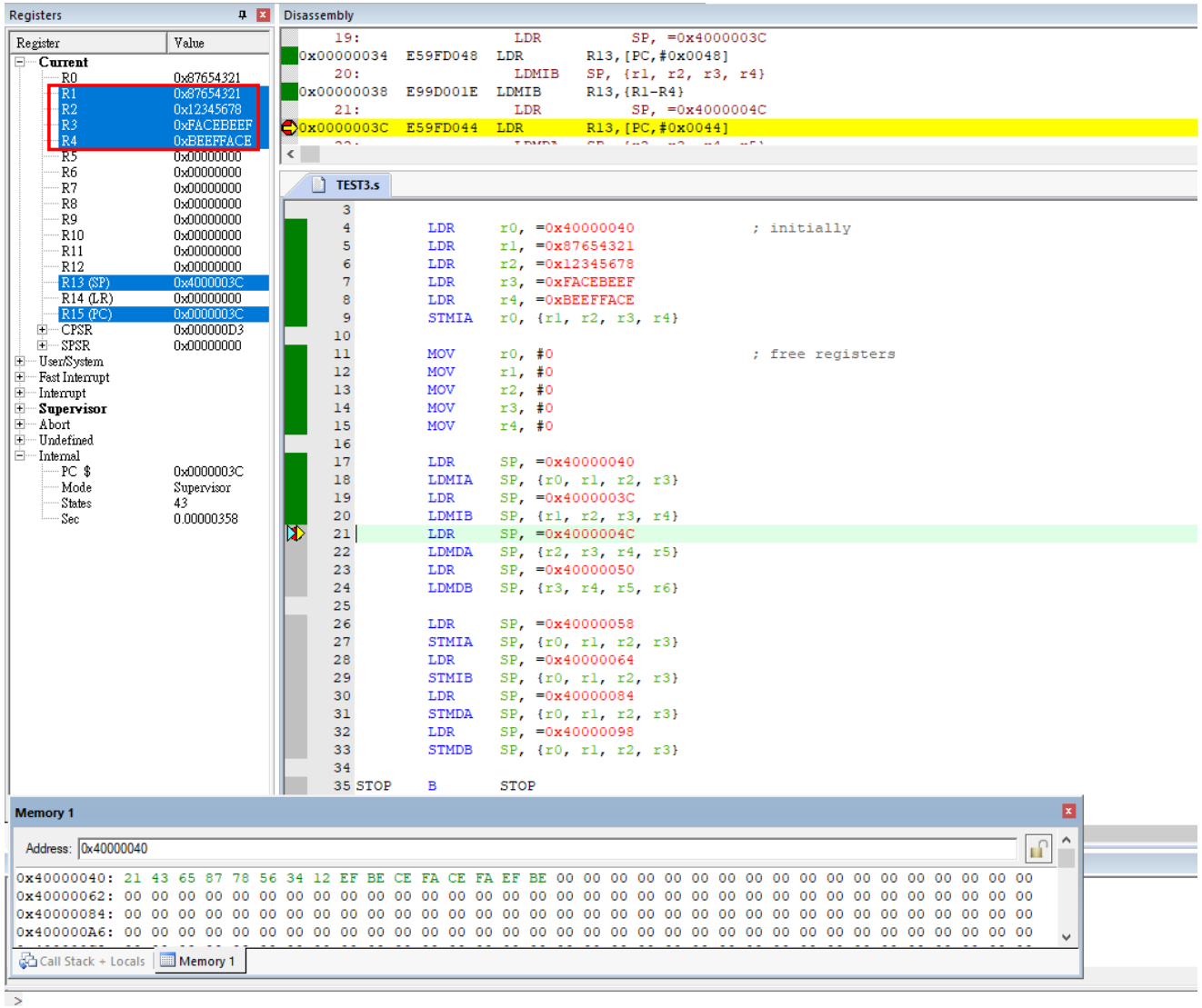
3. Initially


Registers
Register
Value
Current
R0 0x00000000
R1 0x00000000
R2 0x00000000
R3 0x00000000
R4 0x00000000
R5 0x00000000
R6 0x00000000
R7 0x00000000
R8 0x00000000
R9 0x00000000
R10 0x00000000
R11 0x00000000
R12 0x00000000
R13 (SP) 0x00000000
R14 (LR) 0x00000000
R15 (PC) 0x0000002C
CPSR 0x000000D3
SPSR 0x00000000
User/System
Fast Interrupt
Interrupt
Supervisor
Abort
Undefined
Internal
PC $ 0x0000002C
Mode Supervisor
States 25
Sec 0.00000208
Disassembly
0x00000024 E3A03000 MOV R3,#0x00000000
15: MOV r4, #0
16:
0x00000028 E3A04000 MOV R4,#0x00000000
17: LDR SP, =0x40000040
0x0000002C E59FD03C LDR R13,[PC,#0x003C]
TEST3.s
3
4 LDR r0, =0x40000040 ; initially
5 LDR r1, =0x87654321
6 LDR r2, =0x12345678
7 LDR r3, =0xFACEBEEF
8 LDR r4, =0xBEEFFACE
9 STMIA r0, {r1, r2, r3, r4}
10
11 MOV r0, #0 ; free registers
12 MOV r1, #0
13 MOV r2, #0
14 MOV r3, #0
15 MOV r4, #0
16
17 LDR SP, =0x40000040
18 LDMIA SP, {r0, r1, r2, r3}
19 LDR SP, =0x4000003C
20 LDMIB SP, {r1, r2, r3, r4}
21 LDR SP, =0x4000004C
22 LDMDA SP, {r2, r3, r4, r5}
23 LDR SP, =0x40000050
24 LDMDB SP, {r3, r4, r5, r6}
25
26 LDR SP, =0x40000058
27 STMIA SP, {r0, r1, r2, r3}
28 LDR SP, =0x40000064
29 STMIB SP, {r0, r1, r2, r3}
30 LDR SP, =0x40000084
31 STMDA SP, {r0, r1, r2, r3}
32 LDR SP, =0x40000098
33 STMDB SP, {r0, r1, r2, r3}
34
35 STOP B STOP
Memory 1
Address: 0x40000040
0x40000040: 21 43 65 87 78 56 34 12 EF BE CE FA CE FA EF BE 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x40000062: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x40000084: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x400000A6: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
Call Stack + Locals
Memory 1

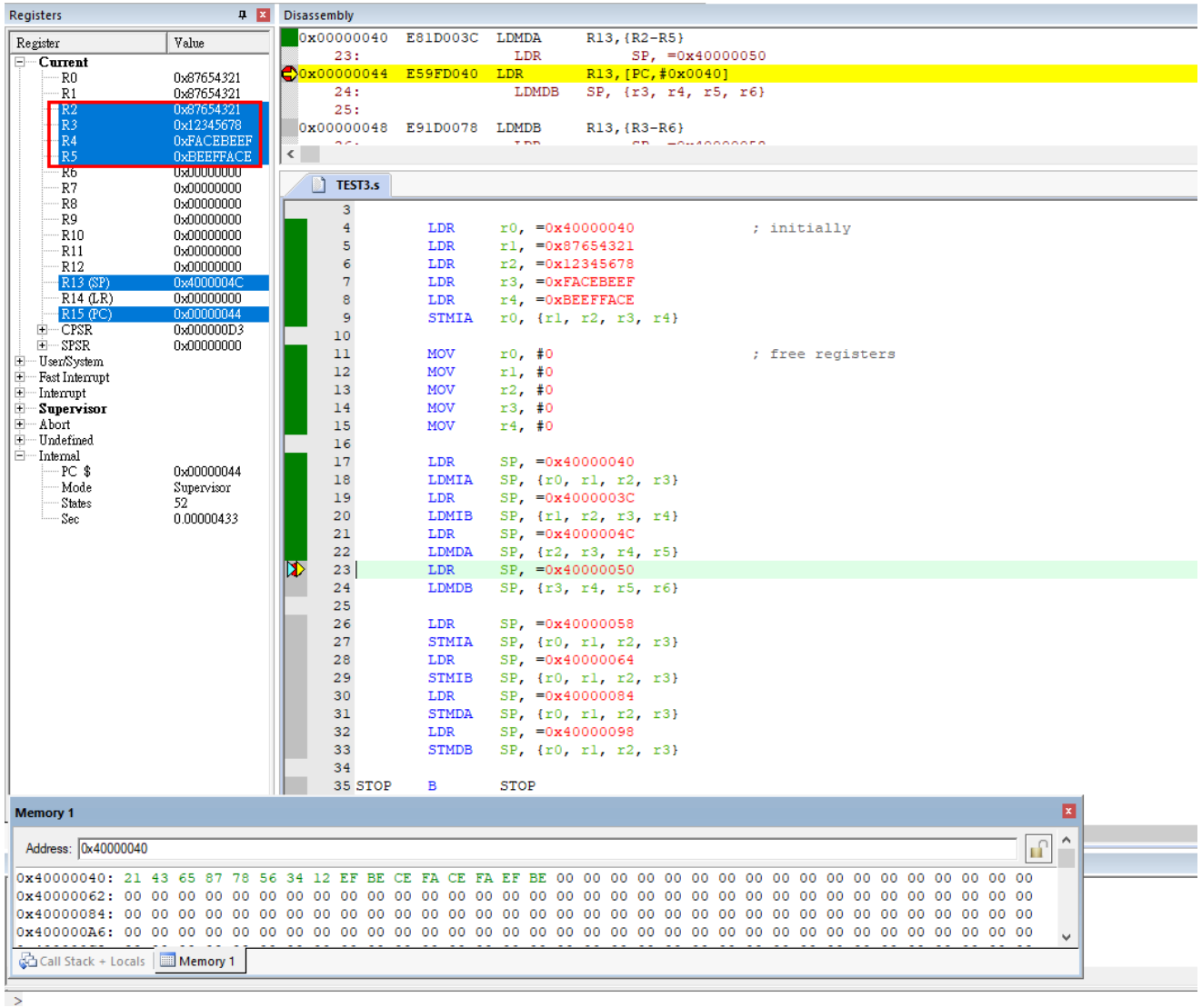
3.(1)


Registers
Register
Value
Current
R0 0x87654321
R1 0x12345678
R2 0xFACEBEEF
R3 0xBEEFFACE
R4 0x00000000
R5 0x00000000
R6 0x00000000
R7 0x00000000
R8 0x00000000
R9 0x00000000
R10 0x00000000
R11 0x00000000
R12 0x00000000
R13 (SP) 0x40000040
R14 (LR) 0x00000000
R15 (PC) 0x00000034
CPSR 0x000000D3
SPSR 0x00000000
User/System
Fast Interrupt
Interrupt
Supervisor
Abort
Undefined
Internal
PC $ 0x00000034
Mode Supervisor
States 34
Sec 0.00000283
Disassembly
19: LDR SP, =0x4000003C
0x00000034 E59FD048 LDR R13,[PC,#0x0048]
20: LDMIB SP, {r1, r2, r3, r4}
0x00000038 E99D001E LDMIB R13,{R1-R4}
21: LDR SP, =0x4000004C
0x0000003C E59FD044 LDR R13,[PC,#0x0044]
TEST3.s
4 LDR r0, =0x40000040 ; initially
5 LDR r1, =0x87654321
6 LDR r2, =0x12345678
7 LDR r3, =0xFACEBEEF
8 LDR r4, =0xBEEFFACE
9 STMIA r0, {r1, r2, r3, r4}
11 MOV r0, #0 ; free registers
12 MOV r1, #0
13 MOV r2, #0
14 MOV r3, #0
15 MOV r4, #0
17 LDR SP, =0x40000040
18 LDMIA SP, {r0, r1, r2, r3}
19 LDR SP, =0x4000003C
20 LDMIB SP, {r1, r2, r3, r4}
21 LDR SP, =0x4000004C
22 LDMDA SP, {r2, r3, r4, r5}
23 LDR SP, =0x40000050
24 LDMDB SP, {r3, r4, r5, r6}
26 LDR SP, =0x40000058
27 STMIA SP, {r0, r1, r2, r3}
28 LDR SP, =0x40000064
29 STMIB SP, {r0, r1, r2, r3}
30 LDR SP, =0x40000084
31 STMDA SP, {r0, r1, r2, r3}
32 LDR SP, =0x40000098
33 STMDB SP, {r0, r1, r2, r3}
35 STOP B STOP
Memory 1
Address: 0x40000040
0x40000040: 21 43 65 87 78 56 34 12 EF BE CE FA CE FA EF BE 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x40000062: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x40000084: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x400000A6: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
Call Stack + Locals
Memory 1

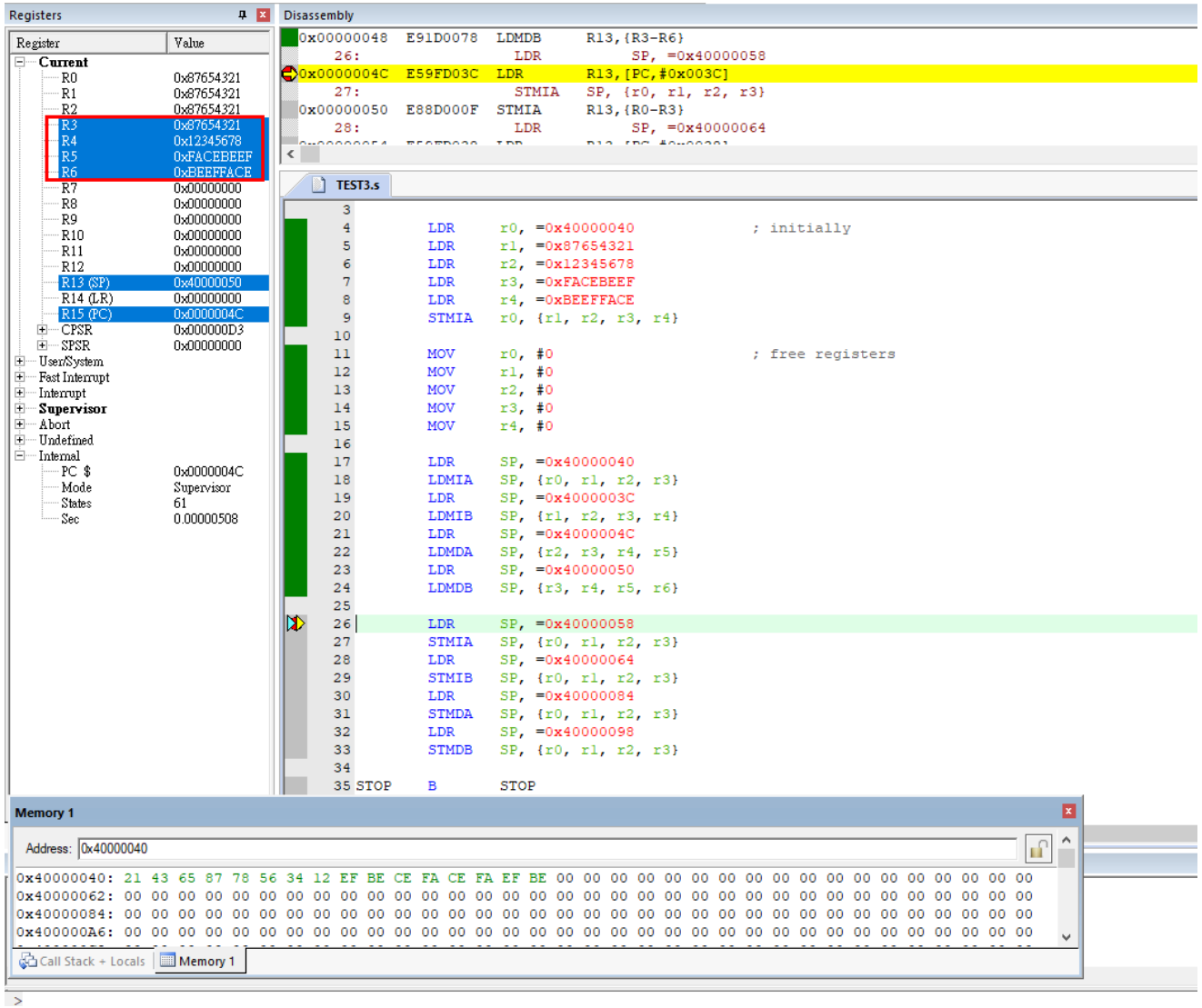
3.(2)


Registers
Register
Value
Current
R0 0x87654321
R1 0x87654321
R2 0x12345678
R3 0xFACEBEEF
R4 0xBEEFFACE
R5 0x00000000
R6 0x00000000
R7 0x00000000
R8 0x00000000
R9 0x00000000
R10 0x00000000
R11 0x00000000
R12 0x00000000
R13 (SP) 0x4000003C
R14 (LR) 0x00000000
R15 (PC) 0x0000003C
CPSR 0x000000D3
SPSR 0x00000000
User/System
Fast Interrupt
Interrupt
Supervisor
Abort
Undefined
Internal
PC $ 0x0000003C
Mode Supervisor
States 43
Sec 0.00000358
Disassembly
19: LDR SP, =0x4000003C
0x00000034 E59FD048 LDR R13,[PC,#0x0048]
20: LDMIB SP, {r1, r2, r3, r4}
0x00000038 E99D001E LDMIB R13,{R1-R4}
21: LDR SP, =0x4000004C
0x0000003C E59FD044 LDR R13,[PC,#0x0044]
TEST3.s
3
4 LDR r0, =0x40000040 ; initially
5 LDR r1, =0x87654321
6 LDR r2, =0x12345678
7 LDR r3, =0xFACEBEEF
8 LDR r4, =0xBEEFFACE
9 STMIA r0, {r1, r2, r3, r4}
10
11 MOV r0, #0 ; free registers
12 MOV r1, #0
13 MOV r2, #0
14 MOV r3, #0
15 MOV r4, #0
16
17 LDR SP, =0x40000040
18 LDMIA SP, {r0, r1, r2, r3}
19 LDR SP, =0x4000003C
20 LDMIB SP, {r1, r2, r3, r4}
21 LDR SP, =0x4000004C
22 LDMDA SP, {r2, r3, r4, r5}
23 LDR SP, =0x40000050
24 LDMDB SP, {r3, r4, r5, r6}
25
26 LDR SP, =0x40000058
27 STMIA SP, {r0, r1, r2, r3}
28 LDR SP, =0x40000064
29 STMIB SP, {r0, r1, r2, r3}
30 LDR SP, =0x40000084
31 STMDA SP, {r0, r1, r2, r3}
32 LDR SP, =0x40000098
33 STMDB SP, {r0, r1, r2, r3}
34
35 STOP B STOP
Memory 1
Address: 0x40000040
0x40000040: 21 43 65 87 78 56 34 12 EF BE CE FA CE FA EF BE 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x40000062: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x40000084: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x400000A6: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
Call Stack + Locals
Memory 1

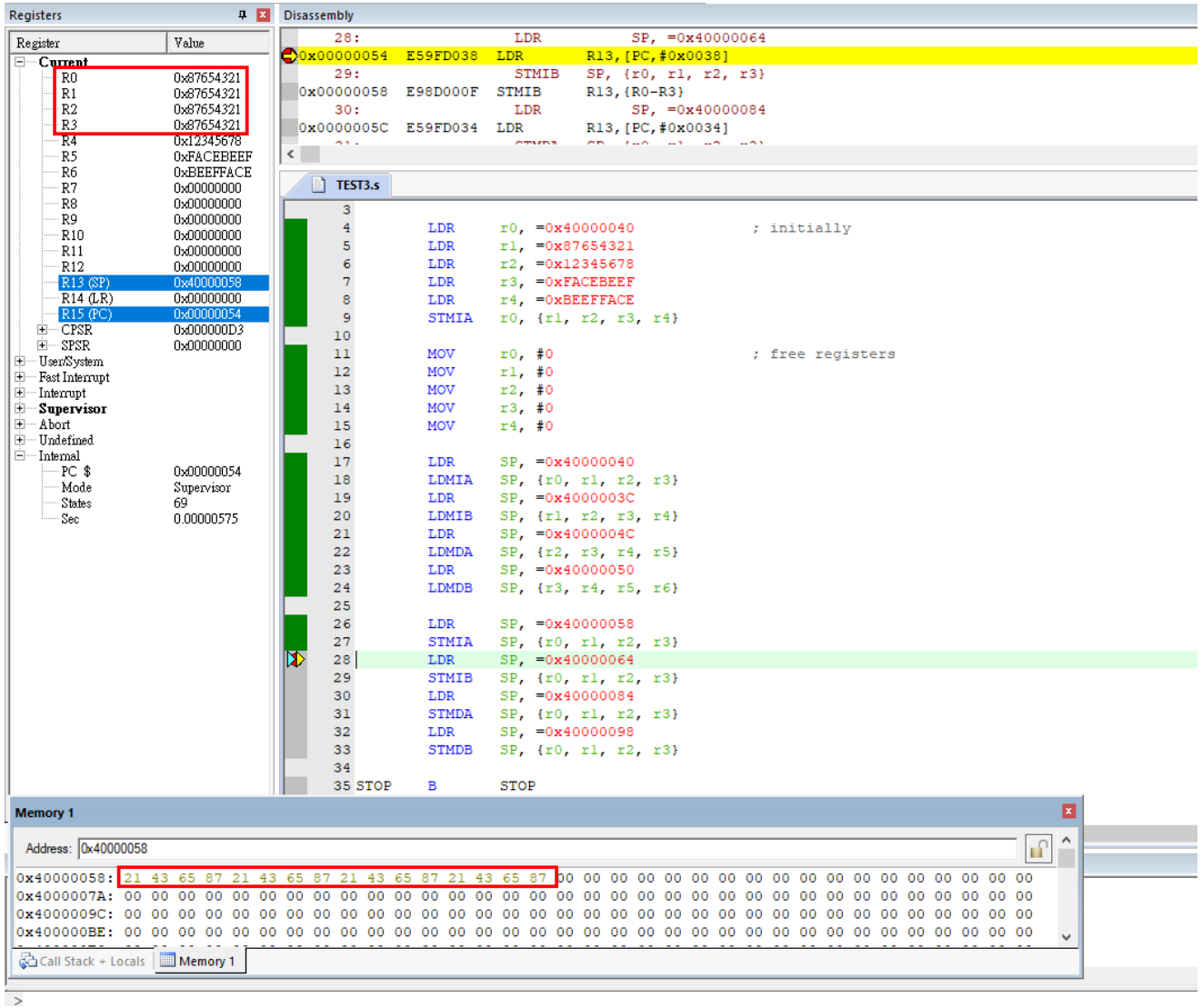
3.(3)


Registers
Register
Value
Current
R0 0x87654321
R1 0x87654321
R2 0x87654321
R3 0x12345678
R4 0xFACEBEEF
R5 0xBEEFFACE
R6 0x00000000
R7 0x00000000
R8 0x00000000
R9 0x00000000
R10 0x00000000
R11 0x00000000
R12 0x00000000
R13 (SP) 0x4000004C
R14 (LR) 0x00000000
R15 (PC) 0x00000044
CPSR 0x000000D3
SPSR 0x00000000
User/System
Fast Interrupt
Interrupt
Supervisor
Abort
Undefined
Internal
PC $ 0x00000044
Mode Supervisor
States 52
Sec 0.00000433
Disassembly
0x00000040 E81D003C LDMDA R13,{R2-R5}
23: LDR SP, =0x40000050
0x00000044 E59FD040 LDR R13,[PC,#0x0040]
24: LDMDB SP, {r3, r4, r5, r6}
25:
0x00000048 E91D0078 LDMDB R13,{R3-R6}
TEST3.s
3
4 LDR r0, =0x40000040 ; initially
5 LDR r1, =0x87654321
6 LDR r2, =0x12345678
7 LDR r3, =0xFACEBEEF
8 LDR r4, =0xBEEFFACE
9 STMIA r0, {r1, r2, r3, r4}
10
11 MOV r0, #0 ; free registers
12 MOV r1, #0
13 MOV r2, #0
14 MOV r3, #0
15 MOV r4, #0
16
17 LDR SP, =0x40000040
18 LDMIA SP, {r0, r1, r2, r3}
19 LDR SP, =0x4000003C
20 LDMIB SP, {r1, r2, r3, r4}
21 LDR SP, =0x4000004C
22 LDMDA SP, {r2, r3, r4, r5}
23 LDR SP, =0x40000050
24 LDMDB SP, {r3, r4, r5, r6}
25
26 LDR SP, =0x40000058
27 STMIA SP, {r0, r1, r2, r3}
28 LDR SP, =0x40000064
29 STMIB SP, {r0, r1, r2, r3}
30 LDR SP, =0x40000084
31 STMDA SP, {r0, r1, r2, r3}
32 LDR SP, =0x40000098
33 STMDB SP, {r0, r1, r2, r3}
34
35 STOP B STOP
Memory 1
Address: 0x40000040
0x40000040: 21 43 65 87 78 56 34 12 EF BE CE FA CE FA EF BE 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x40000062: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x40000084: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x400000A6: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
Call Stack + Locals
Memory 1

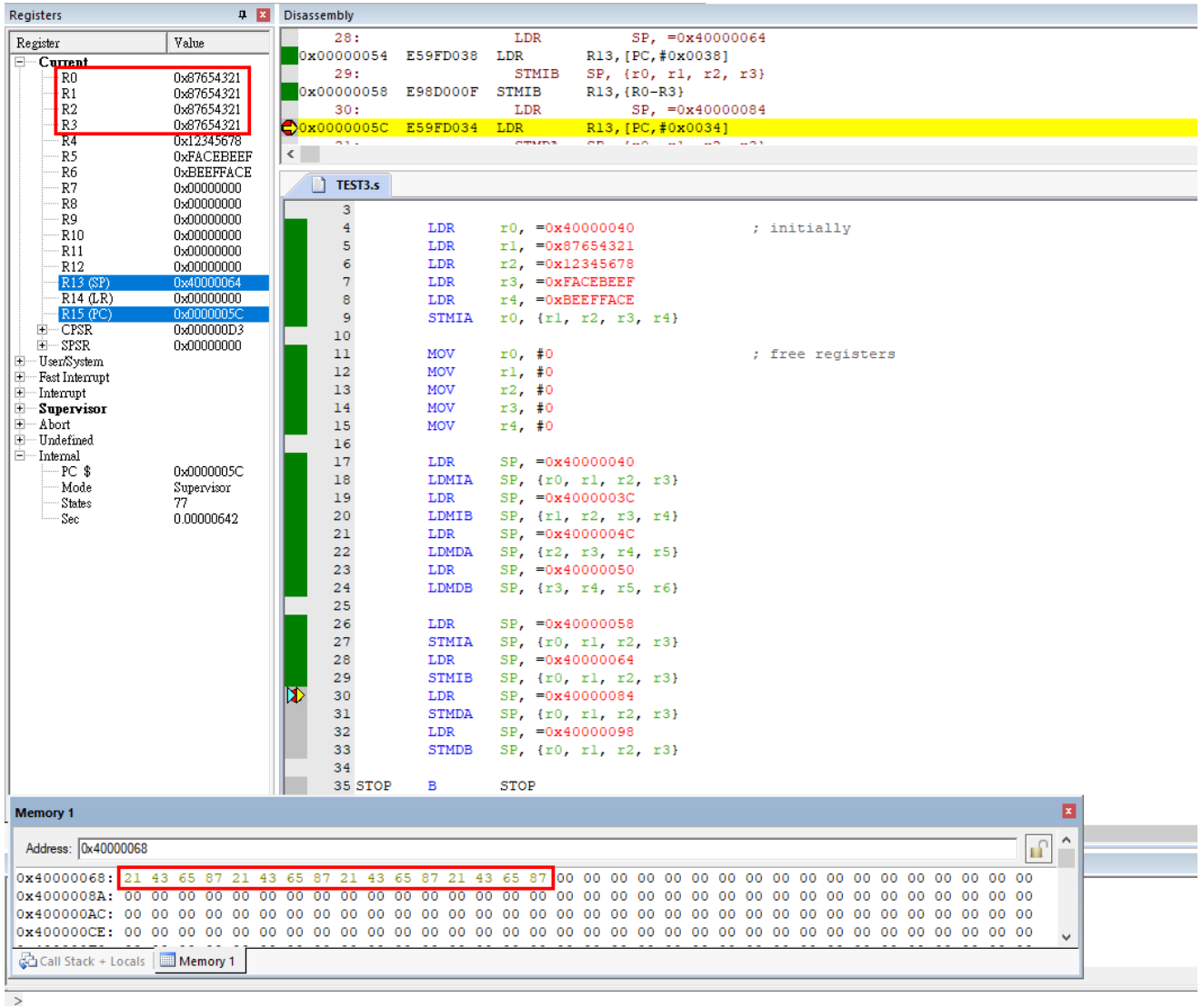
3.(4)


Registers
Register
Value
Current
R0 0x87654321
R1 0x87654321
R2 0x87654321
R3 0x87654321
R4 0x12345678
R5 0xFACEBEEF
R6 0xBEEFFACE
R7 0x00000000
R8 0x00000000
R9 0x00000000
R10 0x00000000
R11 0x00000000
R12 0x00000000
R13 (SP) 0x40000050
R14 (LR) 0x00000000
R15 (PC) 0x0000004C
CPSR 0x000000D3
SPSR 0x00000000
User/System
Fast Interrupt
Interrupt
Supervisor
Abort
Undefined
Internal
PC $ 0x0000004C
Mode Supervisor
States 61
Sec 0.00000508
Disassembly
0x00000048 E91D0078 LDMDB R13,{R3-R6}
26: LDR SP, =0x40000058
0x0000004C E59FD03C LDR R13,[PC,#0x003C]
27: STMIA SP, {r0, r1, r2, r3}
0x00000050 E88D000F STMIA R13,{R0-R3}
28: LDR SP, =0x40000064
TEST3.s
3
4 LDR r0, =0x40000040 ; initially
5 LDR r1, =0x87654321
6 LDR r2, =0x12345678
7 LDR r3, =0xFACEBEEF
8 LDR r4, =0xBEEFFACE
9 STMIA r0, {r1, r2, r3, r4}
10
11 MOV r0, #0 ; free registers
12 MOV r1, #0
13 MOV r2, #0
14 MOV r3, #0
15 MOV r4, #0
16
17 LDR SP, =0x40000040
18 LDMIA SP, {r0, r1, r2, r3}
19 LDR SP, =0x4000003C
20 LDMIB SP, {r1, r2, r3, r4}
21 LDR SP, =0x4000004C
22 LDMDA SP, {r2, r3, r4, r5}
23 LDR SP, =0x40000050
24 LDMDB SP, {r3, r4, r5, r6}
25
26 LDR SP, =0x40000058
27 STMIA SP, {r0, r1, r2, r3}
28 LDR SP, =0x40000064
29 STMIB SP, {r0, r1, r2, r3}
30 LDR SP, =0x40000084
31 STMDA SP, {r0, r1, r2, r3}
32 LDR SP, =0x40000098
33 STMDB SP, {r0, r1, r2, r3}
34
35 STOP B STOP
Memory 1
Address: 0x40000040
0x40000040: 21 43 65 87 78 56 34 12 EF BE CE FA CE FA EF BE 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x40000062: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x40000084: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x400000A6: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
Call Stack + Locals
Memory 1

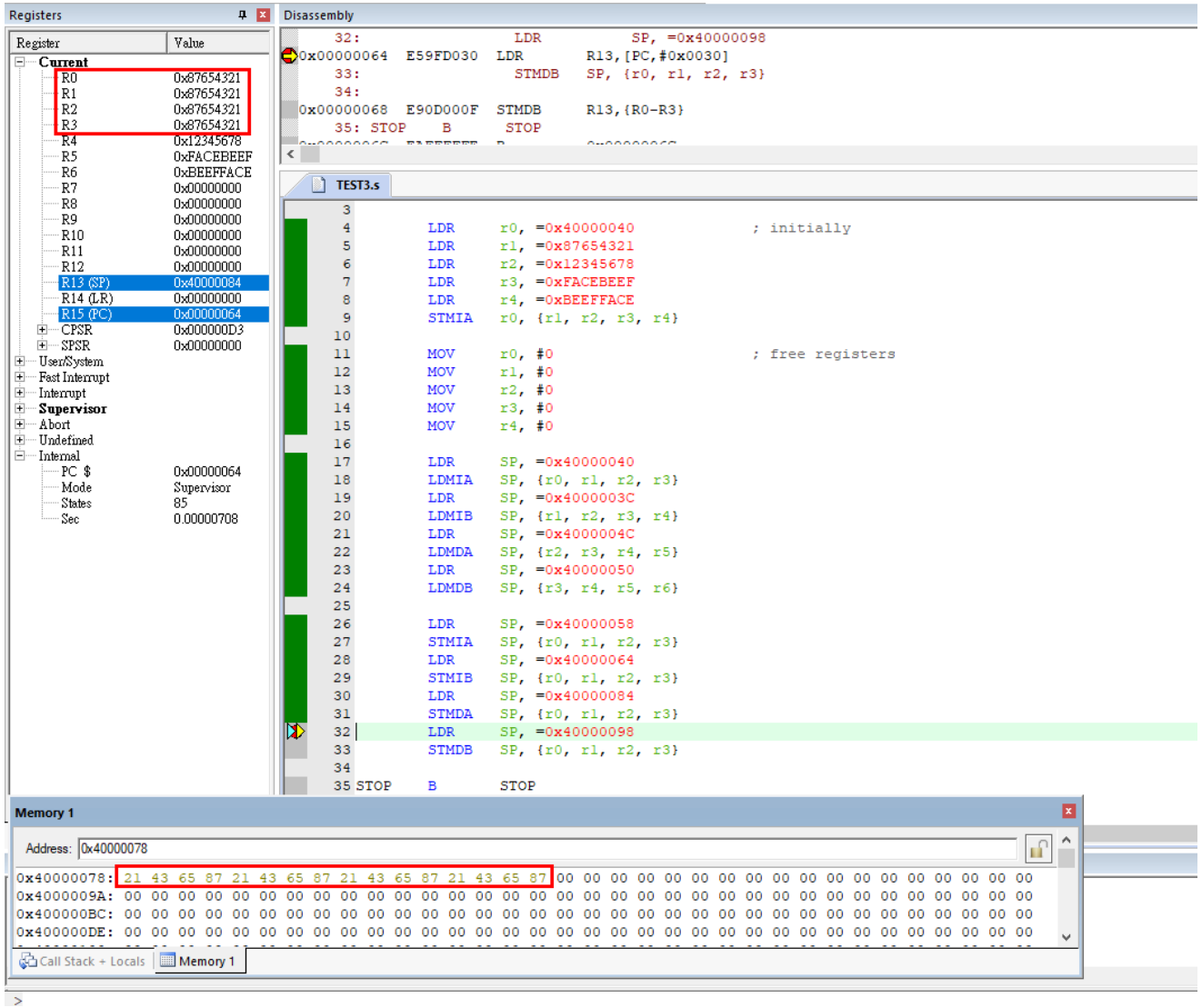
3.(5)


Registers
Register
Value
Current
R0 0x87654321
R1 0x87654321
R2 0x87654321
R3 0x87654321
R4 0x12345678
R5 0xFACEBEEF
R6 0xBEEFFACE
R7 0x00000000
R8 0x00000000
R9 0x00000000
R10 0x00000000
R11 0x00000000
R12 0x00000000
R13 (SP) 0x40000058
R14 (LR) 0x00000000
R15 (PC) 0x00000054
CPSR 0x000000D3
SPSR 0x00000000
User/System
Fast Interrupt
Interrupt
Supervisor
Abort
Undefined
Internal
PC $ 0x00000054
Mode Supervisor
States 69
Sec 0.00000575
Disassembly
28: LDR SP, =0x40000064
0x00000054 E59FD038 LDR R13,[PC,#0x0038]
29: STMIB SP, {r0, r1, r2, r3}
0x00000058 E98D000F STMIB R13,{R0-R3}
30: LDR SP, =0x40000084
0x0000005C E59FD034 LDR R13,[PC,#0x0034]
TEST3.s
3
4 LDR r0, =0x40000040 ; initially
5 LDR r1, =0x87654321
6 LDR r2, =0x12345678
7 LDR r3, =0xFACEBEEF
8 LDR r4, =0xBEEFFACE
9 STMIA r0, {r1, r2, r3, r4}
10
11 MOV r0, #0 ; free registers
12 MOV r1, #0
13 MOV r2, #0
14 MOV r3, #0
15 MOV r4, #0
16
17 LDR SP, =0x40000040
18 LDMIA SP, {r0, r1, r2, r3}
19 LDR SP, =0x4000003C
20 LDMIB SP, {r1, r2, r3, r4}
21 LDR SP, =0x4000004C
22 LDMDA SP, {r2, r3, r4, r5}
23 LDR SP, =0x40000050
24 LDMDB SP, {r3, r4, r5, r6}
25
26 LDR SP, =0x40000058
27 STMIA SP, {r0, r1, r2, r3}
28 LDR SP, =0x40000064
29 STMIB SP, {r0, r1, r2, r3}
30 LDR SP, =0x40000084
31 STMDA SP, {r0, r1, r2, r3}
32 LDR SP, =0x40000098
33 STMDB SP, {r0, r1, r2, r3}
34
35 STOP B STOP
Memory 1
Address: 0x40000058
0x40000058: 21 43 65 87 21 43 65 87 21 43 65 87 21 43 65 87 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x4000007A: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x4000009C: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x400000BE: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
Call Stack + Locals
Memory 1

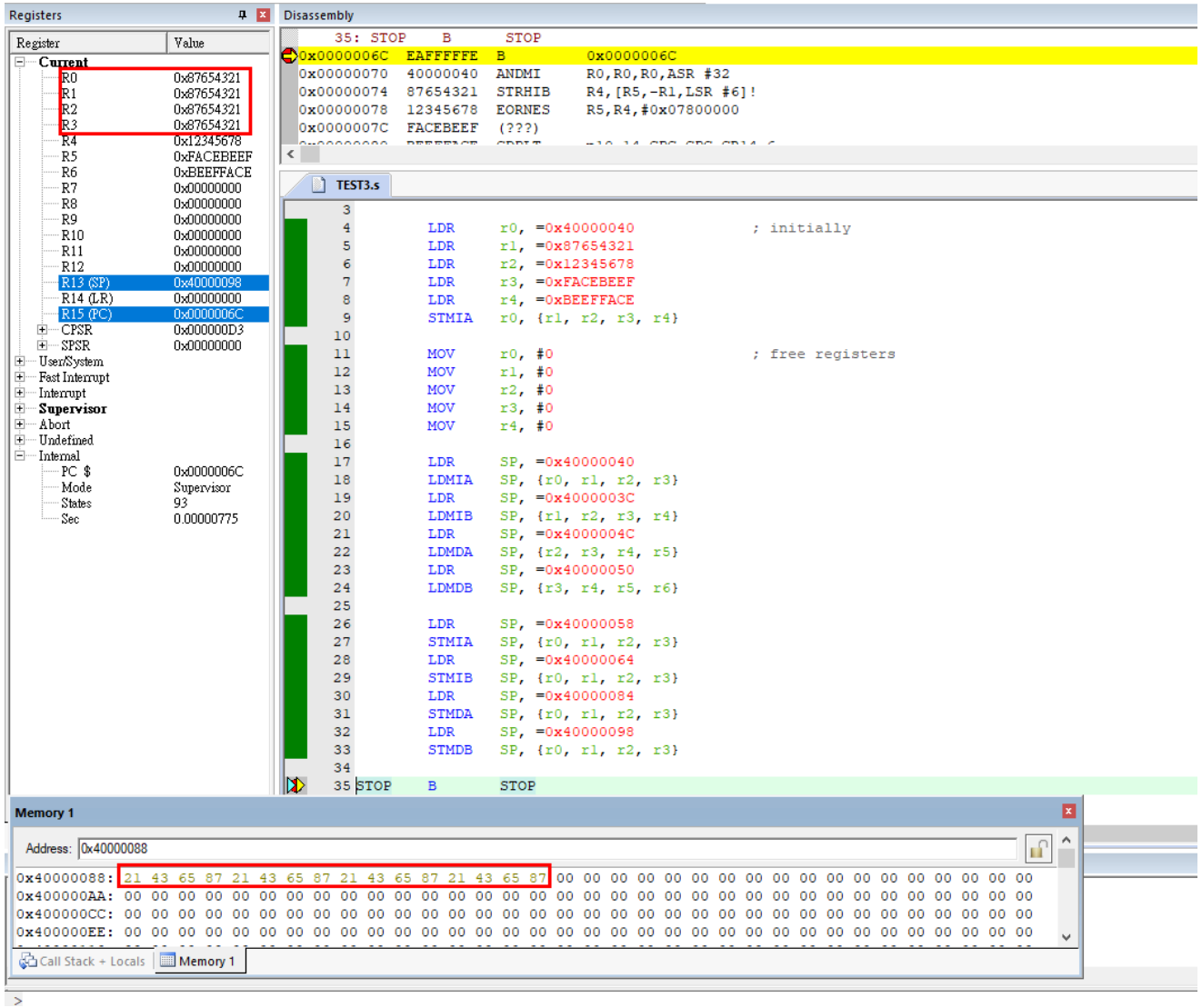
3.(6)


Registers
Register
Value
Current
R0 0x87654321
R1 0x87654321
R2 0x87654321
R3 0x87654321
R4 0x12345678
R5 0xFACEBEEF
R6 0xBEEFFACE
R7 0x00000000
R8 0x00000000
R9 0x00000000
R10 0x00000000
R11 0x00000000
R12 0x00000000
R13 (SP) 0x40000064
R14 (LR) 0x00000000
R15 (PC) 0x0000005C
CPSR 0x000000D3
SPSR 0x00000000
User/System
Fast Interrupt
Interrupt
Supervisor
Abort
Undefined
Internal
PC $ 0x0000005C
Mode Supervisor
States 77
Sec 0.00000642
Disassembly
28: LDR SP, =0x40000064
0x00000054 E59FD038 LDR R13,[PC,#0x0038]
29: STMIB SP, {r0, r1, r2, r3}
0x00000058 E98D000F STMIB R13,{R0-R3}
30: LDR SP, =0x40000084
0x0000005C E59FD034 LDR R13,[PC,#0x0034]
TEST3.s
3
4 LDR r0, =0x40000040 ; initially
5 LDR r1, =0x87654321
6 LDR r2, =0x12345678
7 LDR r3, =0xFACEBEEF
8 LDR r4, =0xBEEFFACE
9 STMIA r0, {r1, r2, r3, r4}
10
11 MOV r0, #0 ; free registers
12 MOV r1, #0
13 MOV r2, #0
14 MOV r3, #0
15 MOV r4, #0
16
17 LDR SP, =0x40000040
18 LDMIA SP, {r0, r1, r2, r3}
19 LDR SP, =0x4000003C
20 LDMIB SP, {r1, r2, r3, r4}
21 LDR SP, =0x4000004C
22 LDMDA SP, {r2, r3, r4, r5}
23 LDR SP, =0x40000050
24 LDMDB SP, {r3, r4, r5, r6}
25
26 LDR SP, =0x40000058
27 STMIA SP, {r0, r1, r2, r3}
28 LDR SP, =0x40000064
29 STMIB SP, {r0, r1, r2, r3}
30 LDR SP, =0x40000084
31 STMDA SP, {r0, r1, r2, r3}
32 LDR SP, =0x40000098
33 STMDB SP, {r0, r1, r2, r3}
34
35 STOP B STOP
Memory 1
Address: 0x40000068
0x40000068: 21 43 65 87 21 43 65 87 21 43 65 87 21 43 65 87 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x4000008A: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x400000AC: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x400000CE: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
Call Stack + Locals
Memory 1

3.(7)


Registers
Register
Value
Current
R0 0x87654321
R1 0x87654321
R2 0x87654321
R3 0x87654321
R4 0x12345678
R5 0xFACEBEEF
R6 0xBEEFFACE
R7 0x00000000
R8 0x00000000
R9 0x00000000
R10 0x00000000
R11 0x00000000
R12 0x00000000
R13 (SP) 0x40000084
R14 (LR) 0x00000000
R15 (PC) 0x00000064
CPSR 0x000000D3
SPSR 0x00000000
User/System
Fast Interrupt
Interrupt
Supervisor
Abort
Undefined
Internal
PC $ 0x00000064
Mode Supervisor
States 85
Sec 0.00000708
Disassembly
32: LDR SP, =0x40000098
0x00000064 E59FD030 LDR R13,[PC,#0x0030]
33: STMDB SP, {r0, r1, r2, r3}
34:
0x00000068 E90D000F STMDB R13,{R0-R3}
35: STOP B STOP
TEST3.s
4 LDR r0, =0x40000040 ; initially
5 LDR r1, =0x87654321
6 LDR r2, =0x12345678
7 LDR r3, =0xFACEBEEF
8 LDR r4, =0xBEEFFACE
9 STMIA r0, {r1, r2, r3, r4}
11 MOV r0, #0 ; free registers
12 MOV r1, #0
13 MOV r2, #0
14 MOV r3, #0
15 MOV r4, #0
17 LDR SP, =0x40000040
18 LDMIA SP, {r0, r1, r2, r3}
19 LDR SP, =0x4000003C
20 LDMIB SP, {r1, r2, r3, r4}
21 LDR SP, =0x4000004C
22 LDMDA SP, {r2, r3, r4, r5}
23 LDR SP, =0x40000050
24 LDMDB SP, {r3, r4, r5, r6}
26 LDR SP, =0x40000058
27 STMIA SP, {r0, r1, r2, r3}
28 LDR SP, =0x40000064
29 STMIB SP, {r0, r1, r2, r3}
30 LDR SP, =0x40000084
31 STMDA SP, {r0, r1, r2, r3}
32 LDR SP, =0x40000098
33 STMDB SP, {r0, r1, r2, r3}
35 STOP B STOP
Memory 1
Address: 0x40000078
0x40000078: 21 43 65 87 21 43 65 87 21 43 65 87 21 43 65 87 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x4000009A: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x400000BC: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x400000DE: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
Call Stack + Locals
Memory 1

3.(8)


Registers
Register
Value
Current
R0 0x87654321
R1 0x87654321
R2 0x87654321
R3 0x87654321
R4 0x12345678
R5 0xFACEBEEF
R6 0xBEEFFACE
R7 0x00000000
R8 0x00000000
R9 0x00000000
R10 0x00000000
R11 0x00000000
R12 0x00000000
R13 (SP) 0x40000098
R14 (LR) 0x00000000
R15 (PC) 0x0000006C
CPSR 0x000000D3
SPSR 0x00000000
User/System
Fast Interrupt
Interrupt
Supervisor
Abort
Undefined
Internal
PC $ 0x0000006C
Mode Supervisor
States 93
Sec 0.00000775
Disassembly
35: STOP B STOP
0x0000006C EAFFFFFE B 0x0000006C
0x00000070 40000040 ANDMI R0,R0,R0,ASR #32
0x00000074 87654321 STRHIB R4,[R5,-R1,LSR #6]!
0x00000078 12345678 EORNES R5,R4,#0x07800000
0x0000007C FACEBEEF (???)
TEST3.s
3
4 LDR r0, =0x40000040 ; initially
5 LDR r1, =0x87654321
6 LDR r2, =0x12345678
7 LDR r3, =0xFACEBEEF
8 LDR r4, =0xBEEFFACE
9 STMIA r0, {r1, r2, r3, r4}
10
11 MOV r0, #0 ; free registers
12 MOV r1, #0
13 MOV r2, #0
14 MOV r3, #0
15 MOV r4, #0
16
17 LDR SP, =0x40000040
18 LDMIA SP, {r0, r1, r2, r3}
19 LDR SP, =0x4000003C
20 LDMIB SP, {r1, r2, r3, r4}
21 LDR SP, =0x4000004C
22 LDMDA SP, {r2, r3, r4, r5}
23 LDR SP, =0x40000050
24 LDMDB SP, {r3, r4, r5, r6}
25
26 LDR SP, =0x40000058
27 STMIA SP, {r0, r1, r2, r3}
28 LDR SP, =0x40000064
29 STMIB SP, {r0, r1, r2, r3}
30 LDR SP, =0x40000084
31 STMDA SP, {r0, r1, r2, r3}
32 LDR SP, =0x40000098
33 STMDB SP, {r0, r1, r2, r3}
34
35 STOP B STOP
Memory 1
Address: 0x40000088
0x40000088: 21 43 65 87 21 43 65 87 21 43 65 87 21 43 65 87 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x400000AA: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x400000CC: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x400000EE: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
Call Stack + Locals
Memory 1

Q&A

Thanks for your attention !!