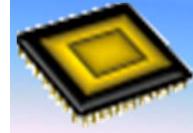


VLSI Chapter 3

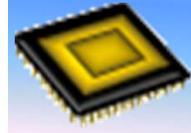
Chapter 3 CMOS Processing Technology



VLSI Chapter 3

Outline

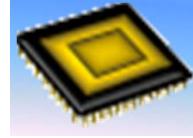
- Fabrication Overview
- Basic CMOS Technology
- Alignment Marks, Critical Dimension Marks
- Layout Design Rules
- Implementing Integrated System Designs



CMOS IC Fabrication

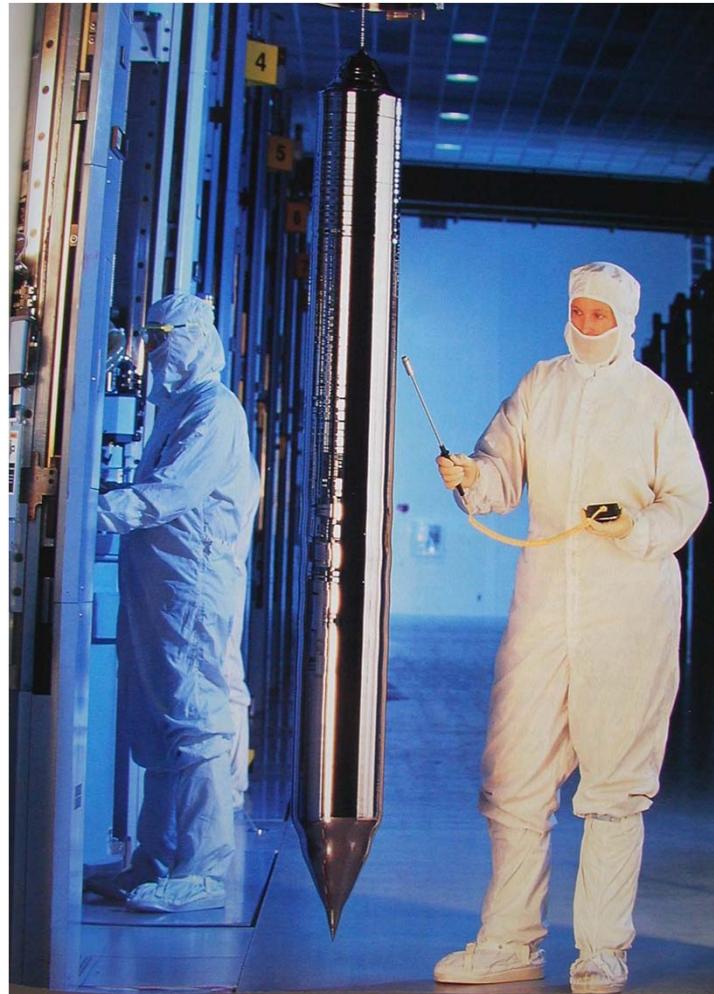
➤ Advantages of silicon (Si)

- despite that germanium (Ge) and gallium arsenic (GaAs), silicon (Si) is currently the most popular IC material
- Silicon has a number of advantages over other materials for IC fabrication
 - an **abundant material**: silicon, which occurs naturally in the form of sand, make up 28% of the Earth's crust
 - silicon has the physical properties needed for creating transistors with **good characteristics**
 - silicon wafer, on which CMOS integrated circuits are built, can be produced using **relatively simple and inexpensive techniques**
 - **silicon dioxide (SiO_2)** can be easily formed on the surface of a silicon wafer as a diffusion barrier to selectively alter the electrical properties in the wafer

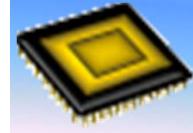


VLSI Chapter 3

Growing the Silicon Ingot



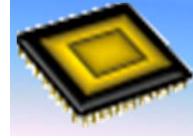
Source: Smithsonian, 2000



VLSI Chapter 3

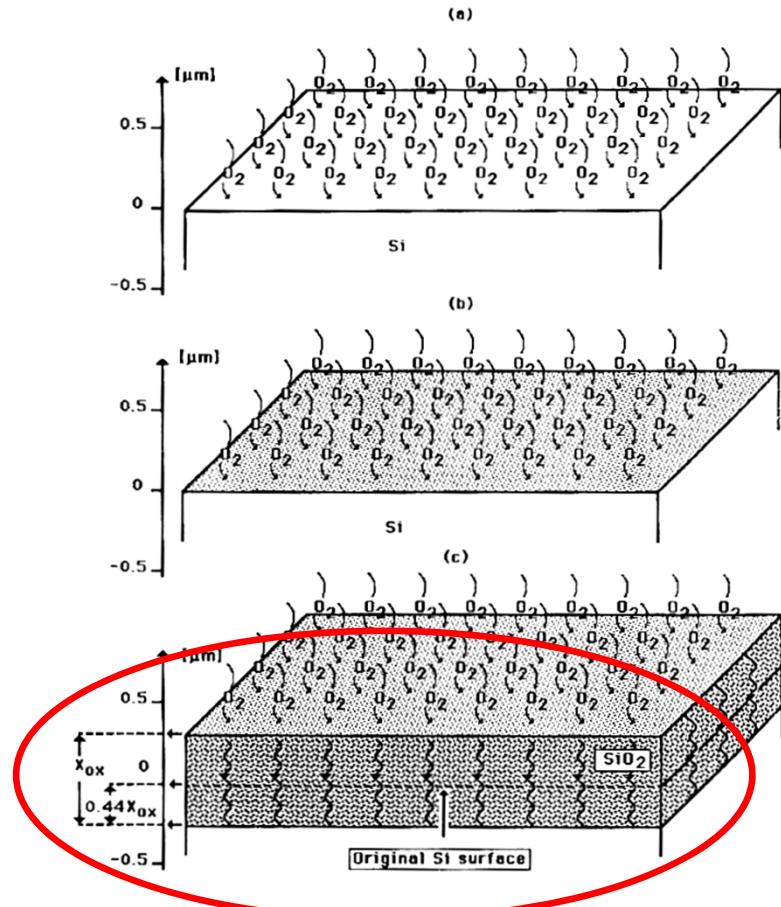
Fabrication Overview

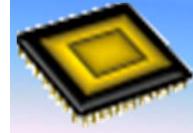
1. Oxidation
2. Photolithography
3. Etching
4. Diffusion
5. Deposition
6. Ion Implantation
7. Epitaxy



Oxidation

- Formation of SiO_2
- Wet Oxidation
- Dry Oxidation
- SiO_2 growth consumes silicon, grows into the substrate.
- SiO_2 is twice the volume of Si, projects above the substrate as well.

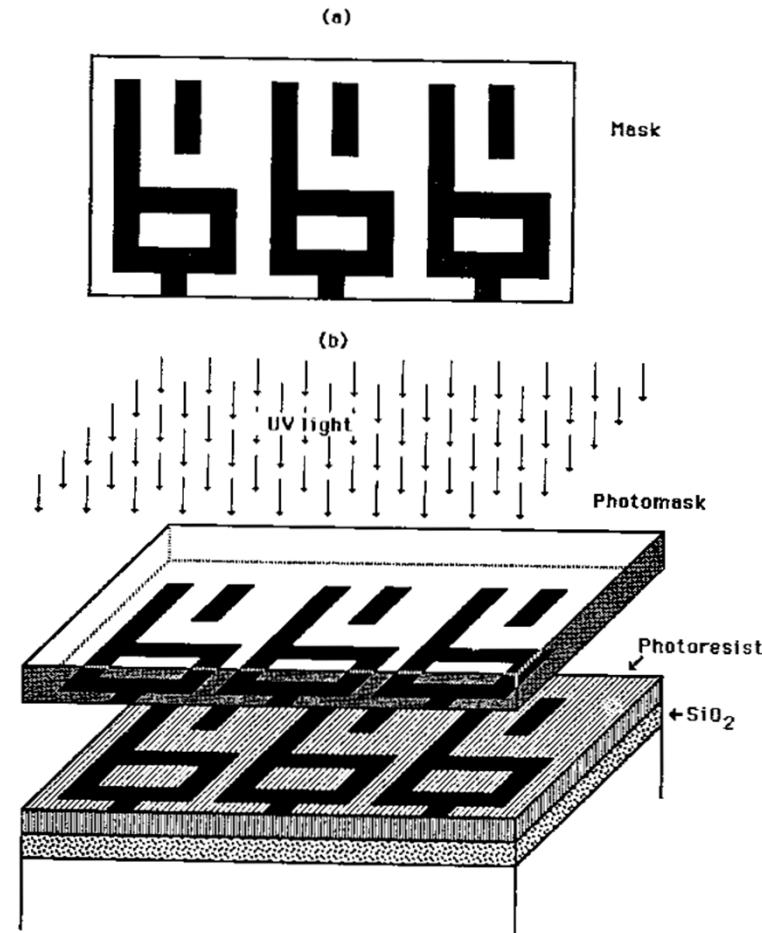


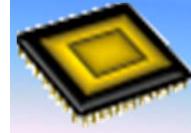


VLSI Chapter 3

Photolithography

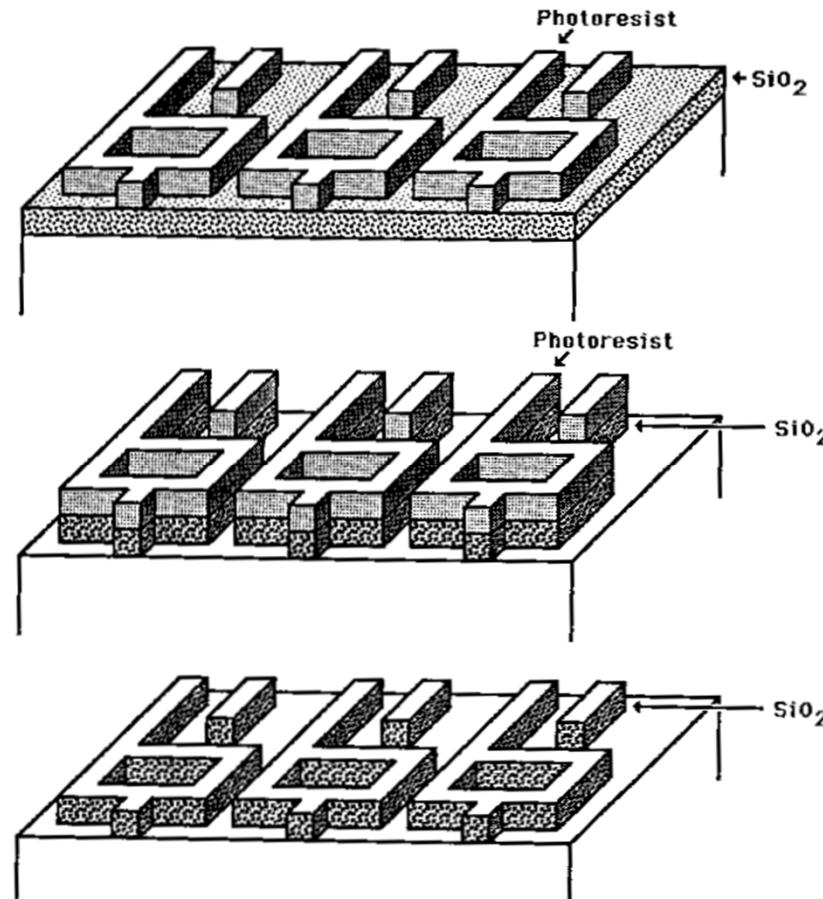
- To transfer a desired pattern onto the surface of a silicon wafer
- Positive Photoresist
- Negative Photoresist
- The number of masks applied to make the IC is often considered to be a measure of how complex the circuit is.



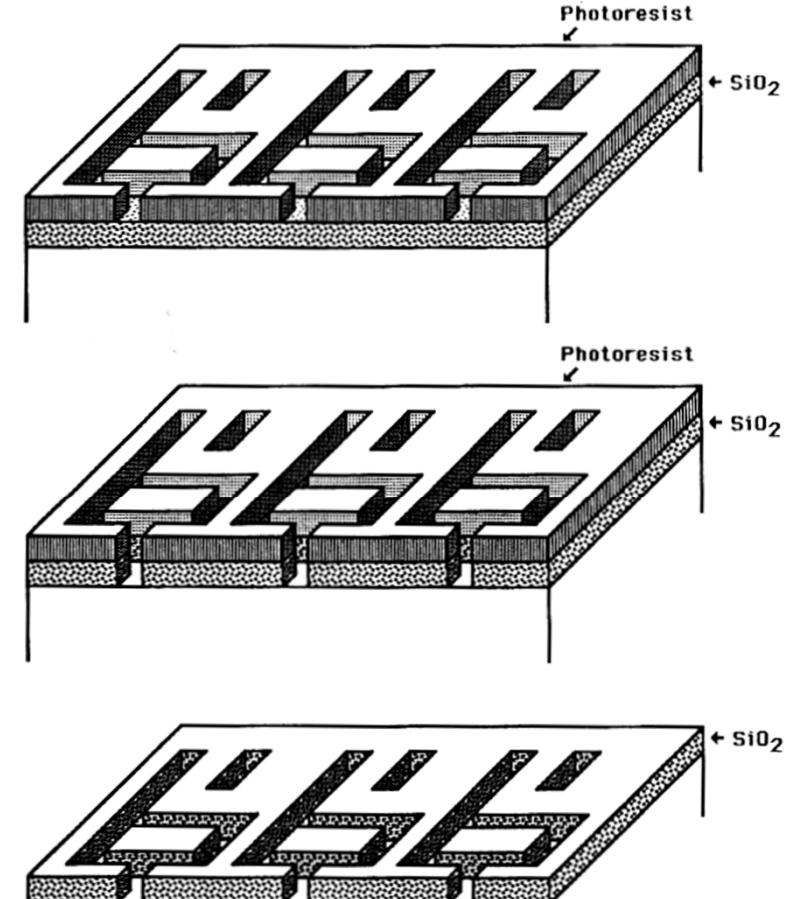


VLSI Chapter 3

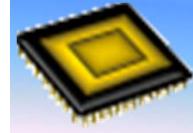
Photolithography(contd.)



Positive Photoresist



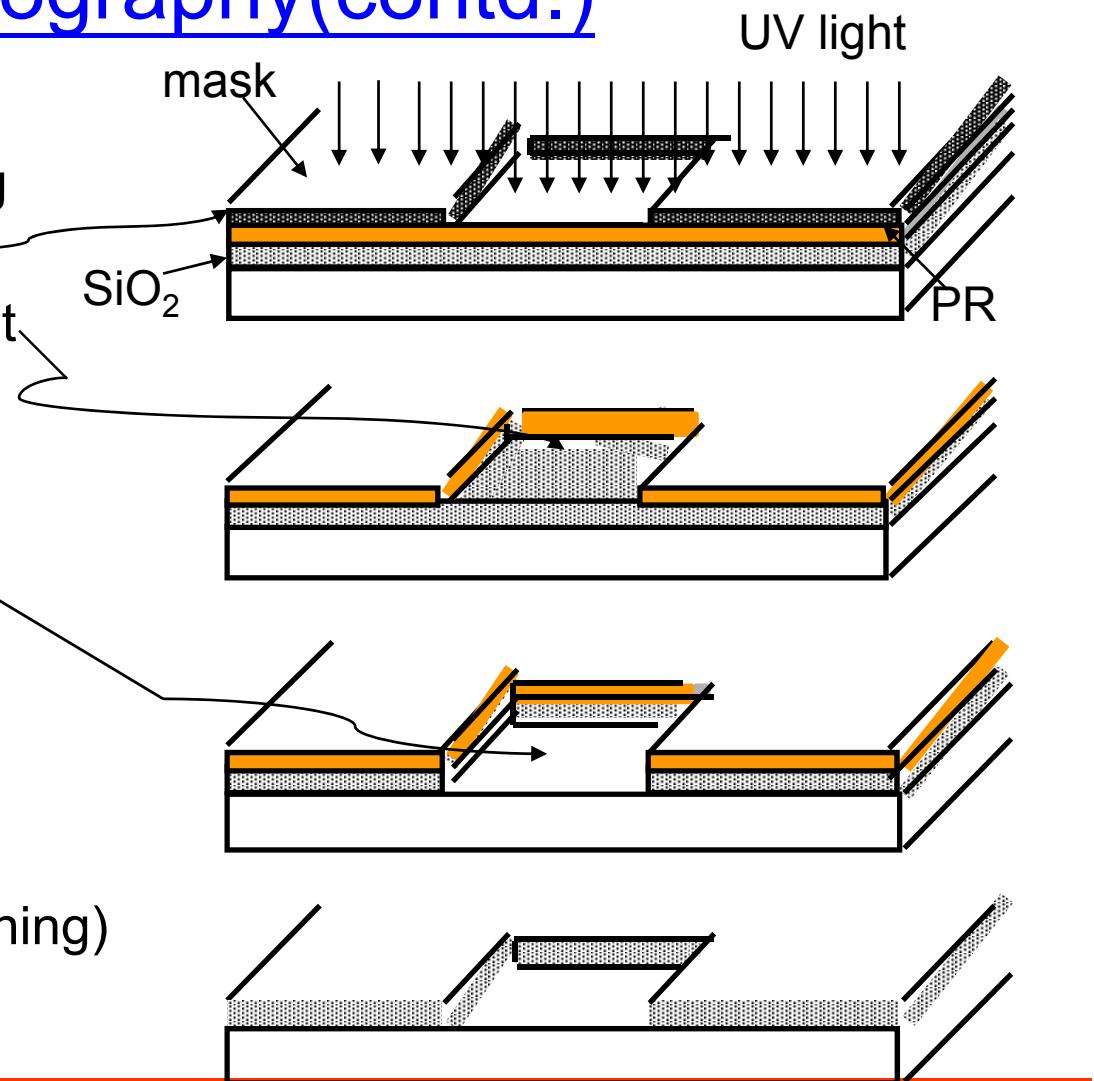
Negative Photoresist

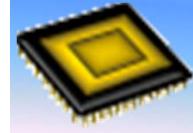


VLSI Chapter 3

Photolithography(contd.)

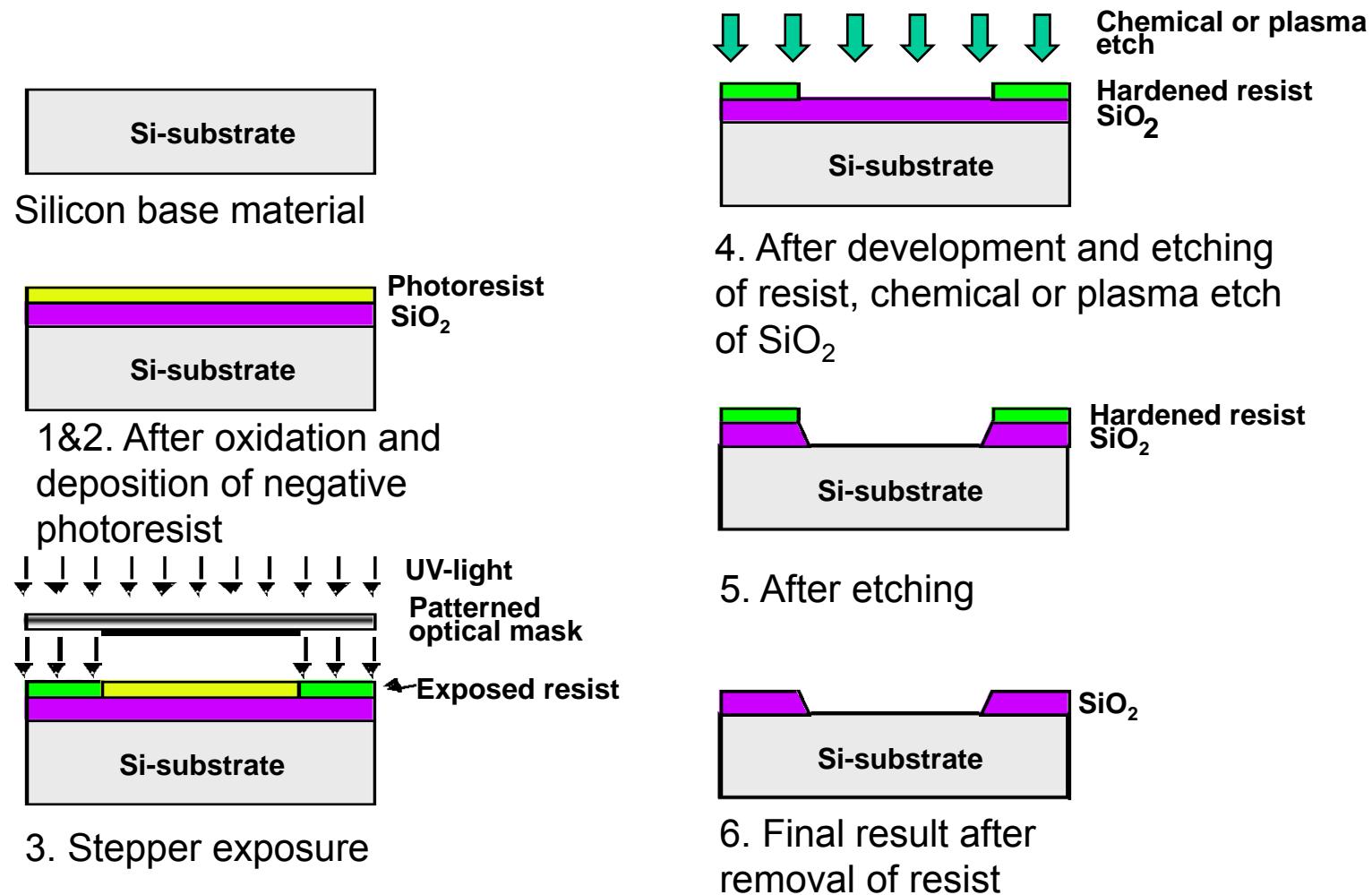
1. Oxidation
2. Photoresist (PR) coating
3. Stepper exposure
4. Photoresist development and bake
5. Acid etching
 - Unexposed (negative PR)
 - Exposed (positive PR)
6. Spin, rinse, and dry
7. Processing step
 - Ion implantation
 - Plasma etching
 - Metal deposition
8. Photoresist removal (ashing)

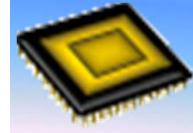




VLSI Chapter 3

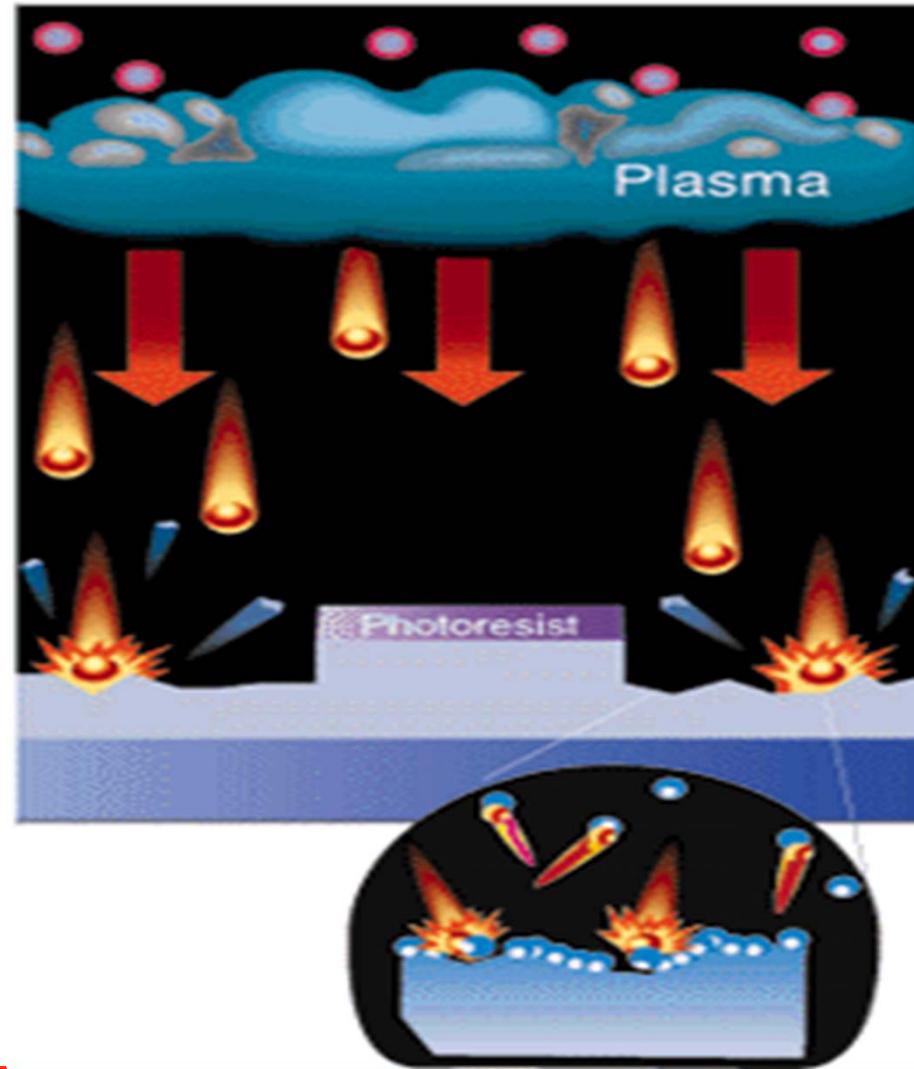
Example of Patterning of SiO_2

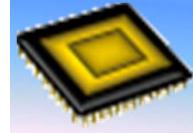




VLSI Chapter 3

Etching

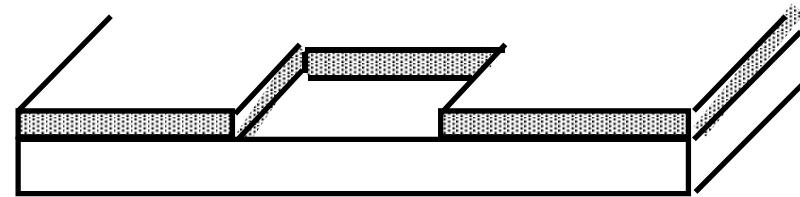




VLSI Chapter 3

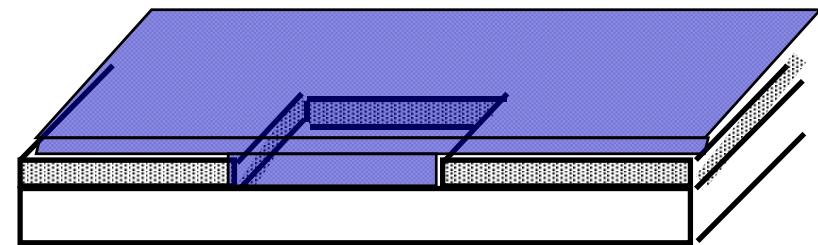
Deposition and Etching

1. Pattern masking
(photolithography)



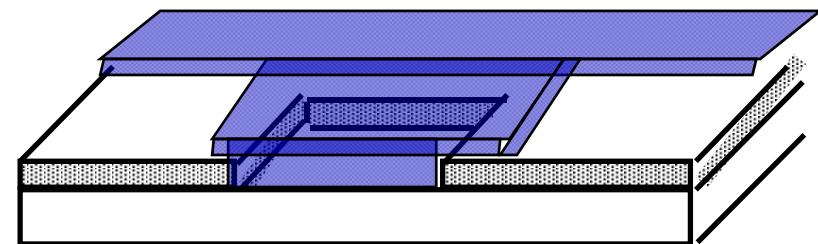
2. Deposit material over entire wafer

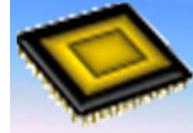
CVD (Si_3N_4)
chemical deposition
(polysilicon)
sputtering (Al)



3. Etch away unwanted material

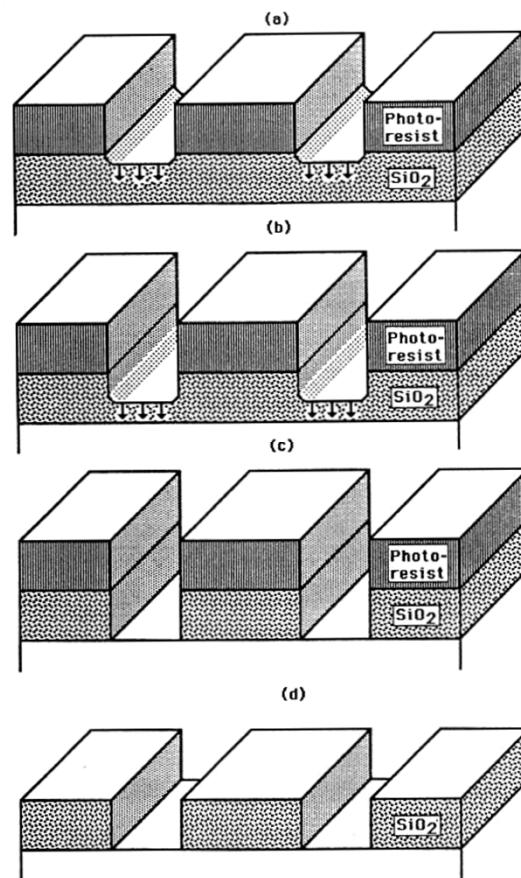
wet etching
dry (plasma) etching



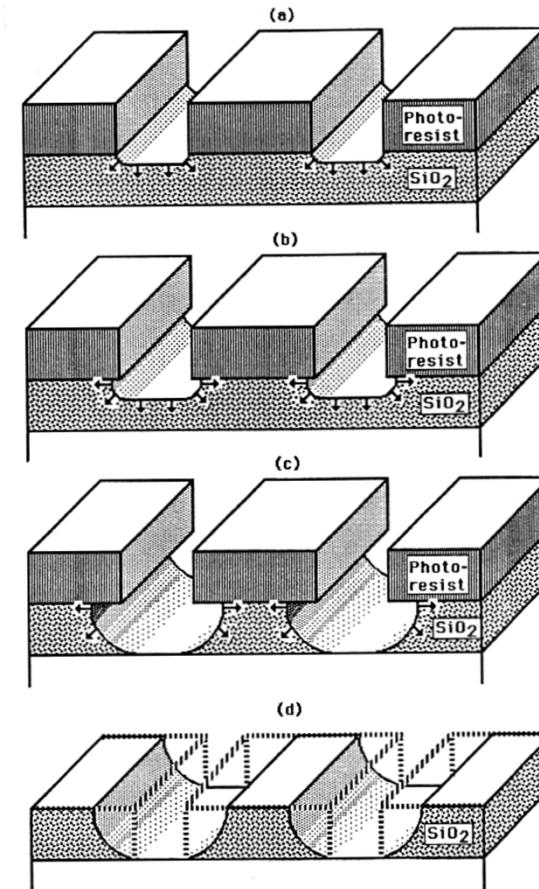


VLSI Chapter 3

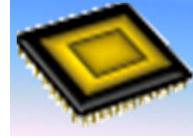
Etching



(1) Dry etching



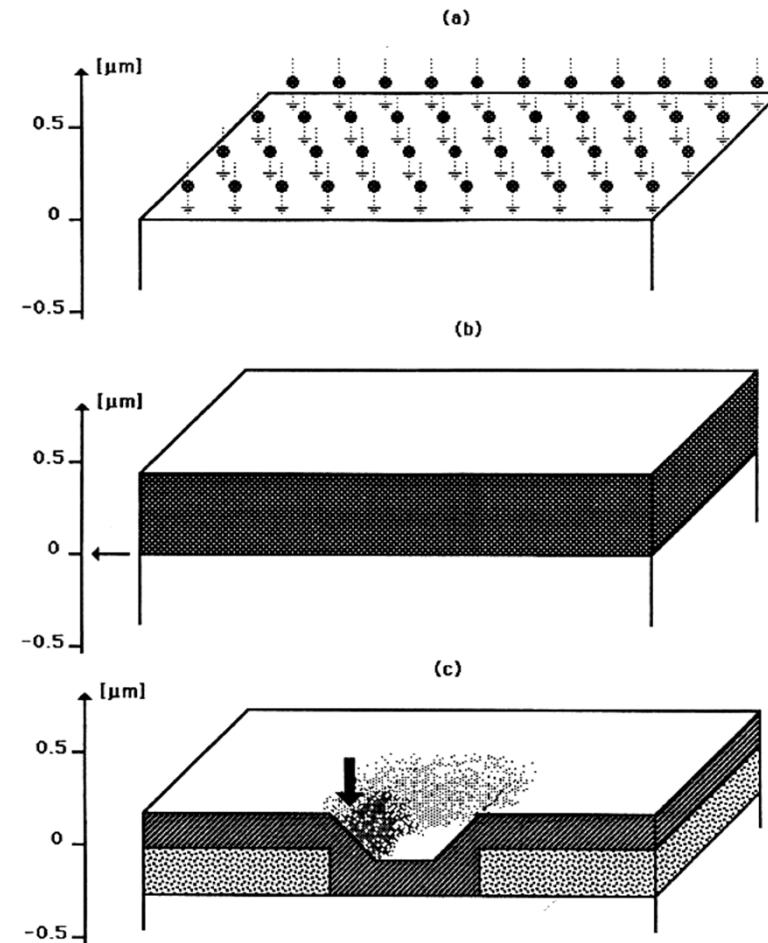
(2) Wet etching

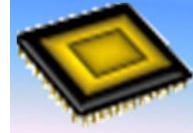


VLSI Chapter 3

Deposition

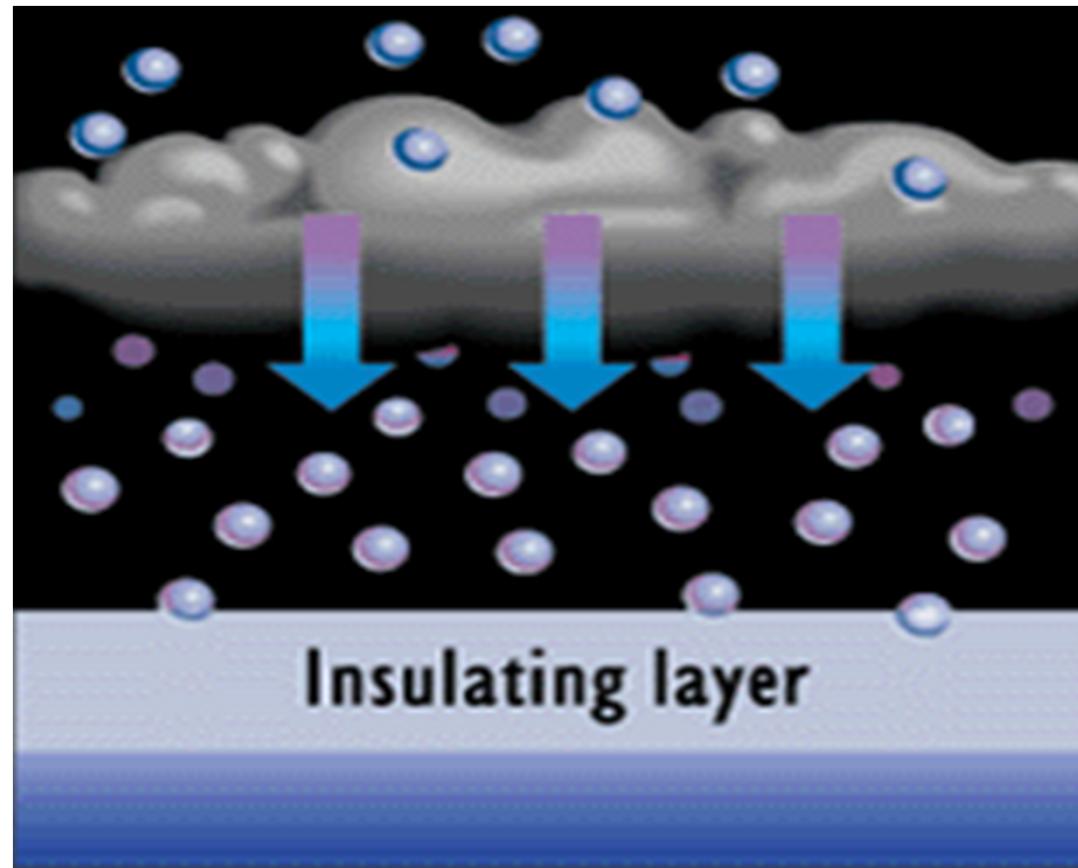
- Thin layers of both conducting materials (metals, metal silicides...) and insulating materials(SiO_2)

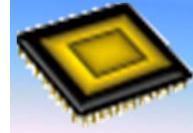




VLSI Chapter 3

Chemical Vapor Deposition (CVD)

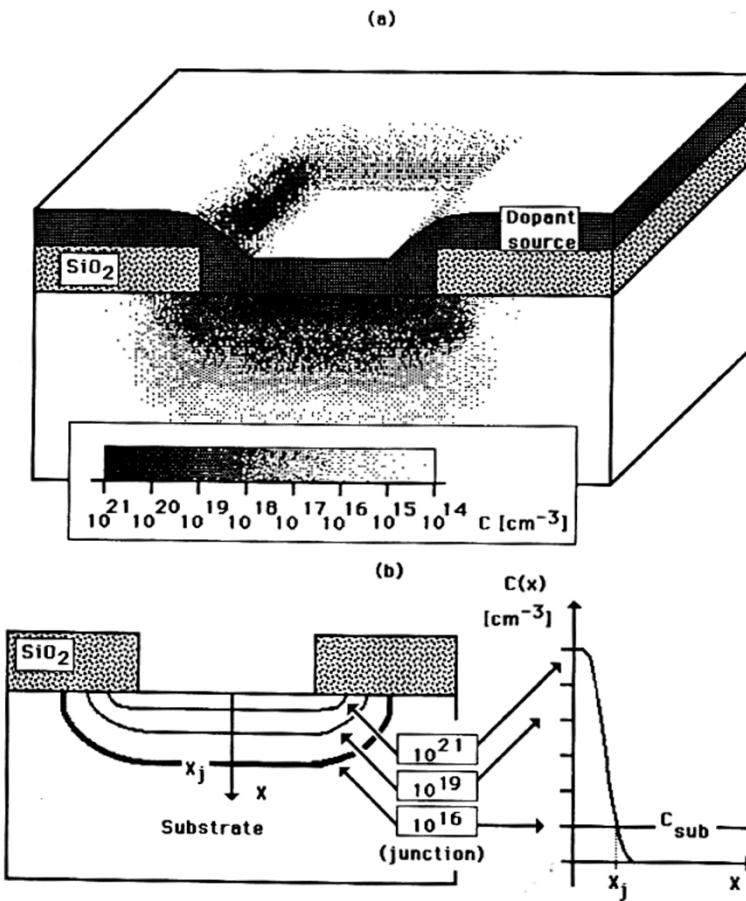


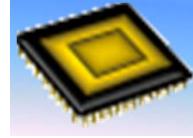


VLSI Chapter 3

Diffusion

- A process allows atoms to move within a solid at elevated temperature

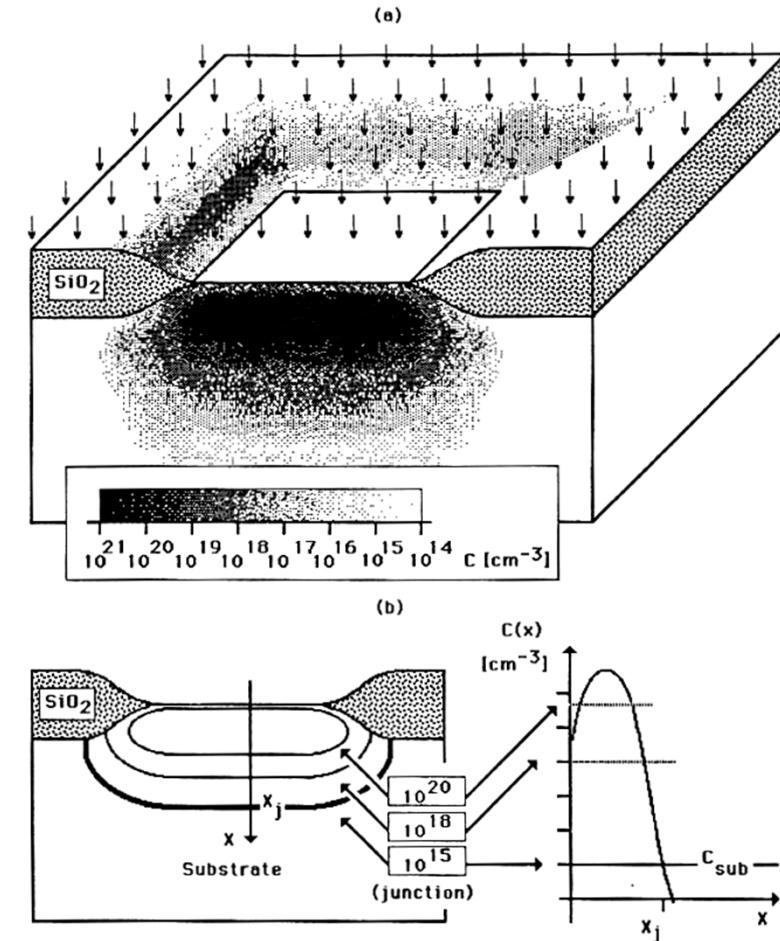


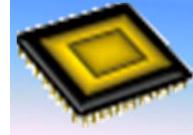


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Ion Implantation

- Decreased lateral spreading of the doped region
- For high-density microcircuit fabrication



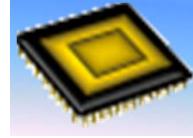


VLSI Chapter 3

Polishing the Wafers



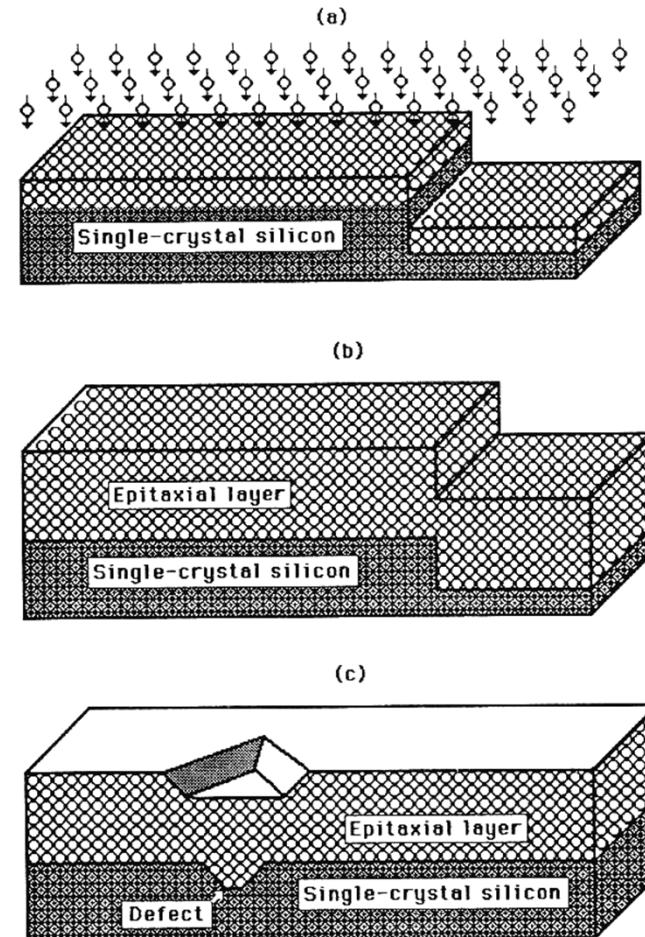
Source: Smithsonian, 2000

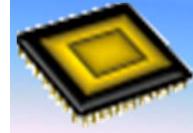


VLSI Chapter 3

Epitaxy

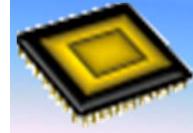
- Deposition of a single crystal Si on a single-crystal substrate





Basic CMOS Technology

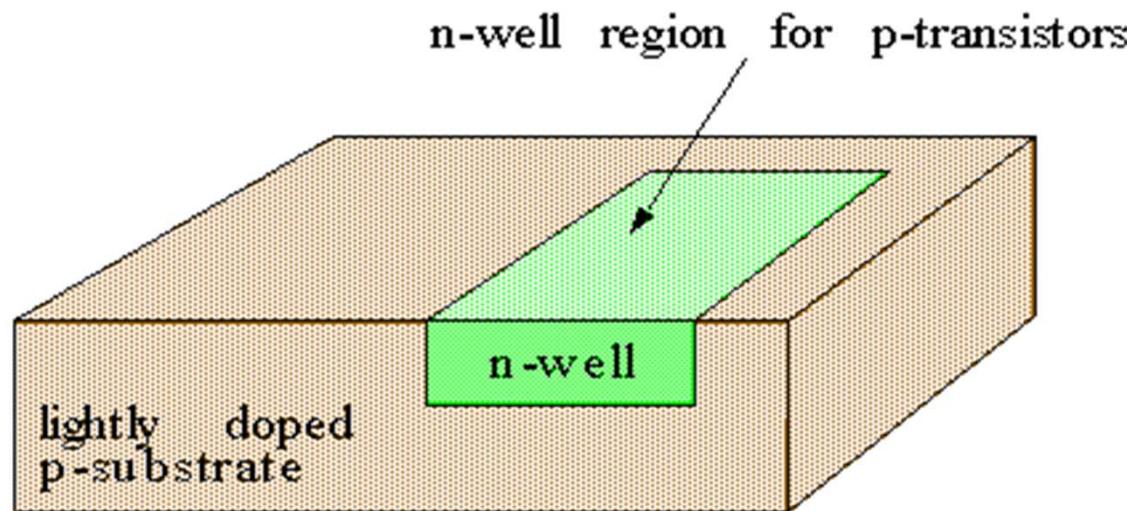
- CMOS technology is recognized as the leading VLSI system technology.
- The four main CMOS technologies are
 - n-well process
 - p-well process
 - twin-tub proceed
 - silicon on insulator (SOI)

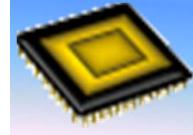


VLSI Chapter 3

N-well Process(1/8)

- n-well mask used to create n-well or n-tub via ion-implantation or deposition/diffusion.

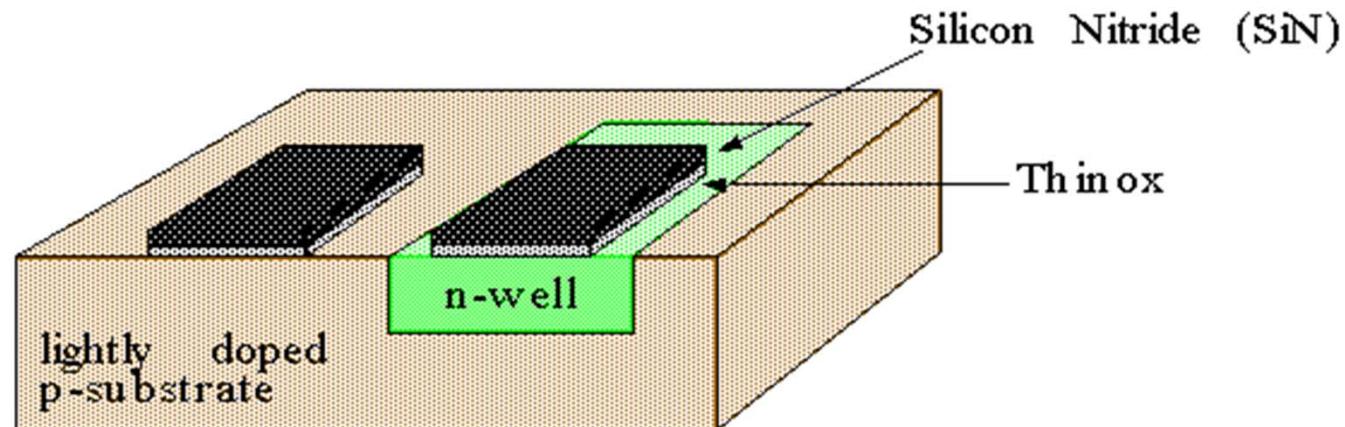


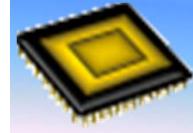


VLSI Chapter 3

N-well Process(2/8)

- active mask defines areas where transistors are fabricated.

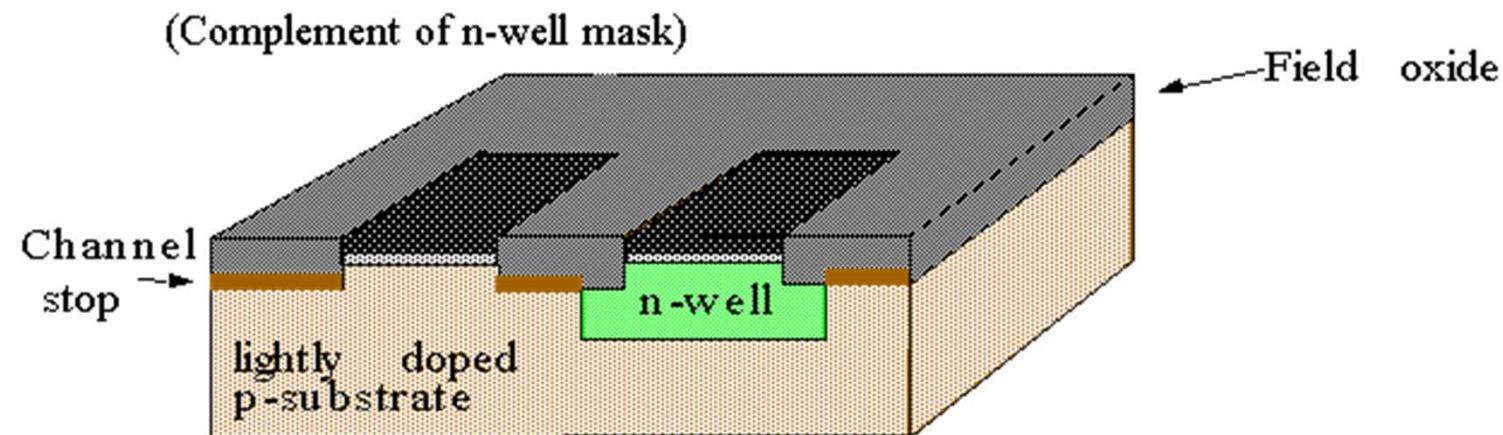


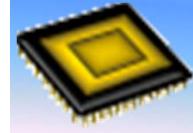


VLSI Chapter 3

N-well Process(3/8)

- p-well mask used to produce channel-stop (p⁺ diffusion), field oxide grown.

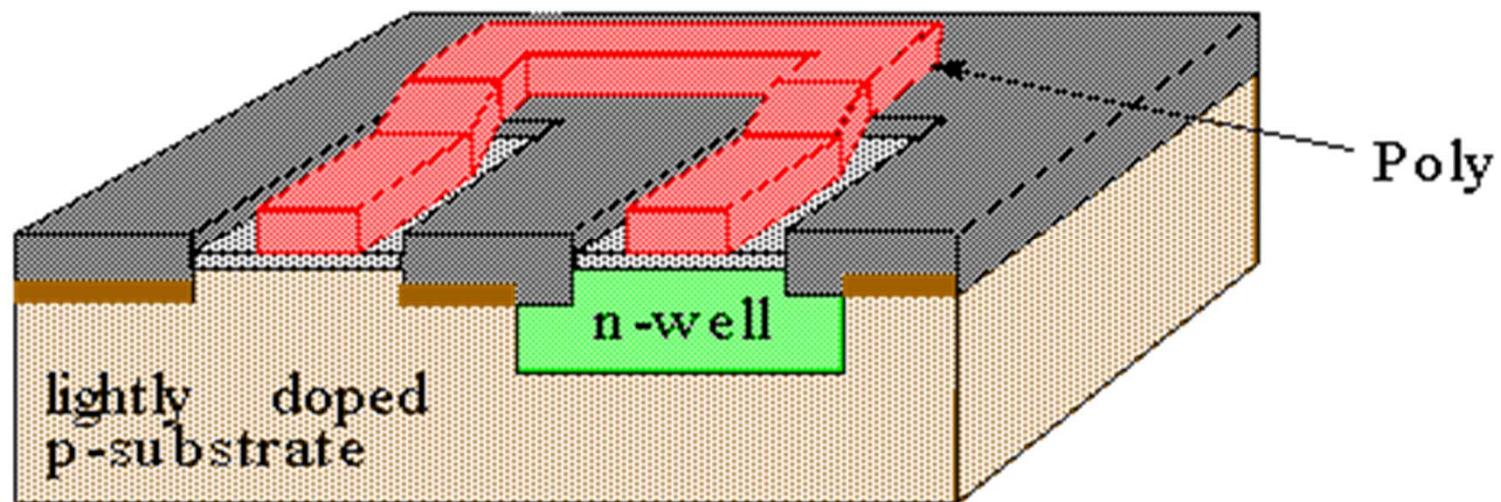


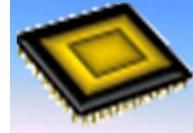


VLSI Chapter 3

N-well Process(4/8)

- poly mask used to etch poly patterns.

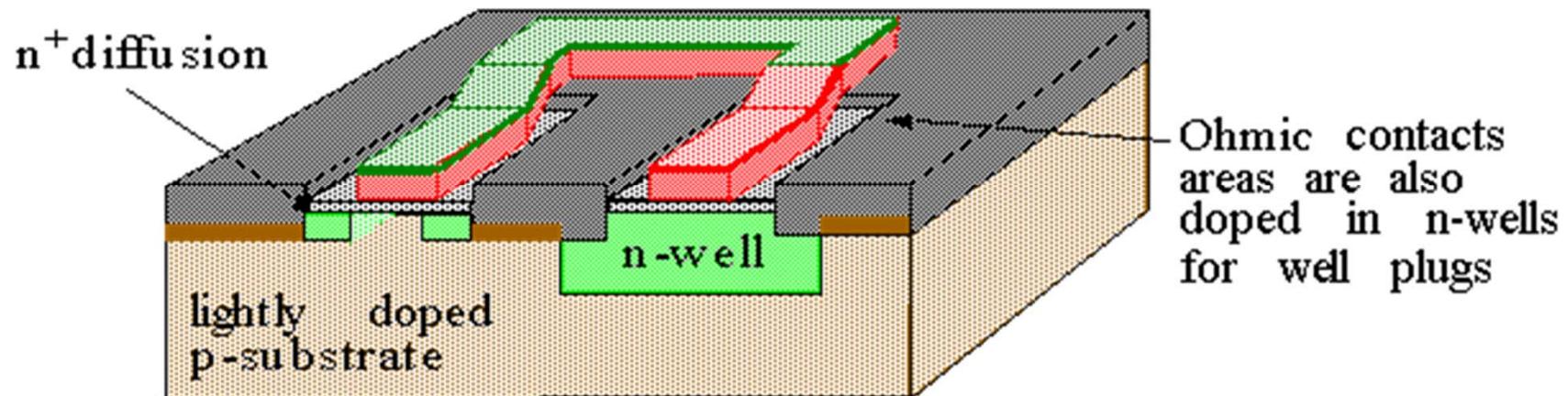


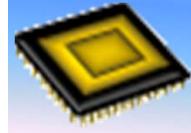


VLSI Chapter 3

N-well Process(5/8)

- n-plus mask (select mask) used to indicate those thin-oxide areas and poly that are to implanted n⁺.



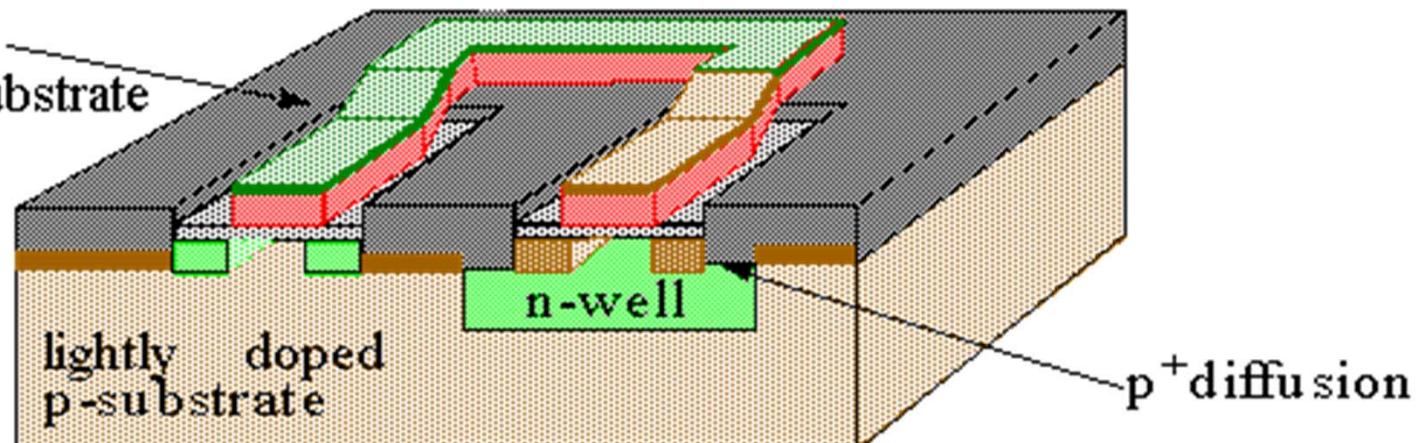


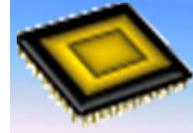
VLSI Chapter 3

N-well Process(6/8)

- p-plus mask used to indicate those thin-oxide areas and poly that are to implanted p^+ .

Ohmic contacts
areas are also
doped in p-substrate
for well plugs

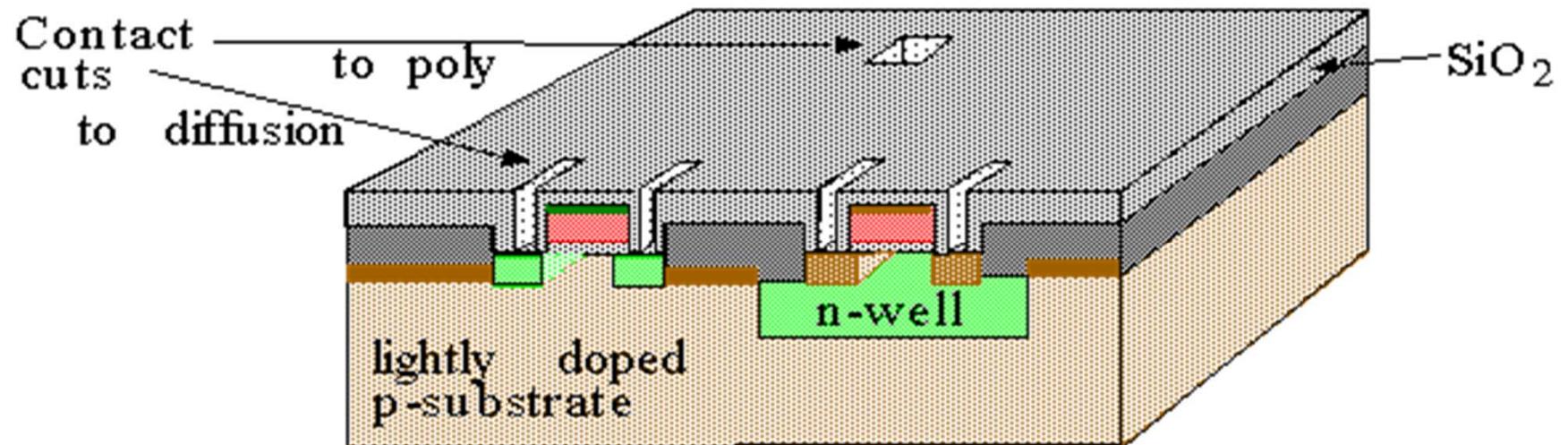


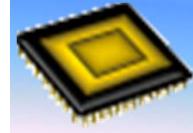


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N-well Process(7/8)

- Surface is covered with SiO_2 and contact cuts made.

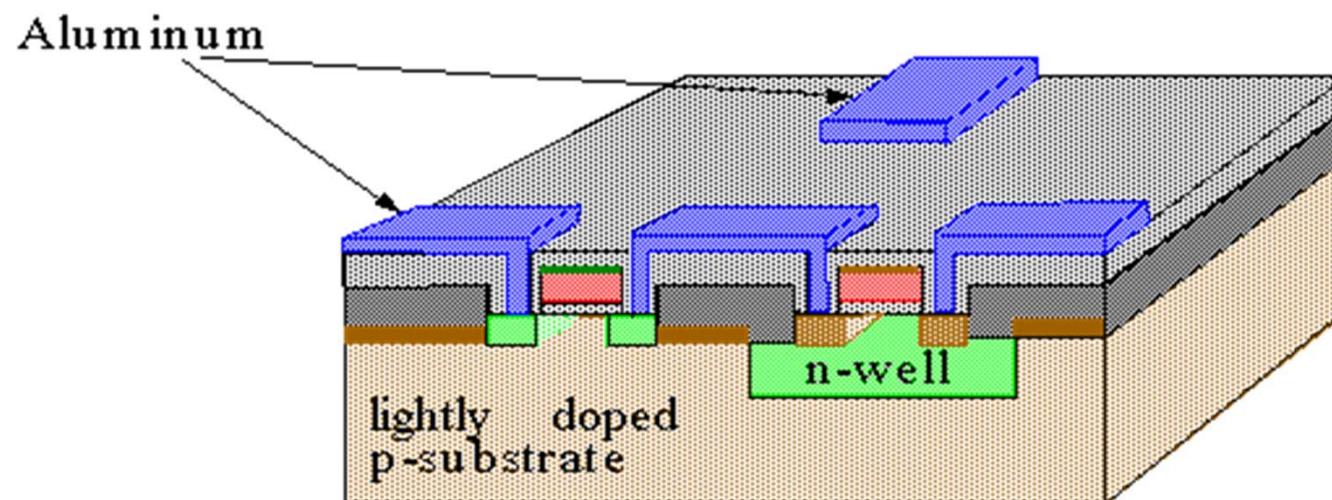


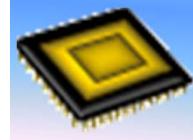


VLSI Chapter 3

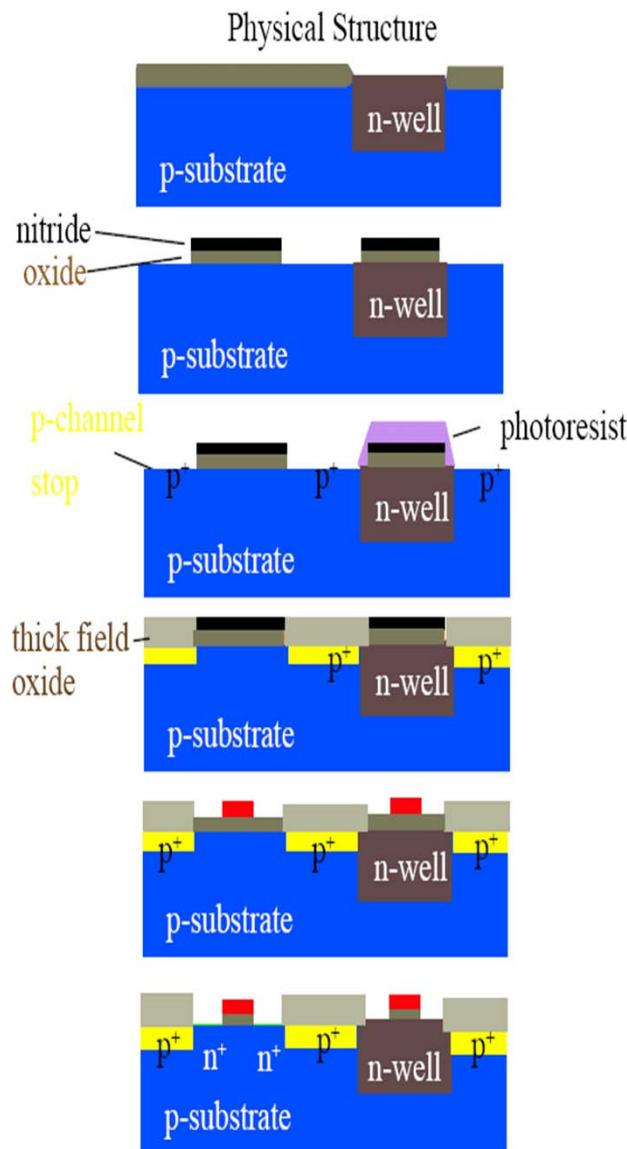
N-well Process(8/8)

- Metallization applied and etched using metal mask .
- The wafer is then passivated and opening to bond pads are etched.

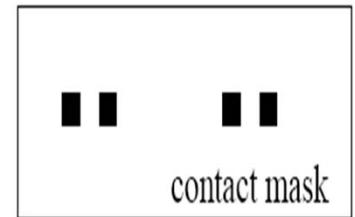
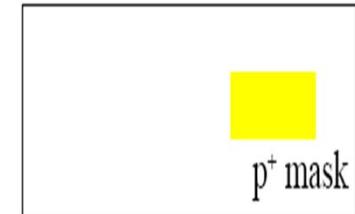
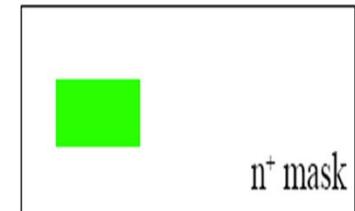
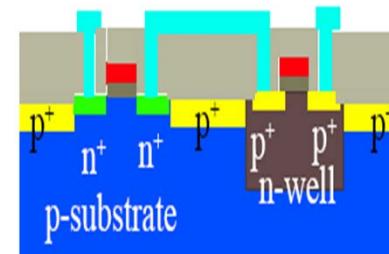
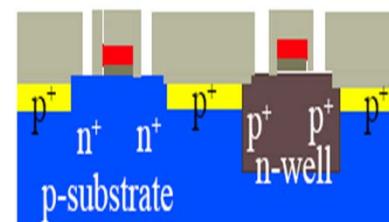
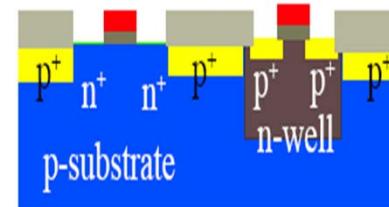
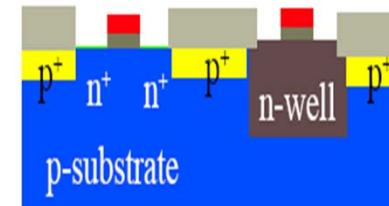
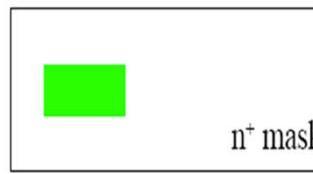
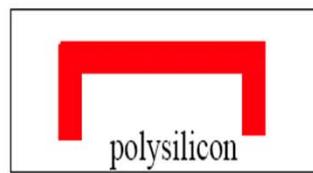
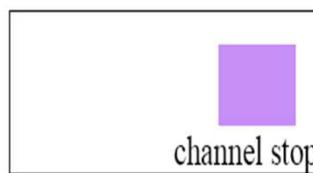
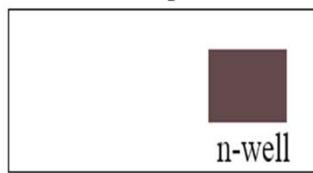


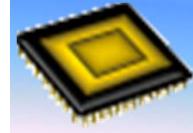


VLSI Chapter 3



Mask Top View

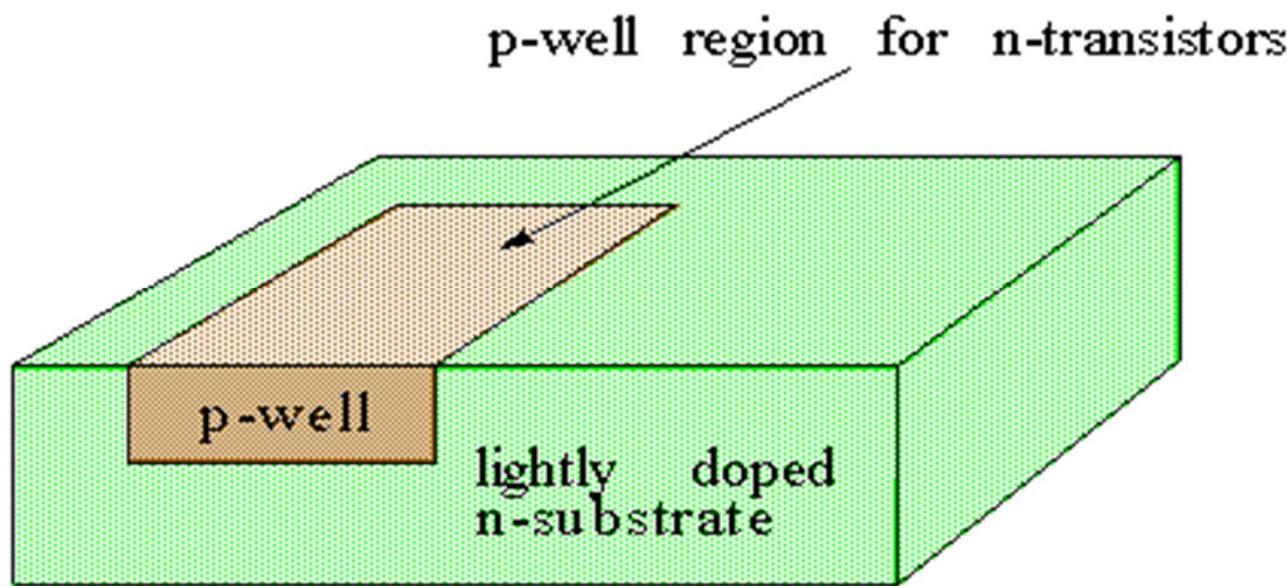


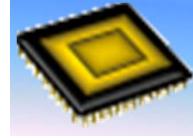


VLSI Chapter 3

P-well Process

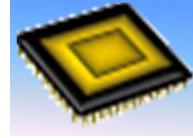
- Similar to n-well process except a p-well is implanted rather than an n-well.





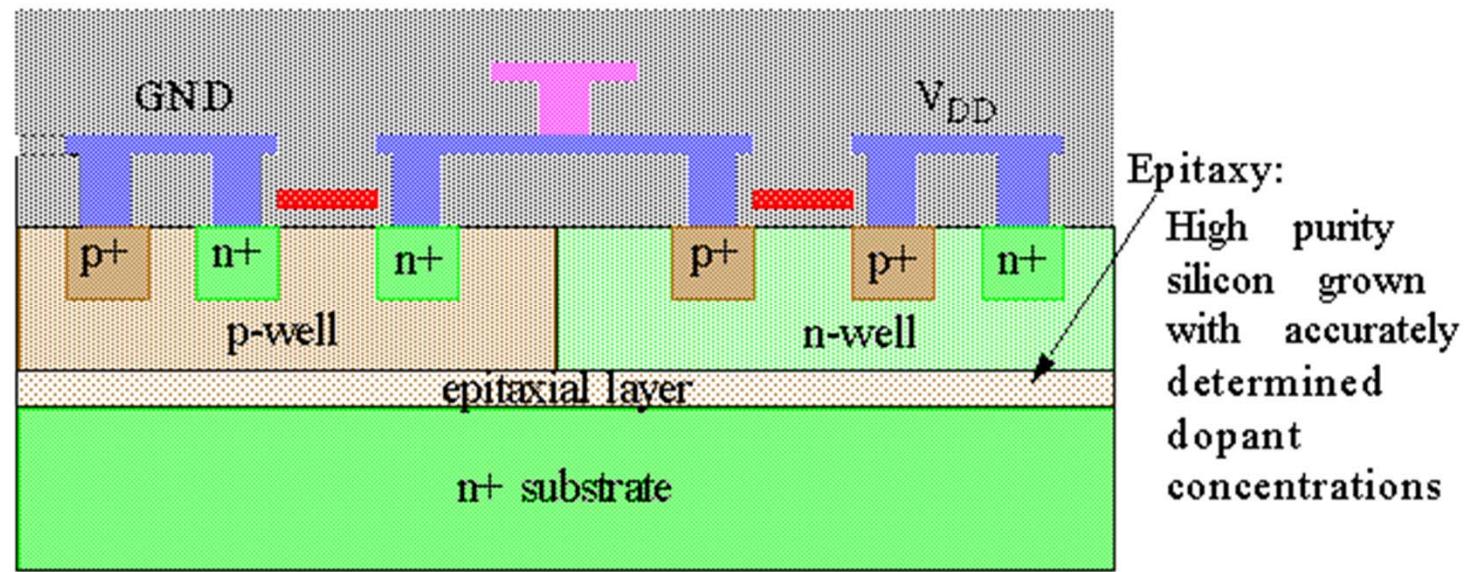
P-well Process(contd.)

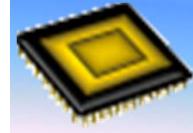
- Produces n- and p-transistors that are more balanced.
- Transistors that reside in the native substrate tend to have better characteristics.
- In general, p-devices are lower gain than n-devices.
- Therefore, p-well process naturally moderate the differences.



Twin-Tub Process

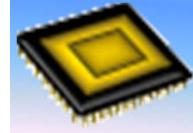
- Allows independent optimization of gain, threshold voltage, etc. of n-type and p-type devices.





SOI Process

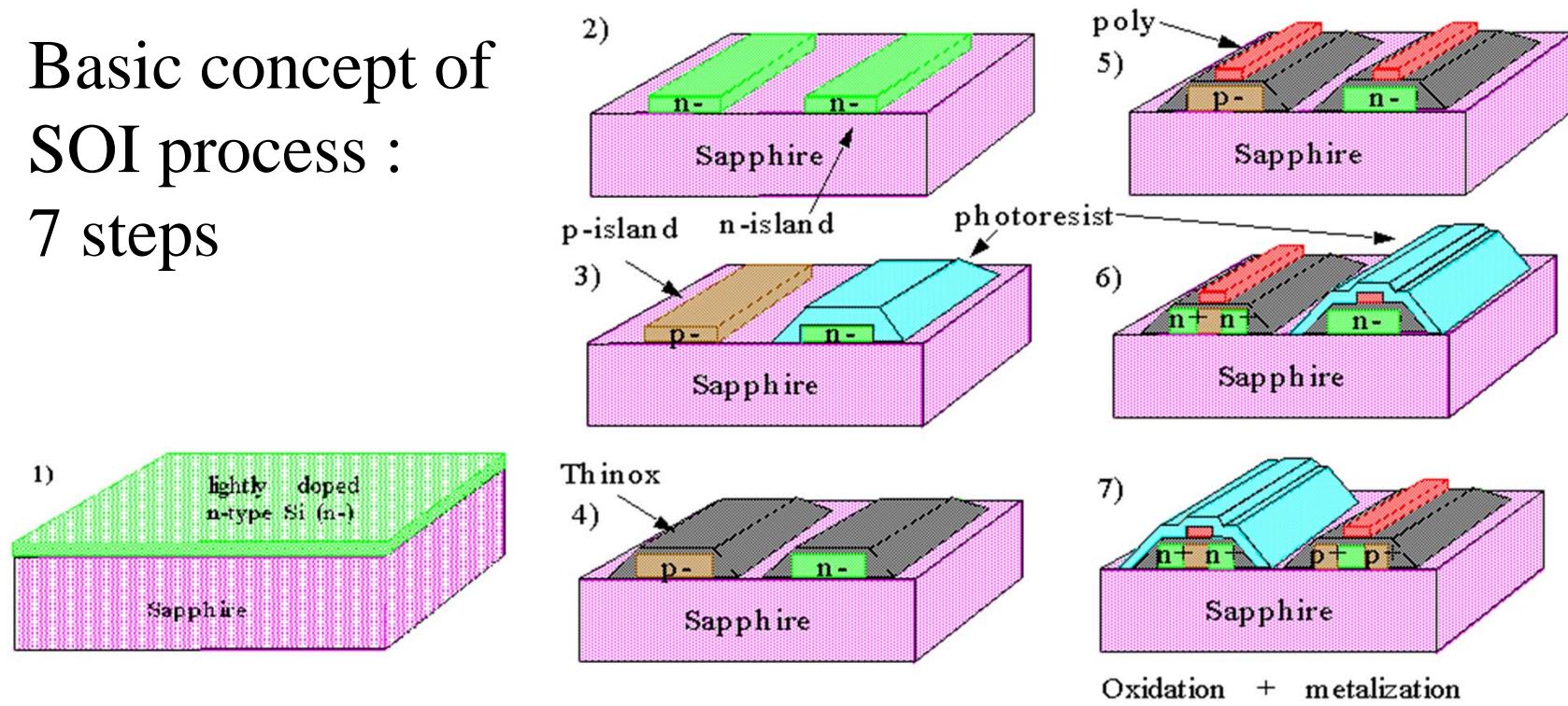
- Instead of silicon substrate, use an insulating substrate.
- Silicon can be grown on:
 - Sapphire or
 - SiO_2 which in turn has been grown on silicon.

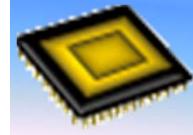


VLSI Chapter 3

SOI Process(contd.)

Basic concept of
SOI process :
7 steps



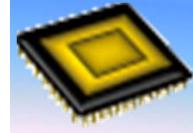


VLSI Chapter 3

Alignment Marks, Critical Dimension Marks

<u>LAYER</u>	<u>ALIGNMENT SEQUENCE</u>	<u>TOLERANCE</u>
1. N-Well		
2. Active	↑	≤ 0.05um
3. Poly	↑ ↑ ↑	≤ 0.05um
4. N+ S/D		≤ 0.08um
5. P+ S/D		≤ 0.08um
6. Contact	↑	≤ 0.05um
7. Metal	↑	≤ 0.08um
8. Pad	↑	≤ 0.08um

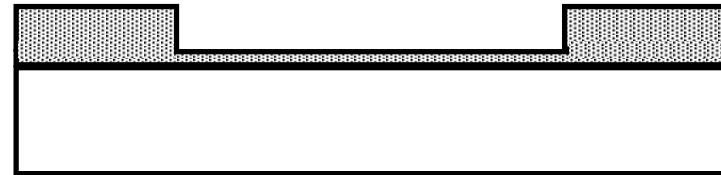
- Layers are to be aligned relative to each other



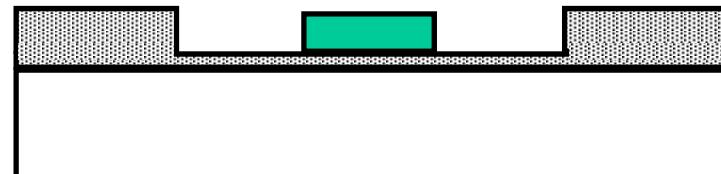
VLSI Chapter 3

Self-Aligned Gates

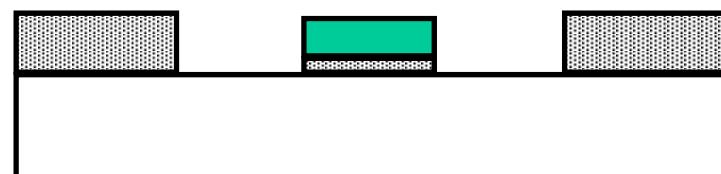
1. Create thin oxide in the “active” regions, thick elsewhere



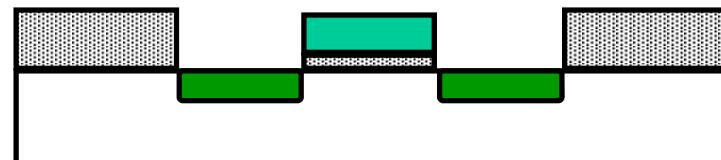
2. Deposit polysilicon

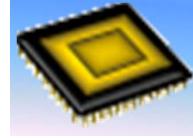


3. Etch thin oxide from active region (poly acts as a mask for the diffusion)



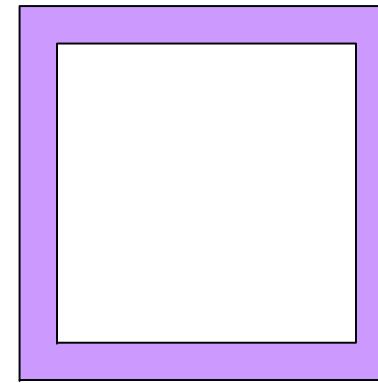
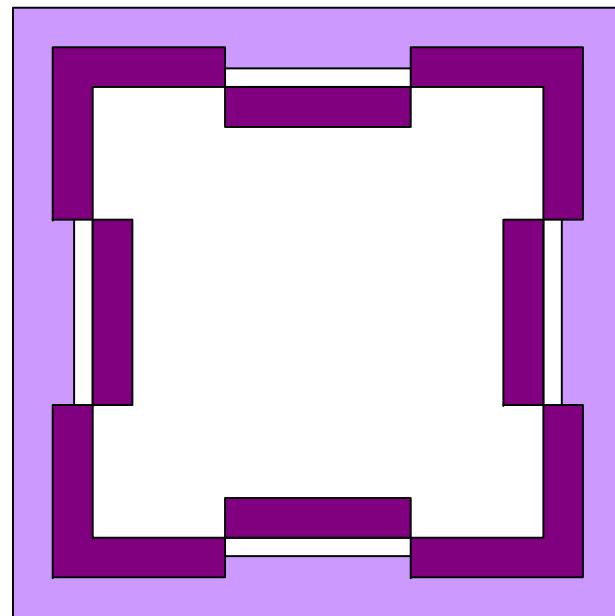
4. Implant dopant



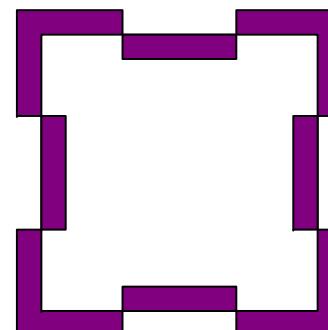


Alignment Marks (Alignment Key)

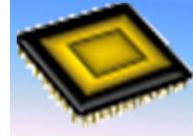
- The marks consist of a number of “squares” and “fortress”



square:
(Active)

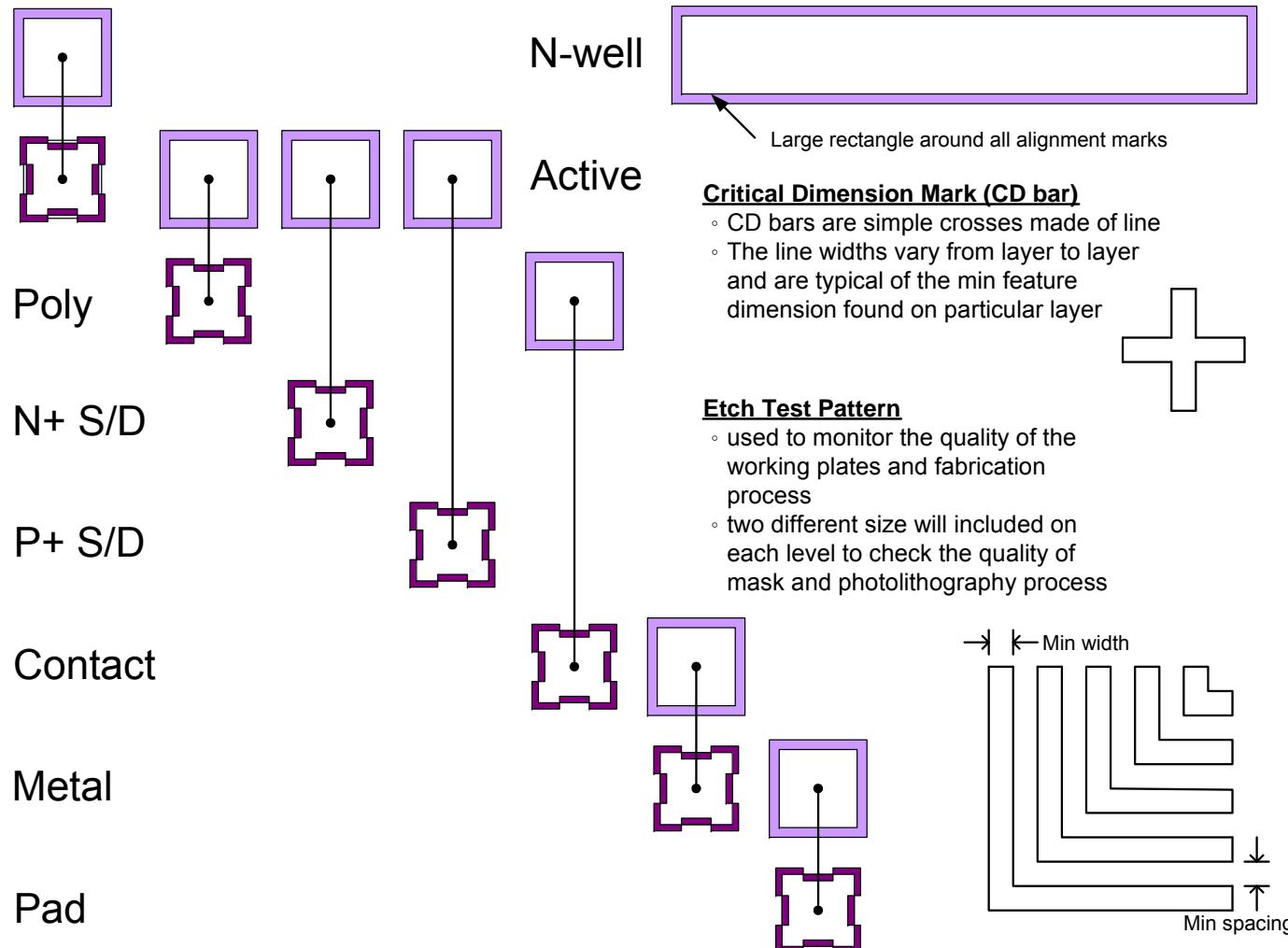


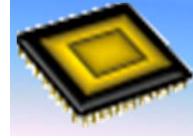
fortress:
(Poly)



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Alignment marks for mask layers





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Misalignment and Actual IC

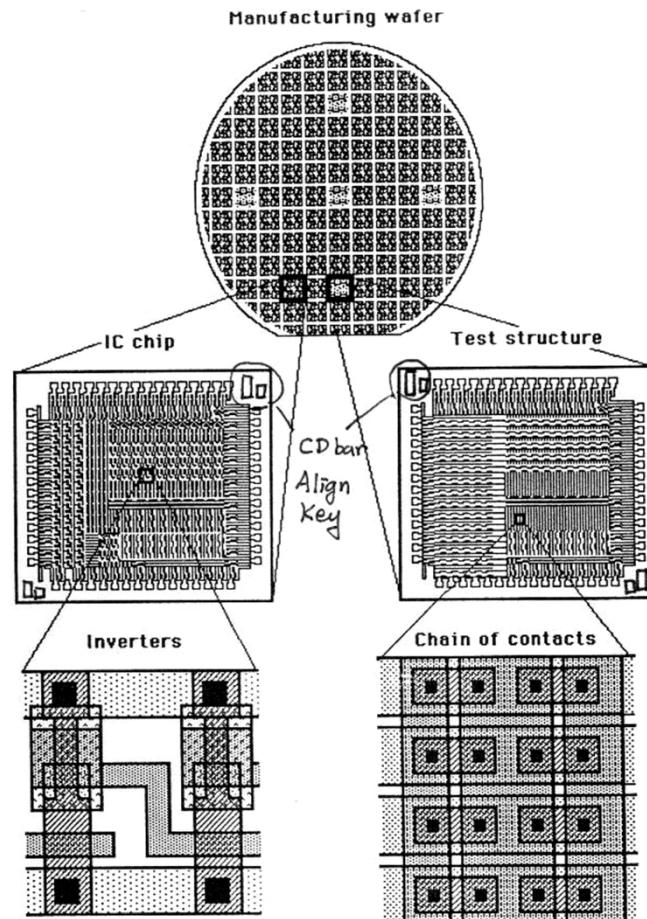


Figure 2-3: Manufacturing wafer.

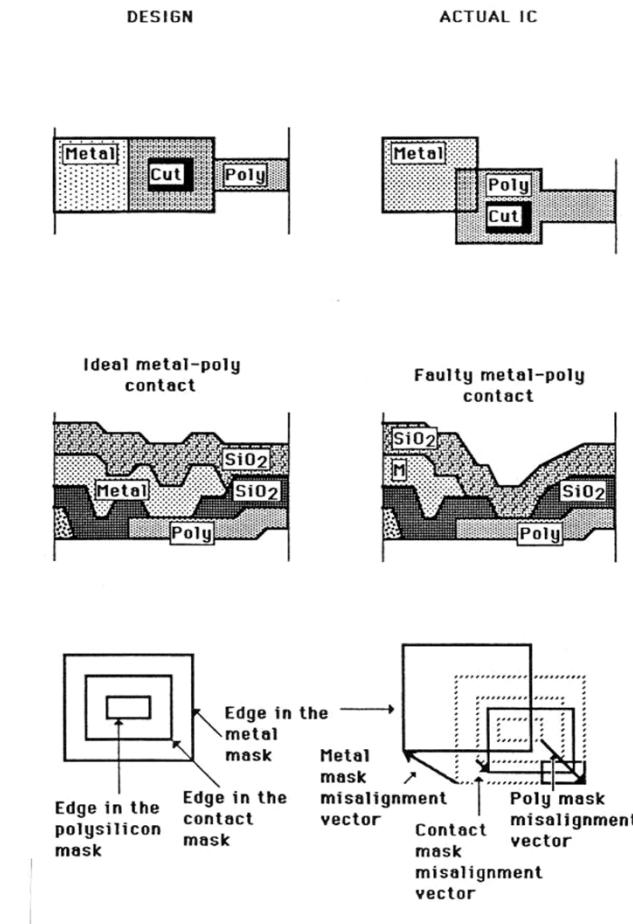
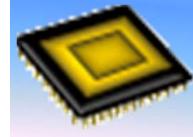


Figure 2-6: Misalignment of the metal, poly, and contact masks.



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Misalignment and Actual IC (contd.)

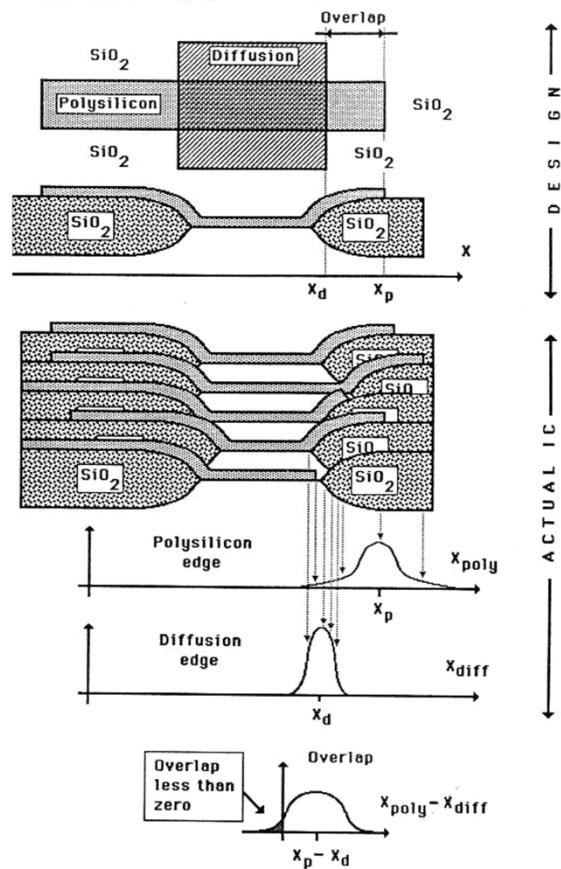


Figure 2-9: Minimal spacing between edges of two regions, determined by fluctuations in the location of the boundaries of these regions in the actual IC.

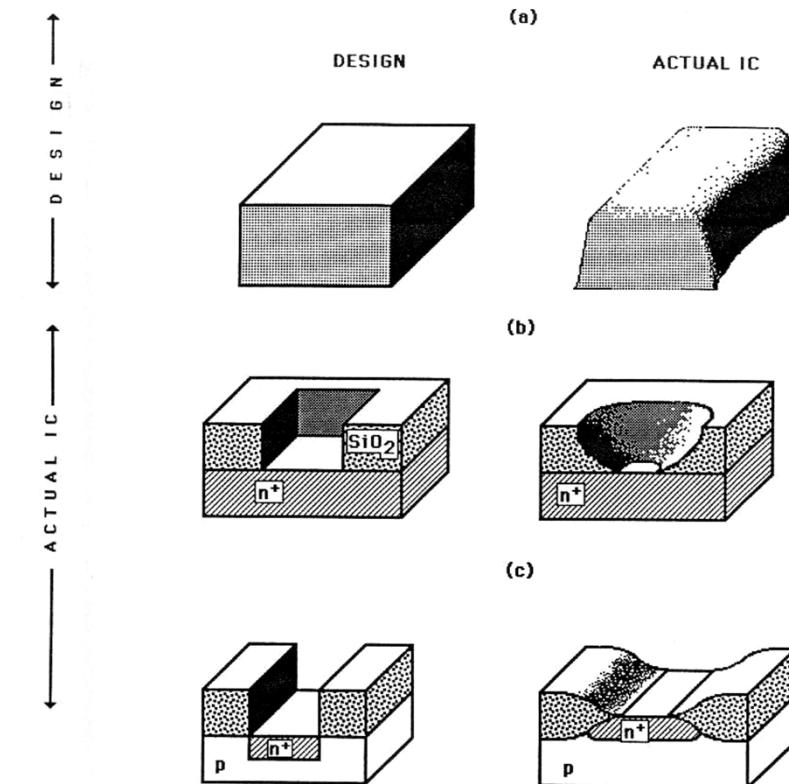
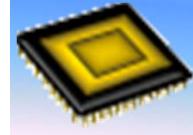
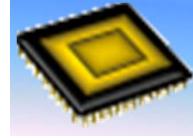


Figure 2-8: Discrepancies between concepts used in the design and actual elements of the IC, showing a metal line (a), contact cut (b), and diffusion region (c).



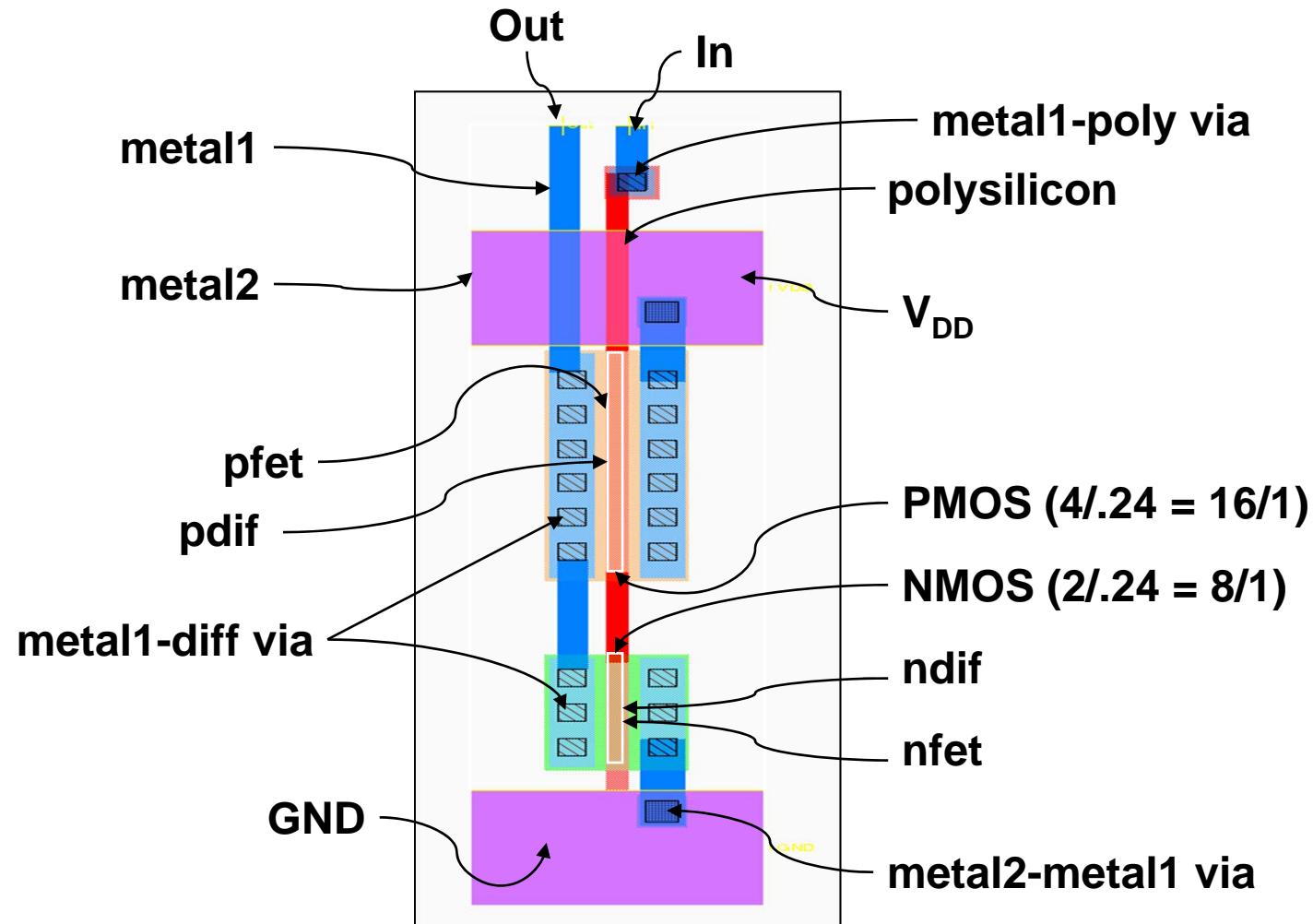
Layout Design Rules

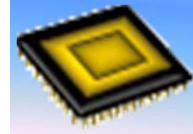
- In general, design rules represent the **best possible compromise between performance and yield.**
- To obtain the circuit with **optimum yield** is as small a geometry as possible without compromising reliability of the circuit.



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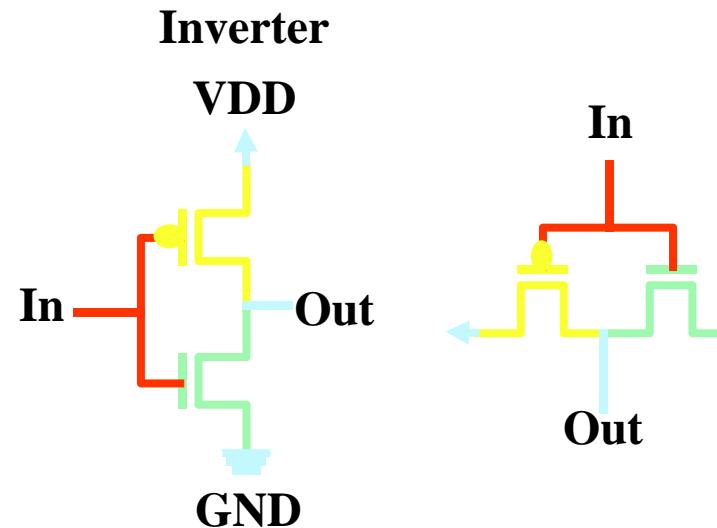
Example: Inverter Layout



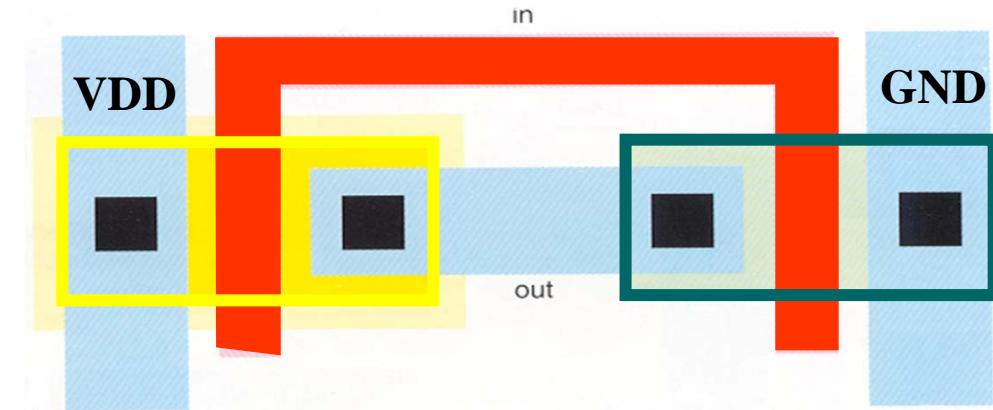


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Layout and Cross-Section View of Inverter



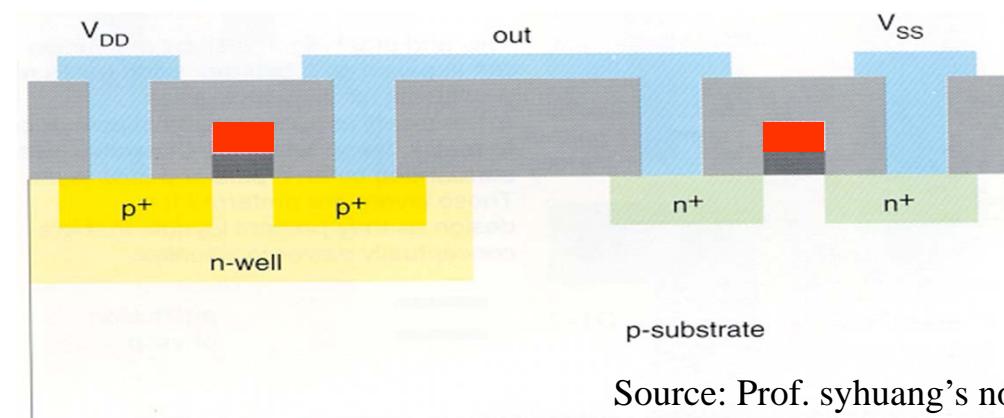
Top View or Layout



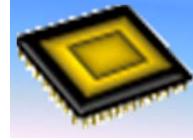
Legend of each layer

N-well
P-diffusion
N-diffusion
Polysilicon
Metal
contact

Cross-Section View

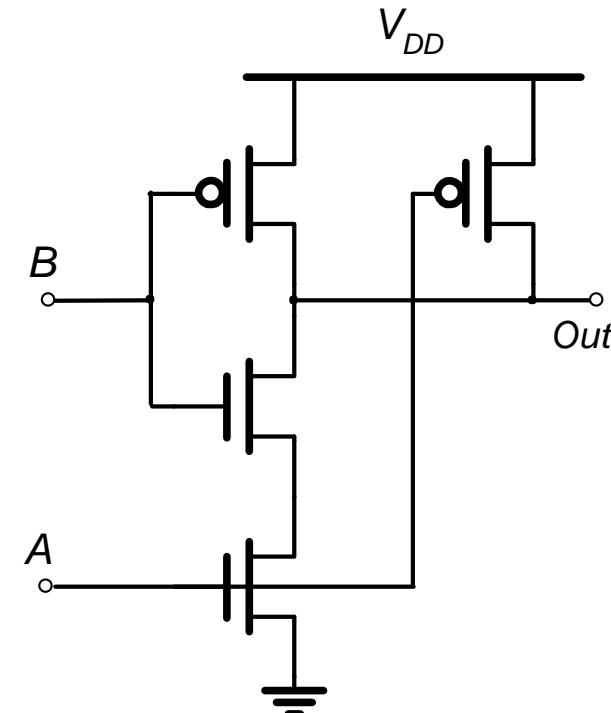
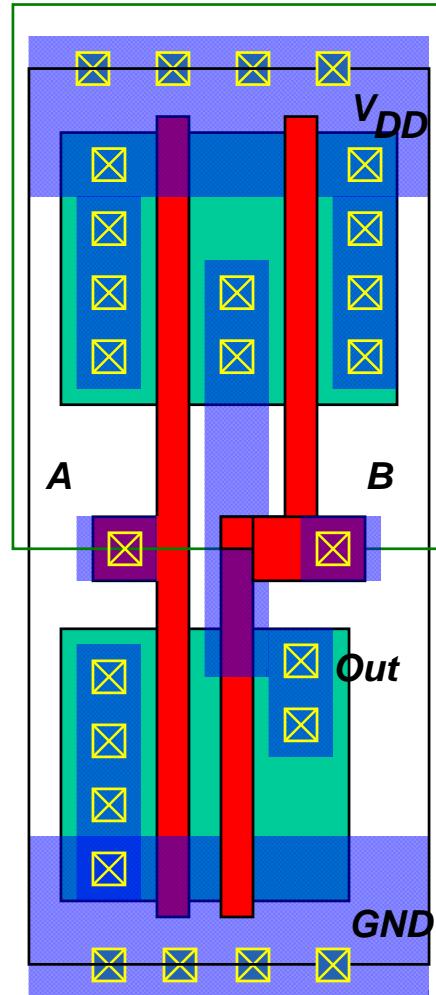


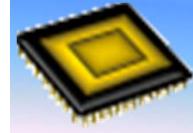
Source: Prof. syhuang's note



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2-input NAND gate

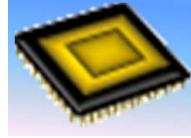




Layout Design Rules(contd.)

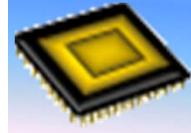
➤ Origin of rules :

- Electrical characteristic(such as breakdown, latch up, punch through ...etc.)
- Mask line width variation
- Lithographic variation (such as Mask Alignment, Mask runout, Exposure Time(under or over)...
- Etching time variation
- Processing variation
- Defects



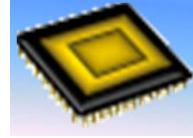
Types of Design Rule

- There are several approaches that can be taken in describing the design rules
 - **Micron Rule** : Normal style for industry design rules are usually given as a list of min.feature sizes and spacings for all the masks required in a given process
 - **Lambda-Based Rule** : popularized by Mead and Conway all the rules were expressed in terms of λ parameter



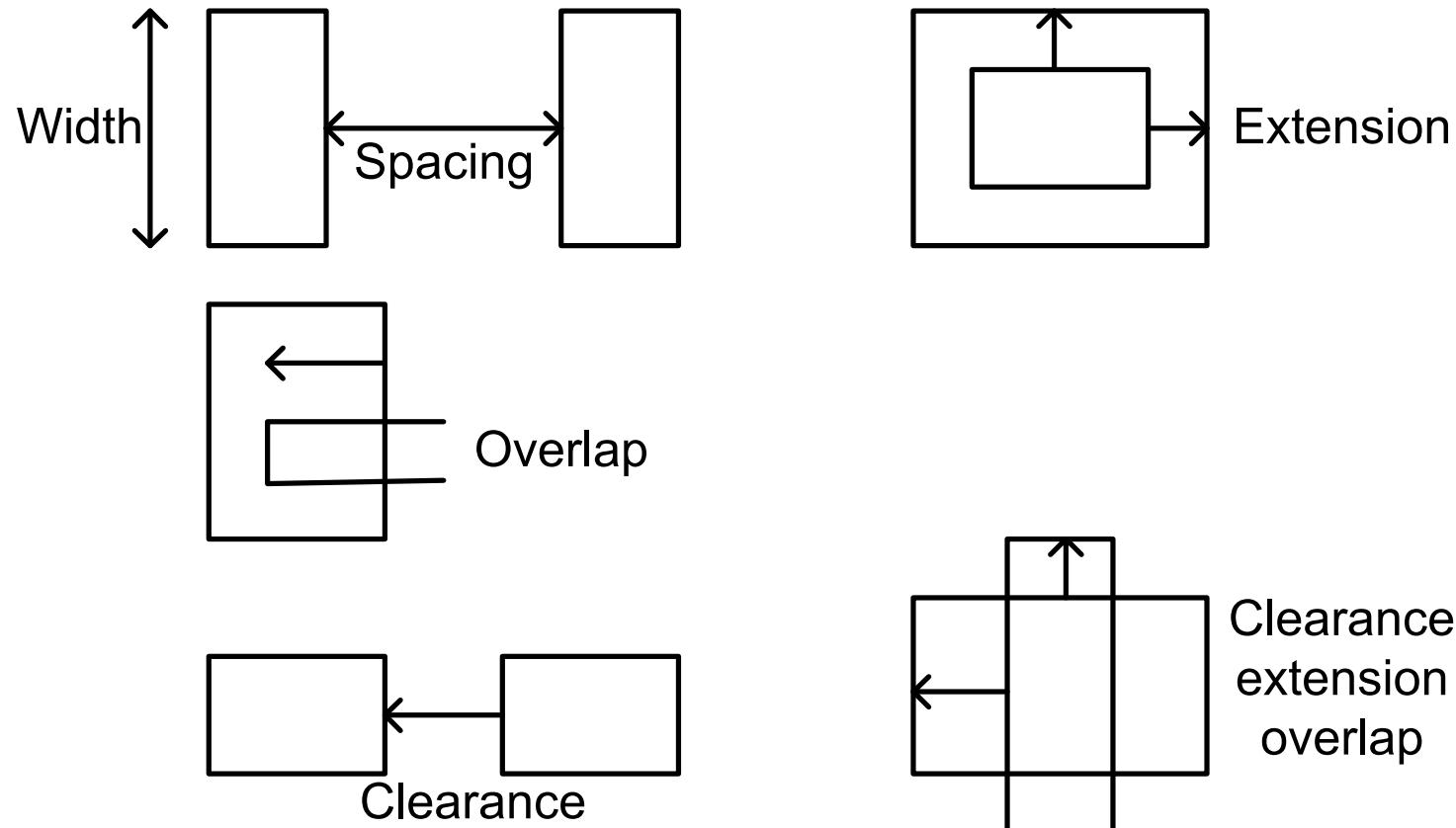
Types of Design Rule(contd.)

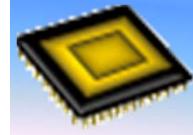
- Lambda-Based Rule
- Advantages :
 - single page rule : simple
 - Portable : can be used by many fab
 - Scaleable
- Disadvantage :
 - Less dense layout
 - Degradation in circuit performance
 - Some rules can't be scaleable as min. feature size reduced



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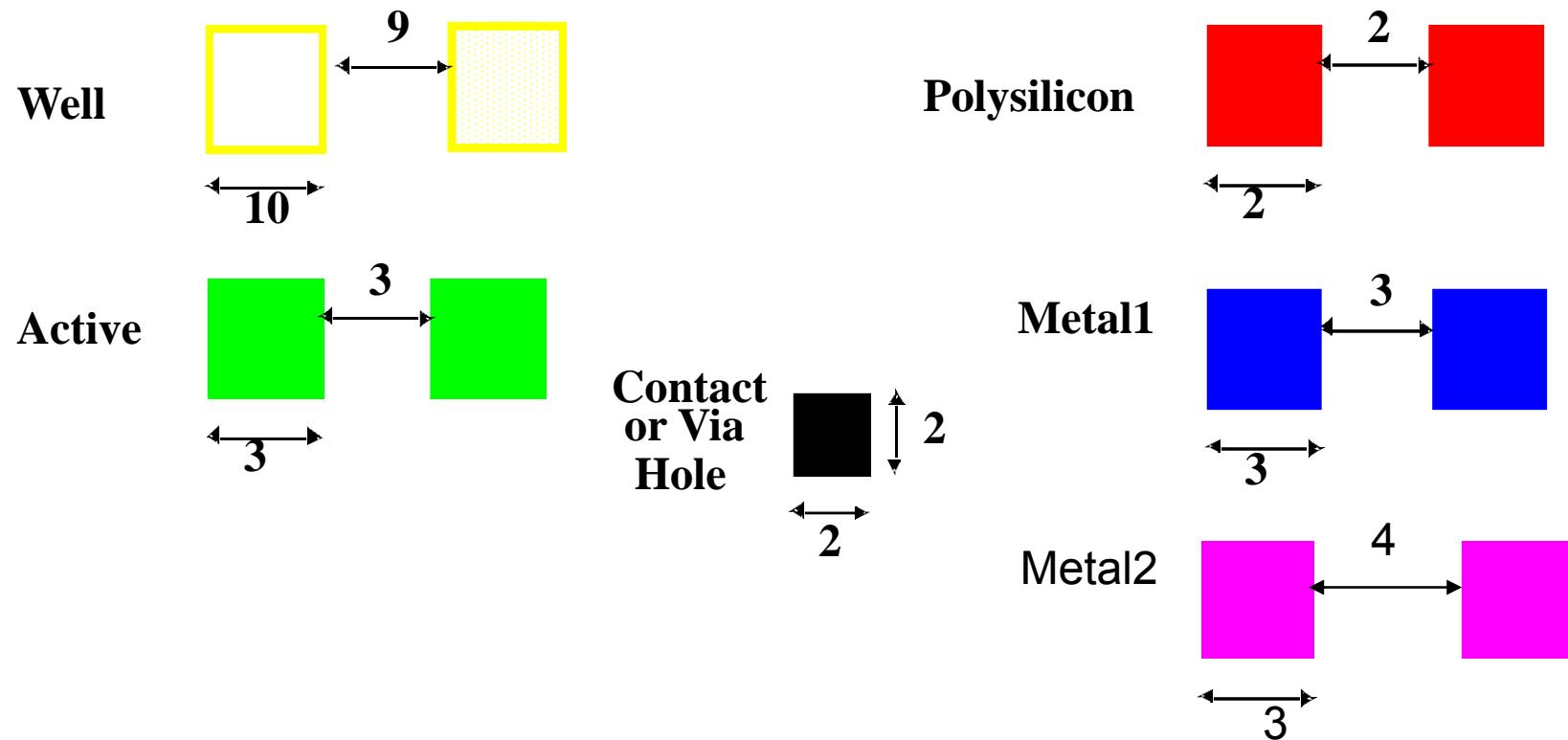
Terminologies of Design Rule

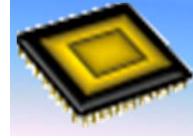




VLSI Chapter 3

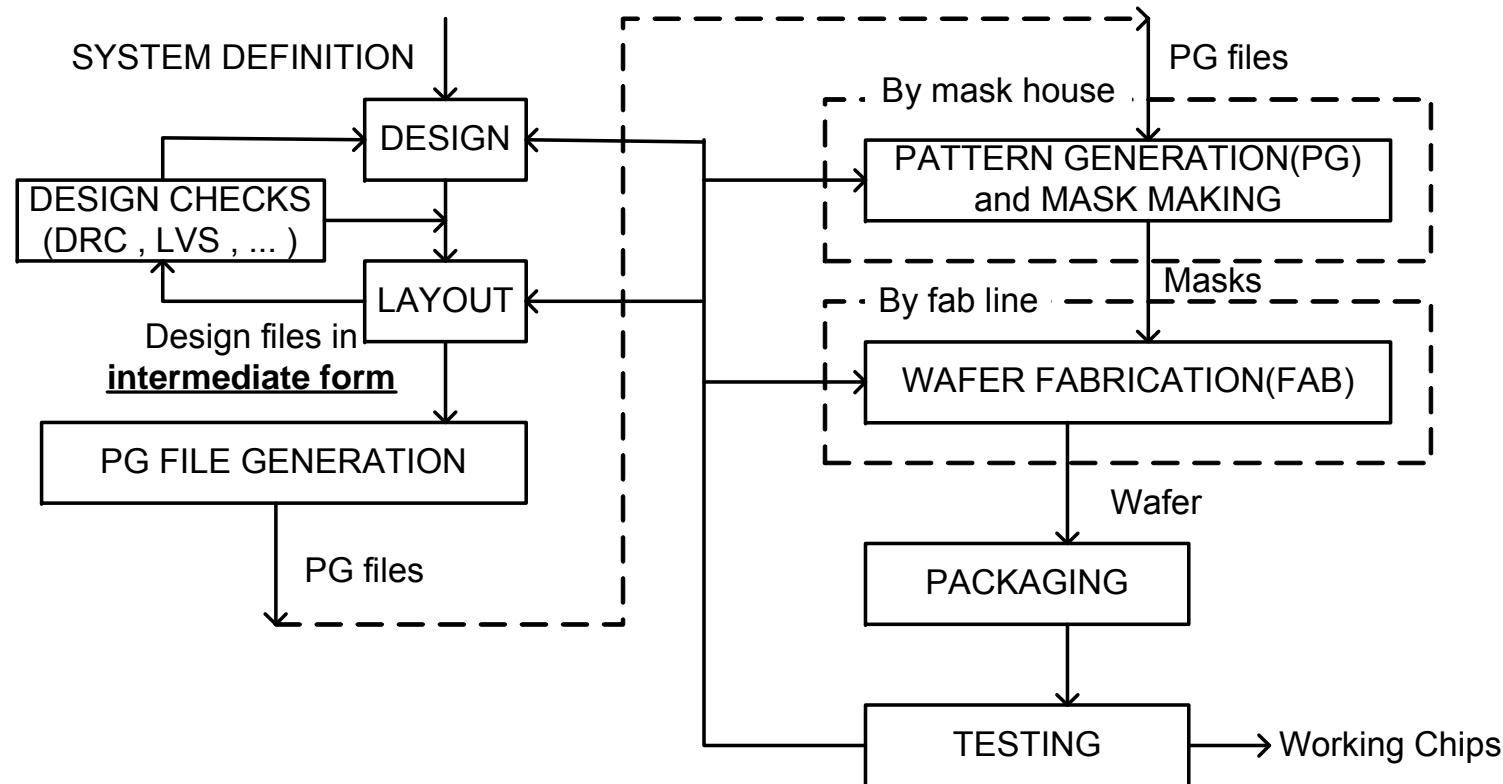
Intra-Layer Design Rules



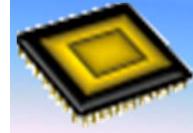


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Implementing Integrated System Designs



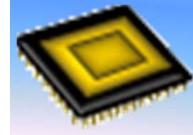
- From Circuit Topology to Patterning Geometry to Wafer Fabrication



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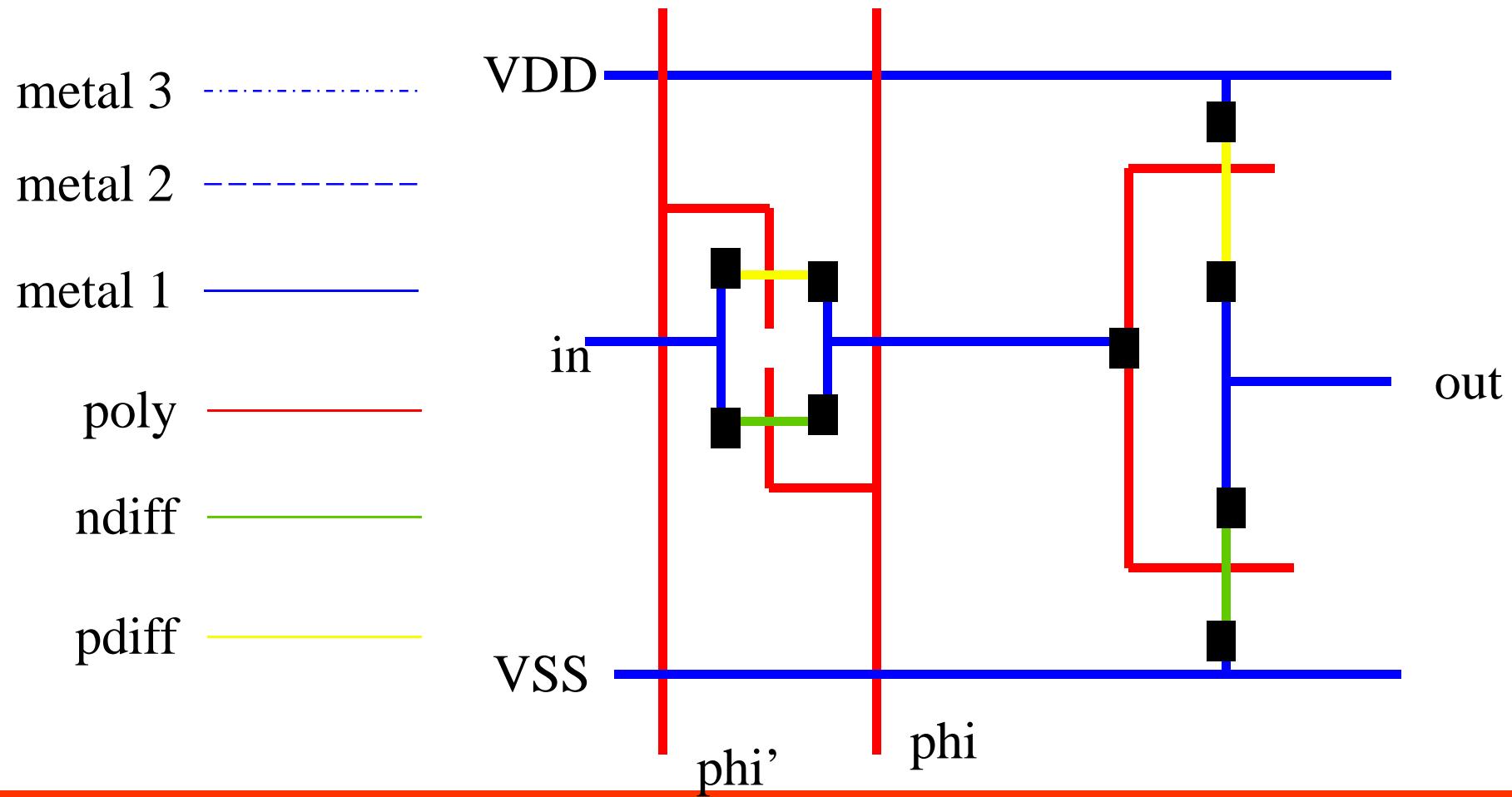
Integrated System Designs (contd.)

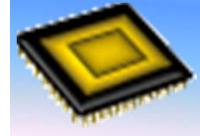
- Overview of implementation of an integrated
- Design Files : describe layout which is represented by intermediate form
- Intermediate Form : 1. CIF(Caltech Intermediate Form) (academic)
 2. GDS II(Industry)
- Pattern Generation(PG) Files : for use by a mask making firm
- Masks : master plate and working plate



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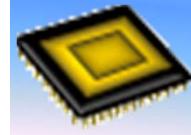
CMOS Stick Diagram





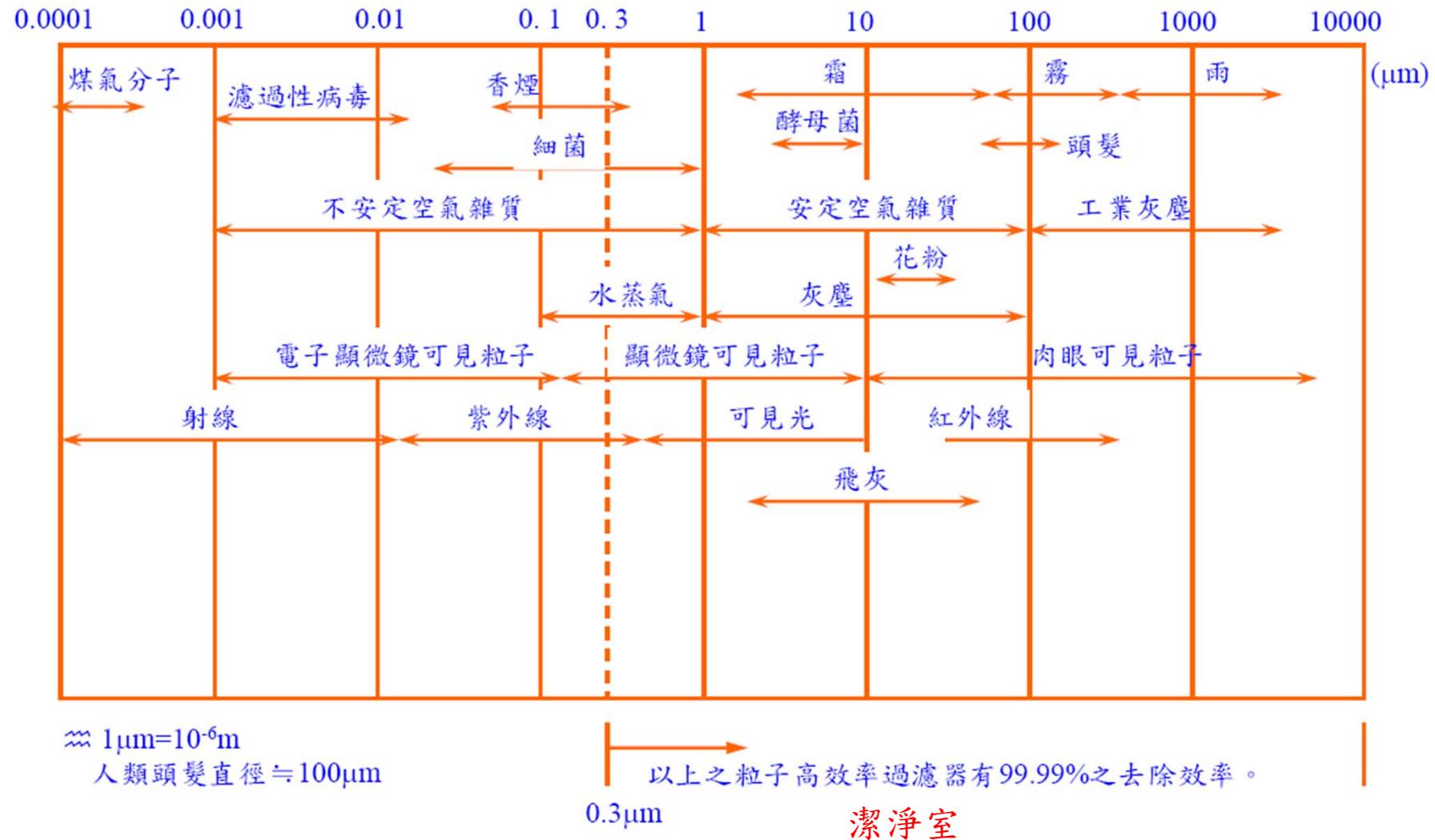
V L S I Chapter 3

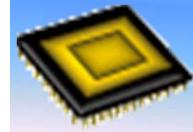
Appendix



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大氣中微塵分佈及粒子大小比較圖



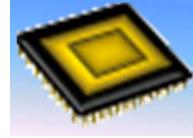


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DRAM DRAM及μ-Processor ICs Processor ICs所容許微粒之尺寸

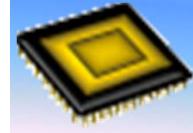
Year of first DRAM shipment	1995	1998	2001	2004	2007
Minimum feature (μm)	0.35	0.25	0.18	0.13	0.10
DRAM device generation (bits)	64M	256M	1G	4G	16G
DRAM cell size (μm^2)	1.50	0.60	0.24	0.096	0.038
DRAM chip size (cm^2)	1.9	2.8	4.2	6.4	9.6
μ -Processor # transistors (10^6)	12.0	28.0	64.0	150.0	350.0
μ -Processor chip size (cm^2)	2.5	3.0	3.6	4.3	5.2
Particulate size (minimum, μm)	0.12	0.08	0.06	0.04	0.03
Part./thin film process step (cm^{-2})	0.05	0.035	0.02	0.015	0.01

Source: The National Technology Roadmap for Semiconductor, SIA, 1994



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Enhancements

interconnect

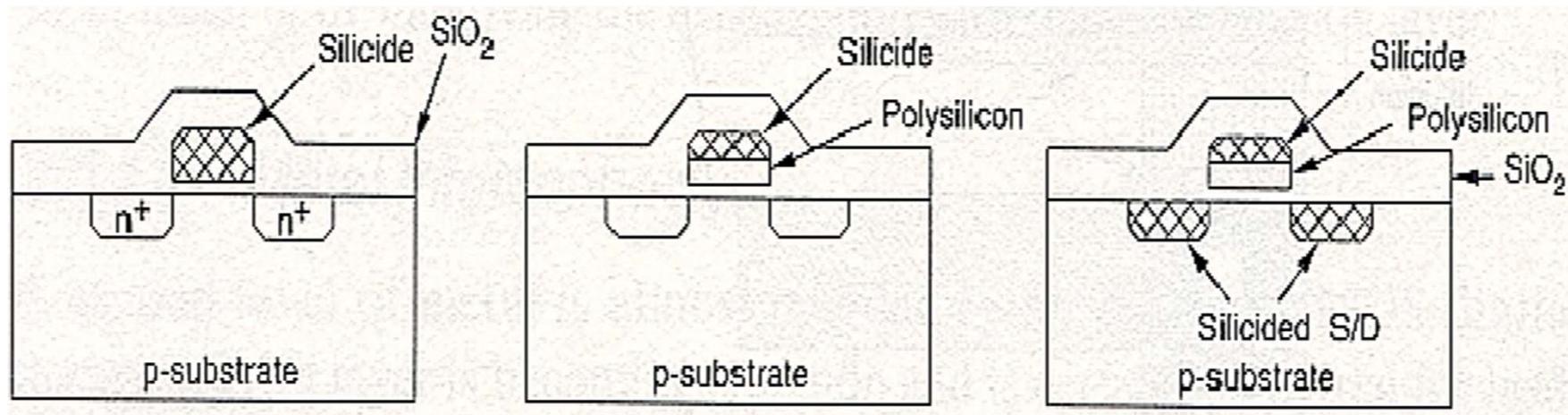
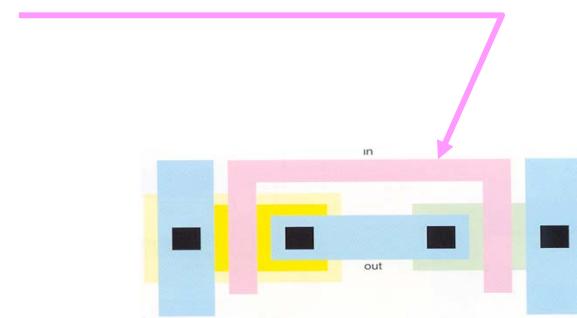
resistance of poly

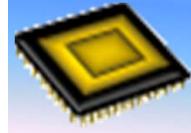
Silicide: silicon + tantalum for gate material

Polycide: silicide upon polysilicon

Salicide (Self Aligned SILICIDE):

Source: Prof. syhuang's note





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Reference

- Douglas A Pucknell, Kamran Eshraghian ,Basic VLSI Design 3rd Ed, Prentice Hall .
- M Michael Vai, VLSI Design, CRC Press, 2000
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- 國家晶片系統設計中心,Dracula Training Manual, 2002.07
- 中央大學電機工程學系,鄭國興老師
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- Digital Integrated Circuits^{2nd}
- 南台科技大學電子系,楊博惠老師
- 中興大學機械系,王昭亮老師
- Maitham Shams (CANADA)
- paulo moreira Switzerland
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- Digital Integrated Circuits^{2nd}

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