第07次實習課-電資

學生：林培瑋

2024 Advanced Mixed-Operation System (AMOS) Lab.

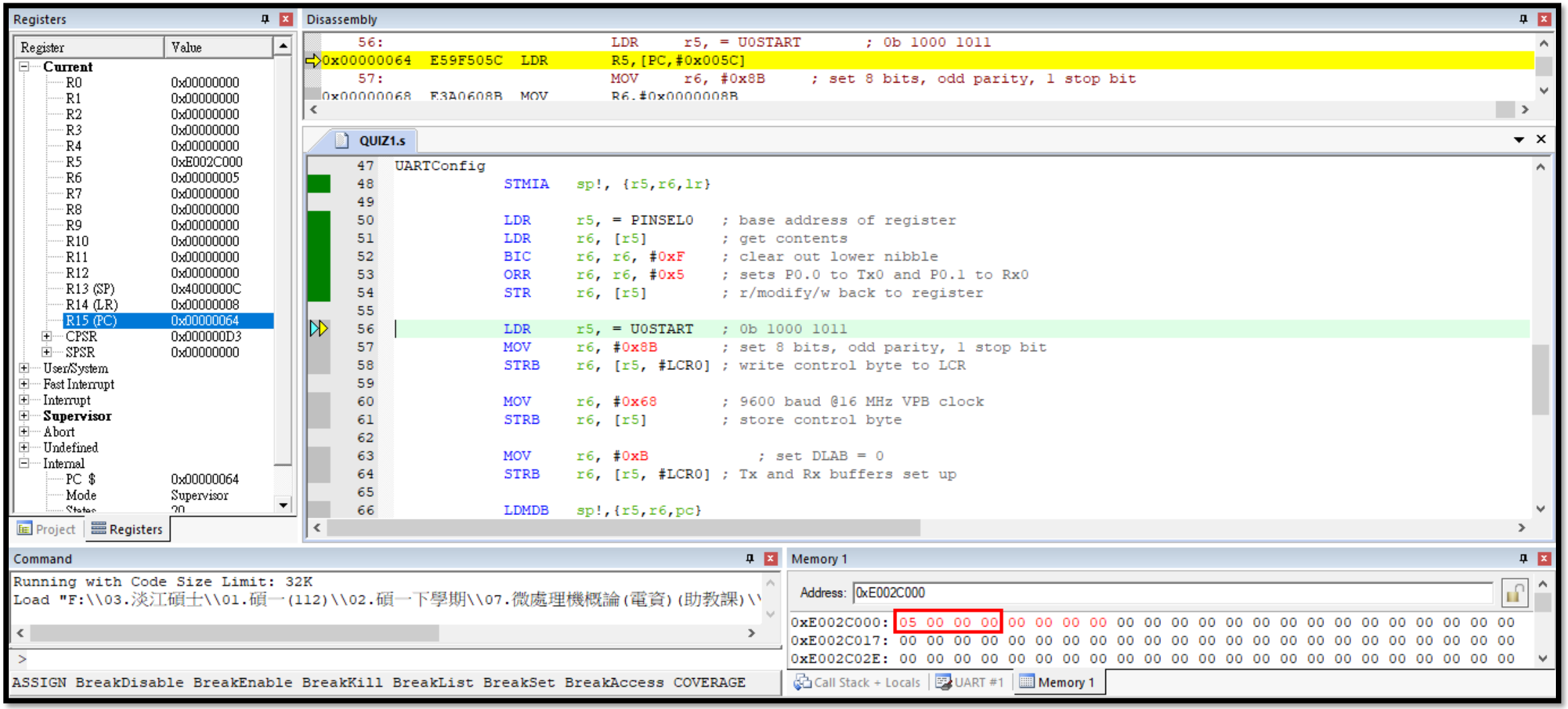
Tamkang University
Department of Electrical and Computer Engineering
No.151, Yingzhuan Rd., Tamsui Dist., New Taipei City 25137, Taiwan (R.O.C.)

第01次隨堂考-評分標準

- 第一題(共4小題)(60%)
  - (1)(a)(15%)
  - (1)(b)(15%)
  - (1)(c)(15%)
  - (2)(a)(15%)
- 第二題(共2小題)(40%)
  - (1)(20%)
  - (2)(20%)

→補繳分數 = 原始分數*0.8

第一題(1)(a)


Registers
Register
Value
Current
R0 0x00000000
R1 0x00000000
R2 0x00000000
R3 0x00000000
R4 0x00000000
R5 0xE002C000
R6 0x00000005
R7 0x00000000
R8 0x00000000
R9 0x00000000
R10 0x00000000
R11 0x00000000
R12 0x00000000
R13 (SP) 0x4000000C
R14 (LR) 0x00000008
R15 (PC) 0x00000064
CPSR 0x000000D3
SPSR 0x00000000
User/System
Fast Interrupt
Interrupt
Supervisor
Abort
Undefined
Internal
PC $ 0x00000064
Mode Supervisor
Project
Registers
Disassembly
56: LDR r5, = U0START ; 0b 1000 1011
0x00000064 E59F505C LDR R5,[PC,#0x005C]
57: MOV r6, #0x8B ; set 8 bits, odd parity, 1 stop bit
0x00000068 E3A0608B MOV R6,#0x0000008B
QUIZ1.s
47 UARTConfig
48 STMIA sp!, {r5,r6,lr}
49
50 LDR r5, = PINSEL0 ; base address of register
51 LDR r6, [r5] ; get contents
52 BIC r6, r6, #0xF ; clear out lower nibble
53 ORR r6, r6, #0x5 ; sets P0.0 to Tx0 and P0.1 to Rx0
54 STR r6, [r5] ; r/modify/w back to register
55
56 LDR r5, = U0START ; 0b 1000 1011
57 MOV r6, #0x8B ; set 8 bits, odd parity, 1 stop bit
58 STRB r6, [r5, #LCR0] ; write control byte to LCR
59
60 MOV r6, #0x68 ; 9600 baud @16 MHz VPB clock
61 STRB r6, [r5] ; store control byte
62
63 MOV r6, #0xB ; set DLAB = 0
64 STRB r6, [r5, #LCR0] ; Tx and Rx buffers set up
65
66 LDMDB sp!,{r5,r6,pc}
Command
Running with Code Size Limit: 32K
Load "F:\\03.淡江碩士\\01.碩一(112)\\02.碩一下學期\\07.微處理機概論(電資)(助教課)\\
ASSIGN BreakDisable BreakEnable BreakKill BreakList BreakSet BreakAccess COVERAGE
Memory 1
Address: 0xE002C000
0xE002C000: 05 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0xE002C017: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0xE002C02E: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
Call Stack + Locals
UART #1
Memory 1

第一題(1)(b)

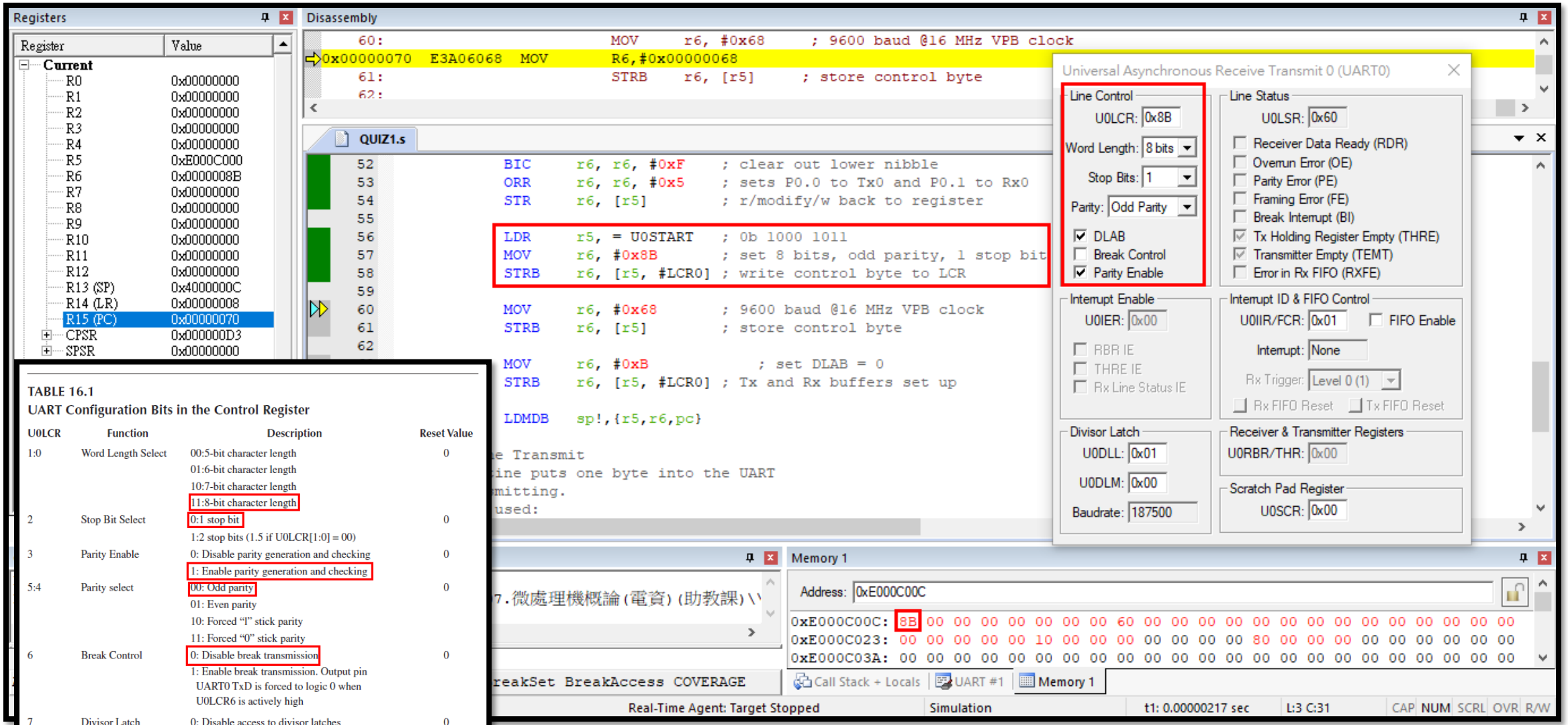
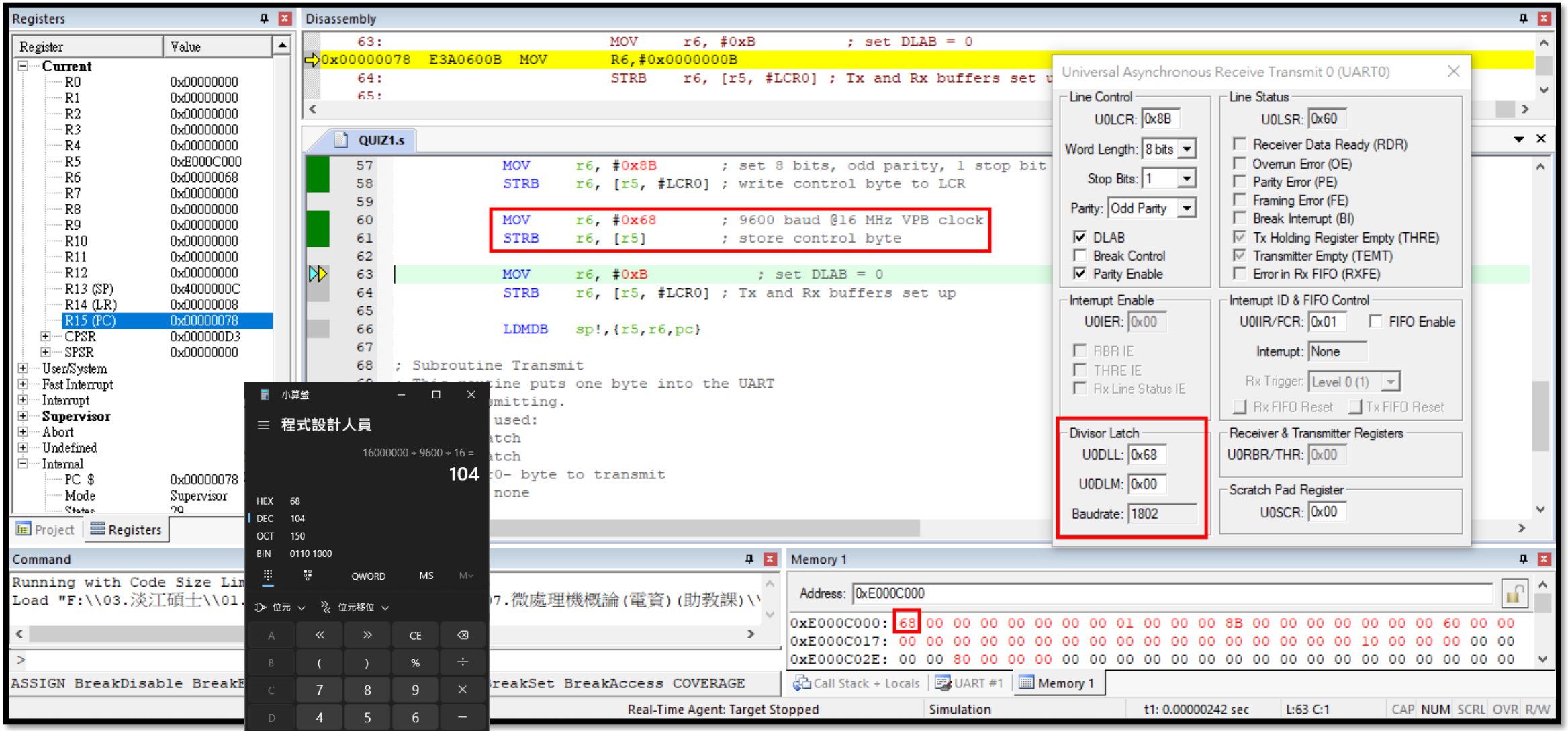


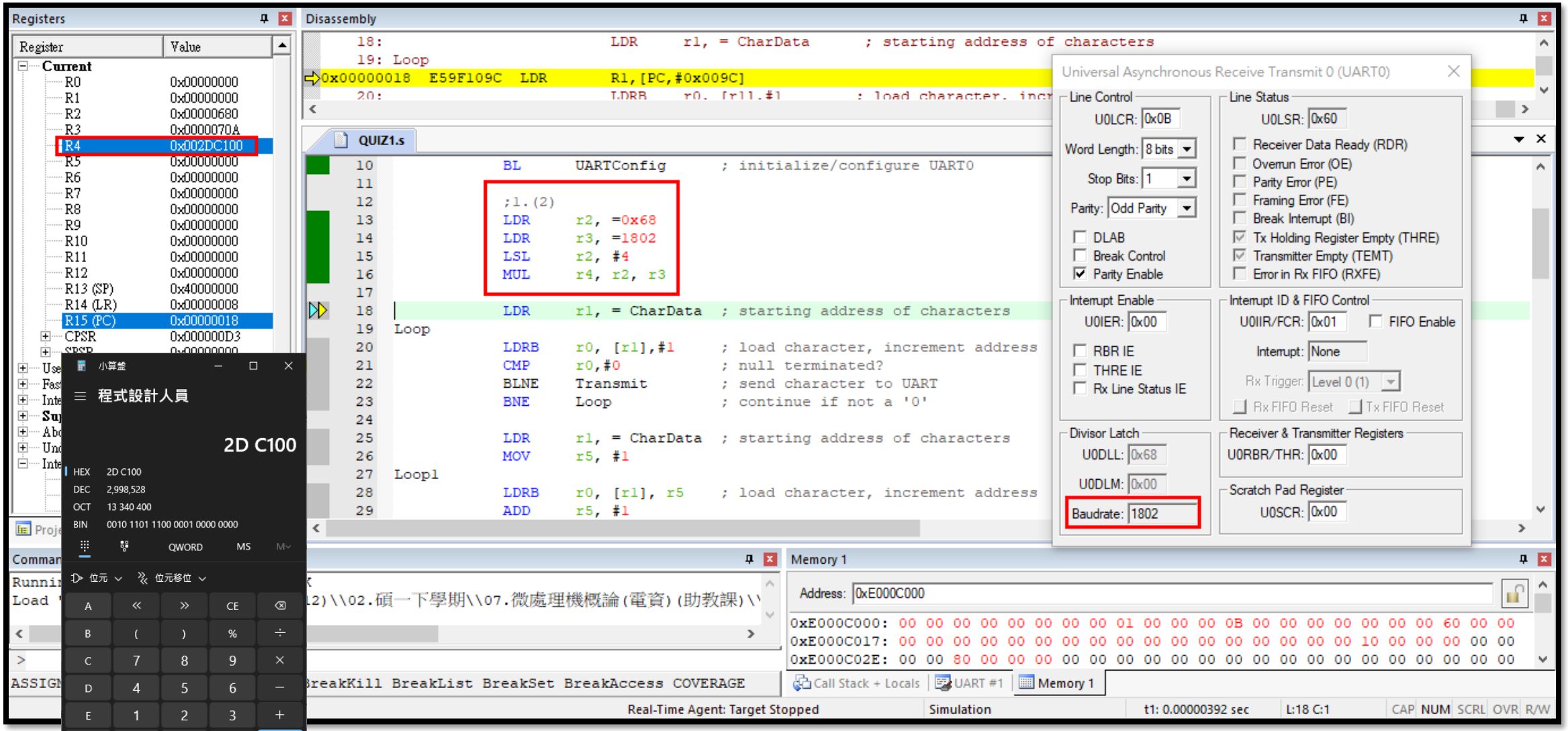
TABLE 16.1
UART Configuration Bits in the Control Register

U0LCR	Function	Description	Reset Value
1:0	Word Length Select	00:5-bit character length	0
		01:6-bit character length	
		10:7-bit character length	
		11:8-bit character length	
2	Stop Bit Select	0:1 stop bit	0
		1:2 stop bits (1.5 if U0LCR[1:0] = 00)	
3	Parity Enable	0: Disable parity generation and checking	0
		1: Enable parity generation and checking	
5:4	Parity select	00: Odd parity	0
		01: Even parity	
		10: Forced "1" stick parity	
		11: Forced "0" stick parity	
6	Break Control	0: Disable break transmission	0
		1: Enable break transmission. Output pin UART0 TxD is forced to logic 0 when U0LCR6 is actively high	
7	Divisor Latch Access Bit	0: Disable access to divisor latches	0
		1: Enable access to divisor latches	

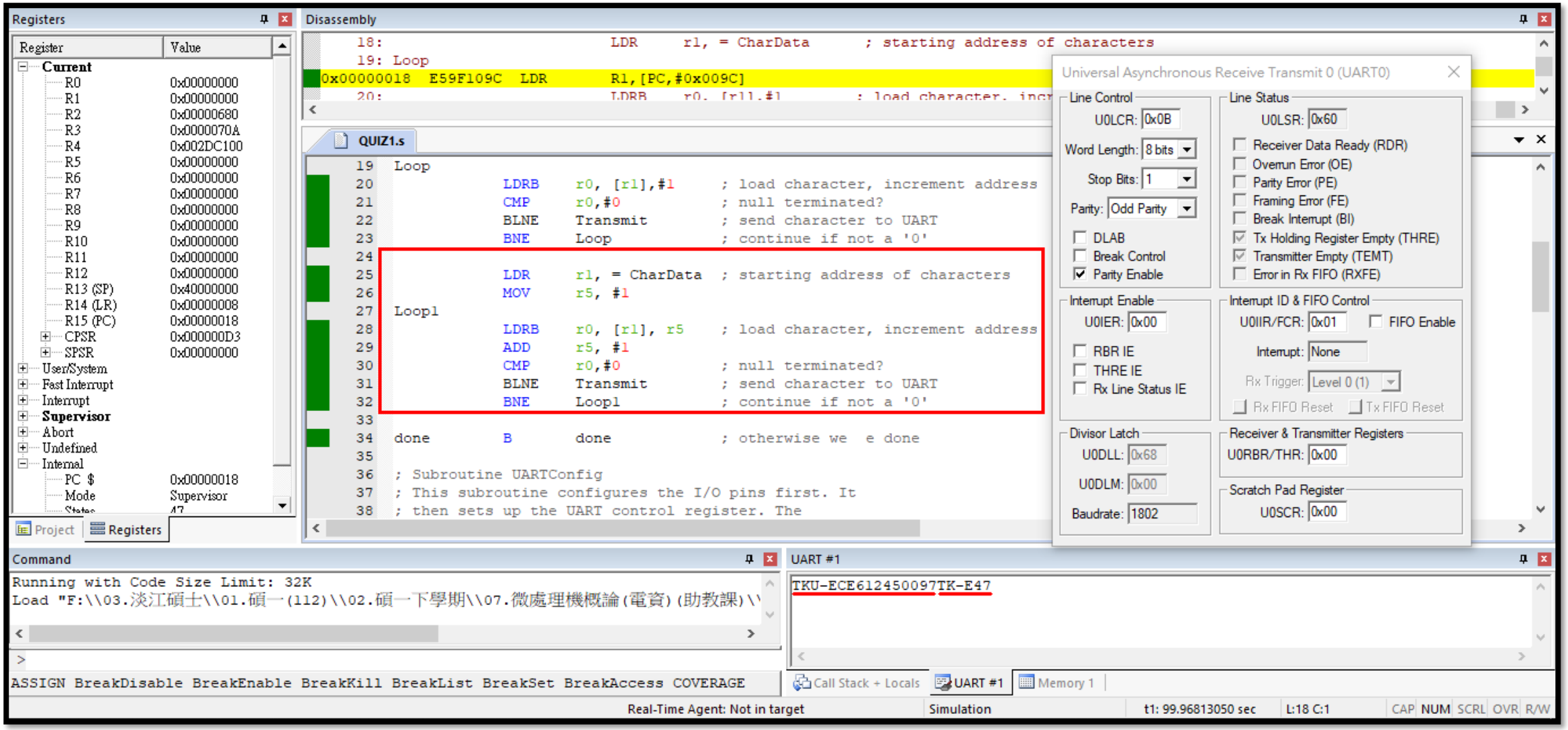
第一題(1)(c)


Registers
Register
Value
Current
R0 0x00000000
R1 0x00000000
R2 0x00000000
R3 0x00000000
R4 0x00000000
R5 0xE000C000
R6 0x00000068
R7 0x00000000
R8 0x00000000
R9 0x00000000
R10 0x00000000
R11 0x00000000
R12 0x00000000
R13 (SP) 0x4000000C
R14 (LR) 0x00000008
R15 (PC) 0x00000078
CPSR 0x000000D3
SPSR 0x00000000
User/System
Fast Interrupt
Interrupt
Supervisor
Abort
Undefined
Internal
PC $ 0x00000078
Mode Supervisor
Project
Registers
Disassembly
63: MOV r6, #0xB ; set DLAB = 0
0x00000078 E3A0600B MOV R6,#0x0000000B
64: STRB r6, [r5, #LCR0] ; Tx and Rx buffers set u
65:
QUIZ1.s
57 MOV r6, #0x8B ; set 8 bits, odd parity, 1 stop bit
58 STRB r6, [r5, #LCR0] ; write control byte to LCR
59
60 MOV r6, #0x68 ; 9600 baud @16 MHz VPB clock
61 STRB r6, [r5] ; store control byte
62
63 MOV r6, #0xB ; set DLAB = 0
64 STRB r6, [r5, #LCR0] ; Tx and Rx buffers set up
65
66 LDMDB sp!,{r5,r6,pc}
67
68 ; Subroutine Transmit
smitting.
used:
atch
atch
0- byte to transmit
none
Universal Asynchronous Receive Transmit 0 (UART0)
Line Control
U0LCR: 0x8B
Word Length: 8 bits
Stop Bits: 1
Parity: Odd Parity
DLAB
Break Control
Parity Enable
Line Status
U0LSR: 0x60
Receiver Data Ready (RDR)
Overrun Error (OE)
Parity Error (PE)
Framing Error (FE)
Break Interrupt (BI)
Tx Holding Register Empty (THRE)
Transmitter Empty (TEMT)
Error in Rx FIFO (RXFE)
Interrupt Enable
U0IER: 0x00
RBR IE
THRE IE
Rx Line Status IE
Interrupt ID & FIFO Control
U0IIR/FCR: 0x01
FIFO Enable
Interrupt: None
Rx Trigger: Level 0 (1)
Rx FIFO Reset
Tx FIFO Reset
Divisor Latch
U0DLL: 0x68
U0DLM: 0x00
Baudrate: 1802
Receiver & Transmitter Registers
U0RBR/THR: 0x00
Scratch Pad Register
U0SCR: 0x00
小算盤
程式設計人員
16000000 ÷ 9600 ÷ 16 =
104
HEX 68
DEC 104
OCT 150
BIN 0110 1000
QWORD
MS
Command
Running with Code Size Lim
Load "F:\\03.淡江碩士\\01.
7.微處理機概論(電資)(助教課)\\
ASSIGN BreakDisable BreakE
reakSet BreakAccess COVERAGE
Memory 1
Address: 0xE000C000
0xE000C000: 68 00 00 00 00 00 00 00 01 00 00 00 8B 00 00 00 00 00 00 00 60 00 00
0xE000C017: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 10 00 00 00 00 00
0xE000C02E: 00 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
Call Stack + Locals
UART #1
Memory 1
Real-Time Agent: Target Stopped
Simulation
t1: 0.00000242 sec
L:63 C:1
CAP NUM SCRL OVR R/W

第一題(2)(a)


Registers
Register
Value
Current
R0 0x00000000
R1 0x00000000
R2 0x00000680
R3 0x0000070A
R4 0x002DC100
R5 0x00000000
R6 0x00000000
R7 0x00000000
R8 0x00000000
R9 0x00000000
R10 0x00000000
R11 0x00000000
R12 0x00000000
R13 (SP) 0x40000000
R14 (LR) 0x00000008
R15 (PC) 0x00000018
CPSR 0x000000D3
Disassembly
18: LDR r1, = CharData ; starting address of characters
19: Loop
0x00000018 E59F109C LDR R1,[PC,#0x009C]
20: LDRB r0, [r1],#1 ; load character, incr
QUIZ1.s
10 BL UARTConfig ; initialize/configure UART0
11
12 ;1.(2)
13 LDR r2, =0x68
14 LDR r3, =1802
15 LSL r2, #4
16 MUL r4, r2, r3
17
18 LDR r1, = CharData ; starting address of characters
19 Loop
20 LDRB r0, [r1],#1 ; load character, increment address
21 CMP r0,#0 ; null terminated?
22 BLNE Transmit ; send character to UART
23 BNE Loop ; continue if not a '0'
24
25 LDR r1, = CharData ; starting address of characters
26 MOV r5, #1
27 Loop1
28 LDRB r0, [r1], r5 ; load character, increment address
29 ADD r5, #1
小算盤
程式設計人員
2D C100
HEX 2D C100
DEC 2,998,528
OCT 13 340 400
BIN 0010 1101 1100 0001 0000 0000
QWORD MS
Universal Asynchronous Receive Transmit 0 (UART0)
Line Control
U0LCR: 0x0B
Word Length: 8 bits
Stop Bits: 1
Parity: Odd Parity
DLAB
Break Control
Parity Enable
Line Status
U0LSR: 0x60
Receiver Data Ready (RDR)
Overrun Error (OE)
Parity Error (PE)
Framing Error (FE)
Break Interrupt (BI)
Tx Holding Register Empty (THRE)
Transmitter Empty (TEMT)
Error in Rx FIFO (RXFE)
Interrupt Enable
U0IER: 0x00
RBR IE
THRE IE
Rx Line Status IE
Interrupt ID & FIFO Control
U0IIR/FCR: 0x01
FIFO Enable
Interrupt: None
Rx Trigger: Level 0 (1)
Rx FIFO Reset
Tx FIFO Reset
Divisor Latch
U0DLL: 0x68
U0DLM: 0x00
Baudrate: 1802
Receiver & Transmitter Registers
U0RBR/THR: 0x00
Scratch Pad Register
U0SCR: 0x00
Memory 1
Address: 0xE000C000
0xE000C000: 00 00 00 00 00 00 00 00 01 00 00 00 0B 00 00 00 00 00 00 00 60 00 00
0xE000C017: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 10 00 00 00 00 00
0xE000C02E: 00 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
Call Stack + Locals
UART #1
Memory 1
Real-Time Agent: Target Stopped
Simulation
t1: 0.00000392 sec
L:18 C:1
CAP NUM SCRL OVR R/W

第二題(1)&(2)


Registers
Register
Value
Current
R0 0x00000000
R1 0x00000000
R2 0x00000680
R3 0x0000070A
R4 0x002DC100
R5 0x00000000
R6 0x00000000
R7 0x00000000
R8 0x00000000
R9 0x00000000
R10 0x00000000
R11 0x00000000
R12 0x00000000
R13 (SP) 0x40000000
R14 (LR) 0x00000008
R15 (PC) 0x00000018
CPSR 0x000000D3
SPSR 0x00000000
User/System
Fast Interrupt
Interrupt
Supervisor
Abort
Undefined
Internal
PC $ 0x00000018
Mode Supervisor
Project
Registers
Disassembly
18: LDR r1, = CharData ; starting address of characters
19: Loop
0x00000018 E59F109C LDR R1,[PC,#0x009C]
QUIZ1.s
19 Loop
20 LDRB r0, [r1],#1 ; load character, increment address
21 CMP r0,#0 ; null terminated?
22 BLNE Transmit ; send character to UART
23 BNE Loop ; continue if not a '0'
24
25 LDR r1, = CharData ; starting address of characters
26 MOV r5, #1
27 Loop1
28 LDRB r0, [r1], r5 ; load character, increment address
29 ADD r5, #1
30 CMP r0,#0 ; null terminated?
31 BLNE Transmit ; send character to UART
32 BNE Loop1 ; continue if not a '0'
33
34 done B done ; otherwise we e done
35
36 ; Subroutine UARTConfig
37 ; This subroutine configures the I/O pins first. It
38 ; then sets up the UART control register. The
Universal Asynchronous Receive Transmit 0 (UART0)
Line Control
U0LCR: 0x0B
Word Length: 8 bits
Stop Bits: 1
Parity: Odd Parity
DLAB
Break Control
Parity Enable
Line Status
U0LSR: 0x60
Receiver Data Ready (RDR)
Overrun Error (OE)
Parity Error (PE)
Framing Error (FE)
Break Interrupt (BI)
Tx Holding Register Empty (THRE)
Transmitter Empty (TEMT)
Error in Rx FIFO (RXFE)
Interrupt Enable
U0IER: 0x00
RBR IE
THRE IE
Rx Line Status IE
Interrupt ID & FIFO Control
U0IIR/FCR: 0x01
FIFO Enable
Interrupt: None
Rx Trigger: Level 0 (1)
Rx FIFO Reset
Tx FIFO Reset
Divisor Latch
U0DLL: 0x68
U0DLM: 0x00
Baudrate: 1802
Receiver & Transmitter Registers
U0RBR/THR: 0x00
Scratch Pad Register
U0SCR: 0x00
Command
Running with Code Size Limit: 32K
Load "F:\\03.淡江碩士\\01.碩一(112)\\02.碩一下學期\\07.微處理機概論(電資)(助教課)\\
ASSIGN BreakDisable BreakEnable BreakKill BreakList BreakSet BreakAccess COVERAGE
UART #1
TKU-ECE612450097TK-E47
Call Stack + Locals
UART #1
Memory 1
Real-Time Agent: Not in target
Simulation
t1: 99.96813050 sec
L:18 C:1
CAP NUM SCRL OVR R/W

Q&A

Thanks for your attention !!