

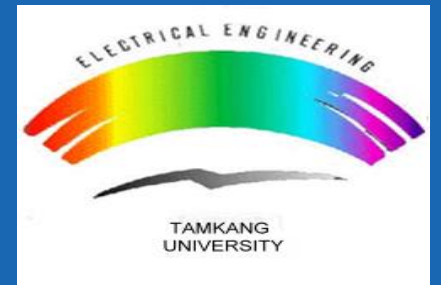
第09次實習課

學生：林培瑋

2024 Advanced Mixed-Operation System (AMOS) Lab.



Tamkang University
Department of Electrical and Computer Engineering
No.151, Yingzhuan Rd., Tamsui Dist., New Taipei City 25137, Taiwan (R.O.C.)

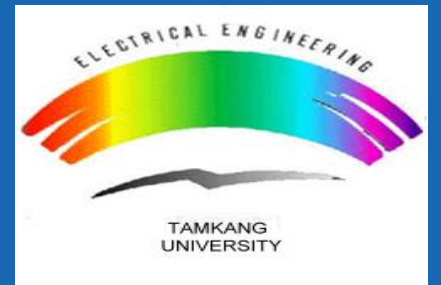


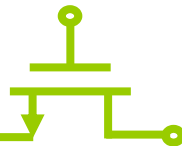
第一次作業

2024 Advanced Mixed-Operation System (AMOS) Lab.



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❖ 第一部分(60%)：

- 第1題(20%)：輸出正確，並包含F5、F10、F11執行結果&心得。
- 第2題(20%)：輸出正確反向字串，並包含F5、F10、F11執行結果(&心得)。
- 第3題(20%)：UART0視窗顯示大約9600 baud。

❖ 第二部分(40%)：

- 加入Receive(20%)：(F5、)F10、F11執行結果&心得。
- 加入三種錯誤偵測(20%)：(F5、)F10、F11執行結果(&心得)。

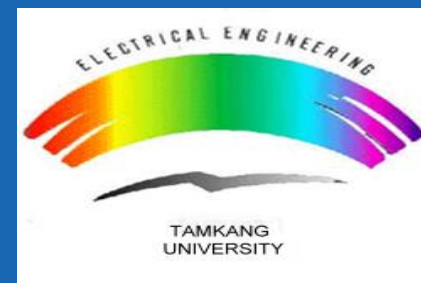
- 不計分：截圖中**看不到學號、姓名**。
- 一半分數：截圖不完整、心得不完整。
- 以最後繳交的版本為準。
- 遲交者分數 = 原始分數*0.5

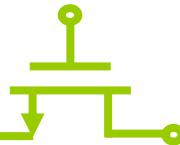
第一次作業-UART初始化

2024 Advanced Mixed-Operation System (AMOS) Lab.



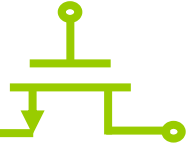
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P. W. LIN

設定資料傳輸格式(DLAB=1)



Register	Value
R0	0x00000000
R1	0x00000000
R2	0x00000000
R3	0x00000000
R4	0x00000000
R5	0xE000C000
R6	0x00000083
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x4000000C
R14 (LR)	0x00000008
R15 (PC)	0x00000044
CPSR	0x000000D3
SFSR	0x00000000

- UserSystem
- Fast Interrupt
- Interrupt
- Supervisor
- About
- Undefined
- Internal
 - PC \$ 0x00000044
 - Mode Supervisor
 - States 26
 - Sec 0.00000217

```

42:      MOV     r6, #0x61      ; 9600 baud @15 MHz VPB clock
0x00000044 E3A06061 MOV     R6,#0x00000061
43:      STRB    r6, [r5]      ; store control byte
0x00000048 F5C56000 STRB    R6,[R5]

```

```

32 UARTConfig
33      STMIA    sp!, {r5,r6,lr}
34      LDR     r5, = PINSEL0  ; base address of register
35      LDR     r6, [r5]      ; get contents
36      BIC     r6, r6, #0xF   ; clear out lower nibble
37      ORR     r6, r6, #0x5   ; sets P0.0 to Tx0 and P0.1 to Rx0
38      STR     r6, [r5]      ; r/modify/w back to register
39      LDR     r5, = U0START
40      MOV     r6, #0x83      ; set 8 bits, no parity, 1 stop bit
41      STRB    r6, [r5, #LCR0] ; write control byte to LCR
42      MOV     r6, #0x61      ; 9600 baud @15 MHz VPB clock
43      STRB    r6, [r5]      ; store control byte
44      MOV     r6, #3         ; set DLAB = 0
45      STRB    r6, [r5, #LCR0] ; Tx and Rx buffers set up
46      LDMDMB  sp!, {r5,r6,pc}
47
48 ; Subroutine Transmit
49 ; This routine puts one byte into the UART
50 ; for transmitting.
51 ; Register used:
52 ; r5 - scratch
53 ; r6 - scratch
54 ; inputs: r0- byte to transmit
55 ; outputs: none
56 ;
57
58 Transmit
59      STMIA    sp!, {r5, r6, lr}
60      LDR     r5, = U0START
61 wait   LDRB    r6, [r5, #LSR0] ; get status of buffer
62      TST     r6, #0x20      ; buffer empty?
63      BEQ     wait          ; spin until buffer's empty
64      STRB    r0, [r5]
65      LDMDMB  sp!, {r5, r6, pc}

```

Line Control

U0LCR: 0x83

Word Length: 8 bits

Stop Bits: 1

Parity: Odd Parity

☒ DLAB
☐ Break Control
☐ Parity Enable

Line Status

U0LSR: 0x60

☐ Receiver Data Ready (RDR)
☐ Overrun Error (OE)
☐ Parity Error (PE)
☐ Framing Error (FE)
☐ Break Interrupt (BI)
☒ Tx Holding Register Empty (THRE)
☒ Transmitter Empty (TEMT)
☐ Error in Rx FIFO (RXFE)

Interrupt Enable

U0IER: 0x00

☐ RBR IE
☐ THRE IE
☐ Rx Line Status IE

Interrupt ID & FIFO Control

U0IIR/FCR: 0x01

☐ FIFO Enable

Interrupt: None

Rx Trigger: Level 0 (1)

☐ Rx FIFO Reset ☐ Tx FIFO Reset

Divisor Latch

U0DLL: 0x01

U0DLM: 0x00

Baudrate: 187500

Receiver & Transmitter Registers

U0RBR/THR: 0x00

Scratch Pad Register

U0SCR: 0x00

Command

Running with Code Size Limit: 32K

Load "F:\03.淡江碩士\01.碩一(112)\02.碩一下學期\07.微處理機概論(電資)(助教課)\04.作業\第01次作業\02.解答\HW1_1.s"

Memory 1

Address: 0xE000C00C

0xE000C00C:	83 00 00 00 00 00 00 00 60 00
0xE000C00E:	00 00 80 00
0xE000C050:	00 00
0xE000C072:	00 00
0xE000C094:	00 00
0xE000C0B6:	00 00
0xE000C0D8:	00 00
0xE000C0FA:	00 00
0xE000C11C:	00 00

Project

Registers

Command

Running with Code Size Limit: 32K

Load "F:\03.淡江碩士\01.碩一(112)\02.碩一下學期\07.微處理機概論(電資)(助教課)\04.作業\第01次作業\02.解答\HW1_1.s"

Memory 1

Address: 0xE000C00C

0xE000C00C:	83 00 00 00 00 00 00 00 60 00
0xE000C00E:	00 00 80 00
0xE000C050:	00 00
0xE000C072:	00 00
0xE000C094:	00 00
0xE000C0B6:	00 00
0xE000C0D8:	00 00
0xE000C0FA:	00 00
0xE000C11C:	00 00

Project

Registers

Command

Running with Code Size Limit: 32K

Load "F:\03.淡江碩士\01.碩一(112)\02.碩一下學期\07.微處理機概論(電資)(助教課)\04.作業\第01次作業\02.解答\HW1_1.s"

Memory 1

Address: 0xE000C00C

0xE000C00C:	83 00 00 00 00 00 00 00 60 00
0xE000C00E:	00 00 80 00
0xE000C050:	00 00
0xE000C072:	00 00
0xE000C094:	00 00
0xE000C0B6:	00 00
0xE000C0D8:	00 00
0xE000C0FA:	00 00
0xE000C11C:	00 00

Project

Registers

Command

Running with Code Size Limit: 32K

Load "F:\03.淡江碩士\01.碩一(112)\02.碩一下學期\07.微處理機概論(電資)(助教課)\04.作業\第01次作業\02.解答\HW1_1.s"

Memory 1

Address: 0xE000C00C

0xE000C00C:	83 00 00 00 00 00 00 00 60 00
0xE000C00E:	00 00 80 00
0xE000C050:	00 00
0xE000C072:	00 00
0xE000C094:	00 00
0xE000C0B6:	00 00
0xE000C0D8:	00 00
0xE000C0FA:	00 00
0xE000C11C:	00 00

Project

Registers

Command

Running with Code Size Limit: 32K

Load "F:\03.淡江碩士\01.碩一(112)\02.碩一下學期\07.微處理機概論(電資)(助教課)\04.作業\第01次作業\02.解答\HW1_1.s"

Memory 1

Address: 0xE000C00C

0xE000C00C:	83 00 00 00 00 00 00 00 60 00
0xE000C00E:	00 00 80 00
0xE000C050:	00 00
0xE000C072:	00 00
0xE000C094:	00 00
0xE000C0B6:	00 00
0xE000C0D8:	00 00
0xE000C0FA:	00 00
0xE000C11C:	00 00

Project

Registers

Command

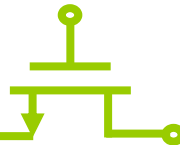
Running with Code Size Limit: 32K

Load "F:\03.淡江碩士\01.碩一(112)\02.碩一下學期\07.微處理機概論(電資)(助教課)\04.作業\第01次作業\02.解答\HW1_1.s"

Memory 1

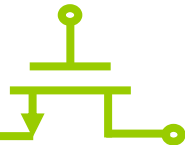
Address: 0xE000C00C

0xE000C00C:	83 00 00 00 00 00 00 00 60 00
0xE000C00E:	00 00 80 00
0xE000C050:	00 00
0xE000C072:	00 00
0xE000C094:	00 00
0xE000C0B6:	00 00
0xE000C0D8:	00 00
0xE000C0FA:	00 00
0xE000C11C:	00 00



P. W. LIN

設為Receive/Transmit功能(DLAB=0)



Register	Value
R0	0x00000000
R1	0x00000000
R2	0x00000000
R3	0x00000000
R4	0x00000000
R5	0xE000C000
R6	0x00000003
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x4000000C
R14 (LR)	0x00000008
R15 (PC)	0x00000054
CPSR	0x000000D3
SFPR	0x00000000
PC \$	0x00000054
Mode	Supervisor
States	32
Sec	0.00000267

```

46:          LDMDB  sp!, {r5,r6,pc}
47:
48: ; Subroutine Transmit
49: ; This routine puts one byte into the UART

HW1_1_1.s
36      BIC      r6, r6, #0xF ; clear out lower nibble
37      ORR      r6, r6, #0x5 ; sets P0.0 to Tx0 and P0.1 to Rx0
38      STR      r6, [r5] ; r/modify/w back to register
39      LDR      r5, =U0START
40      MOV      r6, #0x83 ; set 8 bits, no parity, 1 stop bit
41      STRB     r6, [r5, #LCR0] ; write control byte to LCR
42      MOV      r6, #0x61 ; 9600 baud @15 MHz VFB clock
43      STRB     r6, [r5] ; store control byte
44      MOV      r6, #3 ; set DLAB = 0
45      STRB     r6, [r5, #LCR0] ; Tx and Rx buffers set up
46      LDMDB   sp!, {r5,r6,pc}
47
48 ; Subroutine Transmit
49 ; This routine puts one byte into the UART
50 ; for transmitting.
51 ; Register used:
52 ; r5 - scratch
53 ; r6 - scratch
54 ; inputs: r0- byte to transmit
55 ; outputs: none
56 ;
57
58 Transmit
59      STMIA     sp!, {r5, r6, lr}
60      LDR      r5, =U0START
61 wait   LDRB     r6, [r5, #LSR0] ; get status of buffer
62      TST      r6, #0x20 ; buffer empty?
63      BEQ      wait ; spin until buffer's empty
64      STRB     r0, [r5]
65      LDMDB   sp!, {r5, r6, pc}
66 CharData
67      DCB      "TKU-ECE612450097",0
68      END

```

Line Control

U0LCR: 0x03

Word Length: 8 bits

Stop Bits: 1

Parity: Odd Parity

☐ DLAB
 ☐ Break Control
 ☐ Parity Enable

Interrupt Enable

U0IER: 0x00

☐ RBR IE
 ☐ THRE IE
 ☐ Rx Line Status IE

Divisor Latch

U0DLL: 0x61

U0DLM: 0x00

Baudrate: 1932

Line Status

U0LSR: 0x60

☐ Receiver Data Ready (RDR)
 ☐ Overrun Error (OE)
 ☐ Parity Error (PE)
 ☐ Framing Error (FE)
 ☐ Break Interrupt (BI)
 ☒ Tx Holding Register Empty (THRE)
 ☒ Transmitter Empty (TEMT)
 ☐ Error in Rx FIFO (RXFE)

Interrupt ID & FIFO Control

U0IIR/FCR: 0x01

☐ FIFO Enable

Interrupt: None

Rx Trigger: Level 0 (1)

☐ Rx FIFO Reset
 ☐ Tx FIFO Reset

Receiver & Transmitter Registers

U0RBR/THR: 0x00

Scratch Pad Register

U0SCR: 0x00

Command

Running with Code Size Limit: 32K

Load "F:\03.淡江碩士\01.碩一(112)\02.碩一下學期\07.微處理機概論(電資)(助教課)\04.作業\第01次作業\02.解答\HW1_1.s"

ASSIGN BreakDisable BreakEnable BreakKill BreakList BreakSet BreakAccess COVERAGE COVTOFILE DEFINE DIR Display Enter

Memory 1

Address: 0xE000C00C

0xE000C00C:	03 00 00 00 00 00 00 00 60 00
0xE000C00E:	00 00 80 00
0xE000C010:	00 00
0xE000C012:	00 00
0xE000C014:	00 00
0xE000C016:	00 00
0xE000C018:	00 00
0xE000C01A:	00 00
0xE000C01C:	00 00

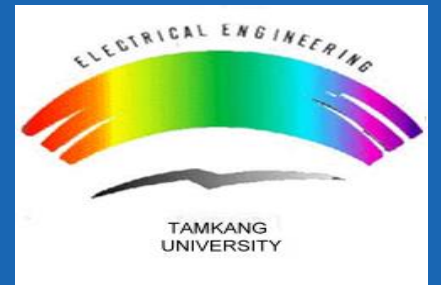
Call Stack + Locals | UART #1 | Memory 1

第一次作業-第一部分

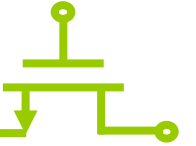
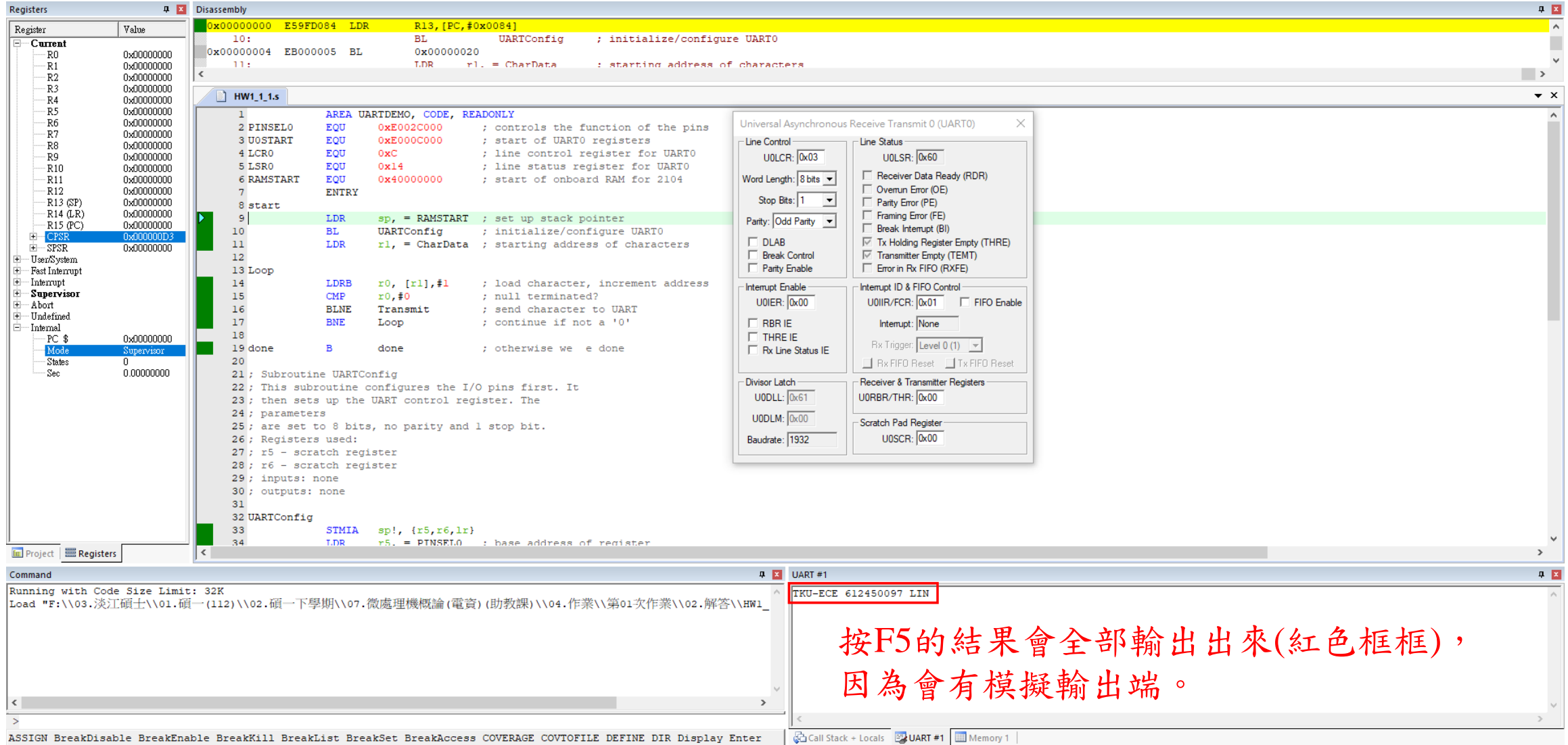
2024 Advanced Mixed-Operation System (AMOS) Lab.



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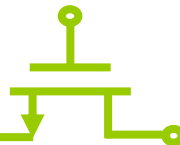
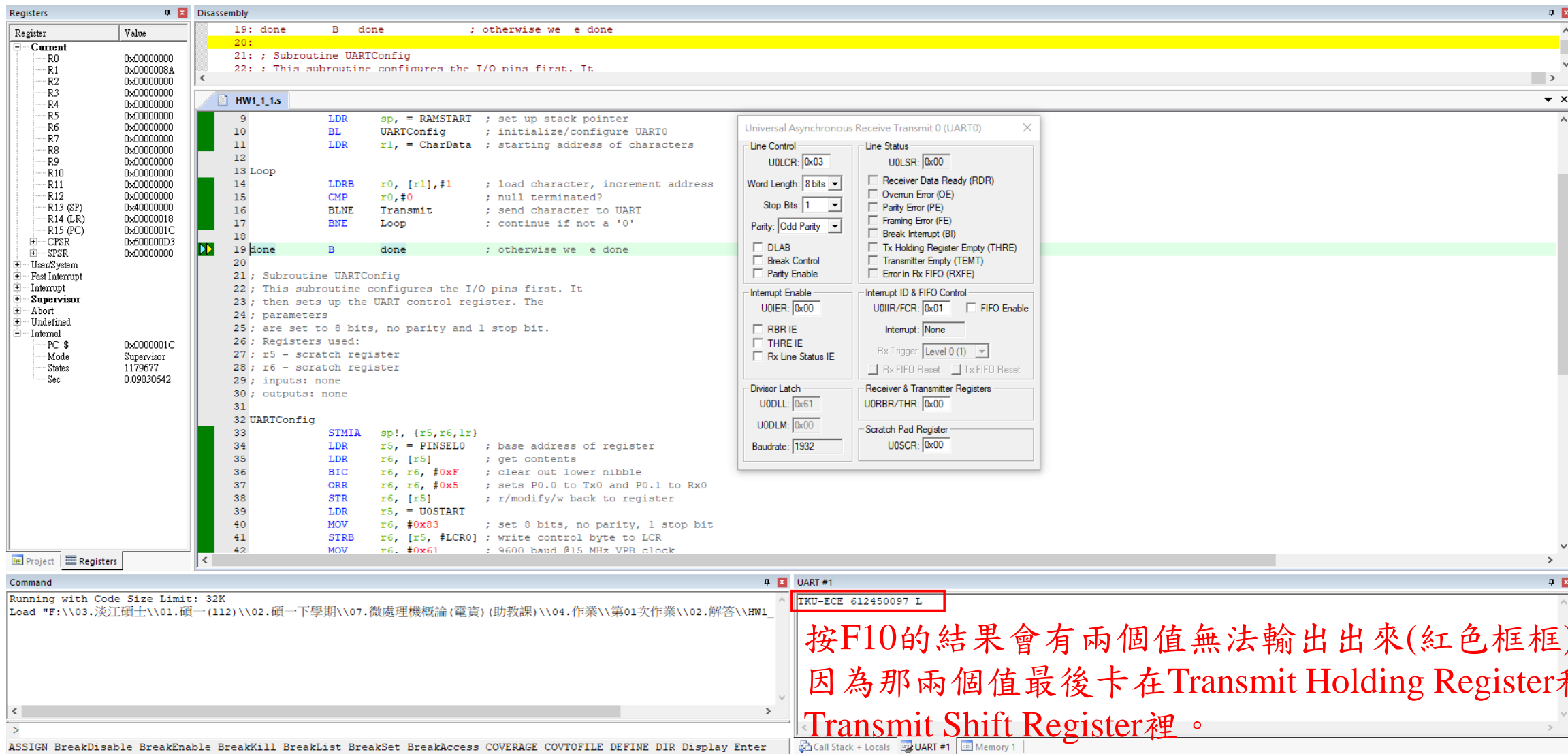


執行心得-1(F5)

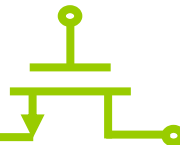
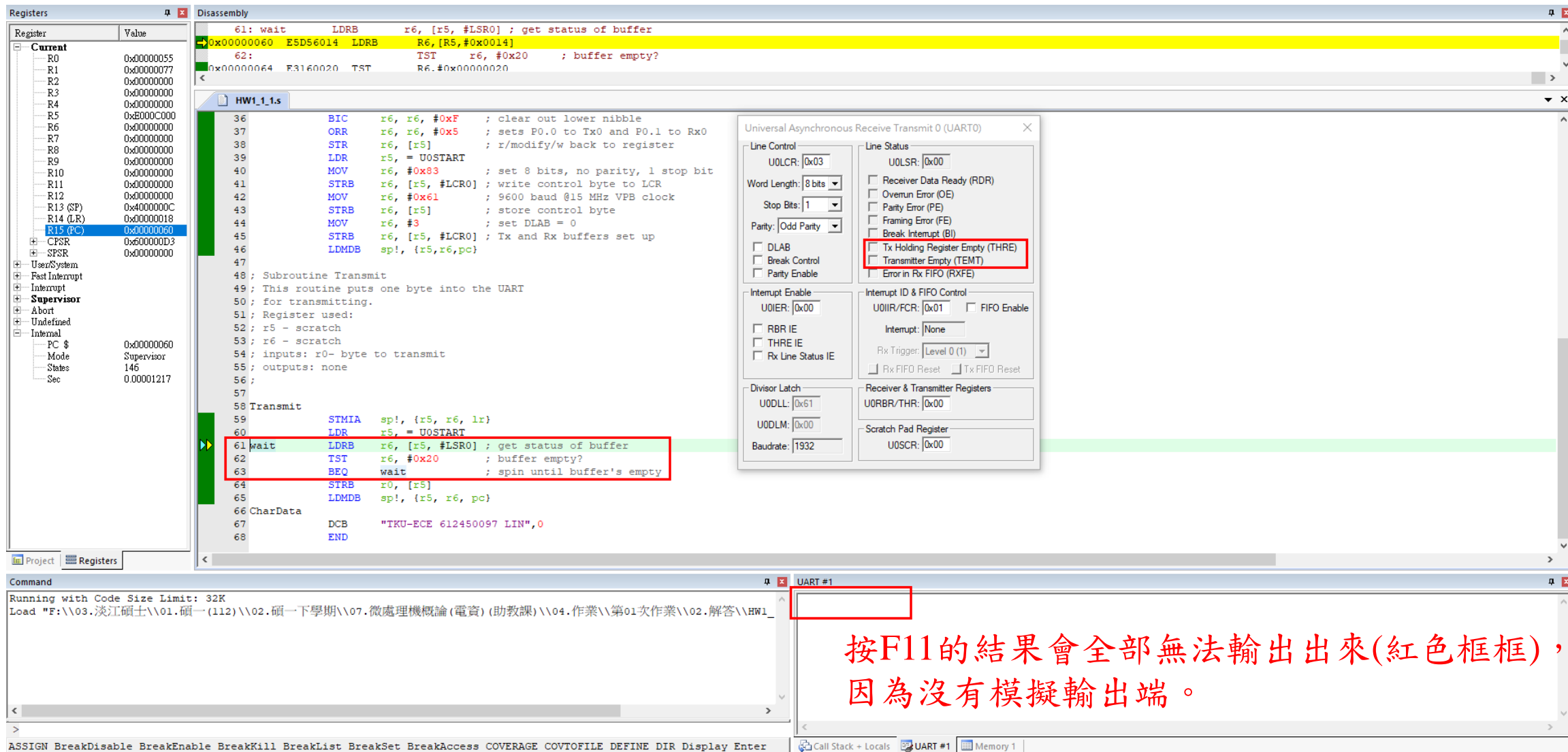
The screenshot displays the Keil uVision IDE interface during a simulation. The main window shows assembly code for a program named 'HW1_1.s'. The code includes comments and instructions for initializing UART0, setting up a stack pointer, and a loop for transmitting characters. The 'Registers' window on the left shows the current state of registers, with R10, R11, R12, R13, R14, and R15 all set to 0x00000000. The 'Universal Asynchronous Receive Transmitt 0 (UART0)' configuration window is open, showing settings for Line Control (U0LCR: 0x03), Line Status (U0LSR: 0x60), Word Length (8 bits), Stop Bits (1), Parity (Odd Parity), and various interrupt and FIFO controls. The 'Command' window at the bottom shows the command 'Running with Code Size Limit: 32K' and the file path 'Load "F:\03.淡江碩士\01.碩一(112)\02.碩一下學期\07.微處理機概論(電資)(助教課)\04.作業\第01次作業\02.解答\HW1_1.s"'. The 'UART #1' window shows the output 'TKU-ECE 612450097 LIN', which is highlighted with a red box.

按F5的結果會全部輸出出來(紅色框框)，
因為會有模擬輸出端。

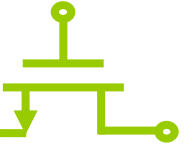
The screenshot displays the Keil uVision IDE interface during a simulation. The main window shows assembly code for a subroutine named `UARTConfig`, which configures the UART0 peripheral. The code includes instructions for setting the stack pointer, initializing the UART control register, and configuring the baud rate and parity. The `Registers` window on the left shows the current state of the processor registers, including the Program Counter (PC) at `0x0000001C`. The `Universal Asynchronous Receive Transmitt 0 (UART0)` configuration window is open, showing settings for line control, line status, interrupt enable, and divisor latch. The `Command` window at the bottom shows the command prompt, and the `UART #1` window displays the output of the UART, with two values highlighted in red boxes: `TKU-ECE 612450097 L`.

按F10的結果會有兩個值無法輸出出來(紅色框框)，因為那兩個值最後卡在Transmit Holding Register和Transmit Shift Register裡。

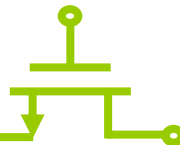



The screenshot displays the Keil uVision IDE interface during a simulation. The main window shows assembly code for a routine named 'Transmit'. The code includes instructions like 'LDRB r6, [r5, #LSR0]' and 'TST r6, #0x20'. A red box highlights lines 61-63, which are part of a 'wait' loop. The 'Registers' window on the left shows the current state of registers, with R15 (PC) highlighted. The 'Universal Asynchronous Receive Transmitt 0 (UART0)' configuration window is open, showing settings for 'Line Control' and 'Line Status'. The 'Line Status' section has 'Tx Holding Register Empty (THRE)' and 'Transmitter Empty (TEMT)' checked, indicated by a red box. The 'Command' window at the bottom shows the command 'F11' being executed. A red box highlights the 'UART #1' window, which is currently empty.

按F11的結果會全部無法輸出出來(紅色框框)，因為沒有模擬輸出端。



與第一部分相同。



Register	Value
R0	0x000000E9
R1	0x0000007E
R2	0xFFFFFFFF
R3	0x00000000
R4	0x00000000
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x40000000
R14 (LR)	0x00000024
R15 (PC)	0x00000028
CPSR	0xA00000D3
SFSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC	0x00000028
Mode	Supervisor
States	1179665
Sec	0.09830542

```

0x00000024 AFFFFFFA BGE 0x00000014
21: done B done ; otherwise we e done
22:
23: ; Subroutine UARTConfig
24: ; This subroutine configures the I/O pins first. It
25: ; then sets up the UART control register. The
26: ;
10 BL UARTConfig ; initialize/configure UART0
11 LDR r1, = CharData ; starting address of characters
12 LDR r2, =21
13 ADD r1, #20
14 Loop
15 LDRB r0, [r1], #-1 ; load character, increment address
16 SUB r2, #1
17 CMP r2, #0 ; null terminated?
18 BLGE Transmit ; send character to UART
19 BGE Loop ; continue if not a '0'
20
21 done B done ; otherwise we e done
22
23 ; Subroutine UARTConfig
24 ; This subroutine configures the I/O pins first. It
25 ; then sets up the UART control register. The
26 ; parameters
27 ; are set to 8 bits, no parity and 1 stop bit.
28 ; Registers used:
29 ; r5 - scratch register
30 ; r6 - scratch register
31 ; inputs: none
32 ; outputs: none
33
34 UARTConfig
35 STMIA sp!, {r5,r6,lr}
36 LDR r5, = PINSEL0 ; base address of register
37 LDR r6, [r5] ; get contents
38 BIC r6, r6, #0xF ; clear out lower nibble
39 ORR r6, r6, #0x5 ; sets P0.0 to Tx0 and P0.1 to Rx0
40 STR r6, [r5] ; r/modify/w back to register
41 LDR r5, = U0START
42 MOV r6, #0x33 ; set 8 bits, no parity, 1 stop bit
43 STRB r6, [r5, #LCR0] ; write control byte to LCR
44 MOV r6, #0x61 ; 9600 baud @15 MHz VPP clock

```

Line Control

U0LCR: 0x03

Word Length: 8 bits

Stop Bits: 1

Parity: Odd Parity

DLAB

Break Control

Parity Enable

Line Status

U0LSR: 0x00

Receiver Data Ready (RDR)

Overrun Error (OE)

Parity Error (PE)

Framing Error (FE)

Break Interrupt (BI)

Tx Holding Register Empty (THRE)

Transmitter Empty (TEMT)

Error in Rx FIFO (RXFE)

Interrupt Enable

U0IER: 0x00

RBR IE

THRE IE

Rx Line Status IE

Interrupt ID & FIFO Control

U0IIR/FCR: 0x01

FIFO Enable

Interrupt: None

Rx Trigger: Level 0 (1)

Rx FIFO Reset

Tx FIFO Reset

Divisor Latch

U0DLL: 0x61

U0DLM: 0x00

Baudrate: 1932

Receiver & Transmitter Registers

U0RRR/THR: 0x00

Scratch Pad Register

U0SCR: 0x00

Command

Running with Code Size Limit: 32K

Load "F:\03.淡江碩士\01.碩一(112)\02.碩一下學期\07.微處理機概論(電資)(助教課)\04.作業\第01次作業\02.解答\HW1

UART #1

NIL 790054216 ECE-U

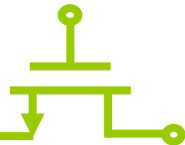
ASSIGN BreakDisable BreakEnable BreakKill BreakList BreakSet BreakAccess COVERAGE COVTOFILE DEFINE DIR Display Enter

Call Stack + Locals

UART #1

Memory 1

與第一部分相同。



Register	Value
R0	0x0000004C
R1	0x00000091
R2	0x00000012
R3	0x00000000
R4	0x00000000
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x4000000C
R14 (LR)	0x00000024
R15 (PC)	0x00000074
CPSR	0x500000D3
SFPR	0x00000000

User/System
Fast Interrupt
Interrupt
Supervisor
Abort
Undefined
Internal

PC \$ 0x00000074
Mode Supervisor
States 176
Sec 0.00001467

```

63: wait    LDRB    r6, [r5, #LSR0] ; get status of buffer
0x0000006C E5D56014 LDRB    R6, [R5, #0x0014]
64:        TST     r6, #0x20      ; buffer empty?
0x00000070 E3160020 TST     R6, #0x00000020
65:        BEQ     wait          ; spin until buffer's empty
0x00000074 0AFFFFFC BEQ     0x0000006C

```

```

37      LDR     r6, [r5]      ; get contents
38      BIC     r6, r6, #0xF   ; clear out lower nibble
39      ORR     r6, r6, #0x5    ; sets P0.0 to Tx0 and P0.1 to Rx0
40      STR     r6, [r5]      ; r/modify/w back to register
41      LDR     r5, =U0START
42      MOV     r6, #0x83      ; set 8 bits, no parity, 1 stop bit
43      STRB    r6, [r5, #LCR0] ; write control byte to LCR
44      MOV     r6, #0x61      ; 9600 baud @15 MHz VPB clock
45      STRB    r6, [r5]      ; store control byte
46      MOV     r6, #3         ; set DLAB = 0
47      STRB    r6, [r5, #LCR0] ; Tx and Rx buffers set up
48      LDMDMB  sp!, {r5, r6, pc}
49
50 ; Subroutine Transmit
51 ; This routine puts one byte into the UART
52 ; for transmitting.
53 ; Register used:
54 ; r5 - scratch
55 ; r6 - scratch
56 ; inputs: r0- byte to transmit
57 ; outputs: none
58 ;
59
60 Transmit
61      STMIA    sp!, {r5, r6, lr}
62      LDR     r5, =U0START
63 wait    LDRB    r6, [r5, #LSR0] ; get status of buffer
64        TST     r6, #0x20      ; buffer empty?
65        BEQ     wait          ; spin until buffer's empty
66      STRB    r0, [r5]
67      LDMDMB  sp!, {r5, r6, pc}
68 CharData
69      DCB     "TKU-ECE 612450097 LIN", 0
70      END

```

Line Control

U0LCR: 0x03

Word Length: 8 bits

Stop Bits: 1

Parity: Odd Parity

☐ DLAB
☐ Break Control
☐ Parity Enable

Interrupt Enable

U0IER: 0x00

☐ RBR IE
☐ THRE IE
☐ Rx Line Status IE

Divisor Latch

U0DLL: 0x61

U0DLM: 0x00

Baudrate: 1932

Line Status

U0LSR: 0x00

☐ Receiver Data Ready (RDR)
☐ Overrun Error (OE)
☐ Parity Error (PE)
☐ Framing Error (FE)
☐ Break Interrupt (BI)

☐ Tx Holding Register Empty (THRE)
☐ Transmitter Empty (TEMT)
☐ Error in Rx FIFO (RXFE)

Interrupt ID & FIFO Control

U0IIR/FCR: 0x01

☐ FIFO Enable

Interrupt: None

Rx Trigger: Level 0 (1)

☐ Rx FIFO Reset ☐ Tx FIFO Reset

Receiver & Transmitter Registers

U0RBR/THR: 0x00

Scratch Pad Register

U0SCR: 0x00

Command

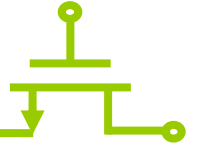
Running with Code Size Limit: 32K

Load "F:\03.淡江碩士\01.碩一(112)\02.碩一下學期\07.微處理機概論(電資)(助教課)\04.作業\第01次作業\02.解答\HW1

ASSIGN BreakDisable BreakEnable BreakKill BreakList BreakSet BreakAccess COVERAGE COVTOFILE DEFINE DIR Display Enter

Call Stack + Locals
UART #1
Memory 1

與第一部分相同。



Register	Value
R0	0x00000000
R1	0x00000000
R2	0x00000000
R3	0x00000000
R4	0x00000000
R5	0xE000C000
R6	0x00000013
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x4000000C
R14 (LR)	0x00000008
R15 (PC)	0x0000004C
CPSR	0x000000D3
SPSR	0x00000000
UserSystem	
Fast Interrupt	
Interrupt	
Supervisor	
About	
Undefined	
Internal	
PC \$	0x0000004C
Mode	29
States	
Sec	0.00000242

```

0x00000044 E3A06013 MOV R6,#0x00000013
43: STRB r6, [r5] ; store control byte
0x00000048 E5C56000 STRB R6,[R5]
44: MOV r6, #3 ; set DLAB = 0
0x0000004C E3A06003 MOV R6,#0x00000003
45: STRB r6, [r5, #LCR0] ; Tx and Rx buffers set up
0x00000050 E5C56000 STRB R6,[R5, #LCR0]

HW1_1.3.s
32 UARTConfig
33 STMIA sp!, {r5, r6, lr}
34 LDR r5, = PINSEL0 ; base address of register
35 LDR r6, [r5] ; get contents
36 BIC r6, r6, #0xF ; clear out lower nibble
37 ORR r6, r6, #0x5 ; sets P0.0 to Tx0 and P0.1 to Rx0
38 STR r6, [r5] ; r/modify/w back to register
39 LDR r5, = UOSTART
40 MOV r6, #0x83 ; set 8 bits, no parity, 1 stop bit
41 STRB r6, [r5, #LCR0] ; write control byte to LCR
42 MOV r6, #0x13 ; 9600 baud @16 MHz VPB clock
43 STRB r6, [r5] ; store control byte
44 MOV r6, #3 ; set DLAB = 0
45 STRB r6, [r5, #LCR0] ; Tx and Rx buffers set up
46 LDMDB sp!, {r5, r6, pc}
47
48 ; Subroutine Transmit
49 ; This routine puts one byte into the UART
50 ; for transmitting.
51 ; Register used:
52 ; r5 - scratch
53 ; r6 - scratch
54 ; inputs: r0- byte to transmit
55 ; outputs: none
56 ;
57
58 Transmit
59 STMIA sp!, {r5, r6, lr}
60 LDR r5, = UOSTART
61 wait LDRB r6, [r5, #LSR0] ; get status of buffer
62 TST r6, #0x20 ; buffer empty?

```

Line Control

U0LCR: 0x83

Word Length: 8 bits

Stop Bits: 1

Parity: Odd Parity

☒ DLAB
 ☐ Break Control
 ☐ Parity Enable

Interrupt Enable

U0IER: 0x00

☐ RBR IE
 ☐ THRE IE
 ☐ Rx Line Status IE

Divisor Latch

U0DLL: 0x13

U0DLM: 0x00

Baudrate: 9600

Line Status

U0LSR: 0x60

☐ Receiver Data Ready (RDR)
 ☐ Overrun Error (OE)
 ☐ Parity Error (PE)
 ☐ Framing Error (FE)
 ☐ Break Interrupt (BI)

☒ Tx Holding Register Empty (THRE)
 ☒ Transmitter Empty (TEMT)
 ☐ Error in Rx FIFO (RXFE)

Interrupt ID & FIFO Control

U0IIR/FCR: 0x01 ☐ FIFO Enable

Interrupt: None

Rx Trigger: Level 0 (1)

☐ Rx FIFO Reset
 ☐ Tx FIFO Reset

Receiver & Transmitter Registers

U0RRR/THR: 0x00

Scratch Pad Register

U0SCR: 0x00

小算盤

程式設計人員

97 × 16 × 1932 =

2,998,464

HEX 2D C0C0

DEC 2,998,464

OCT 13 340 300

BIN 0010 1101 1100 0000 1100 0000

QWORD MS Mv

位元 位元移位

A << >> CE <X>

B () % ÷

C 7 8 9 ×

D 4 5 6 -

E 1 2 3 +

F %/ 0 . =

小算盤

程式設計人員

2998464 ÷ 9600 × 16 =

19

HEX 13

DEC 19

OCT 23

BIN 0001 0011

QWORD MS Mv

位元 位元移位

A << >> CE <X>

B () % ÷

C 7 8 9 ×

D 4 5 6 -

E 1 2 3 +

F %/ 0 . =

Command

Running with Code Size Limit: 32K

Load "F:\03.淡江碩士\01.碩一(112)\02.碩一下學期\07.微處理機概論(電資)(助教課)\04.作業\第01次作業\02.解答\HW1_1.3.s"

ASSIGN BreakDisable BreakEnable BreakKill BreakList BreakSet BreakAccess COVTOFILE DEFINE DIR Display Enter

Memory 1

Address:

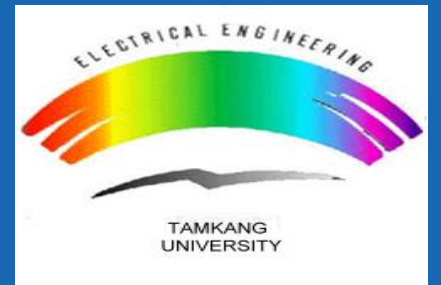
Call Stack + Locals UART #1 Memory 1

第一次作業-第二部分

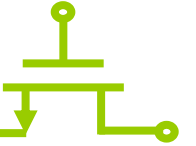
2024 Advanced Mixed-Operation System (AMOS) Lab.



Tamkang University
Department of Electrical and Computer Engineering
No.151, Yingzhuan Rd., Tamsui Dist., New Taipei City 25137, Taiwan (R.O.C.)



執行心得-加入Receive(F5)



Register	Value
R0	0x00000000
R1	0x00000000
R2	0x00000000
R3	0x00000000
R4	0x00000000
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000000
CPSR	0x00000003
SFSR	0x00000000

UserSystem

Fast Interrupt

Interrupt

Supervisor

About

Undefined

Internal

PC \$

Mode Supervisor

States 0

Sec 0.00000000

HW1_2_1.s

```

1  AREA UARTDEMO, CODE, READONLY
2  PINSEL0 EQU 0xE002C000 ; controls the function of the pins
3  UOSTART EQU 0xE000C000 ; start of UART0 registers
4  LCR0 EQU 0xC ; line control register for UART0
5  LSR0 EQU 0x14 ; line status register for UART0
6  RAMSTART EQU 0x10000000 ; start of onboard RAM for 2104
7
8  ENTRY
9  start
10 LDR sp, = RAMSTART ; set up stack pointer
11 BL UARTConfig ; initialize/configure UART0
12 LDR r1, = CharData ; starting address of characters
13 Loop
14 LDRB r0, [r1], #1 ; load character, increment address
15 CMP r0, #0 ; null terminated?
16 BLNE Transmit ; send character to UART
17 BNE Loop ; continue if not a '0'
18
19 MOV r9, #20
20 Loop1
21 BL Receive
22 STRB r0, [r1], #1
23 SUBS r9, r9, #1
24 BNE Loop1
25
26 done B done ; otherwise we e done
27
28 ; Subroutine UARTConfig
29 ; This subroutine configures the I/O pins first. It
30 ; then sets up the UART control register. The
31 ; parameters
32 ; are set to 8 bits, no parity and 1 stop bit.
33 ; Registers used:
34 ; r5 - scratch register
35 ; r6 - scratch register

```

Universal Asynchronous Receive Transmit 0 (UART0)

Line Control

U0LCR: 0x03

Word Length: 8 bits

Stop Bits: 1

Parity: Odd Parity

DLAB

Break Control

Parity Enable

Line Status

U0LSR: 0x60

Receiver Data Ready (RDR)

Overrun Error (OE)

Parity Error (PE)

Framing Error (FE)

Break Interrupt (BI)

Tx Holding Register Empty (THRE)

Transmitter Empty (TEMT)

Error in Rx FIFO (RXFE)

Interrupt Enable

U0IER: 0x00

RBR IE

THRE IE

Rx Line Status IE

Interrupt ID & FIFO Control

U0IIR/FCR: 0x01

FIFO Enable

Interrupt: None

Rx Trigger: Level 0 (1)

Rx FIFO Reset

Tx FIFO Reset

Divisor Latch

U0DLL: 0x61

U0DLM: 0x00

Baudrate: 1932

Receiver & Transmitter Registers

U0RBR/THR: 0x00

Scratch Pad Register

U0SCR: 0x00

Command

Running with Code Size Limit: 32K

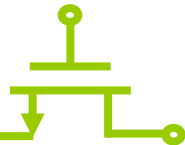
Load "F:\03.淡江碩士\01.碩一(112)\02.碩一下學期\07.微處理機概論(電資)(助教課)\04.作業\第01次作業\02.解答\HW1

UART #1

TKU-ECE 612450097 LIN

按F5的結果會全部輸出出來(紅色框框)，
但最後卡在Receive無窮迴圈，
因為PDR值都為0。

執行心得-加入Receive(F10)



Registers

Register	Value
R0	0x00000000
R1	0x000000BA
R2	0x00000000
R3	0x00000000
R4	0x00000000
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000014
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000018
R15 (PC)	0x00000020
CPSR	0x000000D3
SFSR	0x00000000
UserSystem	
Fast Interrupt	
Interrupt	
Supervisor	
About	
Undefined	
Internal	
PC \$	0x00000020
Supervisor	1179612
States	
Sec	0.09830100

Disassembly

```

0x00000018 1AFFFFFF BNE      0x0000000C
19:          MOV r9, #20
0x0000001C E3A09014 MOV      R9,#0x00000014
21:          BL Receive
0x00000020 EB000018 BL       0x00000088
22:          STPB r0, [r1], #1
23:          SUBS r9, r9, #1
24:          BNE Loop1
25:          MOV r9, #20
26 done     B        done ; otherwise we e done
27
28 ; Subroutine UARTConfig
29 ; This subroutine configures the I/O pins first. It
30 ; then sets up the UART control register. The
31 ; parameters
32 ; are set to 8 bits, no parity and 1 stop bit.
33 ; Registers used:
34 ; r5 - scratch register
35 ; r6 - scratch register
36 ; inputs: none
37 ; outputs: none
38
39 UARTConfig
40          STMIA sp!, {r5,r6,lr}
41          LDR r5, = PINSEL0 ; base address of register
42          LDR r6, [r5] ; get contents
43          BIC r6, r6, #0xF ; clear out lower nibble
44          ORR r6, r6, #0x5 ; sets P0.0 to Tx0 and P0.1 to Rx0
    
```

HW1_2.1.s

```

10          BL      UARTConfig ; initialize/configure UART0
11          LDR      r1, = CharData ; starting address of characters
12
13 Loop
14          LDRB     r0, [r1], #1 ; load character, increment address
15          CMP      r0, #0 ; null terminated?
16          BLNE     Transmit ; send character to UART
17          BNE      Loop ; continue if not a '0'
18
19          MOV r9, #20
20 Loop1
21          BL Receive
22          STPB r0, [r1], #1
23          SUBS r9, r9, #1
24          BNE Loop1
25
26 done     B        done ; otherwise we e done
27
28 ; Subroutine UARTConfig
29 ; This subroutine configures the I/O pins first. It
30 ; then sets up the UART control register. The
31 ; parameters
32 ; are set to 8 bits, no parity and 1 stop bit.
33 ; Registers used:
34 ; r5 - scratch register
35 ; r6 - scratch register
36 ; inputs: none
37 ; outputs: none
38
39 UARTConfig
40          STMIA sp!, {r5,r6,lr}
41          LDR r5, = PINSEL0 ; base address of register
42          LDR r6, [r5] ; get contents
43          BIC r6, r6, #0xF ; clear out lower nibble
44          ORR r6, r6, #0x5 ; sets P0.0 to Tx0 and P0.1 to Rx0
    
```

Universal Asynchronous Receive Transmit 0 (UART0)

Line Control: U0LCR: 0x03

Word Length: 8 bits

Stop Bits: 1

Parity: Odd Parity

Line Status: U0LSR: 0x60

☒ Receiver Data Ready (RDR)

☐ Overrun Error (OE)

☐ Parity Error (PE)

☐ Framing Error (FE)

☐ Break Interrupt (BI)

☒ Tx Holding Register Empty (THRE)

☒ Transmitter Empty (TEMT)

☐ Error in Rx FIFO (RXFE)

Interrupt Enable: U0IER: 0x00

☐ RBR IE

☐ THRE IE

☐ Rx Line Status IE

Interrupt ID & FIFO Control: U0IIR/FCR: 0x01

☐ FIFO Enable

Interrupt: None

Rx Trigger: Level 0 (1)

☐ Rx FIFO Reset

☐ Tx FIFO Reset

Divisor Latch: U0DLL: 0x61

U0DLM: 0x00

Baudrate: 1932

Receiver & Transmitter Registers: U0RBR/THR: 0x00

Scratch Pad Register: U0SCR: 0x00

按F10的結果會全部輸出出來(紅色框框)，
因為重新存取LSR0暫存器，
使原本卡在THR、TSR的兩個字輸出出來。
但最後卡在Receive無窮迴圈，
因為PDR值都為0。

Command

Running with Code Size Limit: 32K

Load "F:\03.淡江碩士\01.碩一(112)\02.碩一下學期\07.微處理機概論(電資)(助教課)\04.作業\第01次作業\02.解答\HW1

ASSIGN BreakDisable BreakEnable BreakKill BreakList BreakSet BreakAccess COVERAGE COVTOFILE DEFINE DIR Display Enter

UART #1

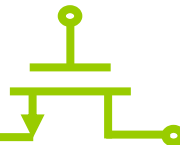
TKU-ECE 612450097 LIN

Call Stack + Locals

UART #1

Memory 1

執行心得-加入Receive(F11)



Register	Value
R0	0x00000055
R1	0x000000A7
R2	0x00000000
R3	0x00000000
R4	0x00000000
R5	0xE000C000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x4000000C
R14 (LR)	0x00000018
R15 (PC)	0x00000074
CPSR	0x600000D3
SFPR	0x00000000

UserSystem
Fast Interrupt
Interrupt
Supervisor
Abort
Undefined
Internal
PC \$
Mode
States
Sec

```

68: wait      LDRB      r6, [r5, #LSR0] ; get status of buffer
69:          E5D56014  LDRB      R6, [R5, #0x0014]
70:          TST       r6, #0x20      ; buffer empty?
71:          BEQ       wait          ; spin until buffer's empty
72:          LDMDB     sp!, {r5, r6, pc}

73:
74: Receive
75:          STMIA     sp!, {r5, r6, lr}
76:          LDR       r5, =UOSTART
77: wait1
78:          LDRB      r6, [r5, #LSR0]
79:          TST       r6, #1
80:          BEQ       wait1
81:          LDRB      r0, [r5]
82:          LDMDB     sp!, {r5, r6, pc}

83:
84: CharData
85:          DCB       "TKU-ECE 612450097 LIN",0
86:          END

```

Line Control
U0LCR: 0x03
Word Length: 8 bits
Stop Bits: 1
Parity: Odd Parity
DLAB
Break Control
Parity Enable

Line Status
U0LSR: 0x00
Receiver Data Ready (RDR)
Overrun Error (OE)
Parity Error (PE)
Framing Error (FE)
Break Interrupt (BI)
Tx Holding Register Empty (THRE)
Transmitter Empty (TEMT)
Error in Rx FIFO (RXFE)

Interrupt Enable
UOIER: 0x00
RBR IE
THRE IE
Rx Line Status IE

Interrupt ID & FIFO Control
UOIER/FCR: 0x01
FIFO Enable
Interrupt: None
Rx Trigger: Level 0 (1)
Rx FIFO Reset
Tx FIFO Reset

Divisor Latch
UODLL: 0x61
UODLM: 0x00
Baudrate: 1932

Receiver & Transmitter Registers
U0RBR/THR: 0x00
Scratch Pad Register
U0SCR: 0x00

Running with Code Size Limit: 32K
Load "F:\03.淡江碩士\01.碩一(112)\02.碩一下學期\07.微處理機概論(電資)(助教課)\04.作業\第01次作業\02.解答\HW1

UART #1

按F11的結果與第一部分相同。

執行心得-加入三種錯誤偵測(F5)



Registers

Register	Value
R0	0x00000000
R1	0x00000000
R2	0x00000000
R3	0x00000000
R4	0x00000000
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000000
CPSR	0x000000D3
SFSR	0x00000000
UserSystem	
Fast Interrupt	
Interrupt	
Supervisor	
About	
Undefined	
Internal	
PC \$	0x00000000
Mode	Supervisor
States	0
Sec	0.00000000

Disassembly

```

0x00000000 E59FD0BC LDR R13,[PC,#0x00BC]
10: BL UARTConfig ; initialize/configure UART0
0x00000004 EB00000A BL 0x00000034
11: LDR r1, = CharData ; starting address of characters
12:
13: Loop
14: LDRB r0, [r1], #1 ; load character, increment address
15: CMP r0, #0 ; null terminated?
16: BLNE Transmit ; send character to UART
17: BNE Loop ; continue if not a '0'
18:
19: MOV r9, #20
20: Loop1
21: BL Receive
22: STRB r0, [r1], #1
23: SUBS r9, r9, #1
24: BNE Loop1
25:
26: done B done ; otherwise we e done
27:
28: Subroutine UARTConfig
29: ; This subroutine configures the I/O pins first. It
30: ; then sets up the UART control register. The
31: ; parameters
32: ; are set to 8 bits, no parity and 1 stop bit.
33: ; Registers used:
34: ; r5 - scratch register
35: ; r6 - scratch register
    
```

Universal Asynchronous Receive Transm 0 (UART0)

Line Control: UOLCR: 0x03

Word Length: 8 bits

Stop Bits: 1

Parity: Odd Parity

Interrupt Enable: UOIER: 0x00

Divisor Latch: UODLL: 0x61, UODLM: 0x00

Baudrate: 1932

Line Status: UOLSR: 0x60

☒ Receiver Data Ready (RDR)

☐ Overrun Error (OE)

☐ Parity Error (PE)

☐ Framing Error (FE)

☐ Break Interrupt (BI)

☒ Tx Holding Register Empty (THRE)

☒ Transmitter Empty (TEMT)

☐ Error in Rx FIFO (RXFE)

Interrupt ID & FIFO Control: UOIRR/FCR: 0x01

Interrupt: None

Rx Trigger: Level 0 (1)

Rx FIFO Reset

Tx FIFO Reset

Receiver & Transmitter Registers: UORBR/THR: 0x00

Scratch Pad Register: UOSCR: 0x00

Receive

```

STMIA sp!, {r5, r6, lr}
LDR r5, =UOSTART
wait1
LDRB r6, [r5, #LSR0]
TST r6, #1
BEQ wait1
TST r6, #0xE
LDRB r0, [r5]
BNE wait1
LDMDB sp!, {r5, r6, pc}
    
```

Command

Running with Code Size Limit: 32K

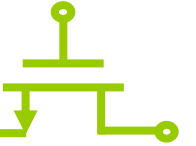
Load "F:\03.淡江碩士\01.碩一(112)\02.碩一下學期\07.微處理機概論(電資)(助教課)\04.作業\第01次作業\02.解答\HW1

UART #1

TKU-ECE 612450097 LIN

與沒有加入錯誤偵測時相同。

執行心得-加入三種錯誤偵測(F10)



Register	Value
R0	0x00000000
R1	0x000000C2
R2	0x00000000
R3	0x00000000
R4	0x00000000
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000014
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x40000000
R14 (LR)	0x00000018
R15 (PC)	0x00000020
CPSR	0x600000D3
SFPR	0x00000000

User/System
Fast Interrupt
Interrupt
Supervisor
Abort
Undefined
Internal
PC \$
Mode
States
Sec

```

0x00000018 1AFFFFFFB BNE      0x0000000C
19:          MOV r9, #20
20: Loop1
0x0000001C E3A09014 MOV     R9,#0x00000014
21:          BL Receive
0x00000020 EB000018 BL      0x00000088
22:          STPB r0, [r1], #1
23:          SUBS r9, r9, #1
24:          BNE Loop1
25: done      B      done      ; otherwise we e done
26:
27:
28: ; Subroutine UARTConfig
29: ; This subroutine configures the I/O pins first. It
30: ; then sets up the UART control register. The
31: ; parameters
32: ; are set to 8 bits, no parity and 1 stop bit.
33: ; Registers used:
34: ; r5 - scratch register
35: ; r6 - scratch register
36: ; inputs: none
37: ; outputs: none
38:
39: UARTConfig
40:          STMIA sp!, {r5,r6,lr}
41:          LDR r5, = PINSEL0 ; base address of register
42:          LDR r6, [r5] ; get contents
43:          BIC r6, r6, #0xF ; clear out lower nibble
44:          ORR r6, r6, #0x5 ; sets P0.0 to Tx0 and P0.1 to Rx0

```

Line Control
U0LCR: 0x03
Word Length: 8 bits
Stop Bits: 1
Parity: Odd Parity
DLAB
Break Control
Parity Enable
Interrupt Enable
U0IER: 0x00
RBR IE
THRE IE
Rx Line Status IE
Divisor Latch
U0DLL: 0x61
U0DLM: 0x00
Baudrate: 1932

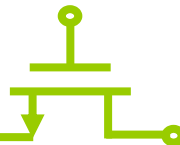
Line Status
U0LSR: 0x60
Receiver Data Ready (RDR)
Overrun Error (OE)
Parity Error (PE)
Framing Error (FE)
Break Interrupt (BI)
Tx Holding Register Empty (THRE)
Transmitter Empty (TEMT)
Error in Rx FIFO (RXFE)
Interrupt ID & FIFO Control
U0IIR/FCR: 0x01
FIFO Enable
Interrupt: None
Rx Trigger: Level 0 (1)
Rx FIFO Reset
Tx FIFO Reset
Receiver & Transmitter Registers
U0RBR/THR: 0x00
Scratch Pad Register
U0SCR: 0x00

Running with Code Size Limit: 32K
Load "F:\03.淡江碩士\01.碩一(112)\02.碩一下學期\07.微處理機概論(電資)(助教課)\04.作業\第01次作業\02.解答\HW1

UART #1
TKU-ECE 612450097 LIN

與沒有加入錯誤偵測時相同。

執行心得-加入三種錯誤偵測(F11)



Registers

Register	Value
R0	0x00000055
R1	0x000000AF
R2	0x00000000
R3	0x00000000
R4	0x00000000
R5	0xE000C000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x4000000C
R14 (LR)	0x00000018
R15 (PC)	0x0000007C
CPSR	0x600000D3
SFPR	0x00000000

☒ User/System
☒ Fast Interrupt
☒ Interrupt
☒ Supervisor
☒ Abort
☒ Undefined
☒ Internal

PC \$ 0x0000007C
 Mode Supervisor
 States 234
 Sec 0.00001950

Disassembly

```

68: wait    LDRB    r6, [r5, #LSR0] ; get status of buffer
0x00000074 E5D56014 LDRB    R6, [R5, #0x0014]
69:         TST     r6, #0x20      ; buffer empty?
0x00000078 E3160020 TST     R6, #0x00000020
70:         BEQ     wait          ; spin until buffer's empty
0x0000007C 0AFFFFFC BEQ     0x00000074
71:         STRB    r0, [r5]
72:         LDMDB   sp!, {r5, r6, pc}
73:
74 Receive
75         STMIA   sp!, {r5, r6, lr}
76         LDR     r5, =U0START
77 waitl
78         LDRB    r6, [r5, #LSR0]
79         TST     r6, #1
80         BEQ     waitl
81         TST     r6, #0xE
82         LDRB    r0, [r5]
83         BNE     waitl
84         LDMDB   sp!, {r5, r6, pc}
85
86 CharData
87         DCB     "TKU-ECE 612450097 LIN", 0
88         END
        
```

Universal Asynchronous Receive Transmit 0 (UART0)

Line Control: U0LCR: 0x03

Word Length: 8 bits

Stop Bits: 1

Parity: Odd Parity

☐ DLAB
☐ Break Control
☐ Parity Enable

Line Status: U0LSR: 0x00

☐ Receiver Data Ready (RDR)
☐ Overrun Error (OE)
☐ Parity Error (PE)
☐ Framing Error (FE)
☐ Break Interrupt (BI)
☒ Tx Holding Register Empty (THRE)
☐ Transmitter Empty (TEMT)
☐ Error in Rx FIFO (RXFE)

Interrupt Enable: U0IER: 0x00

☐ RBR IE
☐ THRE IE
☐ Rx Line Status IE

Interrupt ID & FIFO Control: U0IIR/FCR: 0x01

☐ FIFO Enable
 Interrupt: None
 Rx Trigger: Level 0 (1)
☐ Rx FIFO Reset ☐ Tx FIFO Reset

Divisor Latch: U0DLL: 0x61, U0DLM: 0x00

Baudrate: 1932

Receiver & Transmitter Registers: U0RBR/THR: 0x00

Scratch Pad Register: U0SCR: 0x00

Command

Running with Code Size Limit: 32K

Load "F:\03.淡江碩士\01.碩一(112)\02.碩一下學期\07.微處理機概論(電資)(助教課)\04.作業\第01次作業\02.解答\HW1"

ASSIGN BreakDisable BreakEnable BreakKill BreakList BreakSet BreakAccess COVTOFILE DEFINE DIR Display Enter

UART #1

與沒有加入錯誤偵測時相同。

Q&A

Thanks for your attention !!