

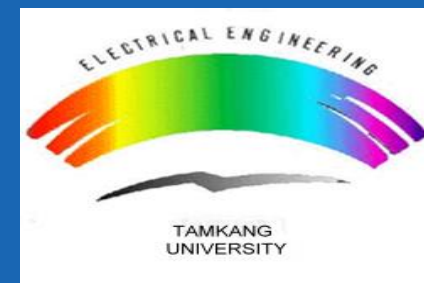
第07次組語實習課

學生：林培瑋

2023 Advanced Mixed-Operation System (AMOS) Lab.



Tamkang University
Department of Electrical and Computer Engineering
No.151, Yingzhuan Rd., Tamsui Dist., New Taipei City 25137, Taiwan (R.O.C.)

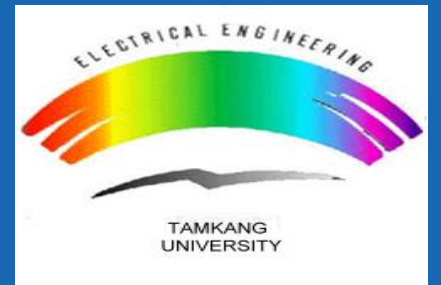


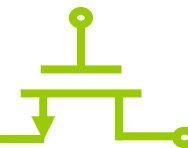
第二次作業

2023 Advanced Mixed-Operation System (AMOS) Lab.



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- ❖ 第一部分(20%)：共2題，1題10%。
- ❖ 第二部分(20%)：標出data1~data10位置，一個1%。
(記憶體沒有框出數值，10%)
- ❖ 第三部分(60%)：共21小題，1小題3%。

不計分	一半分數
程式碼沒有學號、姓名	沒截到記憶體視窗 (第二部分、第三部分1.(2))
暫存器模糊不清楚	結果存在與題目不同的暫存器
暫存器視窗沒拉開	暫存器視窗拉太寬
暫存器數值不正確	第三部分截圖不完整

➤ 以最後繳交的版本為準

➤ 遲交者成績 = 原始成績*0.5

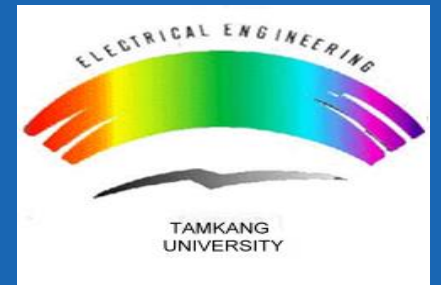


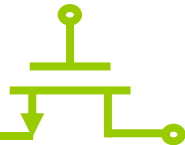
PART1

2023 Advanced Mixed-Operation System (AMOS) Lab.



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小算盤

科學

$6 \times \text{sqr}(731) - 9 \times 731 + 2 =$

3,199,589

小算盤

程式設計人員

30 D265

HEX 30 D265

DEC 3,199,589

OCT 14 151 145

BIN 0011 0000 1101 0010 0110 0101

Register	Value
Current	
R0	0x00000006
R1	0x00000009
R2	0x0030D265
R3	0x000002DB
R4	0x00082759
R5	0x0030EC16
R6	0x000019B3
R7	0x0030D263
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000020
CPSR	0x000000D3
SPSR	0x00000000
Supervisor	
PC \$	0x00000020
Mode	Supervisor
States	20
Sec	0.00000167

Disassembly

0x0000001C	E2872002	ADD	R2,R7,#0x00000002
13: stop	B	stop	
0x00000020	EAFFFFFE	B	0x00000020
0x00000024	000002DB	??EQ	
0x00000028	00000000	ANDEQ	R0,R0,R0
0x0000002C	00000000	ANDEQ	R0,R0,R0
0x00000030	00000000	ANDEQ	R0,R0,R0

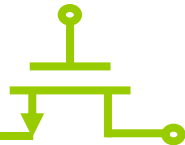
HW2-Part1-1.s

```

1      AREA      LIN_612450097, CODE, READONLY
2
3      ENTRY
4
5      LDR        r3, =0x2DB ; r3 = x = 731
6      MUL        r4, r3, r3 ; r4 = x^2
7      MOV        r0, #6 ; r0 = 6
8      MUL        r5, r4, r0 ; r5 = 6 * x^2
9      MOV        r1, #9 ; r1 = 9
10     MUL        r6, r3, r1 ; r6 = 9 * x
11     SUB        r7, r5, r6 ; r7 = 6 * x^2 - 9 * x
12     ADD        r2, r7, #2 ; r2 = 6 * x^2 - 9 * x + 2
13     stop      B      stop
14     END

```





小算盤

程式設計人員

FFFF FFFF FFFF EE8A

HEX FFFF FFFF FFFF EE8A
DEC -4,470
OCT 1 777 777 777 777 767 212
BIN 1111 1111 1111 1111 1111 1111 1111 1111
1111 1111 1111 1111 1110 1110 1000 1010

QWORD MS M*

位元 位元移位

A	<<	>>	CE	<X
B	()	%	÷
C	7	8	9	×
D	4	5	6	-
E	1	2	3	+
F	+/-	0	.	=

Registers

Register	Value
Current	
R0	0xFFFFF6B
R1	0xFFFFEF1F
R2	0xFFFFFFFF
R3	0x00000095
R4	0x000010E1
R5	0x00000000
R6	0x00000000
R7	0xFFFFEE8A
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000020
CPSR	0x000000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC \$	0x00000020
Mode	Supervisor
States	22
Sec	0.00000183

Disassembly

```

0x0000001C E0807001 ADD R7,R0,R1
13: stop B stop
0x00000020 EAffffff B 0x00000020
0x00000024 000010E1 ANDEQ R1,R0,R1,ROR #1
0x00000028 00000000 ANDEQ R0,R0,R0
0x0000002C 00000000 ANDEQ R0,R0,R0
0x00000030 00000000 ANDEQ R0,R0,R0

```

HW2-Part1-2.s

```

1 AREA LIN_612450097, CODE, READONLY
2 ENTRY
3
4 LDR r3, =149
5 LDR r4, =4321
6 LDR r2, =0xFFFFFFFF
7 EOR r0, r3, r2 ; r0 = -149
8 ADD r0, #1
9 EOR r1, r4, r2 ; r1 = -4321
10 ADD r1, #1
11 ADD r7, r0, r1 ; r7 = -149 + (-4321) = -4470
12
13 stop B stop
14 END

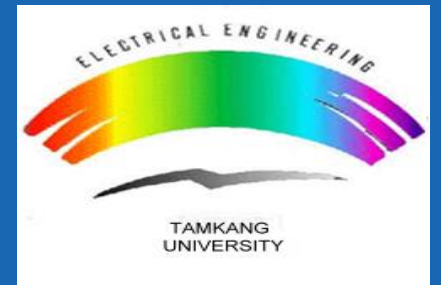
```

PART2

2023 Advanced Mixed-Operation System (AMOS) Lab.



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Registers

Register	Value
R0	0x0000002C
R1	0x00000034
R2	0x00000044
R3	0x00000049
R4	0x0000004B
R5	0x0000004C
R6	0x00000054
R7	0x00000057
R8	0x0000005C
R9	0x0000006A
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000028
CPSR	0x000000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC \$	0x00000028
Mode	Supervisor
States	10
Sec	0.00000083

Disassembly

```

15: stop B stop
0x00000028 EFFFFFFE B 0x00000028
0x0000002C FE378ECC (???)
0x00000030 0000FF6B ANDEQ PC,R0,R1,ROR #30
0x00000034 0000FE37 ANDEQ PC,R0,R7,LSR R14
0x00000038 00000001 ANDEQ R0,R0,R1
0x0000003C 00000000 ANDEQ R0,R0,R5
    
```

HW2-Part2.s

```

1 AREA LIN_612450097, CODE, READONLY
2 ENTRY
3
4 ADR r0, data1
5 ADR r1, data2
6 ADR r2, data3
7 ADR r3, data4
8 ADR r4, data5
9 ADR r5, data6
10 ADR r6, data7
11 ADR r7, data8
12 ADR r8, data9
13 ADR r9, data10
14
15 stop B stop
16 data1 DCW 0x8ECC, 0xFE37, -149
17 data2 DCD 0xFE37, 1, 5, 20
18 data3 DCB 0xCF, 23, 39, 0x54, 250
19 data4 DCWU 0x1234
20 data5 DCB 255
21 data6 DCDU 0x12345678, -4321
22 data7 DCB 0xA3
23 ALIGN 4, 3
24 data8 DCWU 0xFC25
25 ALIGN
26 data9 DCB "MVP_N. Jokic", 0
27 data10 DCW 0xEF12
28 END
    
```

Memory 1

Address: 0x0000002C

0x0000002C:	CC 8E 37 FE 6B FF 00 00	37 FE 00 00 01 00 00 00	05 00 00 00 14 00 00 00	CF 17 27 54 FA 34 12 FE	79 56 34 12 1F EF FF FF
0x00000054:	A3 00 00 25 FC 00 00 00	4D 56 50 5F 4E 2E 20 4A	6F 6B 69 63 00 00 12 EF	00 00 00 00 00 00 00 00	00 00 00 00 00 00 00 00
0x0000007C:	00 00 00 00 00 00 00 00	00 00 00 00 00 00 00 00	00 00 00 00 00 00 00 00	00 00 00 00 00 00 00 00	00 00 00 00 00 00 00 00
0x000000A4:	00 00 00 00 00 00 00 00	00 00 00 00 00 00 00 00	00 00 00 00 00 00 00 00	00 00 00 00 00 00 00 00	00 00 00 00 00 00 00 00
0x000000CC:	00 00 00 00 00 00 00 00	00 00 00 00 00 00 00 00	00 00 00 00 00 00 00 00	00 00 00 00 00 00 00 00	00 00 00 00 00 00 00 00
0x000000F4:	00 00 00 00 00 00 00 00	00 00 00 00 00 00 00 00	00 00 00 00 00 00 00 00	00 00 00 00 00 00 00 00	00 00 00 00 00 00 00 00
0x0000011C:	00 00 00 00 00 00 00 00	00 00 00 00 00 00 00 00	00 00 00 00 00 00 00 00	00 00 00 00 00 00 00 00	00 00 00 00 00 00 00 00
0x00000144:	00 00 00 00 00 00 00 00	00 00 00 00 00 00 00 00	00 00 00 00 00 00 00 00	00 00 00 00 00 00 00 00	00 00 00 00 00 00 00 00
0x0000016C:	00 00 00 00 00 00 00 00	00 00 00 00 00 00 00 00	00 00 00 00 00 00 00 00	00 00 00 00 00 00 00 00	00 00 00 00 00 00 00 00

Call Stack + Locals | Memory

40 43 48 62

4*10+3 4*12+0

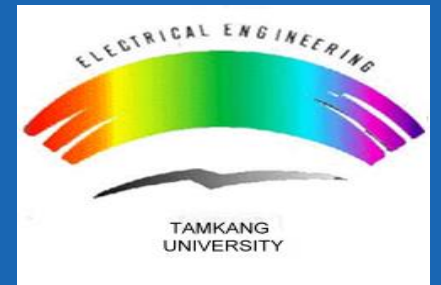


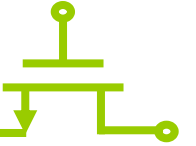
PART3

2023 Advanced Mixed-Operation System (AMOS) Lab.



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Registers

Register	Value
Current	
R0	0x00000000
R1	0x00000000
R2	0x00000000
R3	0x40000000
R4	0x00000060
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000008
CPSR	0x000000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC \$	0x00000008
Mode	Supervisor
States	2
Sec	0.00000017

Disassembly

```

0x00000000 E3A03101 MOV R3,#0x40000000
5:          LDR      r4, =0x60
0x00000004 E3A04060 MOV R4,#0x00000060
7:          STR      r6, [r3, #8]
0x00000008 E5836008 STR R6,[R3,#0x0008]
0:          STPB     r7, [r3, #12]

```

HW2-Part3-1-1-v1.s

```

1      AREA LIN_612450097, CODE, READONLY
2      ENTRY
3
4      LDR      r3, =0x40000000
5      LDR      r4, =0x60
6
7      STR      r6, [r3, #8]
8      STPB     r7, [r3], #12
9      LDRH     r5, [r3], #12
10     LDR      r12, [r3, #4]!
11     LDR      r6, [r3, r4, ROR #28]!
12     LDR      r0, [r3, r4, LSL #2]
13
14
15     stop    B      stop
16     END

```

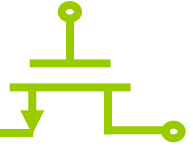
Memory 1

Address: 0x40000000

0x40000000:	00 00
0x4000001B:	00 00
0x40000036:	00 00
0x40000051:	00 00
0x4000006C:	00 00
0x40000087:	00 00
0x400000A2:	00 00

Call Stack + Locals Memory 1





Registers

Register	Value
Current	
R0	0x00000000
R1	0x00000000
R2	0x00000000
R3	0x40000000
R4	0x00000060
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x0000000C
+ CPSR	0x000000D3
+ SPSR	0x00000000
User/System	
+ Fast Interrupt	
+ Interrupt	
Supervisor	
+ Abort	
+ Undefined	
Internal	
PC \$	0x0000000C
Mode	Supervisor
States	4
Sec	0.00000033

Disassembly

```

0x00000008 E5836008 STR R6, [R3, #0x0008]
8: STRB r7, [r3], #12
0x0000000C E4C3700C STRB R7, [R3], #0x000C
9: LDRH r5, [r3], #12
0x00000010 E0D350BC LDRH R5, [R3], #0x0C
10: LDR r12, [r3, #4]!
0x00000014 E5836008 STR R6, [R3, #0x0008]

```

HW2-Part3-1-1-v1.s

```

1 AREA LIN_612450097, CODE, READONLY
2 ENTRY
3
4 LDR r3, =0x40000000
5 LDR r4, =0x60
6
7 STR r6, [r3, #8]
8 STRB r7, [r3], #12
9 LDRH r5, [r3], #12
10 LDR r12, [r3, #4]!
11 LDR r6, [r3, r4, ROR #28]!
12 LDR r0, [r3, r4, LSL #2]
13
14
15 stop B stop
16 END

```

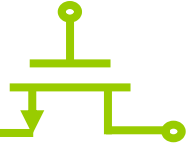
Memory 1

Address: 0x40000000

0x40000000:	00 00
0x4000001B:	00 00
0x40000036:	00 00
0x40000051:	00 00
0x4000006C:	00 00
0x40000087:	00 00
0x400000A2:	00 00

Call Stack + Locals | Memory 1





Registers

Register	Value
Current	
R0	0x00000000
R1	0x00000000
R2	0x00000000
R3	0x4000000C
R4	0x00000060
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000010
CPSR	0x000000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC \$	0x00000010
Mode	Supervisor
States	6
Sec	0.00000050

Disassembly

```

0x00000008 E5836008 STR R6, [R3, #0x0008]
8: STRB r7, [r3], #12
0x0000000C E4C3700C STRB R7, [R3], #0x000C
9: LDRH r5, [r3], #12
0x00000010 E0D350BC LDRH R5, [R3], #0x0C
10: LDR r12, [r3, #4]!
0x00000014 E5D3C004 LDR R12, [R3, #0x0014]

```

HW2-Part3-1-1-v1.s

```

1 AREA LIN_612450097, CODE, READONLY
2 ENTRY
3
4 LDR r3, =0x40000000
5 LDR r4, =0x60
6
7 STR r6, [r3, #8]
8 STRB r7, [r3], #12
9 LDRH r5, [r3], #12
10 LDR r12, [r3, #4]!
11 LDR r6, [r3, r4, ROR #28]!
12 LDR r0, [r3, r4, LSL #2]
13
14
15 stop B stop
16 END

```

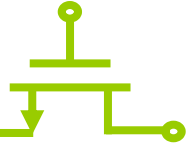
Memory 1

Address: 0x40000000

0x40000000:	00 00
0x4000001B:	00 00
0x40000036:	00 00
0x40000051:	00 00
0x4000006C:	00 00
0x40000087:	00 00
0x400000A2:	00 00

Call Stack + Locals Memory 1





Registers

Register	Value
Current	
R0	0x00000000
R1	0x00000000
R2	0x00000000
R3	0x40000018
R4	0x00000060
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000014
CPSR	0x000000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC \$	0x00000014
Mode	Supervisor
States	9
Sec	0.00000075

Disassembly

```

10:      LDR      r12,[r3,#4]!
0x00000014 E5B3C004 LDR      R12,[R3,#0x0004]!
11:      LDR      r6,[r3,r4,ROR #28]!
0x00000018 E7B36E64 LDR      R6,[R3,R4,ROR #28]!
12:      LDR      r0,[r3,r4,LSL #2]
13:
14:

```

HW2-Part3-1-1-v1.s

```

1      AREA LIN_612450097, CODE, READONLY
2      ENTRY
3
4      LDR      r3,=0x40000000
5      LDR      r4,=0x60
6
7      STR      r6,[r3,#8]
8      STRB     r7,[r3],#12
9      LDRH     r5,[r3],#12
10     LDR      r12,[r3,#4]!
11     LDR      r6,[r3,r4,ROR #28]!
12     LDR      r0,[r3,r4,LSL #2]
13
14
15     stop    B      stop
16     END

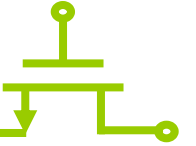
```

Memory 1

Address: 0x40000000

0x40000000:	00 00
0x4000001B:	00 00
0x40000036:	00 00
0x40000051:	00 00
0x4000006C:	00 00
0x40000087:	00 00
0x400000A2:	00 00

Call Stack + Locals Memory 1



Registers

Register	Value
Current	
R0	0x00000000
R1	0x00000000
R2	0x00000000
R3	0x4000001C
R4	0x00000060
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000018
CPSR	0x000000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC \$	0x00000018
Mode	Supervisor
States	12
Sec	0.00000100

Disassembly

```

10:      LDR      r12,[r3,#4]!
0x00000014  E5B3C004  LDR      R12,[R3,#0x0004]!
11:      LDR      r6,[r3,r4,ROR #28]!
0x00000018  E7B36E64  LDR      R6,[R3,R4,ROR #28]!
12:      LDR      r0,[r3,r4,LSL #2]
13:
14:

```

HW2-Part3-1-1-v1.s

```

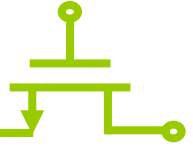
1      AREA LIN_612450097, CODE, READONLY
2      ENTRY
3
4      LDR      r3,=0x40000000
5      LDR      r4,=0x60
6
7      STR      r6,[r3,#8]
8      STRB     r7,[r3],#12
9      LDRH     r5,[r3],#12
10     LDR      r12,[r3,#4]!
11     LDR      r6,[r3,r4,ROR #28]!
12     LDR      r0,[r3,r4,LSL #2]
13
14
15     stop    B      stop
16     END

```

Memory 1

Address: 0x40000000

0x40000000:	00 00
0x4000001B:	00 00
0x40000036:	00 00
0x40000051:	00 00
0x4000006C:	00 00
0x40000087:	00 00
0x400000A2:	00 00



Registers

Register	Value
Current	
R0	0x00000000
R1	0x00000000
R2	0x00000000
R3	0x4000061C
R4	0x00000060
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x0000001C
CPSR	0x000000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC \$	0x0000001C
Mode	Supervisor
States	15
Sec	0.00000125

Disassembly

```

0x00000018 E7B36E64 LDR R6, [R3, R4, ROR #28]!
12: LDR r0, [r3, r4, LSL #2]
13:
14:
0x0000001C E7930104 LDR R0, [R3, R4, LSL #2]
15: stop B stop

```

HW2-Part3-1-1-v1.s

```

1 AREA LIN_612450097, CODE, READONLY
2 ENTRY
3
4 LDR r3, =0x40000000
5 LDR r4, =0x60
6
7 STR r6, [r3, #8]
8 STRB r7, [r3], #12
9 LDRH r5, [r3], #12
10 LDR r12, [r3, #4]!
11 LDR r6, [r3, r4, ROR #28]!
12 LDR r0, [r3, r4, LSL #2]
13
14
15 stop B stop
16 END

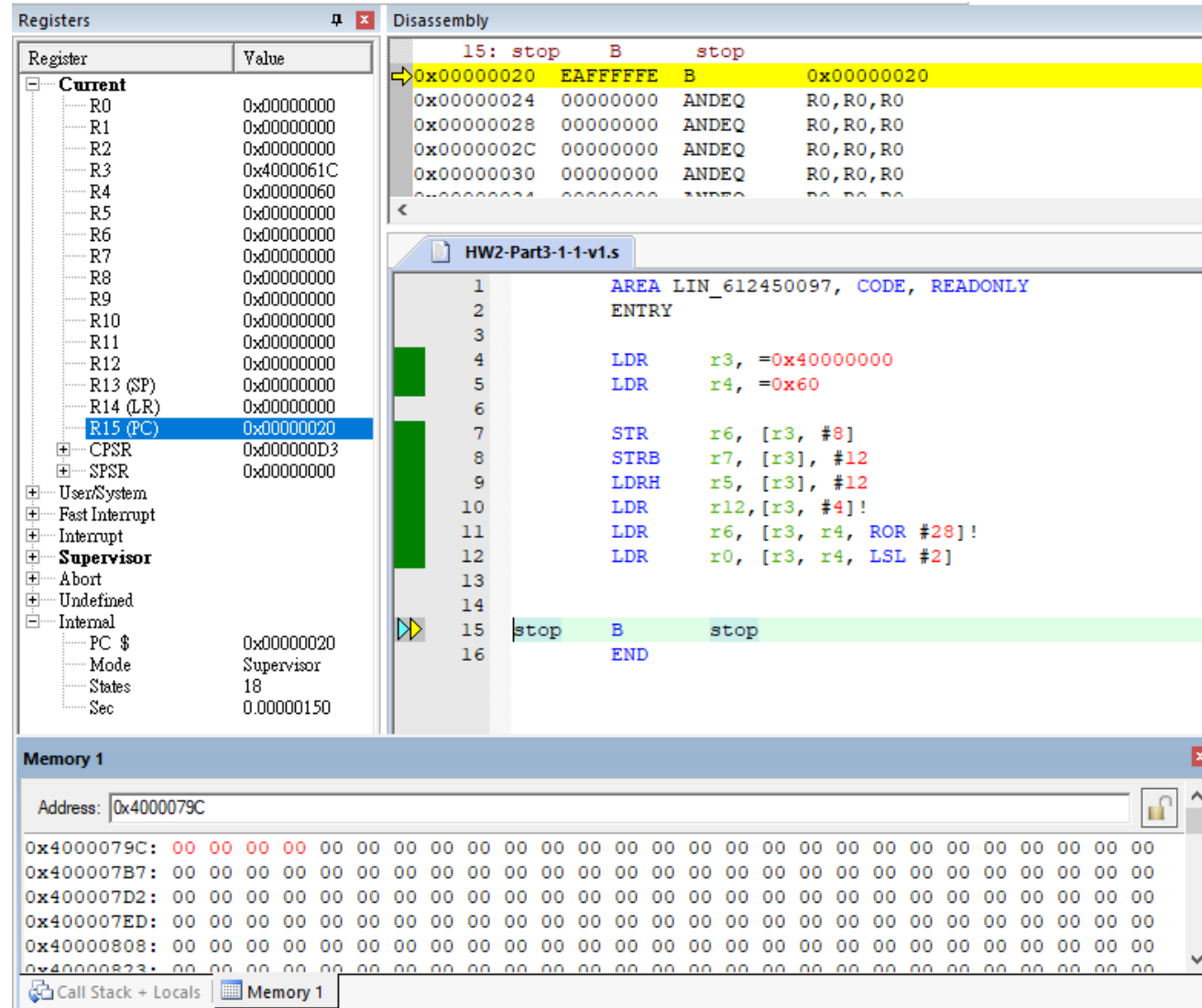
```

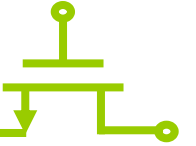
Memory 1

Address: 0x4000061C

0x4000061C:	00 00
0x40000637:	00 00
0x40000652:	00 00
0x4000066D:	00 00
0x40000688:	00 00
0x400006A3:	00 00

Call Stack + Locals Memory 1





Registers

Register	Value
R0	0x00000000
R1	0x00000000
R2	0x00000000
R3	0x40000000
R4	0x00000060
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x0000000C
CPSR	0x000000D3
SPSR	0x00000000
UserSystem	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC \$	0x0000000C
Mode	Supervisor
States	4
Sec	0.00000033

Disassembly

```

0x00000008 E5836008 STR R6, [R3, #0x0008]
8: LDR r3, =0x40000000
0x0000000C E3A03101 MOV R3, #0x40000000
9: LDR r4, =0x60
0x00000010 E3A04060 MOV R4, #0x00000060
10: STRB r7, [r3], #12
...

```

HW2-Part3-1-1-v2.s

```

1 AREA LIN_612450097, CODE, READONLY
2 ENTRY
3
4 LDR r3, =0x40000000
5 LDR r4, =0x60
6 STR r6, [r3, #8]
7
8 LDR r3, =0x40000000
9 LDR r4, =0x60
10 STRB r7, [r3], #12
11
12 LDR r3, =0x40000000
13 LDR r4, =0x60
14 LDRH r5, [r3], #12
15
16 LDR r3, =0x40000000
17 LDR r4, =0x60
18 LDR r12, [r3, #4]!
19
20 LDR r3, =0x40000000
21 LDR r4, =0x60
22 LDR r6, [r3, r4, ROR #28]!
23
24 LDR r3, =0x40000000
25 LDR r4, =0x60
26 LDR r0, [r3, r4, LSL #2]
27
28
29 stop B stop
30 END

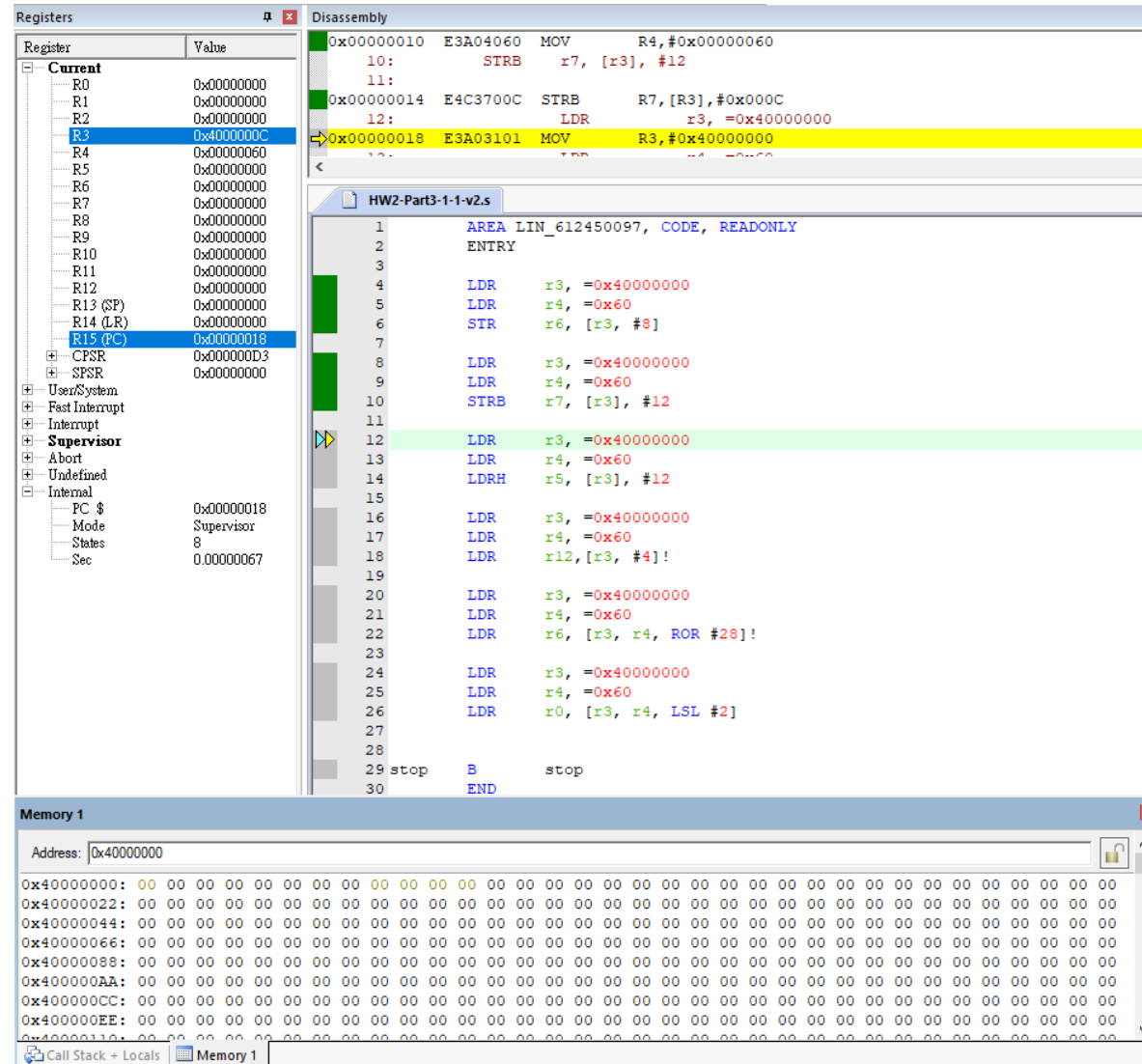
```

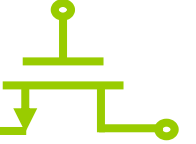
Memory 1

Address: 0x40000000

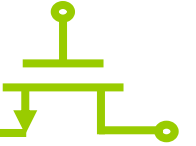
0x40000000:	00 00
0x40000022:	00 00
0x40000044:	00 00
0x40000066:	00 00
0x40000088:	00 00
0x400000AA:	00 00
0x400000CC:	00 00
0x400000EE:	00 00
0x40000110:	00 00







2023/11/6



Registers

Register	Value
R0	0x00000000
R1	0x00000000
R2	0x00000000
R3	0x40000004
R4	0x00000060
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000030
CPSR	0x000000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC \$	0x00000030
Mode	Supervisor
State	18
Sec	0.00000150

Disassembly

```

0x00000028 E3A04060 MOV R4,#0x00000060
18: LDR r12,[r3,#4]!
19:
0x0000002C E5B3C004 LDR R12,[R3,#0x0004]!
20: LDR r3,=0x40000000
0x00000030 E3A03101 MOV R3,#0x40000000
21: LDR r4,=0x60
22:
23:
24:
25:
26:
27:
28:
29: stop B stop
30: END

```

HW2-Part3-1-1-v2.s

```

1 AREA LIN_612450097, CODE, READONLY
2 ENTRY
3
4 LDR r3,=0x40000000
5 LDR r4,=0x60
6 STR r6,[r3,#8]
7
8 LDR r3,=0x40000000
9 LDR r4,=0x60
10 STRB r7,[r3],#12
11
12 LDR r3,=0x40000000
13 LDR r4,=0x60
14 LDRH r5,[r3],#12
15
16 LDR r3,=0x40000000
17 LDR r4,=0x60
18 LDR r12,[r3,#4]!
19
20 LDR r3,=0x40000000
21 LDR r4,=0x60
22 LDR r6,[r3,r4,ROR #28]!
23
24 LDR r3,=0x40000000
25 LDR r4,=0x60
26 LDR r0,[r3,r4,LSL #2]
27
28
29 stop B stop
30 END

```

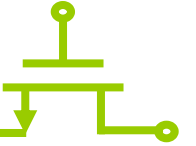
Memory 1

Address: 0x40000000

0x40000000:	00 00
0x40000002:	00 00
0x40000004:	00 00
0x40000006:	00 00
0x40000008:	00 00
0x4000000A:	00 00
0x4000000C:	00 00
0x4000000E:	00 00
0x40000010:	00 00

Call Stack + Locals Memory 1





Registers

Register	Value
R0	0x00000000
R1	0x00000000
R2	0x00000000
R3	0x40000600
R4	0x00000060
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x0000003C
CPSR	0x000000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC \$	0x0000003C
Mode	Supervisor
State	23
Sec	0.00000192

Disassembly

```

0x00000038 E7B36E64 LDR R6, [R3, R4, ROR #28]!
24: LDR r3, =0x40000000
0x0000003C E3A03101 MOV R3, #0x40000000
25: LDR r4, =0x60
0x00000040 E3A04060 MOV R4, #0x00000060
26: LDR r0, [r3, r4, LSL #2]

```

HW2-Part3-1-1-v2.s

```

1 AREA LIN_612450097, CODE, READONLY
2 ENTRY
3
4 LDR r3, =0x40000000
5 LDR r4, =0x60
6 STR r6, [r3, #8]
7
8 LDR r3, =0x40000000
9 LDR r4, =0x60
10 STRB r7, [r3], #12
11
12 LDR r3, =0x40000000
13 LDR r4, =0x60
14 LDRH r5, [r3], #12
15
16 LDR r3, =0x40000000
17 LDR r4, =0x60
18 LDR r12, [r3, #4]!
19
20 LDR r3, =0x40000000
21 LDR r4, =0x60
22 LDR r6, [r3, r4, ROR #28]!
23
24 LDR r3, =0x40000000
25 LDR r4, =0x60
26 LDR r0, [r3, r4, LSL #2]
27
28
29 stop B stop
30 END

```

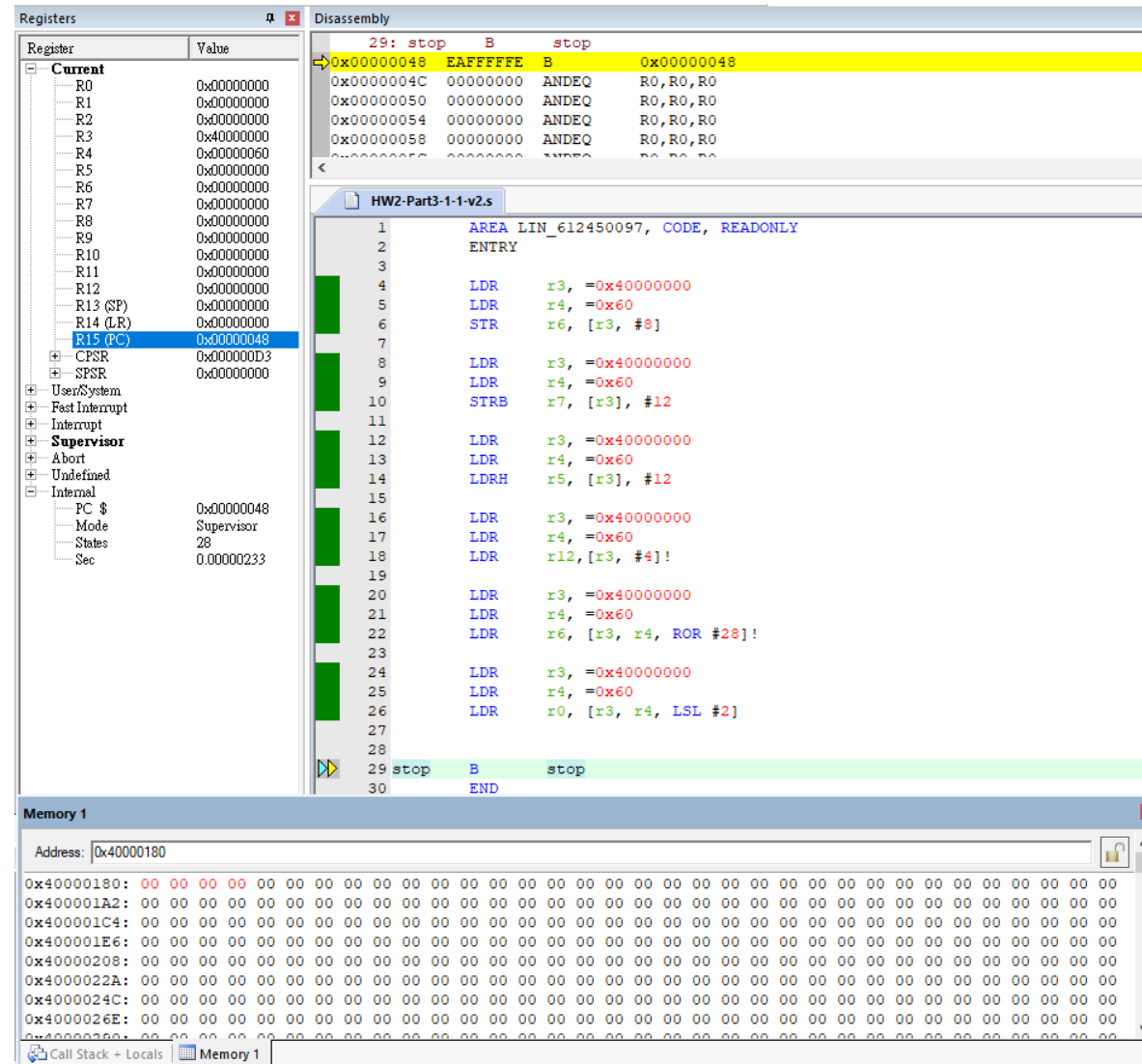
Memory 1

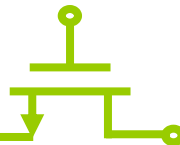
Address: 0x40000600

0x40000600	: 00
0x40000622	: 00
0x40000644	: 00
0x40000666	: 00
0x40000688	: 00
0x400006AA	: 00
0x400006CC	: 00
0x400006EE	: 00
0x40000710	: 00

Call Stack + Locals | Memory 1







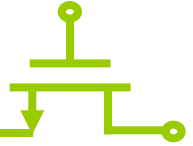
The screenshot displays the Keil uVision IDE interface, specifically the Disassembly and Memory windows.

Disassembly Window:

- Registers:** A list of registers (R0-R15, CPSR, SPSR) and their current values. R15 (PC) is highlighted with the value 0x00000010.
- Disassembly:** A list of assembly instructions with their addresses and operands. The instructions are:
 - 0x00000008: E5836000 STR R6, [R3]
 - 8: LDRB r4, [r3]
 - 9: stop B stop
 - 0x0000000C: E5D34000 LDRB R4, [R3]
 - 10: stop B stop
 - 0x00000010: EAEFFFE B 0x00000010
 - 0x00000014: DEADBEEF CODE
- HW2-Part3-1-2.s:** A source code file showing the assembly instructions corresponding to the disassembly window. The instructions are:
 - 1: AREA LIN_612450097, CODE, READONLY
 - 2: ENTRY
 - 3: stop B stop
 - 4: LDR r6, =0xDEADBEEF
 - 5: LDR r3, =0x40000000
 - 6: stop B stop
 - 7: STR r6, [r3]
 - 8: LDRB r4, [r3]
 - 9: stop B stop
 - 10: stop B stop
 - 11: END

Memory Window:

- Address:** 0x40000000
- Memory Dump:** A table showing memory addresses and their corresponding values. The values are mostly 0x00, indicating a zero-filled memory area.



Registers

Register	Value
Current	
R0	0x00000000
R1	0x00000000
R2	0x12345678
R3	0x87654321
R4	0x00000012
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x0000000C
CPSR	0x000000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC \$	0x0000000C
Mode	Supervisor
States	7
Sec	0.00000058

Disassembly

```

0x00000008 E3A04012 MOV R4,#0x00000012
8: BIC r2, r2, #0xFF000000
0x0000000C E3C224FF BIC R2,R2,#0xFF000000
9: LSL r2, r3, #4
0x00000010 E1A02203 MOV R2,R3,LSL #4
10: LSL r2, r2, r4
0x00000014 E1300413 MOV R2,R2,LSL R4

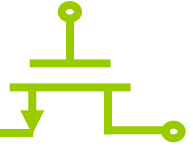
```

HW2-Part3-2-v1.s

```

1 AREA LIN_612450097, CODE, READONLY
2 ENTRY
3
4 LDR r2, =0x12345678
5 LDR r3, =0x87654321
6 LDR r4, =0x00000012
7
8 BIC r2, r2, #0xFF000000
9 LSL r2, r3, #4
10 LSL r2, r2, r4
11 ROR r2, r2, #12
12 AND r2, r2, r3
13 ORR r2, r2, r4
14 EOR r2, r2, r4
15 BIC r2, r2, r4
16 EOR r2, r2, r3, ROR #7
17
18 stop B stop
19 END

```



Registers

Register	Value
Current	
R0	0x00000000
R1	0x00000000
R2	0x00345678
R3	0x87654321
R4	0x00000012
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000010
CPSR	0x000000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC \$	0x00000010
Mode	Supervisor
States	8
Sec	0.00000067

Disassembly

```

0x00000008 E3A04012 MOV R4,#0x00000012
8: BIC r2, r2, #0xFF000000
0x0000000C E3C224FF BIC R2,R2,#0xFF000000
9: LSL r2, r3, #4
0x00000010 E1A02203 MOV R2,R3,LSL #4
10: LSL r2, r2, r4
0x00000014 E1A02203 MOV R2,R3,LSL #4

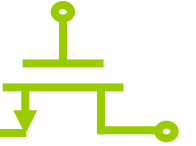
```

HW2-Part3-2-v1.s

```

1 AREA LIN_612450097, CODE, READONLY
2 ENTRY
3
4 LDR r2, =0x12345678
5 LDR r3, =0x87654321
6 LDR r4, =0x00000012
7
8 BIC r2, r2, #0xFF000000
9 LSL r2, r3, #4
10 LSL r2, r2, r4
11 ROR r2, r2, #12
12 AND r2, r2, r3
13 ORR r2, r2, r4
14 EOR r2, r2, r4
15 BIC r2, r2, r4
16 EOR r2, r2, r3, ROR #7
17
18 stop B stop
19 END

```



Registers

Register	Value
Current	
R0	0x00000000
R1	0x00000000
R2	0x76543210
R3	0x87654321
R4	0x00000012
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000014
CPSR	0x000000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC \$	0x00000014
Mode	Supervisor
States	9
Sec	0.00000075

Disassembly

```

10:                                LSL    r2, r2, r4
0x00000014  E1A02412  MOV    R2,R2,LSL R4
11:                                ROR    r2, r2, #12
0x00000018  E1A02662  MOV    R2,R2,ROR #12
12:                                AND    r2, r2, r3
0x0000001C  E0022003  AND    R2,R2,R3
13:                                ORR    r2, r2, r4

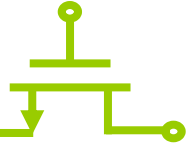
```

HW2-Part3-2-v1.s

```

1      AREA LIN_612450097, CODE, READONLY
2      ENTRY
3
4      LDR    r2, =0x12345678
5      LDR    r3, =0x87654321
6      LDR    r4, =0x00000012
7
8      BIC    r2, r2, #0xFF000000
9      LSL    r2, r3, #4
10     LSL    r2, r2, r4
11     ROR    r2, r2, #12
12     AND    r2, r2, r3
13     ORR    r2, r2, r4
14     EOR    r2, r2, r4
15     BIC    r2, r2, r4
16     EOR    r2, r2, r3, ROR #7
17
18 stop  B      stop
19     END

```



Registers

Register	Value
Current	
R0	0x00000000
R1	0x00000000
R2	0xC8400000
R3	0x87654321
R4	0x00000012
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000018
CPSR	0x000000D3
SPSR	0x00000000
+ User/System	
+ Fast Interrupt	
+ Interrupt	
+ Supervisor	
+ Abort	
+ Undefined	
- Internal	
PC \$	0x00000018
Mode	Supervisor
States	11
Sec	0.00000092

Disassembly

```

10:          LSL     r2, r2, r4
0x00000014 E1A02412 MOV     R2,R2,LSL R4
11:          ROR     r2, r2, #12
0x00000018 E1A02662 MOV     R2,R2,ROR #12
12:          AND     r2, r2, r3
0x0000001C E0022003 AND     R2,R2,R3
13:          ORR     r2, r2, r4

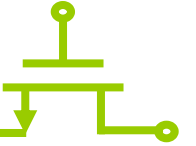
```

HW2-Part3-2-v1.s

```

1          AREA LIN_612450097, CODE, READONLY
2          ENTRY
3
4          LDR     r2, =0x12345678
5          LDR     r3, =0x87654321
6          LDR     r4, =0x00000012
7
8          BIC     r2, r2, #0xFF000000
9          LSL     r2, r3, #4
10         LSL     r2, r2, r4
11         ROR     r2, r2, #12
12         AND     r2, r2, r3
13         ORR     r2, r2, r4
14         EOR     r2, r2, r4
15         BIC     r2, r2, r4
16         EOR     r2, r2, r3, ROR #7
17
18 stop     B       stop
19         END

```



Registers

Register	Value
Current	
R0	0x00000000
R1	0x00000000
R2	0x000C8400
R3	0x87654321
R4	0x00000012
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x0000001C
CPSR	0x000000D3
SPSR	0x00000000
Supervisor	
Abort	
Undefined	
Internal	
PC \$	0x0000001C
Mode	Supervisor
States	12
Sec	0.00000100

Disassembly

```

10:          LSL     r2, r2, r4
0x00000014 E1A02412 MOV     R2,R2,LSL R4
11:          ROR     r2, r2, #12
0x00000018 E1A02662 MOV     R2,R2,ROR #12
12:          AND     r2, r2, r3
0x0000001C E0022003 AND     R2,R2,R3
13:          ORR     r2, r2, r4
14:          EOR     r2, r2, r4
15:          BIC     r2, r2, r4
16:          EOR     r2, r2, r3, ROR #7
17:          stop    B      stop
18:          END

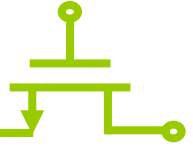
```

HW2-Part3-2-v1.s

```

1  AREA LIN_612450097, CODE, READONLY
2  ENTRY
3
4  LDR     r2, =0x12345678
5  LDR     r3, =0x87654321
6  LDR     r4, =0x00000012
7
8  BIC     r2, r2, #0xFF000000
9  LSL     r2, r3, #4
10 LSL     r2, r2, r4
11 ROR     r2, r2, #12
12 AND     r2, r2, r3
13 ORR     r2, r2, r4
14 EOR     r2, r2, r4
15 BIC     r2, r2, r4
16 EOR     r2, r2, r3, ROR #7
17
18 stop    B      stop
19 END

```



Registers

Register	Value
Current	
R0	0x00000000
R1	0x00000000
R2	0x00040000
R3	0x87654321
R4	0x00000012
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000020
CPSR	0x000000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC \$	0x00000020
Mode	Supervisor
States	13
Sec	0.00000108

Disassembly

```

0x0000001C E0022003 AND R2,R2,R3
13:          ORR r2, r2, r4
0x00000020 E1822004 ORR R2,R2,R4
14:          EOR r2, r2, r4
0x00000024 E0222004 EOR R2,R2,R4
15:          BIC r2, r2, r4
0x00000028 E1C22004 BIC R2,R2,R4

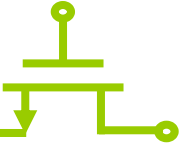
```

HW2-Part3-2-v1.s

```

1      AREA LIN_612450097, CODE, READONLY
2      ENTRY
3
4      LDR    r2, =0x12345678
5      LDR    r3, =0x87654321
6      LDR    r4, =0x00000012
7
8      BIC    r2, r2, #0xFF000000
9      LSL    r2, r3, #4
10     LSL    r2, r2, r4
11     ROR    r2, r2, #12
12     AND    r2, r2, r3
13     ORR    r2, r2, r4
14     EOR    r2, r2, r4
15     BIC    r2, r2, r4
16     EOR    r2, r2, r3, ROR #7
17
18 stop    B      stop
19     END

```

Registers

Register	Value
Current	
R0	0x00000000
R1	0x00000000
R2	0x00040012
R3	0x87654321
R4	0x00000012
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000024
CPSR	0x000000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC \$	0x00000024
Mode	Supervisor
States	14
Sec	0.00000117

Disassembly

```

0x0000001C  E0022003  AND      R2,R2,R3
13:          ORR      r2, r2, r4
0x00000020  E1822004  ORR      R2,R2,R4
14:          EOR      r2, r2, r4
0x00000024  E0222004  EOR      R2,R2,R4
15:          BIC      r2, r2, r4
0x00000028  E1C22004  BIC      R2,R2,R4

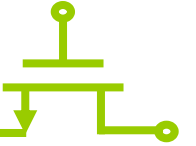
```

HW2-Part3-2-v1.s

```

1      AREA LIN_612450097, CODE, READONLY
2      ENTRY
3
4      LDR      r2, =0x12345678
5      LDR      r3, =0x87654321
6      LDR      r4, =0x00000012
7
8      BIC      r2, r2, #0xFF000000
9      LSL      r2, r3, #4
10     LSL      r2, r2, r4
11     ROR      r2, r2, #12
12     AND      r2, r2, r3
13     ORR      r2, r2, r4
14     EOR      r2, r2, r4
15     BIC      r2, r2, r4
16     EOR      r2, r2, r3, ROR #7
17
18 stop    B      stop
19     END

```



Registers

Register	Value
Current	
R0	0x00000000
R1	0x00000000
R2	0x00040000
R3	0x87654321
R4	0x00000012
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000028
CPSR	0x000000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC \$	0x00000028
Mode	Supervisor
States	15
Sec	0.00000125

Disassembly

```

15:          BIC      r2, r2, r4
0x00000028 E1C22004 BIC      R2,R2,R4
16:          EOR      r2, r2, r3, ROR #7
17:          0x0000002C E02223E3 EOR      R2,R2,R3,ROR #7
18: stop      B        stop
0x00000028 F1FFFFFF B        0x00000028

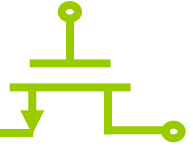
```

HW2-Part3-2-v1.s

```

1      AREA LIN_612450097, CODE, READONLY
2      ENTRY
3
4      LDR      r2, =0x12345678
5      LDR      r3, =0x87654321
6      LDR      r4, =0x00000012
7
8      BIC      r2, r2, #0xFF000000
9      LSL      r2, r3, #4
10     LSL      r2, r2, r4
11     ROR      r2, r2, #12
12     AND      r2, r2, r3
13     ORR      r2, r2, r4
14     EOR      r2, r2, r4
15     BIC      r2, r2, r4
16     EOR      r2, r2, r3, ROR #7
17
18 stop    B        stop
19     END

```



Registers

Register	Value
Current	
R0	0x00000000
R1	0x00000000
R2	0x00040000
R3	0x87654321
R4	0x00000012
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x0000002C
+ CPSR	0x000000D3
+ SPSR	0x00000000
+ User/System	
+ Fast Interrupt	
+ Interrupt	
+ Supervisor	
+ Abort	
+ Undefined	
- Internal	
PC \$	0x0000002C
Mode	Supervisor
States	16
Sec	0.00000133

Disassembly

```

15:                                BIC    r2, r2, r4
0x00000028  E1C22004  BIC    R2,R2,R4
16:                                EOR    r2, r2, r3, ROR #7
17:                                EOR    R2,R2,R3,ROR #7
0x0000002C  E02223E3  EOR    R2,R2,R3,ROR #7
18: stop      B      stop
0x00000000  FFFFFFFF  B      0x00000000

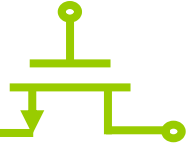
```

HW2-Part3-2-v1.s

```

1      AREA LIN_612450097, CODE, READONLY
2      ENTRY
3
4      LDR    r2, =0x12345678
5      LDR    r3, =0x87654321
6      LDR    r4, =0x00000012
7
8      BIC    r2, r2, #0xFF000000
9      LSL    r2, r3, #4
10     LSL    r2, r2, r4
11     ROR    r2, r2, #12
12     AND    r2, r2, r3
13     ORR    r2, r2, r4
14     EOR    r2, r2, r4
15     BIC    r2, r2, r4
16     EOR    r2, r2, r3, ROR #7
17
18 stop  B      stop
19     END

```



Registers

Register	Value
Current	
R0	0x00000000
R1	0x00000000
R2	0x430ACA86
R3	0x87654321
R4	0x00000012
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000030
CPSR	0x000000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC \$	0x00000030
Mode	Supervisor
States	17
Sec	0.00000142

Disassembly

```

18: stop    B      stop
0x00000030 EFFFFFFE B      0x00000030
0x00000034 12345678 EORNES R5,R4,#0x07800000
0x00000038 87654321 STRHIB R4,[R5,-R1,LSR #6]!
0x0000003C 00000000 ANDEQ  R0,R0,R0
0x00000040 00000000 ANDEQ  R0,R0,R0
0x00000044 00000000 ANDEQ  R0,R0,R0

```

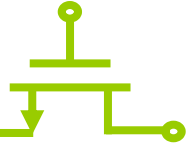
HW2-Part3-2-v1.s

```

1      AREA LIN_612450097, CODE, READONLY
2      ENTRY
3
4      LDR    r2, =0x12345678
5      LDR    r3, =0x87654321
6      LDR    r4, =0x00000012
7
8      BIC    r2, r2, #0xFF000000
9      LSL    r2, r3, #4
10     LSL    r2, r2, r4
11     ROR    r2, r2, #12
12     AND    r2, r2, r3
13     ORR    r2, r2, r4
14     EOR    r2, r2, r4
15     BIC    r2, r2, r4
16     EOR    r2, r2, r3, ROR #7
17
18     stop   B      stop
19     END

```





Registers

Register	Value
Current	
R0	0x00000000
R1	0x00000000
R2	0x00345678
R3	0x87654321
R4	0x00000012
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000010
CPSR	0x000000D3
SPSR	0x00000000
Supervisor	
Abort	
Undefined	
Internal	
PC \$	0x00000010
Mode	Supervisor
States	8
Sec	0.00000067

Disassembly

```

0x00000008 E3A04012 MOV R4,#0x00000012
7:          BIC r2,r2,#0xFF000000
8:
0x0000000C E3C224FF BIC R2,R2,#0xFF000000
9:          LDR r2,=0x12345678
0x00000010 E59F207C LDR R2,[PC,#0x007C]
10:         LDR r2,=0x87654321
11:
12:
13:
14:
15:
16:
17:
18:
19:
20:
21:
22:
23:
24:
25:
26:
27:
28:
29:
30:
31:

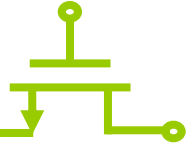
```

HW2-Part3-2-v2.s

```

1      AREA LIN_612450097, CODE, READONLY
2
3      ENTRY
4
5      LDR r2,=0x12345678
6      LDR r3,=0x87654321
7      LDR r4,=0x00000012
8      BIC r2,r2,#0xFF000000
9
10     LDR r2,=0x12345678
11     LDR r3,=0x87654321
12     LDR r4,=0x00000012
13     LSL r2,r3,#4
14
15     LDR r2,=0x12345678
16     LDR r3,=0x87654321
17     LDR r4,=0x00000012
18     LSL r2,r2,r4
19
20     LDR r2,=0x12345678
21     LDR r3,=0x87654321
22     LDR r4,=0x00000012
23     ROR r2,r2,#12
24
25     LDR r2,=0x12345678
26     LDR r3,=0x87654321
27     LDR r4,=0x00000012
28     AND r2,r2,r3
29
30     LDR r2,=0x12345678
31     LDR r3,=0x87654321
32     LDR r4,=0x00000012

```



Registers

Register	Value
Current	
R0	0x00000000
R1	0x00000000
R2	0x76543210
R3	0x87654321
R4	0x00000012
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000020
CPSR	0x000000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC \$	0x00000020
Mode	Supervisor
States	16
Sec	0.00000133

Disassembly

```

0x00000018 E3A04012 MOV R4,#0x00000012
12:          LSL r2, r3, #4
13:
0x0000001C E1A02203 MOV R2,R3,LSL #4
14:          LDR r2, =0x12345678
0x00000020 E59F206C LDR R2, [PC,#0x006C]
15:          LDR r2, =0x12345678

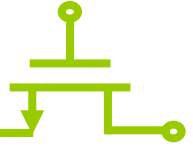
```

HW2-Part3-2-v2.s

```

5          LDR r3, =0x87654321
6          LDR r4, =0x00000012
7          BIC r2, r2, #0xFF000000
8
9          LDR r2, =0x12345678
10         LDR r3, =0x87654321
11         LDR r4, =0x00000012
12         LSL r2, r3, #4
13
14         LDR r2, =0x12345678
15         LDR r3, =0x87654321
16         LDR r4, =0x00000012
17         LSL r2, r2, r4
18
19         LDR r2, =0x12345678
20         LDR r3, =0x87654321
21         LDR r4, =0x00000012
22         ROR r2, r2, #12
23
24         LDR r2, =0x12345678
25         LDR r3, =0x87654321
26         LDR r4, =0x00000012
27         AND r2, r2, r3
28
29         LDR r2, =0x12345678
30         LDR r3, =0x87654321
31         LDR r4, =0x00000012
32         ORR r2, r2, r4
33
34         LDR r2, =0x12345678
35         LDR r3, =0x87654321

```



Registers

Register	Value
Current	
R0	0x00000000
R1	0x00000000
R2	0x59E00000
R3	0x87654321
R4	0x00000012
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000030
CPSR	0x000000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC \$	0x00000030
Mode	Supervisor
States	25
Sec	0.00000208

Disassembly

```

0x00000028 E3A04012 MOV R4,#0x00000012
17:          LSL r2, r2, r4
18:
0x0000002C E1A02412 MOV R2,R2,LSL R4
19:          LDR r2, =0x12
0x00000030 E59F205C LDR R2,[PC,#0x005C
20:          LDR r2, =0x005C

```

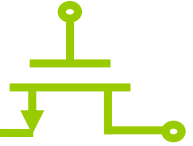
HW2-Part3-2-v2.s

```

10  LDR r3, =0x87654321
11  LDR r4, =0x00000012
12  LSL r2, r3, #4
13
14  LDR r2, =0x12345678
15  LDR r3, =0x87654321
16  LDR r4, =0x00000012
17  LSL r2, r2, r4
18
19  LDR r2, =0x12345678
20  LDR r3, =0x87654321
21  LDR r4, =0x00000012
22  ROR r2, r2, #12
23
24  LDR r2, =0x12345678
25  LDR r3, =0x87654321
26  LDR r4, =0x00000012
27  AND r2, r2, r3
28
29  LDR r2, =0x12345678
30  LDR r3, =0x87654321
31  LDR r4, =0x00000012
32  ORR r2, r2, r4
33
34  LDR r2, =0x12345678
35  LDR r3, =0x87654321
36  LDR r4, =0x00000012
37  EOR r2, r2, r4
38
39  LDR r2, =0x12345678
40  LDR r3, =0x87654321

```





Registers

Register	Value
Current	
R0	0x00000000
R1	0x00000000
R2	0x67812345
R3	0x87654321
R4	0x00000012
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000040
CPSR	0x000000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC \$	0x00000040
Mode	Supervisor
States	33
Sec	0.00000275

Disassembly

```

0x00000038 E3A04012 MOV R4,#0x000000
22: ROR r2, r2, #12
23:
0x0000003C E1A02662 MOV R2,R2,ROR #
24: LDR r2, =0
0x00000040 E59F204C LDR R2,[PC,#0x0
25: LDR r2, =0

```

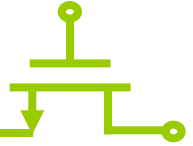
HW2-Part3-2-v2.s

```

15 LDR r3, =0x87654321
16 LDR r4, =0x00000012
17 LSL r2, r2, r4
18
19 LDR r2, =0x12345678
20 LDR r3, =0x87654321
21 LDR r4, =0x00000012
22 ROR r2, r2, #12
23
24 LDR r2, =0x12345678
25 LDR r3, =0x87654321
26 LDR r4, =0x00000012
27 AND r2, r2, r3
28
29 LDR r2, =0x12345678
30 LDR r3, =0x87654321
31 LDR r4, =0x00000012
32 ORR r2, r2, r4
33
34 LDR r2, =0x12345678
35 LDR r3, =0x87654321
36 LDR r4, =0x00000012
37 EOR r2, r2, r4
38
39 LDR r2, =0x12345678
40 LDR r3, =0x87654321
41 LDR r4, =0x00000012
42 BIC r2, r2, r4
43
44 LDR r2, =0x12345678
45 LDR r3, =0x87654321

```





Registers

Register	Value
Current	
R0	0x00000000
R1	0x00000000
R2	0x02244220
R3	0x87654321
R4	0x00000012
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000050
CPSR	0x000000D3
SFSR	0x00000000
Supervisor	
User/System	
Fast Interrupt	
Interrupt	
Abort	
Undefined	
Internal	
PC \$	0x00000050
Mode	Supervisor
States	41
Sec	0.00000342

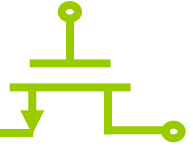
Disassembly

```

0x00000048 E3A04012 MOV R4,#0x00000012
27:      AND r2, r2, r3
28:
0x0000004C E0022003 AND R2,R2,R3
29:      LDR r2, =0x12345678
0x00000050 E59F203C LDR R2,[PC,#0x003C]
30:      LDR r2, =0x12345678
20:      LDR r3, =0x87654321
21:      LDR r4, =0x00000012
22:      ROR r2, r2, #12
23:
24:      LDR r2, =0x12345678
25:      LDR r3, =0x87654321
26:      LDR r4, =0x00000012
27:      AND r2, r2, r3
28:
29:      LDR r2, =0x12345678
30:      LDR r3, =0x87654321
31:      LDR r4, =0x00000012
32:      ORR r2, r2, r4
33:
34:      LDR r2, =0x12345678
35:      LDR r3, =0x87654321
36:      LDR r4, =0x00000012
37:      EOR r2, r2, r4
38:
39:      LDR r2, =0x12345678
40:      LDR r3, =0x87654321
41:      LDR r4, =0x00000012
42:      BIC r2, r2, r4
43:
44:      LDR r2, =0x12345678
45:      LDR r3, =0x87654321
46:      LDR r4, =0x00000012
47:      EOR r2, r2, r3, ROR #7
48:
49: stop   B      stop
50:      END

```





Registers

Register	Value
Current	
R0	0x00000000
R1	0x00000000
R2	0x1234567A
R3	0x87654321
R4	0x00000012
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000060
CPSR	0x000000D3
SPSR	0x00000000
Supervisor	
Abort	
Undefined	
Internal	
PC \$	0x00000060
Mode	Supervisor
States	49
Sec	0.00000408

Disassembly

```

0x00000058 E3A04012 MOV R4,#0x00000012
32:          ORR r2,r2,r4
33:
0x0000005C E1822004 ORR R2,R2,R4
34:          LDR r2,=0x12
0x00000060 E59F202C LDR R2,[PC,#0x002C
35:          LDR r2,=0x00

```

HW2-Part3-2-v2.s

```

21      LDR    r4, =0x00000012
22      ROR    r2, r2, #12
23
24      LDR    r2, =0x12345678
25      LDR    r3, =0x87654321
26      LDR    r4, =0x00000012
27      AND    r2, r2, r3
28
29      LDR    r2, =0x12345678
30      LDR    r3, =0x87654321
31      LDR    r4, =0x00000012
32      ORR    r2, r2, r4
33
34      LDR    r2, =0x12345678
35      LDR    r3, =0x87654321
36      LDR    r4, =0x00000012
37      EOR    r2, r2, r4
38
39      LDR    r2, =0x12345678
40      LDR    r3, =0x87654321
41      LDR    r4, =0x00000012
42      BIC    r2, r2, r4
43
44      LDR    r2, =0x12345678
45      LDR    r3, =0x87654321
46      LDR    r4, =0x00000012
47      EOR    r2, r2, r3, ROR #7
48
49 stop    B      stop
50      END

```



Registers

Register	Value
Current	
R0	0x00000000
R1	0x00000000
R2	0x1234566A
R3	0x87654321
R4	0x00000012
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000070
CPSR	0x000000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC \$	0x00000070
Mode	Supervisor
States	57
Sec	0.00000475

Disassembly

```

0x00000068 E3A04012 MOV R4,#0x00000012
37: EOR r2, r2, r4
38:
0x0000006C E0222004 EOR R2,R2,R4
39: LDR r2, =0x1234566A
0x00000070 E59F201C LDR R2,[PC,#0x001C]
40: LDR r2, =0x87654321
41:
42:
43:
44: LDR r2, =0x12345678
45: LDR r3, =0x87654321
46: LDR r4, =0x00000012
47: EOR r2, r2, r3, ROR #7
48:
49: stop B stop
50: END

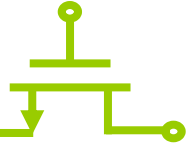
```

HW2-Part3-2-v2.s

```

21 LDR r4, =0x00000012
22 ROR r2, r2, #12
23
24 LDR r2, =0x12345678
25 LDR r3, =0x87654321
26 LDR r4, =0x00000012
27 AND r2, r2, r3
28
29 LDR r2, =0x12345678
30 LDR r3, =0x87654321
31 LDR r4, =0x00000012
32 ORR r2, r2, r4
33
34 LDR r2, =0x12345678
35 LDR r3, =0x87654321
36 LDR r4, =0x00000012
37 EOR r2, r2, r4
38
39 LDR r2, =0x12345678
40 LDR r3, =0x87654321
41 LDR r4, =0x00000012
42 BIC r2, r2, r4
43
44 LDR r2, =0x12345678
45 LDR r3, =0x87654321
46 LDR r4, =0x00000012
47 EOR r2, r2, r3, ROR #7
48
49 stop B stop
50 END

```



Registers

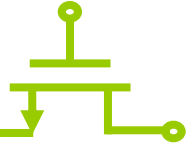
Register	Value
Current	
R0	0x00000000
R1	0x00000000
R2	0x12345678
R3	0x87654321
R4	0x00000012
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000080
CPSR	0x000000D3
SPSR	0x00000000
Supervisor	
Abort	
Undefined	
Internal	
PC \$	0x00000080
Mode	Supervisor
States	65
Sec	0.00000542

Disassembly

```

0x00000078 E3A04012 MOV R4,#0x00000012
42: BIC r2, r2, r4
43:
0x0000007C E1C22004 BIC R2,R2,R4
44: LDR r2, =0x12
0x00000080 E59F200C LDR R2,[PC,#0x000C
45: LDR r2, =0x12
21 LDR r4, =0x00000012
22 ROR r2, r2, #12
23
24 LDR r2, =0x12345678
25 LDR r3, =0x87654321
26 LDR r4, =0x00000012
27 AND r2, r2, r3
28
29 LDR r2, =0x12345678
30 LDR r3, =0x87654321
31 LDR r4, =0x00000012
32 ORR r2, r2, r4
33
34 LDR r2, =0x12345678
35 LDR r3, =0x87654321
36 LDR r4, =0x00000012
37 EOR r2, r2, r4
38
39 LDR r2, =0x12345678
40 LDR r3, =0x87654321
41 LDR r4, =0x00000012
42 BIC r2, r2, r4
43
44 LDR r2, =0x12345678
45 LDR r3, =0x87654321
46 LDR r4, =0x00000012
47 EOR r2, r2, r3, ROR #7
48
49 stop B stop
50 END

```



Registers

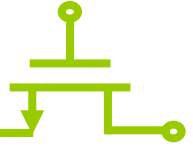
Register	Value
Current	
R0	0x00000000
R1	0x00000000
R2	0x513A9CFE
R3	0x87654321
R4	0x00000012
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000090
CPSR	0x000000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC \$	0x00000090
Mode	Supervisor
States	73
Sec	0.00000608

Disassembly

```

0x000000088 E3A04012 MOV R4,#0x00000012
47: EOR r2, r2, r3, ROR #7
48:
0x00000008C E02223E3 EOR R2,R2,R3,ROR #7
49: stop B stop
->0x000000090 EAEFFFFE B 0x000000090
0x000000094 12345678 EORNEB R5,R4,#0x00000000
<
HW2-Part3-2-v2.s
21 LDR r4, =0x00000012
22 ROR r2, r2, #12
23
24 LDR r2, =0x12345678
25 LDR r3, =0x87654321
26 LDR r4, =0x00000012
27 AND r2, r2, r3
28
29 LDR r2, =0x12345678
30 LDR r3, =0x87654321
31 LDR r4, =0x00000012
32 ORR r2, r2, r4
33
34 LDR r2, =0x12345678
35 LDR r3, =0x87654321
36 LDR r4, =0x00000012
37 EOR r2, r2, r4
38
39 LDR r2, =0x12345678
40 LDR r3, =0x87654321
41 LDR r4, =0x00000012
42 BIC r2, r2, r4
43
44 LDR r2, =0x12345678
45 LDR r3, =0x87654321
46 LDR r4, =0x00000012
47 EOR r2, r2, r3, ROR #7
48
49 stop B stop
50 END

```



Registers

Register	Value
Current	
R0	0xFFFFFFFF
R1	0x00000000
R2	0x00000000
R3	0x00000000
R4	0x00000000
R5	0x00000000
R6	0xABCD8765
R7	0x5432789B
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000010
CPSR	0x000000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC \$	0x00000010
Mode	Supervisor
States	6
Sec	0.00000050

Disassembly

```

0x00000008 E0267000 EOR      R7,R6,R0
7:          ADD      r7, #1
8:          ; (2)
0x0000000C E2877001 ADD      R7,R7,#0x00000001
9:          LDR      r6, =0xABCD8765
0x00000010 E59F6034 LDR      R6,[PC,#0x0034]
10:         LDR      r1, =0x2022 ; 0x00100000000100010
<

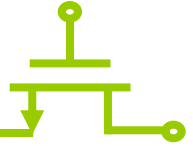
```

HW2-Part3-3-v1.s

```

1      AREA LIN_612450097, CODE, READONLY
2      ENTRY
3      ; (1)
4      LDR      r6, =0xABCD8765
5      LDR      r0, =0xFFFFFFFF
6      EOR      r7, r6, r0
7      ADD      r7, #1
8      ; (2)
9      LDR      r6, =0xABCD8765
10     LDR      r1, =0x2022 ; 0b00100000000100010
11     ORR      r6, r1
12     ; (3)
13     LDR      r6, =0xABCD8765
14     LDR      r2, =0x1011 ; 0b00010000000010001
15     BIC      r6, r2
16     ; (4)
17     LDR      r6, =0xABCD8765
18     LDR      r3, =0x910 ; 0b1001000010000
19     EOR      r6, r3
20     ; (5)
21     LDR      r0, =0xBEEFABCD
22     LDR      r4, =0xFFFF
23     LDR      r5, =0x5555
24     BIC      r0, r4
25     ORR      r0, r5
26
27 stop    B      stop
28     END

```



Registers

Register	Value
Current	
R0	0xFFFFFFFF
R1	0x00002022
R2	0x00000000
R3	0x00000000
R4	0x00000000
R5	0x00000000
R6	0xABCD767
R7	0x5432789B
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x0000001C
CPSR	0x000000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC \$	0x0000001C
Mode	Supervisor
States	13
Sec	0.00000108

Disassembly

```

0x00000018 E1866001 ORR      R6,R6,R1
13:                                LDR      r6, =0xABCD8765
0x0000001C E59F6028 LDR      R6,[PC,#0x0028]
14:                                LDR      r2, =0x1011      ; 0b000100000
0x00000020 E59F202C LDR      R2,[PC,#0x002C]
15:                                BIC      r6, r2
16:                                . . .

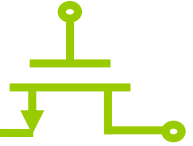
```

HW2-Part3-3-v1.s

```

1      AREA LIN_612450097, CODE, READONLY
2      ENTRY
3      ; (1)
4      LDR      r6, =0xABCD8765
5      LDR      r0, =0xFFFFFFFF
6      EOR      r7, r6, r0
7      ADD      r7, #1
8      ; (2)
9      LDR      r6, =0xABCD8765
10     LDR      r1, =0x2022      ; 0b001000000001000010
11     ORR      r6, r1
12     ; (3)
13     LDR      r6, =0xABCD8765
14     LDR      r2, =0x1011      ; 0b00010000000010001
15     BIC      r6, r2
16     ; (4)
17     LDR      r6, =0xABCD8765
18     LDR      r3, =0x910       ; 0b1001000010000
19     EOR      r6, r3
20     ; (5)
21     LDR      r0, =0xBEEFABCD
22     LDR      r4, =0xFFFF
23     LDR      r5, =0x5555
24     BIC      r0, r4
25     ORR      r0, r5
26
27 stop      B      stop
28     END

```

Registers

Register	Value
Current	
R0	0xFFFFFFFF
R1	0x00002022
R2	0x00001011
R3	0x00000000
R4	0x00000000
R5	0x00000000
R6	0xABCD8764
R7	0x5432789B
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000028
CPSR	0x000000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC \$	0x00000028
Mode	Supervisor
States	20
Sec	0.00000167

Disassembly

```

0x00000020 E59F202C LDR      R2,[PC,#0x002C]
15:                                     BIC      r6, r2
16:                                     ; (4)
0x00000024 E1C66002 BIC      R6,R6,R2
17:                                     LDR      r6, =0xABCD8765
0x00000028 E59F601C LDR      R6,[PC,#0x001C]
18:                                     LDR      r3, =0x910
19:                                     ; 0b10010000

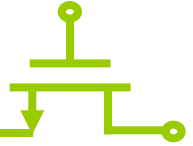
```

HW2-Part3-3-v1.s

```

1      AREA LIN_612450097, CODE, READONLY
2      ENTRY
3      ; (1)
4      LDR      r6, =0xABCD8765
5      LDR      r0, =0xFFFFFFFF
6      EOR      r7, r6, r0
7      ADD      r7, #1
8      ; (2)
9      LDR      r6, =0xABCD8765
10     LDR      r1, =0x2022      ; 0b00100000000100010
11     ORR      r6, r1
12     ; (3)
13     LDR      r6, =0xABCD8765
14     LDR      r2, =0x1011      ; 0b00010000000010001
15     BIC      r6, r2
16     ; (4)
17     LDR      r6, =0xABCD8765
18     LDR      r3, =0x910      ; 0b100100010000
19     EOR      r6, r3
20     ; (5)
21     LDR      r0, =0xBEEFABCD
22     LDR      r4, =0xFFFF
23     LDR      r5, =0x5555
24     BIC      r0, r4
25     ORR      r0, r5
26
27 stop    B      stop
28     END

```



Registers

Register	Value
Current	
R0	0xFFFFFFFF
R1	0x00002022
R2	0x00001011
R3	0x00000910
R4	0x00000000
R5	0x00000000
R6	0xABCD8E75
R7	0x5432789B
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000034
CPSR	0x000000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC \$	0x00000034
Mode	Supervisor
States	25
Sec	0.00000208

Disassembly

```

0x00000030 E0266003 EOR R6,R6,R3
21: LDR r0, =0xBEEFABCD
0x00000034 E59F001C LDR R0,[PC,#0x001C]
22: LDR r4, =0xFFFF
0x00000038 E59F401C LDR R4,[PC,#0x001C]
23: LDR r5, =0x5555
0x0000003C E59F801C LDR R5,[PC,#0x001C]

```

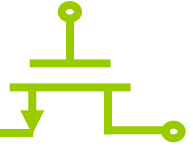
HW2-Part3-3-v1.s

```

1 AREA LIN_612450097, CODE, READONLY
2 ENTRY
3 ; (1)
4 LDR r6, =0xABCD8765
5 LDR r0, =0xFFFFFFFF
6 EOR r7, r6, r0
7 ADD r7, #1
8 ; (2)
9 LDR r6, =0xABCD8765
10 LDR r1, =0x2022 ; 0b00100000000100010
11 ORR r6, r1
12 ; (3)
13 LDR r6, =0xABCD8765
14 LDR r2, =0x1011 ; 0b00010000000010001
15 BIC r6, r2
16 ; (4)
17 LDR r6, =0xABCD8765
18 LDR r3, =0x910 ; 0b100100010000
19 EOR r6, r3
20 ; (5)
21 LDR r0, =0xBEEFABCD
22 LDR r4, =0xFFFF
23 LDR r5, =0x5555
24 BIC r0, r4
25 ORR r0, r5
26
27 stop B stop
28 END

```





Registers

Register	Value
Current	
R0	0xBEEF5555
R1	0x00002022
R2	0x00001011
R3	0x00000910
R4	0x0000FFFF
R5	0x00005555
R6	0xABCD8E75
R7	0x5432789B
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000048
CPSR	0x000000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC \$	0x00000048
Mode	Supervisor
States	36
Sec	0.00000300

Disassembly

```

25:                                ORR        r0, r5
26:                                0x00000044 E1800005 ORR        R0,R0,R5
27: stop        B        stop
0x00000048 EAFFFFFF B        0x00000048
0x0000004C ABCD8765 BLGE    0xFF361DE8
0x00000050 00000000 ANDEQ   R0,R0,R0,LSR, #32

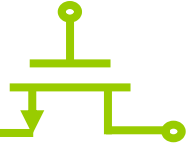
```

HW2-Part3-3-v1.s

```

1      AREA LIN_612450097, CODE, READONLY
2      ENTRY
3      ; (1)
4      LDR    r6, =0xABCD8765
5      LDR    r0, =0xFFFFFFFF
6      EOR    r7, r6, r0
7      ADD    r7, #1
8      ; (2)
9      LDR    r6, =0xABCD8765
10     LDR    r1, =0x2022      ; 0b00100000000100010
11     ORR    r6, r1
12     ; (3)
13     LDR    r6, =0xABCD8765
14     LDR    r2, =0x1011     ; 0b00010000000010001
15     BIC    r6, r2
16     ; (4)
17     LDR    r6, =0xABCD8765
18     LDR    r3, =0x910      ; 0b1001000010000
19     EOR    r6, r3
20     ; (5)
21     LDR    r0, =0xBEEFABCD
22     LDR    r4, =0xFFFF
23     LDR    r5, =0x5555
24     BIC    r0, r4
25     ORR    r0, r5
26
27     stop   B        stop
28     END

```



Registers

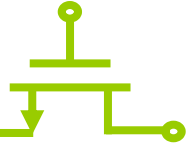
Register	Value
Current	
R0	0xFFFFFFFF
R1	0x00000000
R2	0x00000000
R3	0x00000000
R4	0x00000000
R5	0x00000000
R6	0xABCD8765
R7	0x5432789B
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000010
CPSR	0x000000D3
SPSR	0x00000000
+ User/System	
+ Fast Interrupt	
+ Interrupt	
+ Supervisor	
+ Abort	
+ Undefined	
- Internal	
PC \$	0x00000010
Mode	Supervisor
States	6
Sec	0.00000050

Disassembly

```

0x00000008 E0267000 EOR      R7,R6,R0
7:          ADD      r7, #1
8:          ; (2)
0x0000000C E2877001 ADD      R7,R7,#0x00000001
9:          LDR      r1, =0x2022      ; 0b00100001000010001000100010001000
0x00000010 E59F102C LDR      R1,[PC,#0x002C]
10:         ORR      r6, r1
11:         ; (3)
12:         LDR      r2, =0x1011      ; 0b00010000000010001
13:         BIC      r6, r2
14:         ; (4)
15:         LDR      r3, =0x910       ; 0b100100010000
16:         EOR      r6, r3
17:         ; (5)
18:         LDR      r0, =0xBEEFABCD
19:         LDR      r4, =0xFFFF
20:         LDR      r5, =0x5555
21:         BIC      r0, r4
22:         ORR      r0, r5
23:
24 stop    B        stop
25        END

```



Registers

Register	Value
Current	
R0	0xFFFFFFFF
R1	0x00002022
R2	0x00000000
R3	0x00000000
R4	0x00000000
R5	0x00000000
R6	0xABCD8767
R7	0x5432789B
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000018
CPSR	0x000000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC \$	0x00000018
Mode	Supervisor
States	10
Sec	0.00000083

Disassembly

```

0x00000010 E59F102C LDR      R1,[PC,#0x002C]
10:                ORR      r6, r1
11:                ; (3)
0x00000014 E1866001 ORR      R6,R6,R1
12:                LDR      r2, =0x1011    ; 0b0001000
0x00000018 E59F2028 LDR      R2,[PC,#0x0028]
13:                BIC      r6, r2
14:                ; (4)
0x0000001C E59F3028 LDR      R3,[PC,#0x0028]
15:                LDR      r3, =0x910      ; 0b100100010000
16:                EOR      r6, r3
17:                ; (5)
18:                LDR      r0, =0xBEEFABCD
19:                LDR      r4, =0xFFFF
20:                LDR      r5, =0x5555
21:                BIC      r0, r4
22:                ORR      r0, r5
23:
24 stop          B          stop
25              END

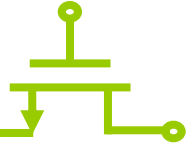
```

HW2-Part3-3-v2.s

```

1      AREA LIN_612450097, CODE, READONLY
2      ENTRY
3      ; (1)
4      LDR      r6, =0xABCD8765
5      LDR      r0, =0xFFFFFFFF
6      EOR      r7, r6, r0
7      ADD      r7, #1
8      ; (2)
9      LDR      r1, =0x2022      ; 0b00100000000100010
10     ORR      r6, r1
11     ; (3)
12     LDR      r2, =0x1011      ; 0b00010000000010001
13     BIC      r6, r2
14     ; (4)
15     LDR      r3, =0x910      ; 0b100100010000
16     EOR      r6, r3
17     ; (5)
18     LDR      r0, =0xBEEFABCD
19     LDR      r4, =0xFFFF
20     LDR      r5, =0x5555
21     BIC      r0, r4
22     ORR      r0, r5
23
24 stop          B          stop
25              END

```



Registers

Register	Value
Current	
R0	0xFFFFFFFF
R1	0x00002022
R2	0x00001011
R3	0x00000000
R4	0x00000000
R5	0x00000000
R6	0xABCD8765
R7	0x5432789B
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000020
CPSR	0x000000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC \$	0x00000020
Mode	Supervisor
States	14
Sec	0.00000117

Disassembly

```

0x00000018 E59F2028 LDR      R2,[PC,#0x0028]
13:          BIC          r6, r2
14:          ; (4)
0x0000001C E1C66002 BIC      R6,R6,R2
15:          LDR          r3, =0x910      ; 0b100100
0x00000020 E3A03E91 MOV      R3,#0x00000910
16:          EOR          r6, r3
17:          ; (5)
0x00000024 E3A03E91 MOV      R3,#0x00000910
18:          LDR          r0, =0xBEEFABCD
19:          LDR          r4, =0xFFFF
20:          LDR          r5, =0x5555
21:          BIC          r0, r4
22:          ORR          r0, r5
23:          ; (6)
24 stop    B          stop
25          END

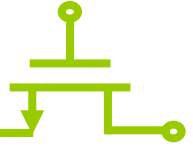
```

HW2-Part3-3-v2.s

```

1      AREA LIN_612450097, CODE, READONLY
2      ENTRY
3      ; (1)
4      LDR      r6, =0xABCD8765
5      LDR      r0, =0xFFFFFFFF
6      EOR      r7, r6, r0
7      ADD      r7, #1
8      ; (2)
9      LDR      r1, =0x2022      ; 0b00100000000100010
10     ORR      r6, r1
11     ; (3)
12     LDR      r2, =0x1011      ; 0b00010000000010001
13     BIC      r6, r2
14     ; (4)
15     LDR      r3, =0x910      ; 0b100100010000
16     EOR      r6, r3
17     ; (5)
18     LDR      r0, =0xBEEFABCD
19     LDR      r4, =0xFFFF
20     LDR      r5, =0x5555
21     BIC      r0, r4
22     ORR      r0, r5
23     ; (6)
24 stop    B          stop
25          END

```



Registers

Register	Value
Current	
R0	0xFFFFFFFF
R1	0x00002022
R2	0x00001011
R3	0x00000910
R4	0x00000000
R5	0x00000000
R6	0xABCDAB76
R7	0x5432789B
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000028
CPSR	0x000000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC \$	0x00000028
Mode	Supervisor
States	16
Sec	0.00000133

Disassembly

```

0x00000020 E3A03E91 MOV R3,#0x00000910
16: EOR r6, r3
17: ; (5)
0x00000024 E0266003 EOR R6,R6,R3
18: LDR r0, =0xBEEFABCD
0x00000028 E59F001C LDR R0,[PC,#0x001C]
19: LDR r4, =0xFFFF

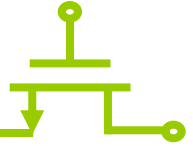
```

HW2-Part3-3-v2.s

```

1 AREA LIN_612450097, CODE, READONLY
2 ENTRY
3 ; (1)
4 LDR r6, =0xABCD8765
5 LDR r0, =0xFFFFFFFF
6 EOR r7, r6, r0
7 ADD r7, #1
8 ; (2)
9 LDR r1, =0x2022 ; 0b0010000000100010
10 ORR r6, r1
11 ; (3)
12 LDR r2, =0x1011 ; 0b0001000000010001
13 BIC r6, r2
14 ; (4)
15 LDR r3, =0x910 ; 0b100100010000
16 EOR r6, r3
17 ; (5)
18 LDR r0, =0xBEEFABCD
19 LDR r4, =0xFFFF
20 LDR r5, =0x5555
21 BIC r0, r4
22 ORR r0, r5
23
24 stop B stop
25 END

```



Registers

Register	Value
Current	
R0	0xBEEF5555
R1	0x00002022
R2	0x00001011
R3	0x00000910
R4	0x0000FFFF
R5	0x00005555
R6	0xABCDAB76
R7	0x5432789B
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x0000003C
CPSR	0x000000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC \$	0x0000003C
Mode	Supervisor
States	27
Sec	0.00000225

Disassembly

24: stop B stop

0x0000003C EFFFFFFE B 0x0000003C

0x00000040 ABCD8765 BLGE 0xFF361DDC

0x00000044 00002022 ANDEQ R2,R0,R2,LSR #32

0x00000048 00001011 ANDEQ R1,R0,R1,LSL R0

0x0000004C BEEFABCD CDPLT p11,14,CR10,CPC,CR13,6

0x00000050 0000FFFF 00000000

<

HW2-Part3-3-v2.s

```

1      AREA LIN_612450097, CODE, READONLY
2      ENTRY
3      ; (1)
4      LDR    r6, =0xABCD8765
5      LDR    r0, =0xFFFFFFFF
6      EOR    r7, r6, r0
7      ADD    r7, #1
8      ; (2)
9      LDR    r1, =0x2022      ; 0b00100000000100010
10     ORR    r6, r1
11     ; (3)
12     LDR    r2, =0x1011      ; 0b00010000000010001
13     BIC    r6, r2
14     ; (4)
15     LDR    r3, =0x910       ; 0b100100010000
16     EOR    r6, r3
17     ; (5)
18     LDR    r0, =0xBEEFABCD
19     LDR    r4, =0xFFFF
20     LDR    r5, =0x5555
21     BIC    r0, r4
22     ORR    r0, r5
23
24 stop B stop
25     END

```


Q&A

Thanks for your attention !!