

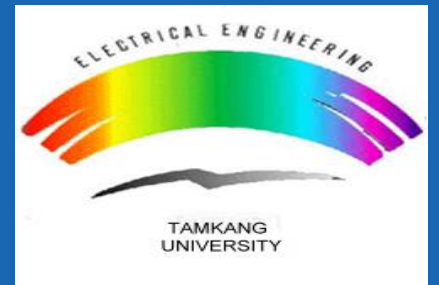
第11次組語實習課

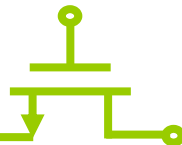
學生：林培瑋

2023 Advanced Mixed-Operation System (AMOS) Lab.



Tamkang University
Department of Electrical and Computer Engineering
No.151, Yingzhuan Rd., Tamsui Dist., New Taipei City 25137, Taiwan (R.O.C.)





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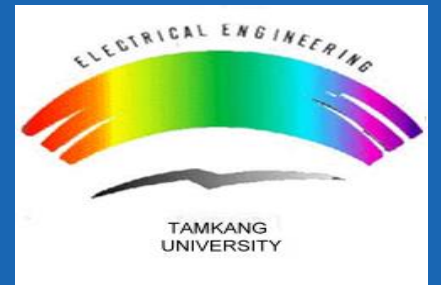


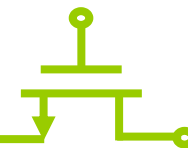
第三次作業

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❖ 八個結果截圖(80%)

- 第一次迴圈(五個截圖)
- 第二~四次迴圈(各一個)

❖ 四個手算過程(20%)

不計分

程式碼沒有學號、姓名

暫存器模糊不清楚

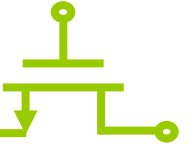
暫存器視窗沒拉開

暫存器數值不正確

➤ 以最後繳交的版本為準

➤ 遲交者成績 = 原始成績*0.5





Registers

Register	Value
R0	0x000000B5
R1	0x000000A5
R2	0x00000000
R3	0x00000000
R4	0x400000F0
R5	0x00000004
R6	0x40000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x0000002C
CPSR	0x000000D3
SFSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC	0x0000002C
Mode	Supervisor
States	13
Sec	0.00000108

Disassembly

```

0x00000028 E2042001 AND R2,R4,#0x00000001
21: MOV r4, r0
0x0000002C E1A04000 MOV R4,R0
22: EOR r4, r4, r0, ROR #2
0x00000030 E0244160 EOR R4,R4,R0,ROR #2
23: EOR r4, r4, r0, ROR #3
0x00000034 E0244150 EOR R4,R4,R0,ROR #3

```

HW_3.s

```

10 LDRB r0, [r1], #1
11
12 ; calculate c0
13 MOV r4, r0
14 EOR r4, r4, r0, ROR #1
15 EOR r4, r4, r0, ROR #3
16 EOR r4, r4, r0, ROR #4
17 EOR r4, r4, r0, ROR #6
18 AND r2, r4, #1
19
20 ; calculate c1
21 MOV r4, r0
22 EOR r4, r4, r0, ROR #2
23 EOR r4, r4, r0, ROR #3
24 EOR r4, r4, r0, ROR #5
25 EOR r4, r4, r0, ROR #6
26 AND r4, r4, #1
27 ORR r2, r2, r4, LSL #1
28
29 ; calculate c2
30 ROR r4, r0, #1
31 EOR r4, r4, r0, ROR #2
32 EOR r4, r4, r0, ROR #3
33 EOR r4, r4, r0, ROR #7
34 AND r4, r4, #1
35 ORR r2, r2, r4, ROR #29
36
37 ; calculate c3
38 ROR r4, r0, #4
39 EOR r4, r4, r0, ROR #5
40 EOR r4, r4, r0, ROR #6
41 EOR r4, r4, r0, ROR #7
42 AND r4, r4, #1

```

Memory 1

Address: 0x40000000

40000000:	00 00
40000018:	00 00
40000030:	00 00
40000048:	00 00

Call Stack + Locals Memory 1

3次作業\\HW_3\\Objects\\HW_3.axf"



解答(2/8)



Registers

Register	Value
R0	0x000000B5
R1	0x000000A5
R2	0x00000000
R3	0x00000000
R4	0x00000001
R5	0x00000004
R6	0x40000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000044
CPSR	0x000000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC \$	0x00000044
Mode	Supervisor
State	19
Sec	0.00000158

Disassembly

```

27:      ORR      r2, r2, r4, LSL #1
28:
29:      ; caculate c2
0x00000044 E1822084 ORR      R2,R2,R4,LSL #1
30:      ROR      r4, r0, #1
0x00000048 E1A040E0 MOV      R4,R0,ROR #1
31:      ROR      r4, r4, r0, ROR #1

```

HW_3.s

```

16:      EOR      r4, r4, r0, ROR #4
17:      EOR      r4, r4, r0, ROR #6
18:      AND      r2, r4, #1
19:
20:      ; caculate c1
21:      MOV      r4, r0
22:      EOR      r4, r4, r0, ROR #2
23:      EOR      r4, r4, r0, ROR #3
24:      EOR      r4, r4, r0, ROR #5
25:      EOR      r4, r4, r0, ROR #6
26:      AND      r4, r4, #1
27:      ORR      r2, r2, r4, LSL #1
28:
29:      ; caculate c2
30:      ROR      r4, r0, #1
31:      EOR      r4, r4, r0, ROR #2
32:      EOR      r4, r4, r0, ROR #3
33:      EOR      r4, r4, r0, ROR #7
34:      AND      r4, r4, #1
35:      ORR      r2, r2, r4, ROR #29
36:
37:      ; caculate c3
38:      ROR      r4, r0, #4
39:      EOR      r4, r4, r0, ROR #5
40:      EOR      r4, r4, r0, ROR #6
41:      EOR      r4, r4, r0, ROR #7
42:      AND      r4, r4, #1
43:      ORR      r2, r2, r4, ROR #25
44:
45:      ; build the final 12-bit result
46:      AND      r4, r0, #1
47:      ORR      r2, r2, r4, LSL #2
48:      BIC      r4, r0, #0xF1
49:      ORR      r2, r2, r4, LSL #3
50:      ROR      r4, r0, #4

```

Memory 1

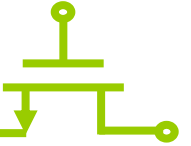
Address: 0x40000000

0x40000000:	00 00
0x40000018:	00 00
0x40000030:	00 00
0x40000048:	00 00

Call Stack + Locals | Memory 1

作業\\HW_3\\Objects\\HW_3.axf"





Registers

Register	Value
R0	0x000000B5
R1	0x000000A5
R2	0x00000002
R3	0x00000000
R4	0x00000000
R5	0x00000004
R6	0x40000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x0000005C
CPSR	0x000000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC \$	0x0000005C
Mode	Supervisor
States	25
Sec	0.00000208

Disassembly

```

0x00000058 E2044001 AND R4,R4,#0x00000001
35:          ORR      r2, r2, r4, ROR #29
36:
37:          ; caculate c3
0x0000005C E1822EE4 ORR R2,R2,R4,ROR #29
38:          ROR      r4, r0, #4
39:
40:          ; caculate c2
41:          ROR      r4, r0, #1
42:          EOR      r4, r4, r0, ROR #2
43:          EOR      r4, r4, r0, ROR #3
44:          EOR      r4, r4, r0, ROR #7
45:          AND      r4, r4, #1
46:          ORR      r2, r2, r4, ROR #29
47:
48:          ; caculate c3
49:          ROR      r4, r0, #4
50:          EOR      r4, r4, r0, ROR #5
51:          EOR      r4, r4, r0, ROR #6
52:          EOR      r4, r4, r0, ROR #7
53:          AND      r4, r4, #1
54:          ORR      r2, r2, r4, ROR #25
55:
56:          ; build the final 12-bit result
57:          AND      r4, r0, #1
58:          ORR      r2, r2, r4, LSL #2
59:          BIC      r4, r0, #0xF1
60:          ORR      r2, r2, r4, LSL #3
61:          BIC      r4, r0, #0x0F
62:          ORR      r2, r2, r4, LSL #4
63:
64:          STR      r2, [r6], #4
65:
66:          SUB      r5, r5, #1
67:          CMP      r5, #0
68:          BGT      LOOP

```

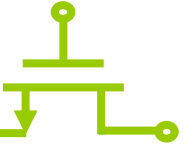
Memory 1

Address: 0x40000000

0x40000000:	00 00
0x40000018:	00 00
0x40000030:	00 00
0x40000048:	00 00

作業\\HW_3\\Objects\\HW_3.axf"





Registers

Register	Value
R0	0x000000B5
R1	0x000000A5
R2	0x00000002
R3	0x00000000
R4	0x00000001
R5	0x00000004
R6	0x40000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000074
CPSR	0x000000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC \$	0x00000074
Mode	Supervisor
States	31
Sec	0.00000258

Disassembly

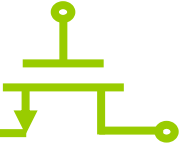
```

0x00000070 E2044001 AND      R4,R4,#0x00000001
43:          ORR      r2, r2, r4, ROR      #25
44:
45:          ; build the final 12-bit result
0x00000074 E1822CE4 ORR      R2,R2,R4,ROR #25
46:          AND      r4, r0, #1
47:
48:
49:
50:
51:
52:
53:
54:
55:
56:
57:
58:
59: stop      B          stop
60:          ALIGN
61:
62: arraya
63:          DCB      0xB5
64:          DCB      0xAA
65:          DCB      0x55
66:          DCB      0x33
        
```

Memory 1

Address: 0x40000000

0x40000000	00 00
0x40000018	00 00
0x40000030	00 00
0x40000048	00 00



Registers

Register	Value
R0	0x000000B5
R1	0x000000A5
R2	0x000000A6
R3	0x00000000
R4	0x000000B0
R5	0x00000003
R6	0x40000004
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x0000000C
CPSR	0x200000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC \$	0x0000000C
Mode	Supervisor
State	45
Sec	0.00000375

Disassembly

```

0x00000008 E3A06101 MOV R6,#0x40000000
9:          MOV r2, #0 ; holds value to
->0x0000000C E3A02000 MOV R2,#0x00000000
10:         LDRB r0, [r1], #1
11:
12:         ; caculate c0
0x00000010 E3A02001 LDRB r0, [r1], #0x0001

```

HW_3.s

```

1      AREA LIN612450097, CODE, READONLY
2
3      ENTRY
4
5      ADR r1, arraya
6      MOV r5, #4 ; counter
7      LDR r6, =0x40000000 ; memory initial address
8
9      LOOP
10     MOV r2, #0 ; holds value to be transmitted
11     LDRB r0, [r1], #1
12
13     ; caculate c0
14     MOV r4, r0
15     EOR r4, r4, r0, ROR #1
16     EOR r4, r4, r0, ROR #3
17     EOR r4, r4, r0, ROR #4
18     EOR r4, r4, r0, ROR #6
19     AND r2, r4, #1
20
21     ; caculate c1
22     MOV r4, r0
23     EOR r4, r4, r0, ROR #2
24     EOR r4, r4, r0, ROR #3
25     EOR r4, r4, r0, ROR #5
26     EOR r4, r4, r0, ROR #6
27     AND r4, r4, #1
28     ORR r2, r2, r4, LSL #1
29
30     ; caculate c2
31     ROR r4, r0, #1
32     EOR r4, r4, r0, ROR #2
33     EOR r4, r4, r0, ROR #3
34     EOR r4, r4, r0, ROR #7
35     AND r4, r4, #1
36     ORR r2, r2, r4, ROR #6

```

Memory 1

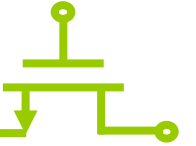
Address: 0x40000000

0x40000000:	A6 0B 00
0x40000018:	00 00
0x40000030:	00 00
0x40000048:	00 00

Call Stack + Locals | Memory 1

作業\\HW_3\\Objects\\HW_3.axf"





Registers

Register	Value
R0	0x000000AA
R1	0x000000A6
R2	0x00000058
R3	0x00000000
R4	0x000000A0
R5	0x00000002
R6	0x40000008
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x0000000C
CPSR	0x200000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC \$	0x0000000C
Mode	Supervisor
State	87
Sec	0.00000725

Disassembly

```

0x00000008 E3A06101 MOV R6,#0x40000000
9:          MOV r2, #0 ; holds value to
0x0000000C E3A02000 MOV R2,#0x00000000
10:         LDRB r0, [r1], #1
11:
12:         ; caculate c0
0x00000010 E3A02001 LDRB r0, [r1], #0x0000
<

```

HW_3.s

```

1 AREA LIN612450097, CODE, READONLY
2
3 ENTRY
4
5 ADR r1, arraya
6 MOV r5, #4 ; counter
7 LDR r6, =0x40000000 ; memory initial address
8
9 LOOP
10 MOV r2, #0 ; holds value to be transmitted
11 LDRB r0, [r1], #1
12
13 ; caculate c0
14 MOV r4, r0
15 EOR r4, r4, r0, ROR #1
16 EOR r4, r4, r0, ROR #3
17 EOR r4, r4, r0, ROR #4
18 EOR r4, r4, r0, ROR #6
19 AND r2, r4, #1
20
21 ; caculate c1
22 MOV r4, r0
23 EOR r4, r4, r0, ROR #2
24 EOR r4, r4, r0, ROR #3
25 EOR r4, r4, r0, ROR #5
26 EOR r4, r4, r0, ROR #6
27 AND r4, r4, #1
28 ORR r2, r2, r4, LSL #1
29
30 ; caculate c2
31 ROR r4, r0, #1
32 EOR r4, r4, r0, ROR #2
33 EOR r4, r4, r0, ROR #3
34 EOR r4, r4, r0, ROR #7
35 AND r4, r4, #1
36 ORR r2, r2, r4, ROR #0

```

Memory 1

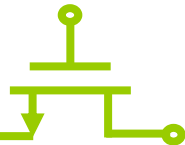
Address: 0x40000000

0x40000000:	A6 0B 00 00 58 0A 00
0x40000018:	00 00
0x40000030:	00 00
0x40000048:	00 00

Call Stack + Locals Memory 1

作業\\HW_3\\Objects\\HW_3.axf"





Registers

Register	Value
R0	0x00000055
R1	0x000000A7
R2	0x0000052F
R3	0x00000000
R4	0x00000050
R5	0x00000001
R6	0x4000000C
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x0000000C
CPSR	0x200000D3
SPSR	0x00000000
User/System	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC \$	0x0000000C
Mode	Supervisor
States	129
Sec	0.00001075

Disassembly

```

0x00000008 E3A06101 MOV R6,#0x40000000
9:          MOV r2, #0 ; holds value to be
0x0000000C E3A02000 MOV R2,#0x00000000
10:         LDRB r0, [r1], #1
11:
12:         ; caculate c0
0x00000010 E4B10001 LDRB R0,[R1],#0x0000

```

HW_3.s

```

1  AREA LIN612450097, CODE, READONLY
2
3  ENTRY
4
5  ADR r1, arraya
6  MOV r5, #4 ; counter
7  LDR r6, =0x40000000 ; memory initial address
8
9  LOOP
10 MOV r2, #0 ; holds value to be transmitted
11 LDRB r0, [r1], #1
12
13 ; caculate c0
14 MOV r4, r0
15 EOR r4, r4, r0, ROR #1
16 EOR r4, r4, r0, ROR #3
17 EOR r4, r4, r0, ROR #4
18 EOR r4, r4, r0, ROR #6
19 AND r2, r4, #1
20
21 ; caculate c1
22 MOV r4, r0
23 EOR r4, r4, r0, ROR #2
24 EOR r4, r4, r0, ROR #3
25 EOR r4, r4, r0, ROR #5
26 EOR r4, r4, r0, ROR #6
27 AND r4, r4, #1
28 ORR r2, r2, r4, LSL #1
29
30 ; caculate c2
31 ROR r4, r0, #1
32 EOR r4, r4, r0, ROR #2
33 EOR r4, r4, r0, ROR #3
34 EOR r4, r4, r0, ROR #7
35 AND r4, r4, #1
36 ORR r2, r2, r4, LSL #1

```

Memory 1

Address: 0x40000000

```

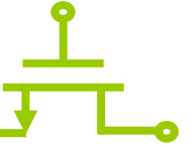
0x40000000: A6 0B 00 00 58 0A 00 00 2F 05 00 00 00 00 00 00 00 00 00 00
0x40000010: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x40000020: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x40000030: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x40000040: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

```

Call Stack + Locals | Memory 1

作業\\HW_3\\Objects\\HW_3.axf"





Registers

Register	Value
Current	
R0	0x000000AA
R1	0x000000A8
R2	0x000000A8
R3	0x00000000
R4	0x000000A0
R5	0x00000000
R6	0x40000010
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x000000A0
CPSR	0x600000D3
SPSR	0x00000000
UserSystem	
Fast Interrupt	
Interrupt	
Supervisor	
Abort	
Undefined	
Internal	
PC \$	0x000000A0
Mode	Supervisor
State	172
Sec	0.00001433

Disassembly

```

59: stop B stop
0x000000A0 EFFFFFFE B 0x000000A0
0x000000A4 AA55AAB5 BGE 0x0156AB80
0x000000A8 00000000 ANDEQ R0,R0,R0
0x000000AC 00000000 ANDEQ R0,R0,R0
0x000000B0 00000000 ANDEQ R0,R0,R0
0x000000B4 00000000 ANDEQ R0,R0,R0

```

HW_3.s

```

35 ORR r2, r2, r4, ROR #29
36
37 ; calculate c3
38 ROR r4, r0, #4
39 EOR r4, r4, r0, ROR #5
40 EOR r4, r4, r0, ROR #6
41 EOR r4, r4, r0, ROR #7
42 AND r4, r4, #1
43 ORR r2, r2, r4, ROR #25
44
45 ; build the final 12-bit result
46 AND r4, r0, #1
47 ORR r2, r2, r4, LSL #2
48 BIC r4, r0, #0xF1
49 ORR r2, r2, r4, LSL #3
50 BIC r4, r0, #0x0F
51 ORR r2, r2, r4, LSL #4
52
53 STR r2, [r6], #4
54
55 SUB r5, r5, #1
56 CMP r5, #0
57 BGT LOOP
58
59 stop B stop
60 ALIGN
61
62 arraya
63 DCB 0xB5
64 DCB 0xAA
65 DCB 0x55
66 DCB 0xAA
67
68 END

```

Memory 1

Address: 0x40000000

0x40000000:	A6 0B 00 00 58 0A 00 00 2F 05 00 00 58 0A 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x40000018:	00 00
0x40000030:	00 00
0x40000048:	00 00

Call Stack + Locals | Memory 1

作業\\HW_3\\Objects\\HW_3.axf"

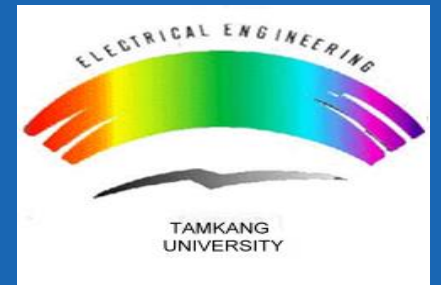


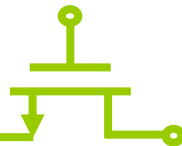
1205正課複習

2023 Advanced Mixed-Operation System (AMOS) Lab.



Tamkang University
Department of Electrical and Computer Engineering
No.151, Yingzhuan Rd., Tamsui Dist., New Taipei City 25137, Taiwan (R.O.C.)

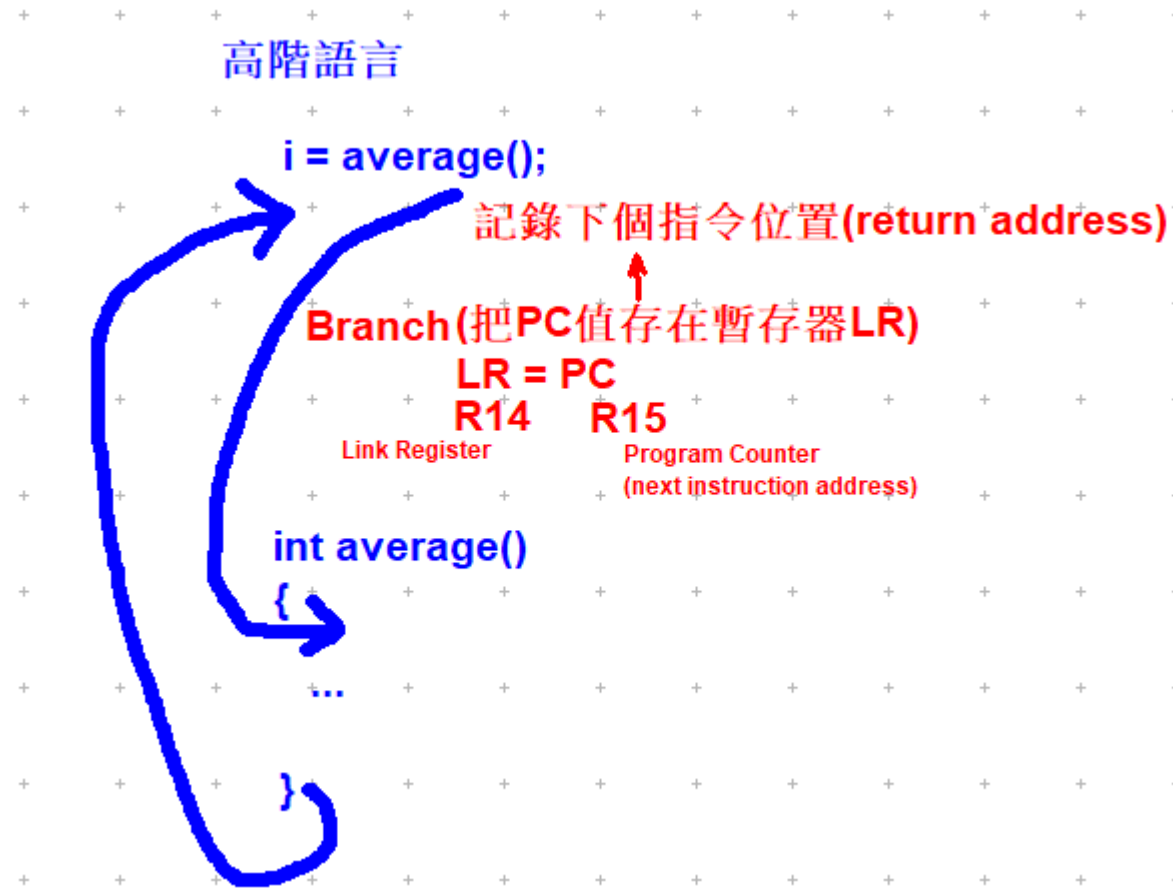
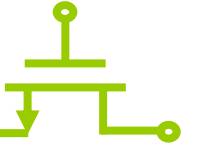




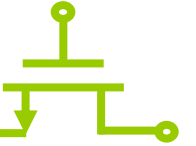
- ❖ Step1：自己創造七組12-bit value
 - 一組正確
 - 四組錯一個checksum bit(分別錯C0、C1、C2、C3)(改checksum bit)
 - 兩組錯兩個checksum bit(一組錯C0與C3，另一組錯C1與C2)(改data bit)
- ❖ Step2：把12-bit value中的8-bit data取出
- ❖ Step3：將分離出來的原始8-bit data，找出checksum bits
- ❖ Step4：比較12-bit value中之checksum bits與8 data bits計算出之checksum bits
- ❖ Step5：checksums錯誤的處理規則
 - 沒有錯誤的與有一個錯誤的→直接取出8-bit data存入r6
 - 兩個錯誤的→找出錯誤的data bit，將該bit反向，再取出8-bit data存入r6



p.109 Subroutine(Procedure/Function)



p.109 Subroutine(Procedure/Function)



註記回來的地方

Branch and Link

stop

func1

MOV PC, LR

MOV R15, R14

Branch and Exchange

可以寫成

AREA Example, CODE

ENTRY

BL func1 LR = PC

BL func2

B stop

LDR r0, =42

LDR r1, =0x12345678

LDR r2, =0xFFFFFFFF

lrr PC <-> LR

LTORG

func2 LDR r3, =0x12345678

;LDR r4, =0x87654321

BX lrr

BigTable

SPACE 4200

END

; mark first instruction

; call first subroutine

; call second subroutine

; terminate the program

; => MOV r0, #42

; => LDR r1, [PC, #N]

; where N=offset to literal pool 1

; => MVN r2, #0

; return from subroutine

; literal pool 1 has 0x12345678

; => LDR r3, [PC, #N]

; N=offset back to literal pool 1

; if this is uncommented, it fails.

; Literal pool 2 is out of reach!

; return from subroutine

; clears 4200 bytes of memory,

; starting here

; literal pool 2 empty

Load program into memory
and 1st instruction address into PC

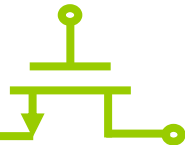
Instruction Cycle :

1. Fetch next inst.(from memory according PC)
2. Update PC
3. Decode
4. Execute

Ex :
BX R5
PC <-> R5



p.109 Subroutine(Procedure/Function)



```

                                AREA Example, CODE
                                ENTRY                                ; mark first instruction
                                BL      func1                        ; call first subroutine
                                BL      func2                        ; call second subroutine
                                B        stop                        ; terminate the program
stop
func1
    LDR    r0, =42                                ; => MOV r0, #42
    LDR    r1, =0x12345678                        ; => LDR r1, [PC, #N]
                                                ; where N=offset to literal pool 1
                                LDR    r2, =0xFFFFFFFF            ; => MVN r2, #0
                                BX      lr                        ; return from subroutine
                                LTORG   指定literal pool位置，
literal pool origin            因為N不能太大。
func2
    LDR    r3, =0x12345678                        ; => LDR r3, [PC, #N]
                                                ; N=offset back to literal pool 1
                                ;LDR    r4, =0x87654321          ; if this is uncommented, it fails.
                                                ; Literal pool 2 is out of reach!
                                BX      lr                        ; return from subroutine

                                BigTable
                                SPACE 4200                        ; clears 4200 bytes of memory,
                                                                ; starting here
                                END                                ; literal pool 2 empty
literal pool
number                        0x12345678 若有假想的指令且未指定literal pool位置，則數值會存在END後面。
    
```

p.110 FIGURE 6.6

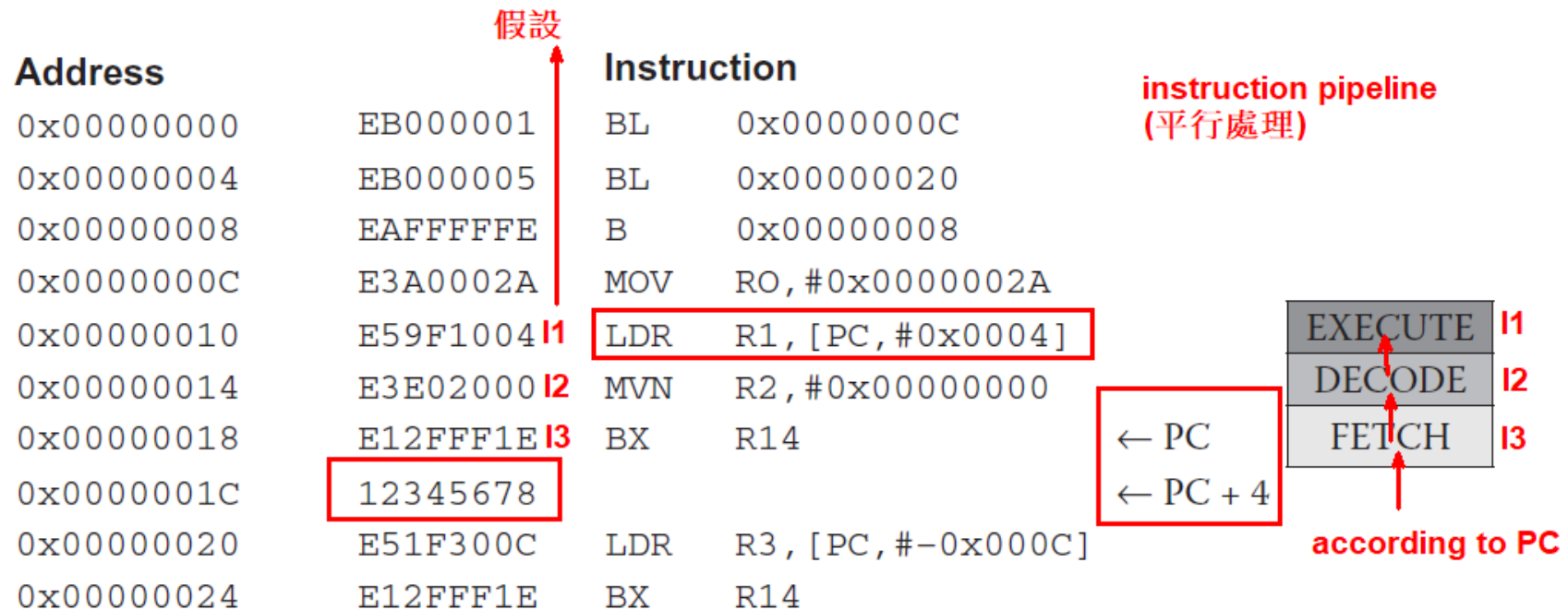
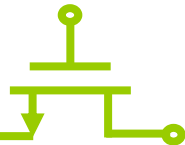


FIGURE 6.6 Disassembly of ARM7TDMI program.

Q&A

Thanks for your attention !!