第2次隨堂考-電資

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第02次隨堂考-評分標準

- 第一題(50%)
  - Empty Descending Stack(10%)
  - 完整程式碼(10%)
  - UART #1視窗(30%)
- 第二題(50%)
  - (a)(25%)
  - (b)(25%)

→補繳分數＝原始分數*0.8

第一題-Empty Descending Stack

```
187 ; empty descending stack
188 Transmit
189             STMDA   sp!, {r5, r6, lr}
190             LDR     r5, = U0START
191 wait        LDRB    r6, [r5, #LSR0] ; get status of buffer
192             TST     r6, #0x20       ; buffer empty?
193             BEQ     wait            ; spin until buffer's empty
194             STRB    r0, [r5]
195             LDMIB   sp!, {r5, r6, pc}
```

第一題-完整程式碼(1/3)

```
1                AREA UARTDEMO, CODE, READONLY
2  PINSEL0       EQU     0xE002C000      ; controls the function of the pins
3  U0START       EQU     0xE000C000      ; start of UART0 registers
4  LCR0          EQU     0xC             ; line control register for UART0
5  LSR0          EQU     0x14            ; line status register for UART0
6  RAMSTART      EQU     0x40000020      ; start of onboard RAM for 2104
7                ENTRY
8  start
9                LDR     sp, = RAMSTART  ; set up stack pointer
10               BL      UARTConfig      ; initialize/configure UART0
11
12               ; 2024!
13               LDR     r1, = StudentData   ; starting address of characters
14               ADD     r1, #39
15               MOV     r2, #5
16 Loop1
17               LDRB    r0, [r1],#1     ; load character, increment address
18               CMP     r2,#0           ; null terminated?
19               BLNE    Transmit        ; send character to UART
20               SUB     r2, #1
21               BNE     Loop1           ; continue if not a '0'
22
23               ; blank
24               LDR     r1, = StudentData   ; starting address of characters
25               ADD     r1, #38
26               LDRB    r0, [r1]        ; load character, increment address
27               BL      Transmit        ; send character to UART
28
29               ; in Spring
30               LDR     r1, = StudentData   ; starting address of characters
31               ADD     r1, #29
32               MOV     r2, #9
33 Loop3
34               LDRB    r0, [r1],#1     ; load character, increment address
35               CMP     r2,#0           ; null terminated?
36               BLNE    Transmit        ; send character to UART
37               SUB     r2, #1
38               BNE     Loop3           ; continue if not a '0'
39
40               ; blank
41               LDR     r1, = StudentData   ; starting address of characters
42               ADD     r1, #28
43               LDRB    r0, [r1]        ; load character, increment address
44               BL      Transmit        ; send character to UART
45
46               ; Midterm Exam
47               LDR     r1, = StudentData   ; starting address of characters
48               ADD     r1, #16
49               MOV     r2, #12
```

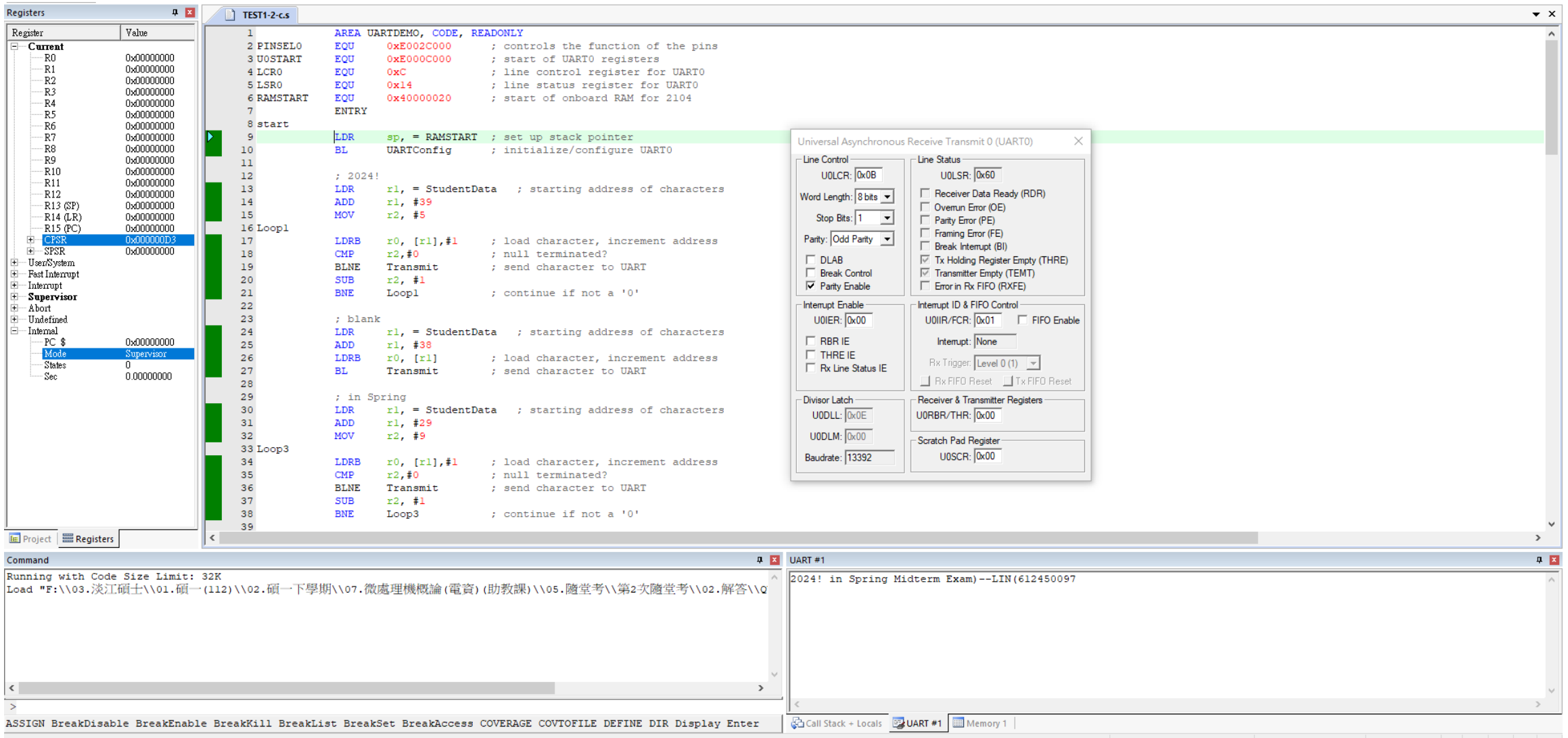
第一題-完整程式碼(2/3)

```
50 Loop5
51              LDRB    r0, [r1],#1     ; load character, increment address
52              CMP     r2,#0           ; null terminated?
53              BLNE    Transmit        ; send character to UART
54              SUB     r2, #1
55              BNE     Loop5           ; continue if not a '0'
56
57              ; )
58              LDR     r1, = StudentData   ; starting address of characters
59              ADD     r1, #14
60              LDRB    r0, [r1]        ; load character, increment address
61              BL      Transmit        ; send character to UART
62
63              ; -
64              LDR     r1, = StudentData   ; starting address of characters
65              ADD     r1, #15
66              LDRB    r0, [r1]        ; load character, increment address
67              BL      Transmit        ; send character to UART
68
69              ; -
70              LDR     r1, = StudentData   ; starting address of characters
71              ADD     r1, #10
72              LDRB    r0, [r1]        ; load character, increment address
73              BL      Transmit        ; send character to UART
74
75              ; LIN
76              LDR     r1, = StudentData   ; starting address of characters
77              ADD     r1, #11
78              MOV     r2, #3
79 Loop6
80              LDRB    r0, [r1],#1     ; load character, increment address
81              CMP     r2,#0           ; null terminated?
82              BLNE    Transmit        ; send character to UART
83              SUB     r2, #1
84              BNE     Loop6           ; continue if not a '0'
85
86              ; (
87              LDR     r1, = StudentData   ; starting address of characters
88              LDRB    r0, [r1]        ; load character, increment address
89              BL      Transmit        ; send character to UART
90
91              ; 612450097
92              LDR     r1, = StudentData   ; starting address of characters
93              ADD     r1, #1
94              MOV     r2, #9
95 Loop7
96              LDRB    r0, [r1],#1     ; load character, increment address
97              CMP     r2,#0           ; null terminated?
98              BLNE    Transmit        ; send character to UART
99              SUB     r2, #1
100             BNE     Loop7           ; continue if not a '0'
```

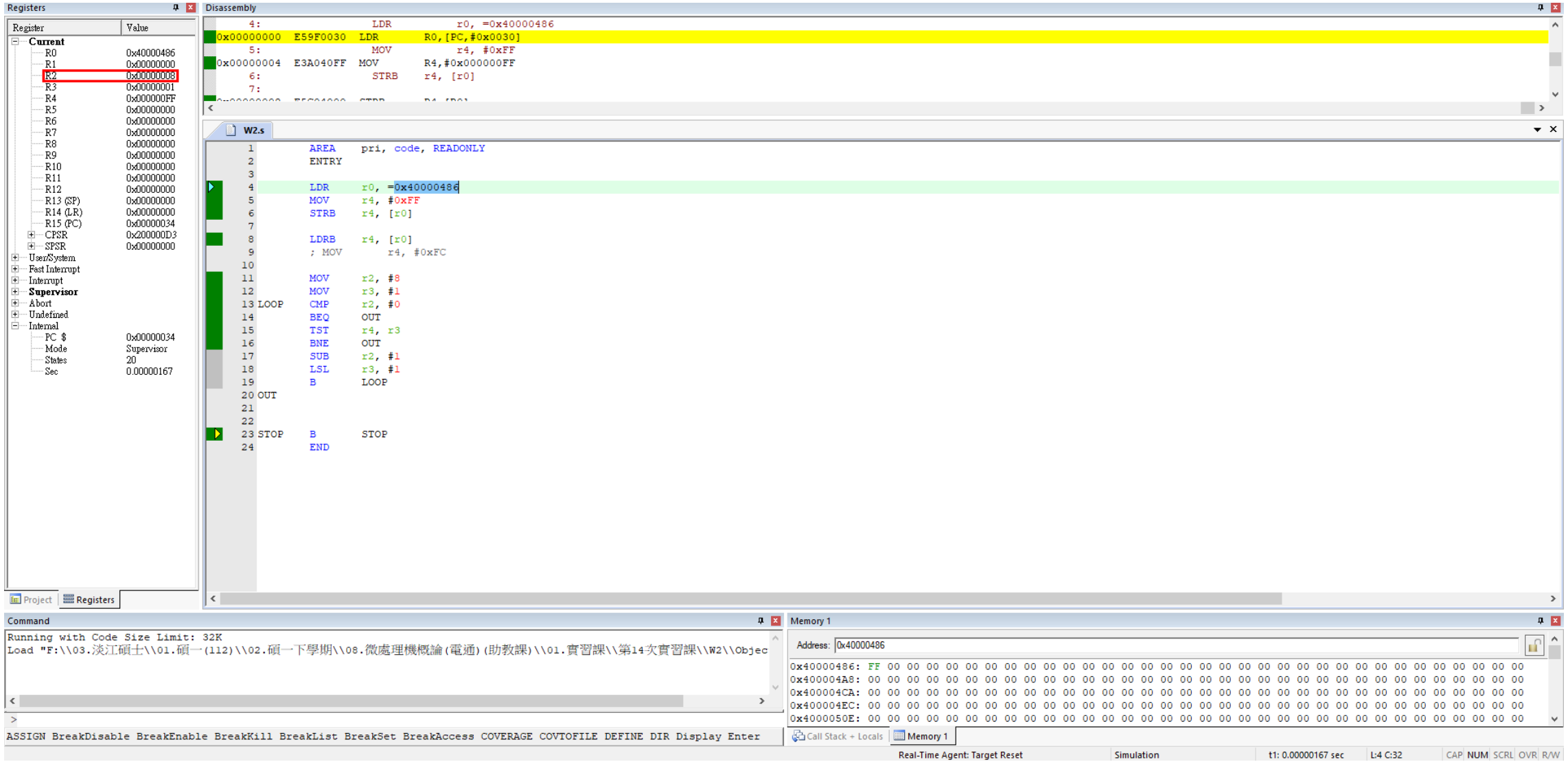
第一題-完整程式碼(3/3)

```
done        B       done            ; otherwise we  e done

; Subroutine UARTConfig
; This subroutine configures the I/O pins first. It
; then sets up the UART control register. The
; parameters
; are set to 8 bits, no parity and 1 stop bit.
; Registers used:
; r5 - scratch register
; r6 - scratch register
; inputs: none
; outputs: none

; full descending stack
UARTConfig
            STMDB   sp!, {r5,r6,lr}

            LDR     r5, = PINSEL0   ; base address of register
            LDR     r6, [r5]        ; get contents
            BIC     r6, r6, #0xF    ; clear out lower nibble
            ORR     r6, r6, #0x5    ; sets P0.0 to Tx0 and P0.1 to Rx0
            STR     r6, [r5]        ; r/modify/w back to register

            LDR     r5, = U0START   ; 0b1000 1011 = 0x8B
            MOV     r6, #0x8B       ; set 8 bits, odd parity, 1 stop bit
            STRB    r6, [r5, #LCR0] ; write control byte to LCR

            MOV     r6, #0xE        ; 12800 baud @3 MHz VPB clock
            STRB    r6, [r5]        ; store control byte

            MOV     r6, #0xB        ; set DLAB = 0
            STRB    r6, [r5, #LCR0] ; Tx and Rx buffers set up

            LDMIA   sp!, {r5,r6,pc}

; Subroutine Transmit
; This routine puts one byte into the UART
; for transmitting.
; Register used:
; r5 - scratch
; r6 - scratch
; inputs: r0- byte to transmit
; outputs: none
;

; empty descending stack
Transmit
            STMDA   sp!, {r5, r6, lr}
            LDR     r5, = U0START
wait        LDRB    r6, [r5, #LSR0] ; get status of buffer
            TST     r6, #0x20       ; buffer empty?
            BEQ     wait            ; spin until buffer's empty
            STRB    r0, [r5]
            LDMIB   sp!, {r5, r6, pc}
StudentData
            DCB     "(612450097-LIN)-Midterm Exam in Spring 2024!",0
            END
```

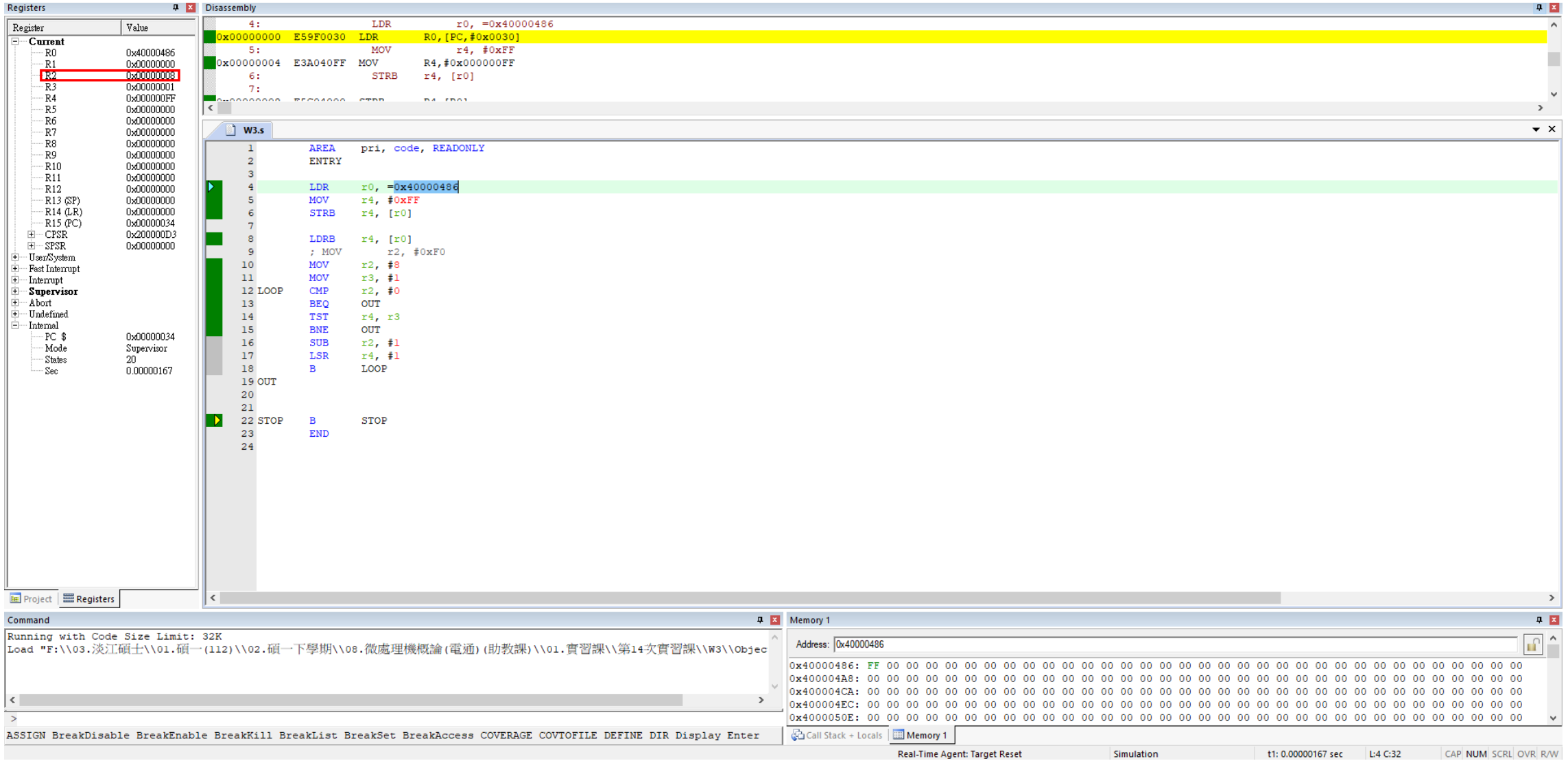
第一題-UART #1視窗


Registers
Register
Value
Current
R0 0x00000000
R1 0x00000000
R2 0x00000000
R3 0x00000000
R4 0x00000000
R5 0x00000000
R6 0x00000000
R7 0x00000000
R8 0x00000000
R9 0x00000000
R10 0x00000000
R11 0x00000000
R12 0x00000000
R13 (SP) 0x00000000
R14 (LR) 0x00000000
R15 (PC) 0x00000000
CPSR 0x000000D3
SPSR 0x00000000
User/System
Fast Interrupt
Interrupt
Supervisor
Abort
Undefined
Internal
PC $ 0x00000000
Mode Supervisor
States 0
Sec 0.00000000
Project
Registers
TEST1-2-c.s
1 AREA UARTDEMO, CODE, READONLY
2 PINSEL0 EQU 0xE002C000 ; controls the function of the pins
3 U0START EQU 0xE000C000 ; start of UART0 registers
4 LCR0 EQU 0xC ; line control register for UART0
5 LSR0 EQU 0x14 ; line status register for UART0
6 RAMSTART EQU 0x40000020 ; start of onboard RAM for 2104
7 ENTRY
8 start
9 LDR sp, = RAMSTART ; set up stack pointer
10 BL UARTConfig ; initialize/configure UART0
11
12 ; 2024!
13 LDR r1, = StudentData ; starting address of characters
14 ADD r1, #39
15 MOV r2, #5
16 Loop1
17 LDRB r0, [r1],#1 ; load character, increment address
18 CMP r2,#0 ; null terminated?
19 BLNE Transmit ; send character to UART
20 SUB r2, #1
21 BNE Loop1 ; continue if not a '0'
22
23 ; blank
24 LDR r1, = StudentData ; starting address of characters
25 ADD r1, #38
26 LDRB r0, [r1] ; load character, increment address
27 BL Transmit ; send character to UART
28
29 ; in Spring
30 LDR r1, = StudentData ; starting address of characters
31 ADD r1, #29
32 MOV r2, #9
33 Loop3
34 LDRB r0, [r1],#1 ; load character, increment address
35 CMP r2,#0 ; null terminated?
36 BLNE Transmit ; send character to UART
37 SUB r2, #1
38 BNE Loop3 ; continue if not a '0'
39
Universal Asynchronous Receive Transmit 0 (UART0)
Line Control
U0LCR: 0x0B
Word Length: 8 bits
Stop Bits: 1
Parity: Odd Parity
DLAB
Break Control
Parity Enable
Line Status
U0LSR: 0x60
Receiver Data Ready (RDR)
Overrun Error (OE)
Parity Error (PE)
Framing Error (FE)
Break Interrupt (BI)
Tx Holding Register Empty (THRE)
Transmitter Empty (TEMT)
Error in Rx FIFO (RXFE)
Interrupt Enable
U0IER: 0x00
RBR IE
THRE IE
Rx Line Status IE
Interrupt ID & FIFO Control
U0IIR/FCR: 0x01
FIFO Enable
Interrupt: None
Rx Trigger: Level 0 (1)
Rx FIFO Reset
Tx FIFO Reset
Divisor Latch
U0DLL: 0x0E
U0DLM: 0x00
Baudrate: 13392
Receiver & Transmitter Registers
U0RBR/THR: 0x00
Scratch Pad Register
U0SCR: 0x00
Command
Running with Code Size Limit: 32K
Load "F:\\03.淡江碩士\\01.碩一(112)\\02.碩一下學期\\07.微處理機概論(電資)(助教課)\\05.隨堂考\\第2次隨堂考\\02.解答\\Q
ASSIGN BreakDisable BreakEnable BreakKill BreakList BreakSet BreakAccess COVERAGE COVTOFILE DEFINE DIR Display Enter
UART #1
2024! in Spring Midterm Exam)--LIN(612450097
Call Stack + Locals
UART #1
Memory 1

第二題-(a)


Registers
Register
Value
Current
R0 0x40000486
R1 0x00000000
R2 0x00000008
R3 0x00000001
R4 0x000000FF
R5 0x00000000
R6 0x00000000
R7 0x00000000
R8 0x00000000
R9 0x00000000
R10 0x00000000
R11 0x00000000
R12 0x00000000
R13 (SP) 0x00000000
R14 (LR) 0x00000000
R15 (PC) 0x00000034
CPSR 0x200000D3
SPSR 0x00000000
User/System
Fast Interrupt
Interrupt
Supervisor
Abort
Undefined
Internal
PC $ 0x00000034
Mode Supervisor
States 20
Sec 0.00000167
Project
Registers
Disassembly
4: LDR r0, =0x40000486
0x00000000 E59F0030 LDR R0,[PC,#0x0030]
5: MOV r4, #0xFF
0x00000004 E3A040FF MOV R4,#0x000000FF
6: STRB r4, [r0]
7:
W2.s
1 AREA pri, code, READONLY
2 ENTRY
3
4 LDR r0, =0x40000486
5 MOV r4, #0xFF
6 STRB r4, [r0]
7
8 LDRB r4, [r0]
9 ; MOV r4, #0xFC
10
11 MOV r2, #8
12 MOV r3, #1
13 LOOP CMP r2, #0
14 BEQ OUT
15 TST r4, r3
16 BNE OUT
17 SUB r2, #1
18 LSL r3, #1
19 B LOOP
20 OUT
21
22
23 STOP B STOP
24 END
Command
Running with Code Size Limit: 32K
Load "F:\\03.淡江碩士\\01.碩一(112)\\02.碩一下學期\\08.微處理機概論(電通)(助教課)\\01.實習課\\第14次實習課\\W2\\Objec
ASSIGN BreakDisable BreakEnable BreakKill BreakList BreakSet BreakAccess COVERAGE COVTOFILE DEFINE DIR Display Enter
Memory 1
Address: 0x40000486
0x40000486: FF 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x400004A8: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x400004CA: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x400004EC: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x4000050E: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
Call Stack + Locals
Memory 1
Real-Time Agent: Target Reset
Simulation
t1: 0.00000167 sec
L:4 C:32
CAP NUM SCRL OVR R/W

第二題-(b)


Registers
Register
Value
Current
R0 0x40000486
R1 0x00000000
R2 0x00000008
R3 0x00000001
R4 0x000000FF
R5 0x00000000
R6 0x00000000
R7 0x00000000
R8 0x00000000
R9 0x00000000
R10 0x00000000
R11 0x00000000
R12 0x00000000
R13 (SP) 0x00000000
R14 (LR) 0x00000000
R15 (PC) 0x00000034
CPSR 0x200000D3
SPSR 0x00000000
User/System
Fast Interrupt
Interrupt
Supervisor
Abort
Undefined
Internal
PC $ 0x00000034
Mode Supervisor
States 20
Sec 0.00000167
Project
Registers
Disassembly
4: LDR r0, =0x40000486
0x00000000 E59F0030 LDR R0,[PC,#0x0030]
5: MOV r4, #0xFF
0x00000004 E3A040FF MOV R4,#0x000000FF
6: STRB r4, [r0]
7:
W3.s
1 AREA pri, code, READONLY
2 ENTRY
3
4 LDR r0, =0x40000486
5 MOV r4, #0xFF
6 STRB r4, [r0]
7
8 LDRB r4, [r0]
9 ; MOV r2, #0xF0
10 MOV r2, #8
11 MOV r3, #1
12 LOOP CMP r2, #0
13 BEQ OUT
14 TST r4, r3
15 BNE OUT
16 SUB r2, #1
17 LSR r4, #1
18 B LOOP
19 OUT
20
21
22 STOP B STOP
23 END
24
Command
Running with Code Size Limit: 32K
Load "F:\\03.淡江碩士\\01.碩一(112)\\02.碩一下學期\\08.微處理機概論(電通)(助教課)\\01.實習課\\第14次實習課\\W3\\Objec
ASSIGN BreakDisable BreakEnable BreakKill BreakList BreakSet BreakAccess COVERAGE COVTOFILE DEFINE DIR Display Enter
Memory 1
Address: 0x40000486
0x40000486: FF 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x400004A8: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x400004CA: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x400004EC: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0x4000050E: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
Call Stack + Locals
Memory 1
Real-Time Agent: Target Reset
Simulation
t1: 0.00000167 sec
L:4 C:32
CAP NUM SCRL OVR R/W

Q&A

Thanks for your attention !!