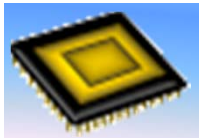
Chapter 2

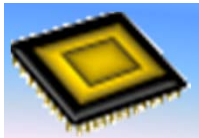
- The Metal – Oxide – Semiconductor (MOS) Transistor



Chapter 2

Chapter 2 The Metal – Oxide – Semiconductor (MOS) Transistor

- MOS technology is the basis for most of the LSI digital memory and up ckts.
- MOS xtor occupies less area the BJT
- MOS xtor involves fewer fabrication steps than BJT ➔ fewer critical defects per unit.
- To realize a given function by dynamic ckt are practical in MOS technology but not in BJT



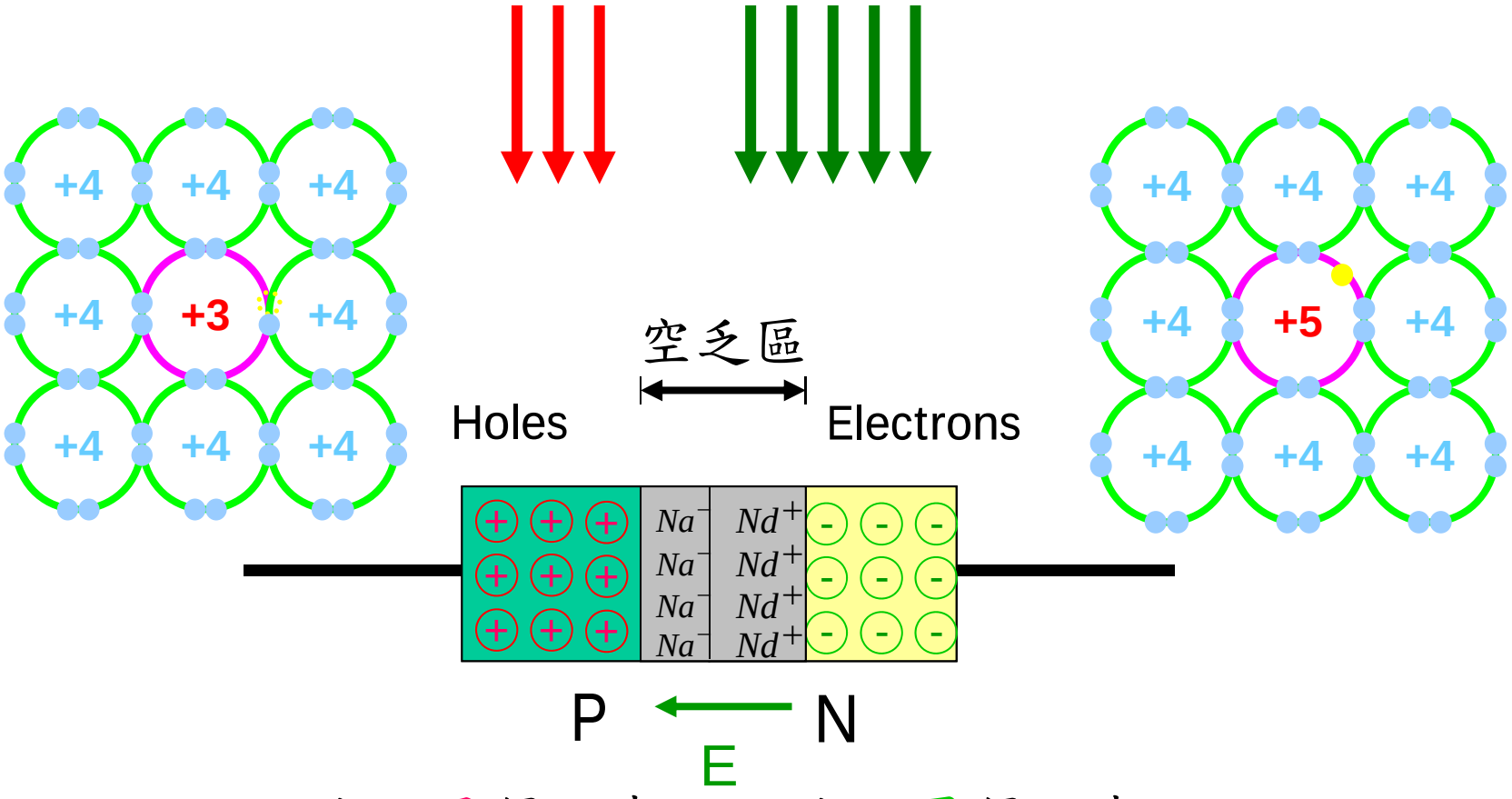
Chapter 2

Chapter 2 The Metal – Oxide – Semiconductor (MOS) Transistor

- 2.1 PN Junction
- 2.2 Alternative MOS Process
- 2.3 Structure and Operation of the MOS Transistor
- 2.4 Threshold Voltage of the MOS Transistor
- 2.5 Current – Voltage Characteristic

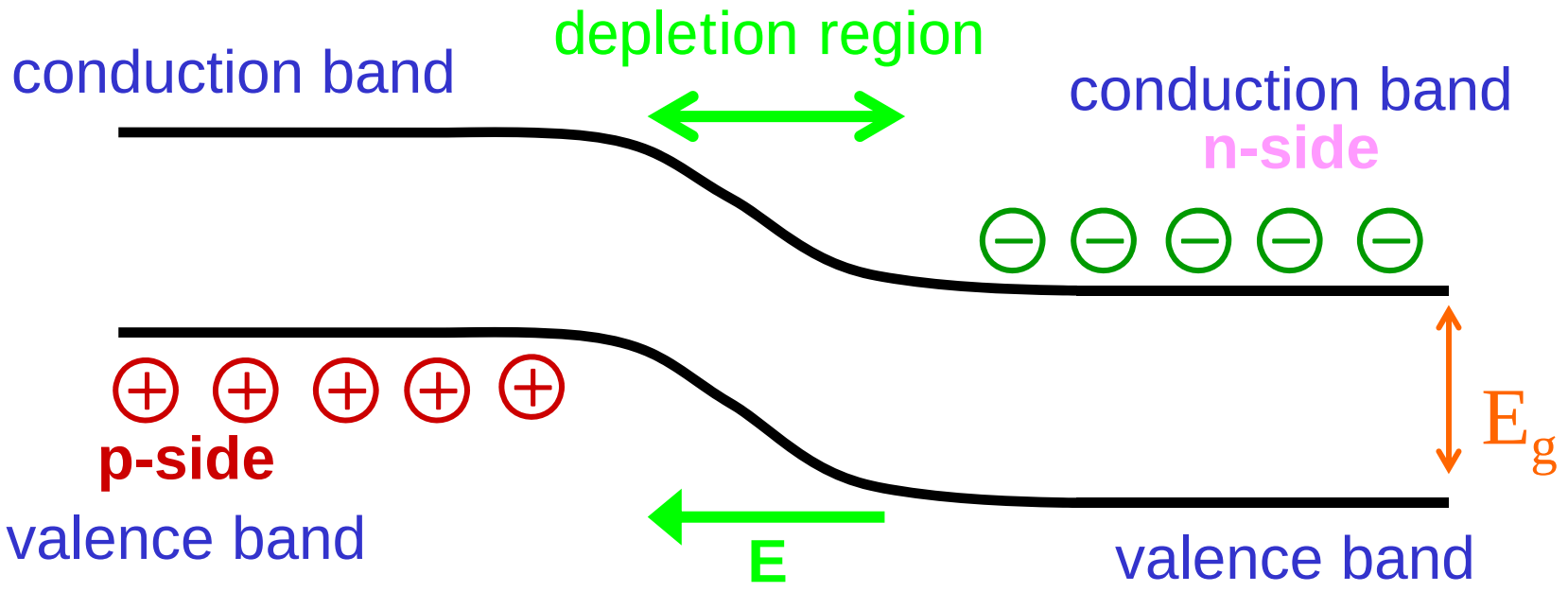
2.1 PN Junction

- Consider a PN junction diode based on Silicon



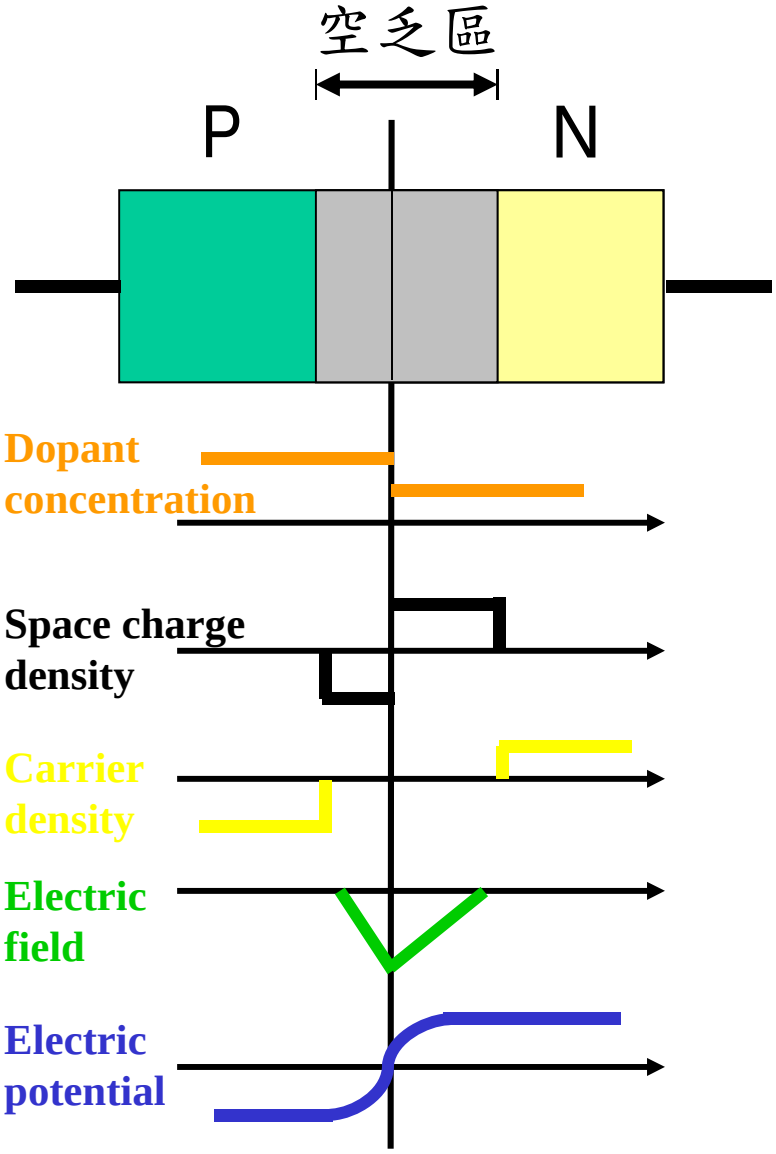
2.1 PN Junction

- A p-n junction diode can also be described by an energy band diagram.
- When a p-n junction is formed, the energy bands bend at the junction.



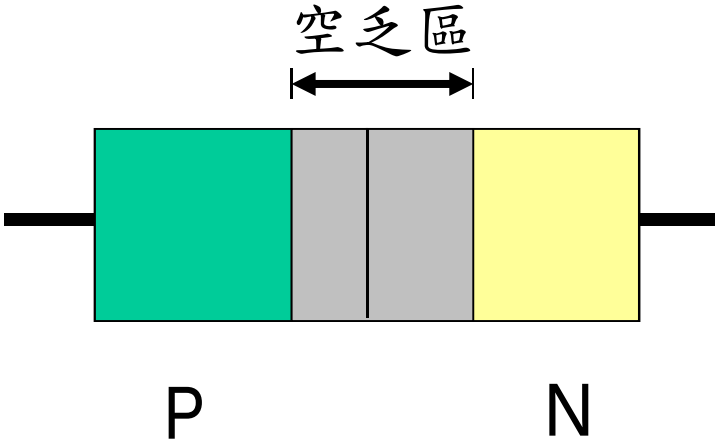
2.1 PN Junction

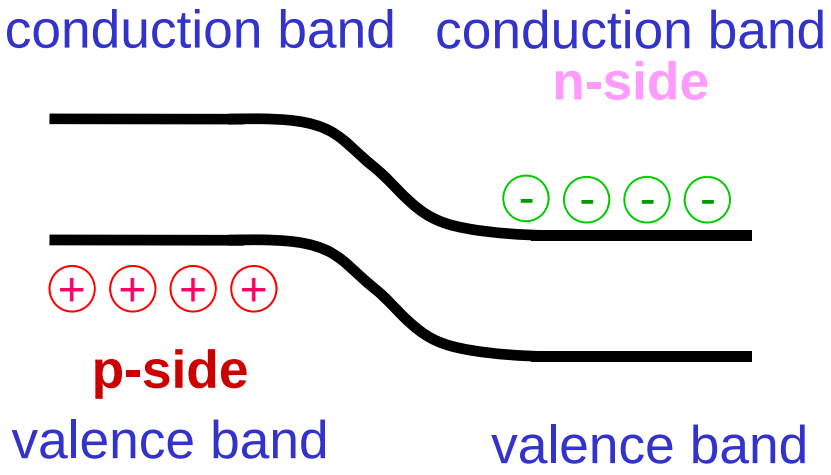
- The gradient of electron and hole densities results in a diffusive migration of majority carriers across the junction.
- The migration leaves a region of net charge of opposite sign on each side, called the space-charge region or depletion region.



2.1 PN Junction

- If the p-side is made negative and the n-side is made positive, the barrier is increased and electrons and holes cannot cross
⇒ **no electric current flows**.
- This situation is called _____.





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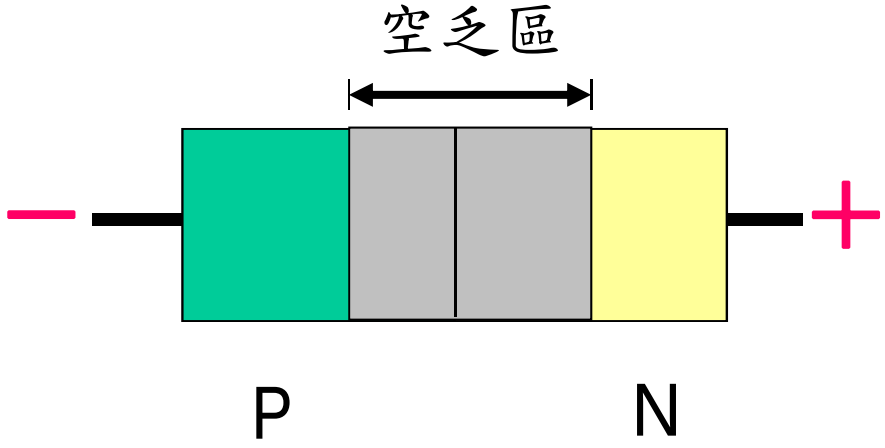
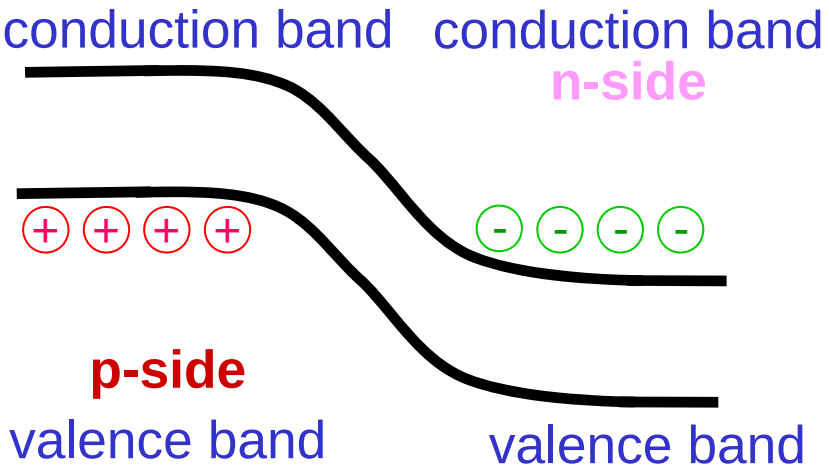
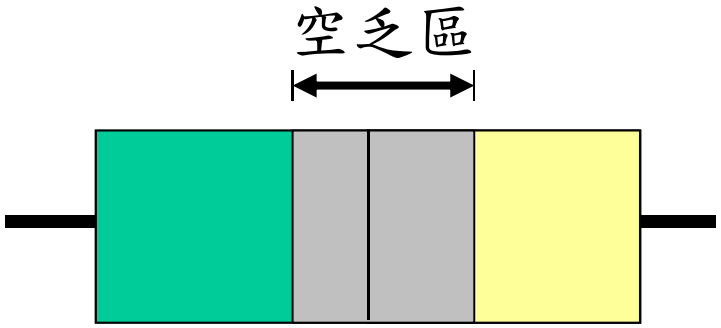




2.1 PN Junction

- If the p-side is made positive and the n-side is made negative, the barrier is reduced and electrons and holes can cross ⇒ **electric current flows**.
- This situation is called _____.



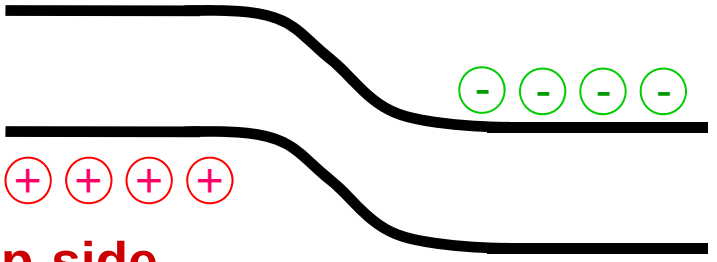
P

N

conduction band

conduction band

n-side



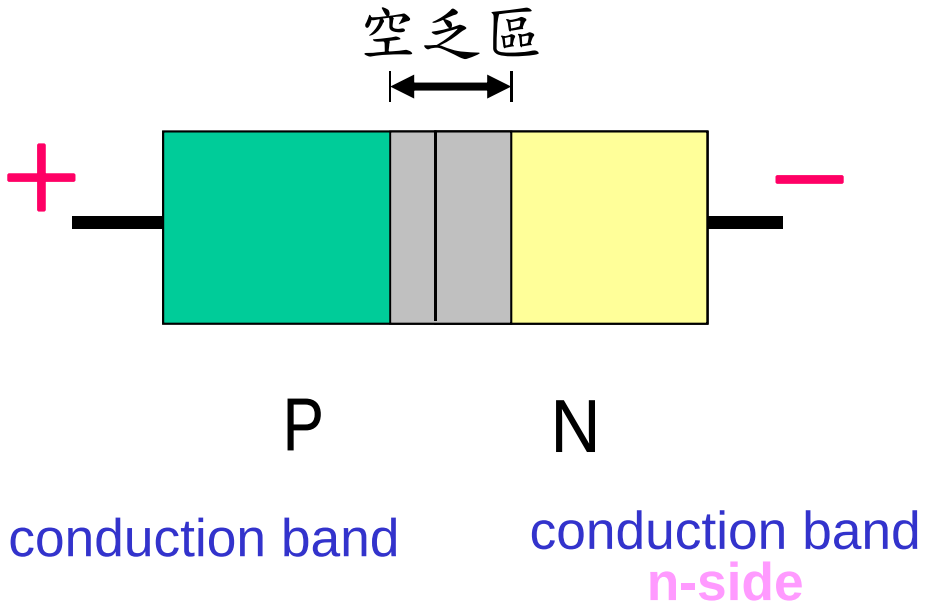
p-side

valence band

valence band

2.1 PN Junction

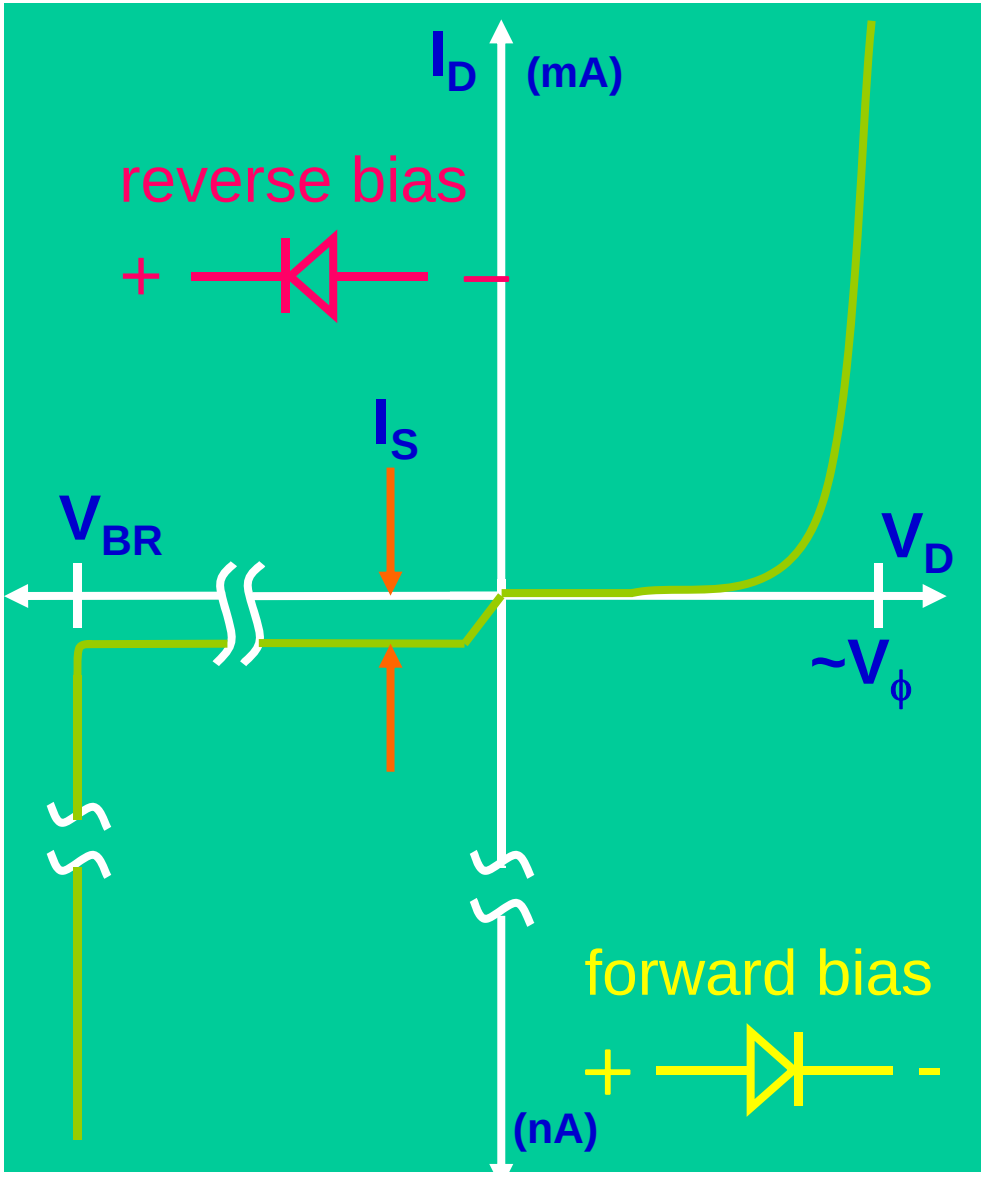
- If the p-side is made positive and the n-side is made negative, the barrier is reduced and electrons and holes can cross ⇒ **electric current flows**.
- This situation is called _____.



2.1 PN Junction

- V_D= Bias Voltage
- I_D= Current through Diode.

  I_D is Negative for Reverse Bias and Positive for Forward Bias
- I_S = _____
- V_{BR}= _____
- V_ϕ = Barrier Potential Voltage

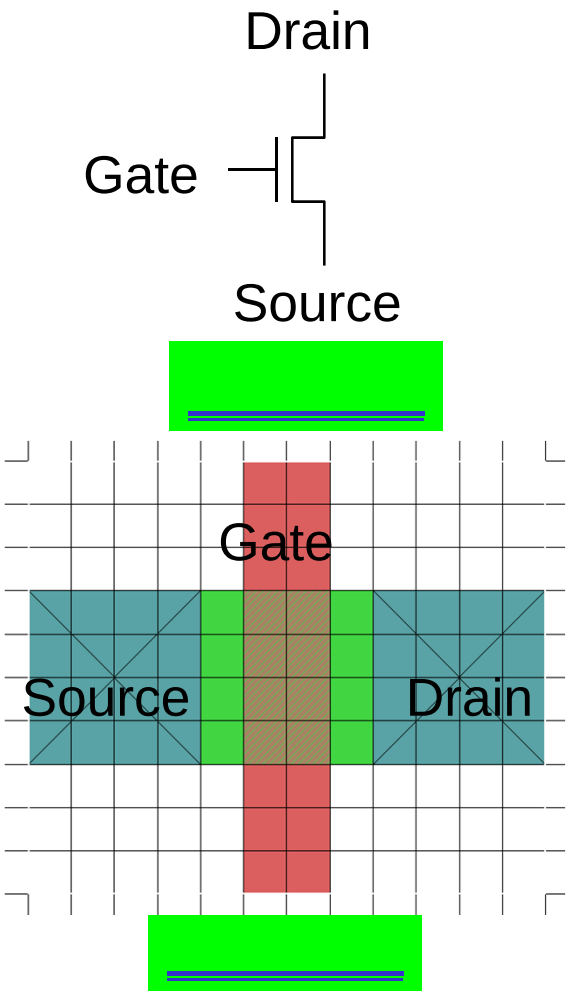


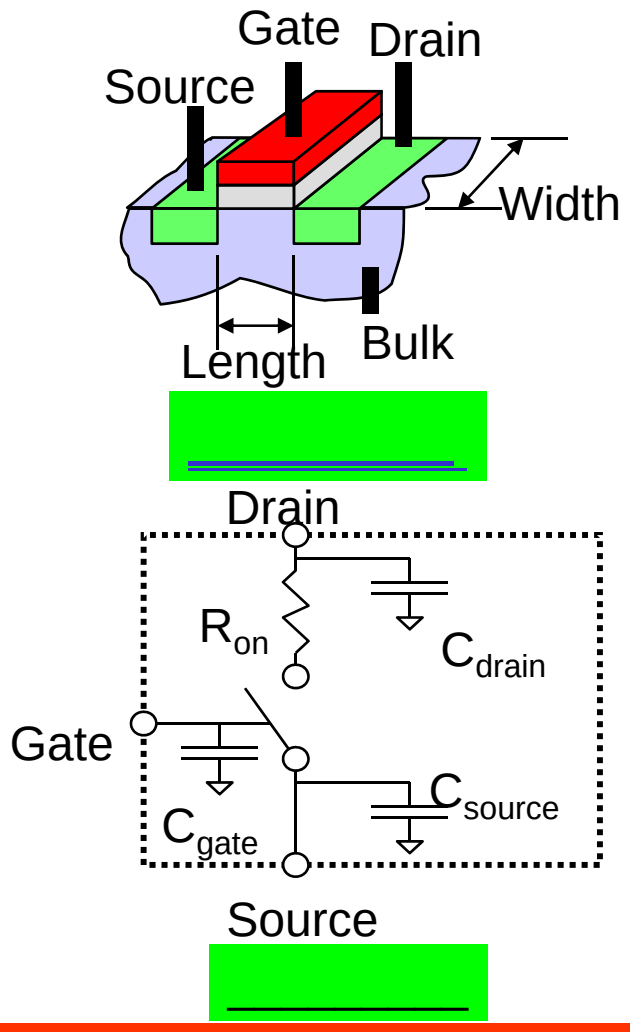
p65

2.2 Alternative MOS Process

- First ckts : in metal-gate PMOS, ±12V power supply voltage, data rates 200Kb/s ~ 1Mb/s
- Today : silicon gate CMOS, power supply ≤5V, data rates up to 300Mb/s
- Reductions in internal dimension
  - Very sharp improvements in the MOS xtor ckt speed
  - BJT ckt speed improves only gradually as dimension reduced
- Limitation of MOS ckts : low driving currents and voltage
  - Bipolar ckts can drive highly capacitive loads and terminated transmission lines at high speed, such as off-chip data bus

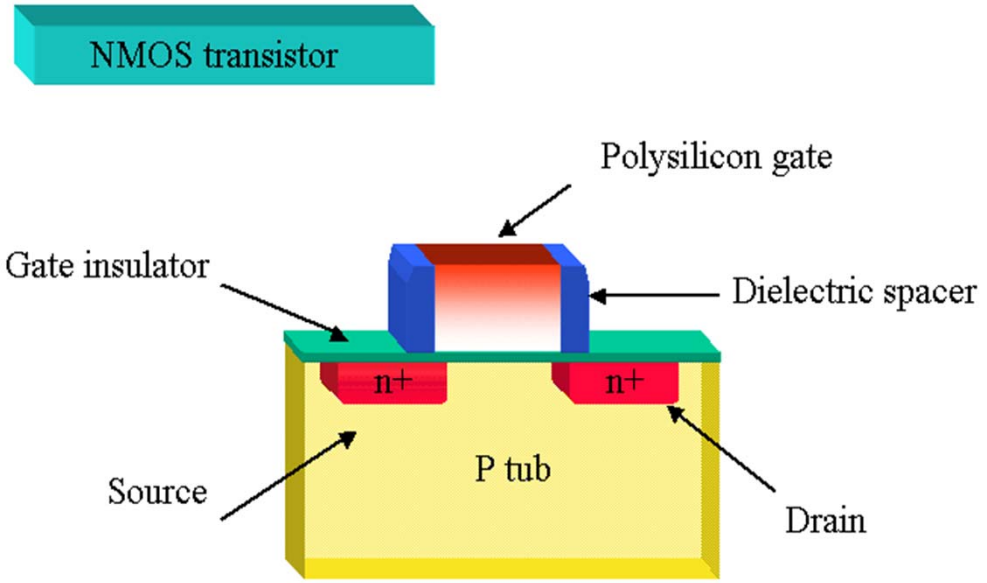
2.2 Alternative MOS Process-- MOS Transistor



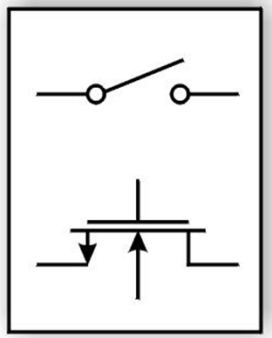


2.2 Alternative MOS Process

- The most prevalent version of MOS technology today is self-aligned silicon-gate NMOS
  - n areas have been doped with donor ions (arsenic)
  - p areas have been doped with acceptor ions (boron)

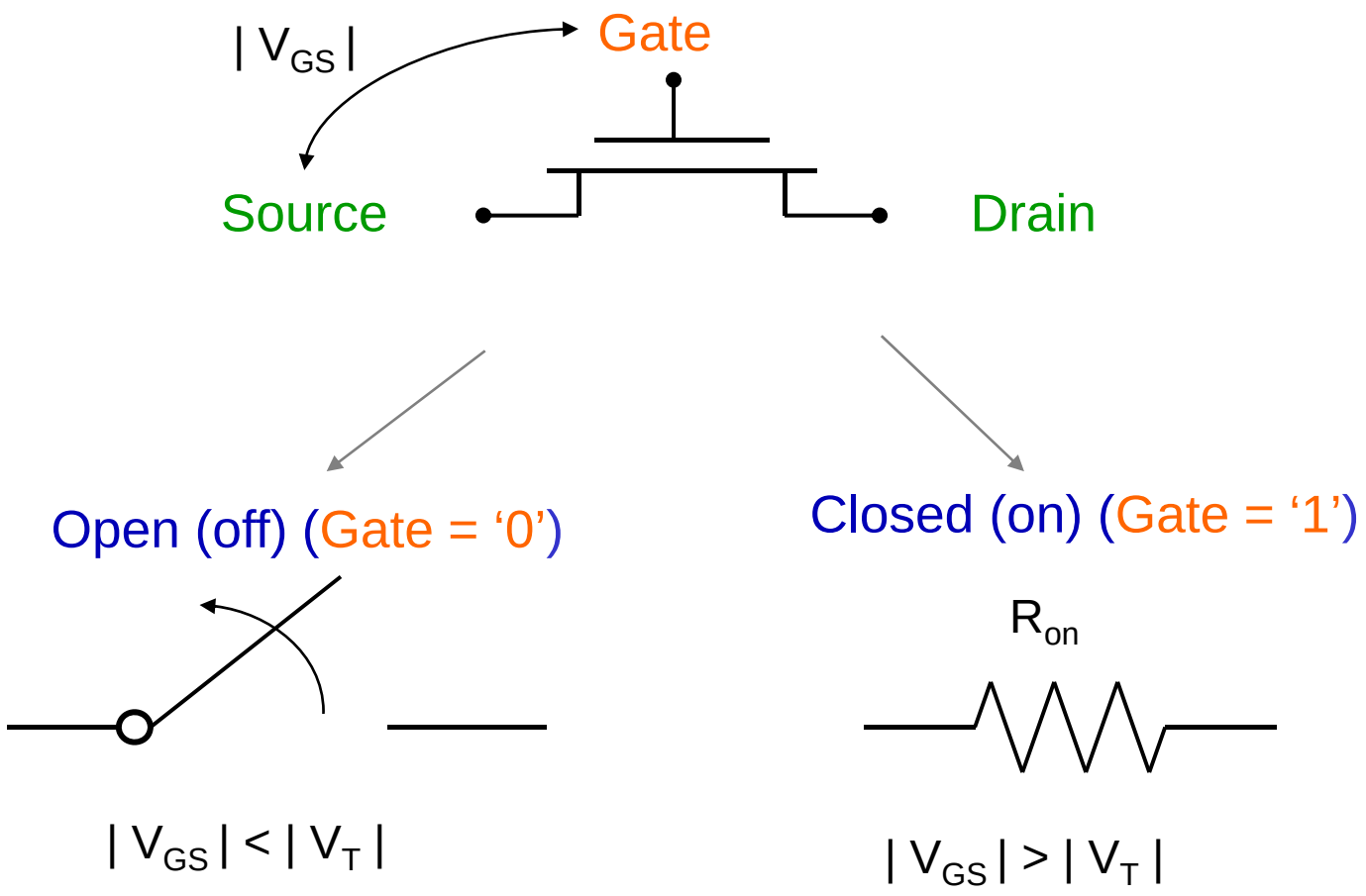


Silicon Switches: The NMOS



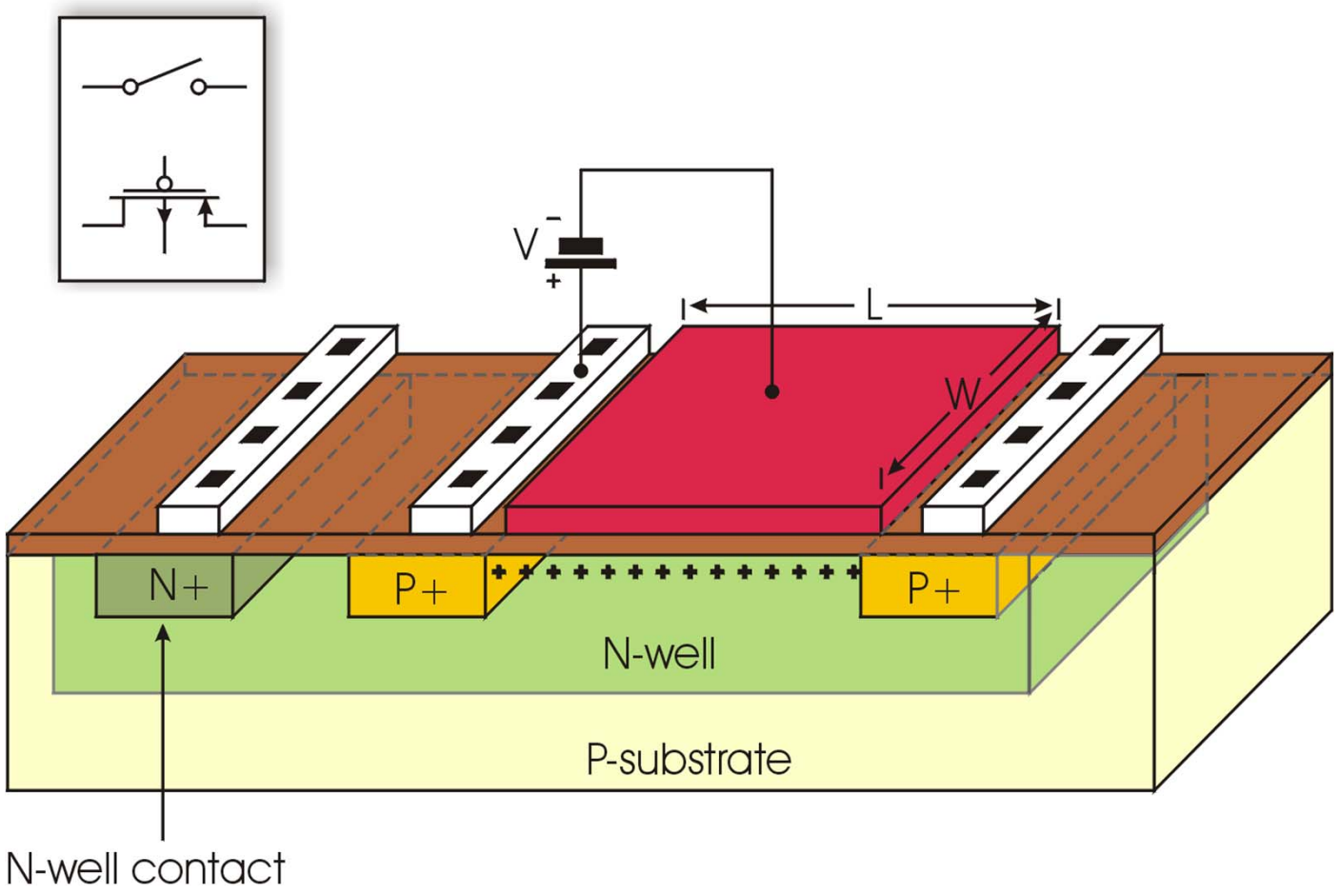
Above silicon:
- Thin oxide (SiO_2) under the gate areas;
- Thick oxide everywhere else;

Switch Model of NMOS Transistor

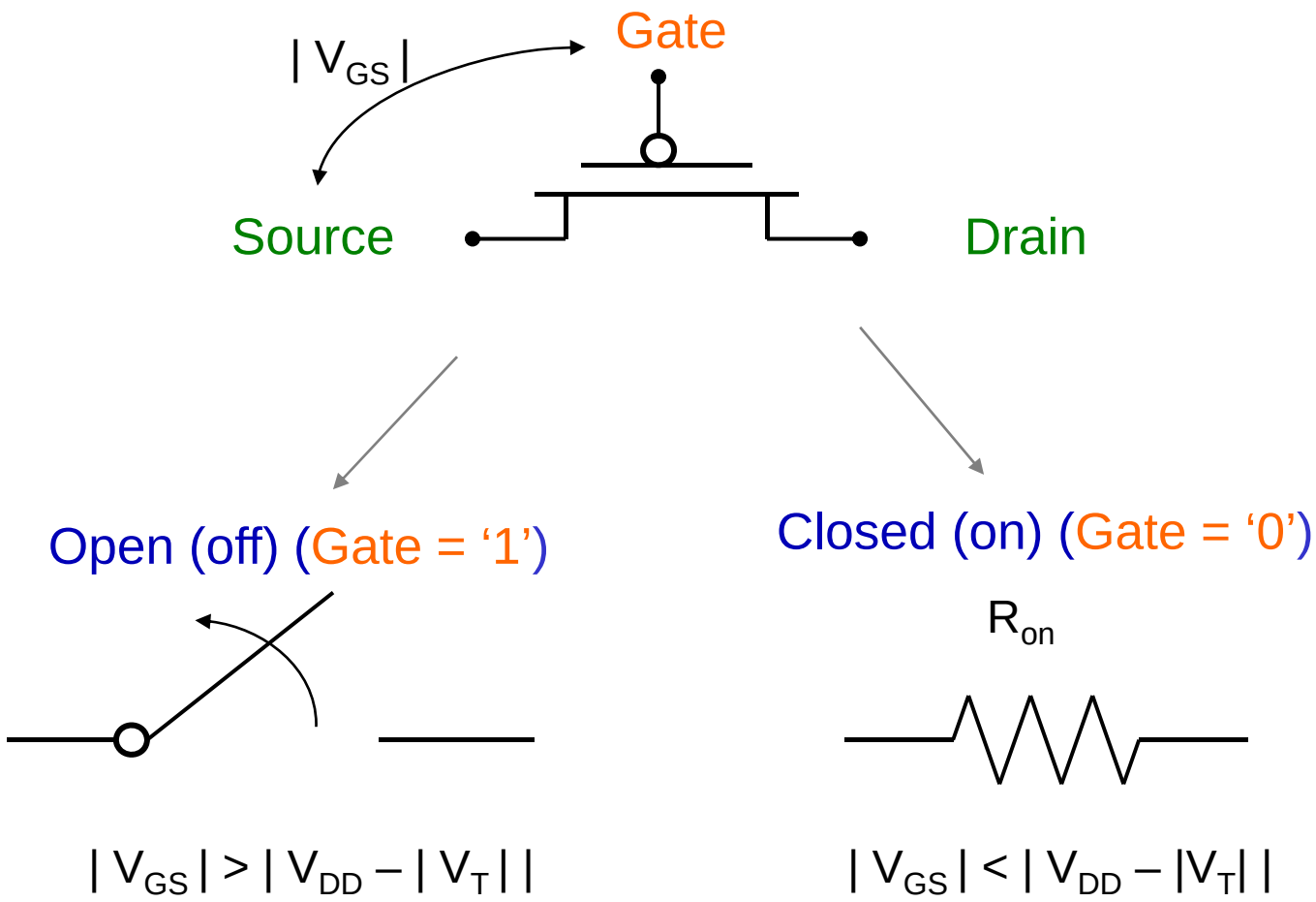


Source: Irwin&Vijay, PSU

Silicon Twitches: The PMOS

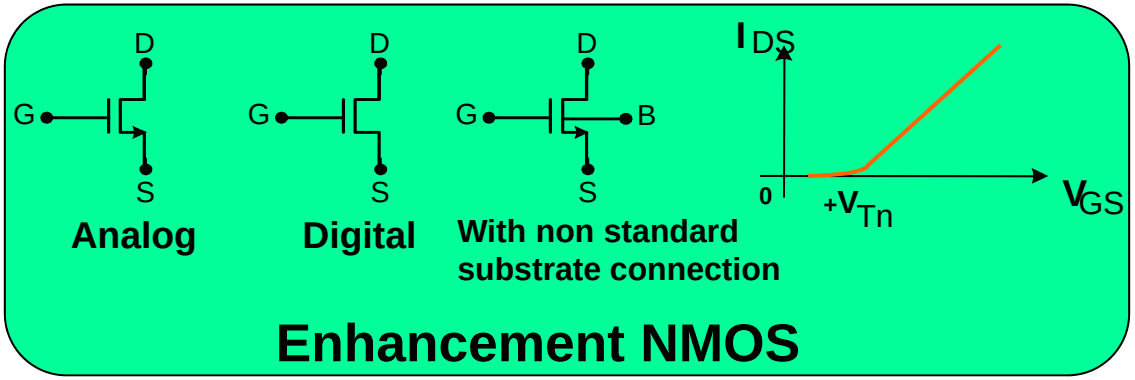


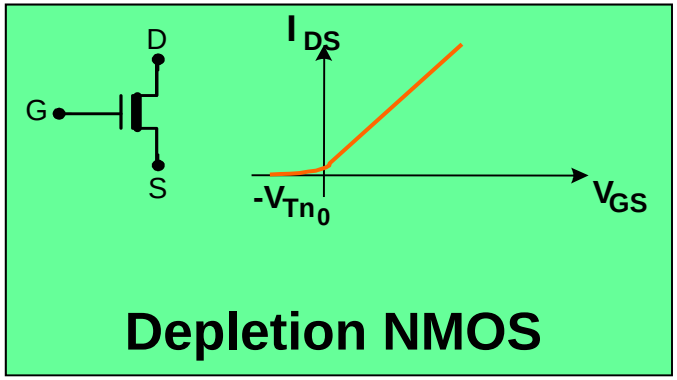
Switch Model of PMOS Transistor

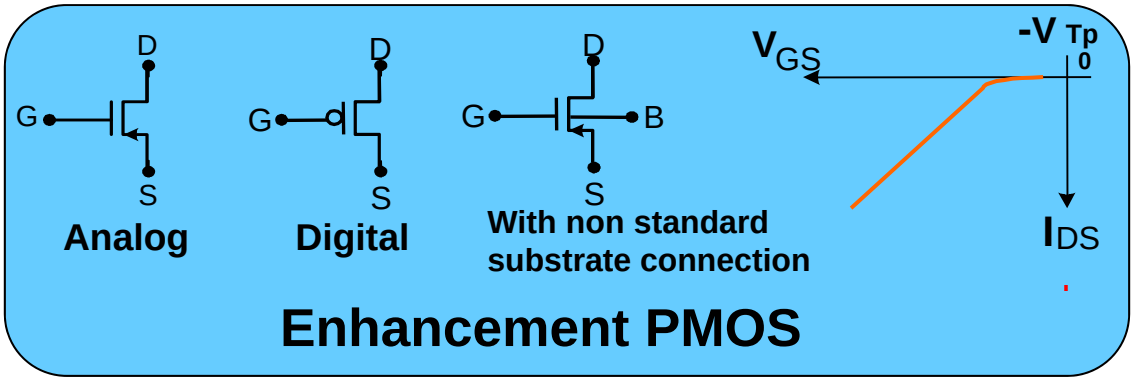


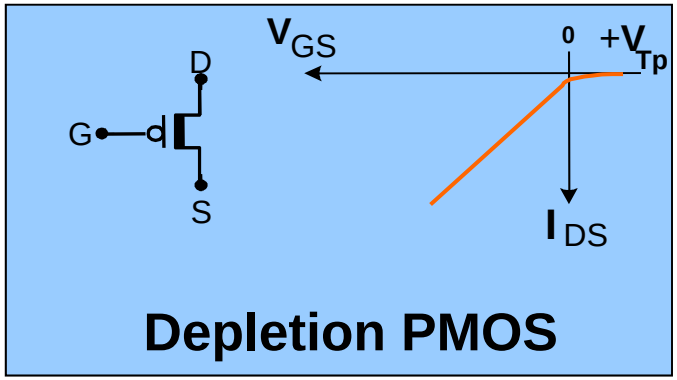
Source: Irwin&Vijay, PSU

2.2 Alternative MOS Process









Enhancement mode transistors are normally OFF (non-conducting with zero bias)

Depletion mode transistors are normally ON (conduct with zero bias)

Most CMOS ICs use Enhancement type MOS

2.2 Alternative MOS Process

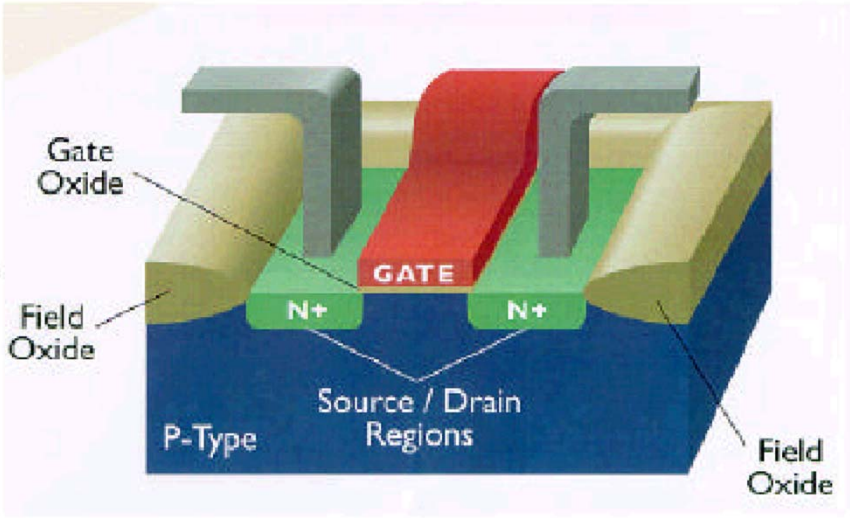
- Enhancement-Mode : the channel conductance is very low (V_G =0), the gate voltage is to increase the channel conductance.
- Depletion-Mode : at V_G =0, the channel conductance is very high (normally-on), the gate voltage is reduce the channel conductance.
- In Commercial application, the Enhancement-Mode MOSFETs are used

2.3 Structure and Operation of the MOS Transistor

- Any analysis or design is only accurate as the models used.

NMOS xtor

- Substrate or body : a single-crystal Si with p-type doping
- Active or transistor region : top surface of the body with thin oxide, where MOS is fabricated.
- Field or passive region : top surface of the body with thick oxide as an isolation between active region.



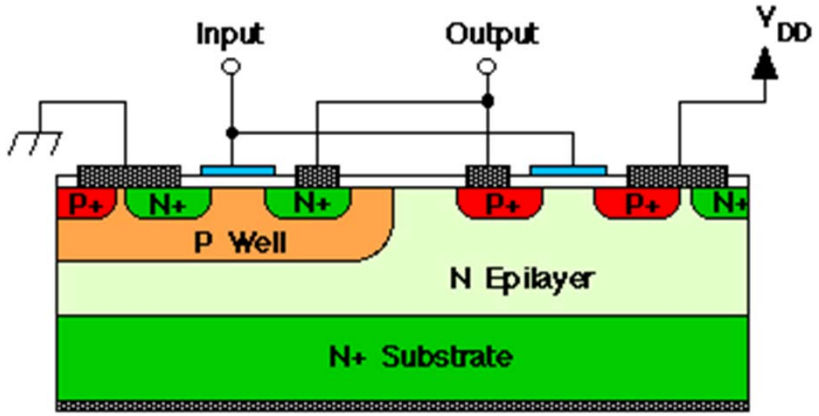
2.3 Structure and Operation of the MOS Transistor

MOS xtor are symmetrical; source and drain are interchangeable

- In NMOS, the more positive electrode is defined as the drain

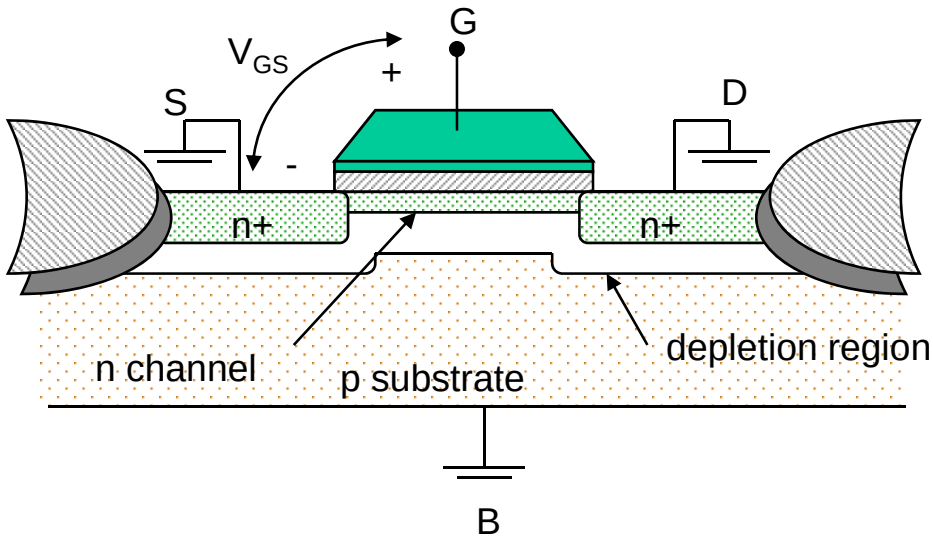
CMOS xtor

- Enhancement-Mode NMOS and PMOS xtors are used in CMOS ckts.
- Gate Length, gate width, and gate oxide thickness are the major parameters determining the electrical characteristics of the MOS xtor.



2.4 Threshold Voltage of the MOS Transistor

- In MOS transistor, Vt is an important parameter.
- Most are related to the material properties. In other words, V_t is largely determined at the time of fabrication, rather than by circuit conditions, like I_{ds} .



2.4 Threshold Voltage of the MOS Transistor

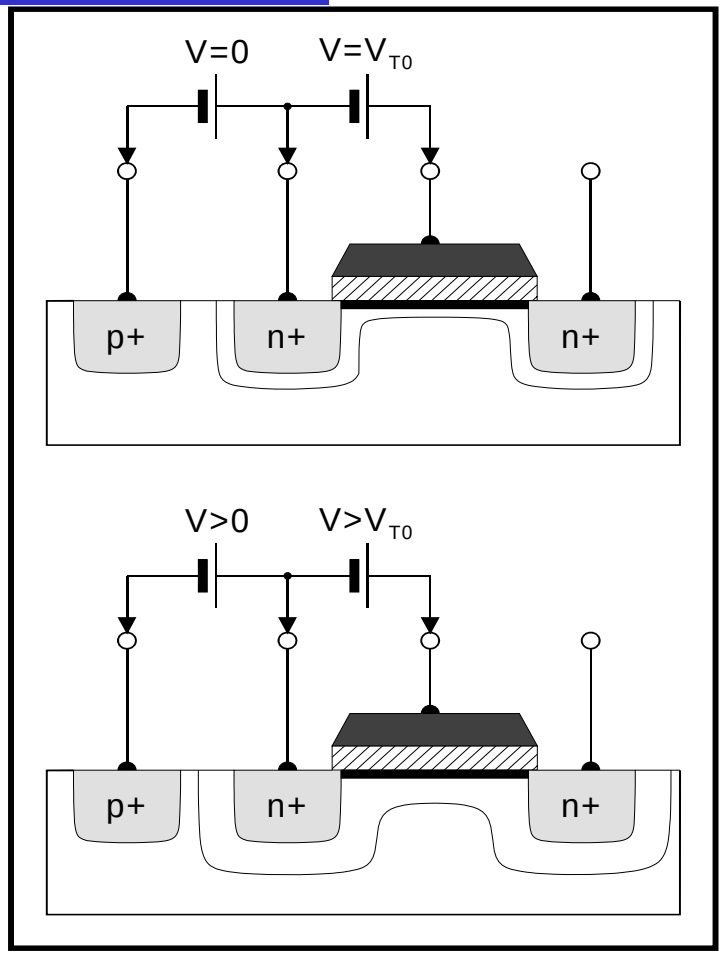
- For example, material parameters that effect V_t include:
  - The gate conductor material (poly vs. metal).
  - The gate insulation material (SiO_2).
  - The thickness of the gate material.
  - The channel doping concentration.
- However, V_t is also dependent on
  - V_{sb} (the voltage between source and substrate), which is normally 0 in digital devices.
  - Temperature: changes by -2mV/degree C for low substrate doping levels.

2.4 Threshold Voltage of the MOS Transistor Added in Body-Effect

- The result of Body-Effect is : as VB drops V_{TH} will increases; this is called “body effect” or “backgate effect”
- It can be proved for following equation

2.4 Threshold Voltage of the MOS Transistor Added in Body-Effect

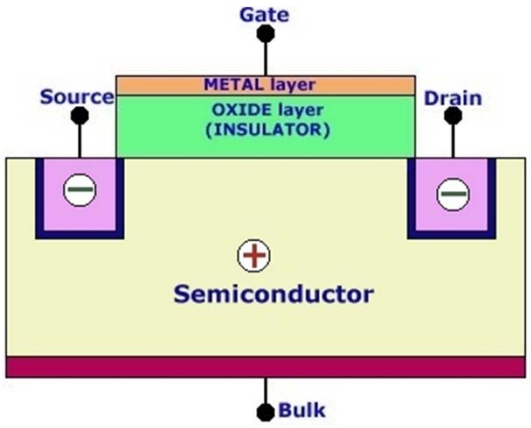
- The threshold depends on:
  - Gate oxide thickness
  - Doping levels
  - Source-to-bulk voltage
- When the semiconductor surface inverts to n-type the channel is in "strong inversion"
- $V_{sb} = 0 \Rightarrow$ strong inversion for:
  - surface potential > $2\phi_F$
- $V_{sb} > 0 \Rightarrow$ strong inversion for:
  - surface potential > $2\phi_F + V_{sb}$

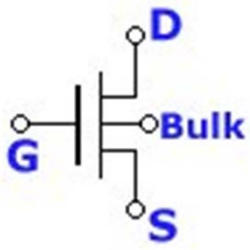


Source: Paulo Moreiar

2.4 Threshold Voltage of the MOS Transistor Added in Body-Effect

- In the analysis of page25 ~ page28, we tacitly assumed that the bulk and the source of the transistor were tied to ground.
- What happens if the bulk voltage of an NMOS drops below the source voltage

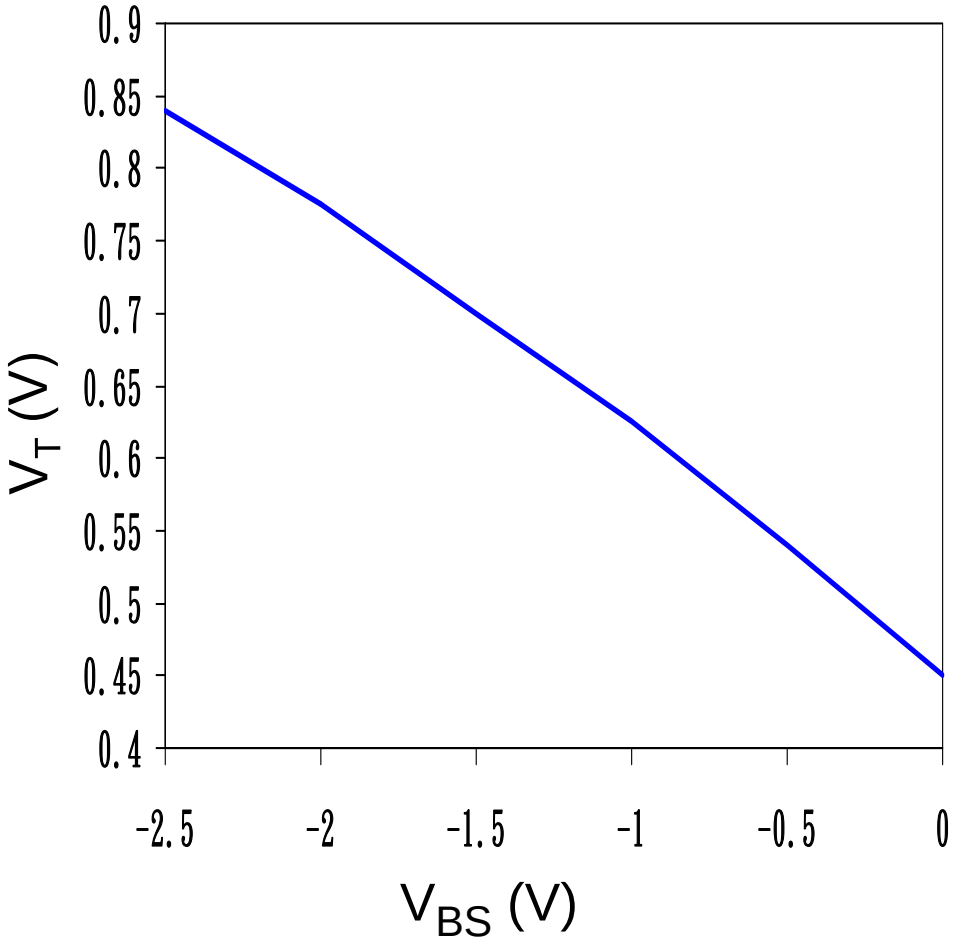




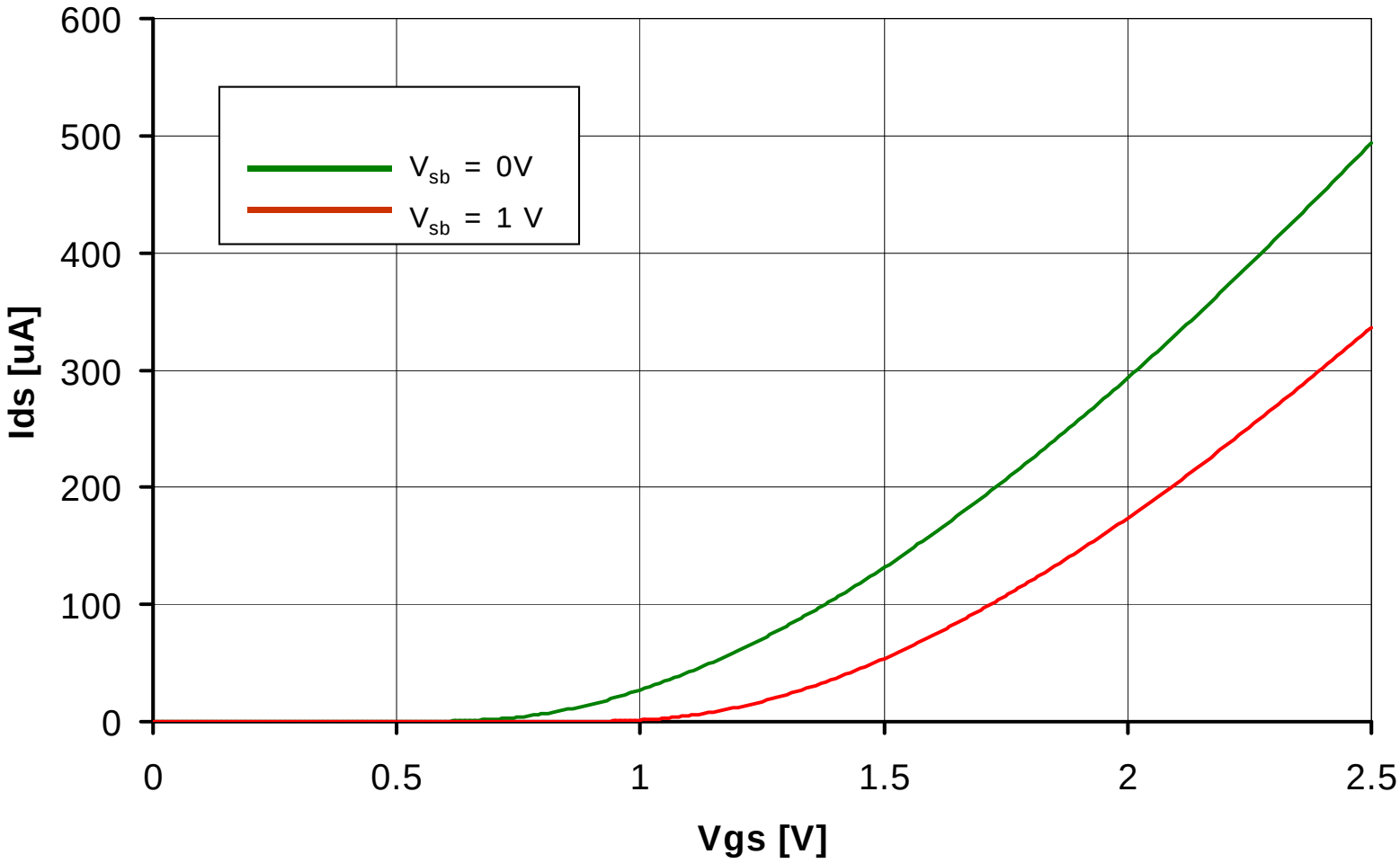
$V_B < 0$

2.4 The Body Effect

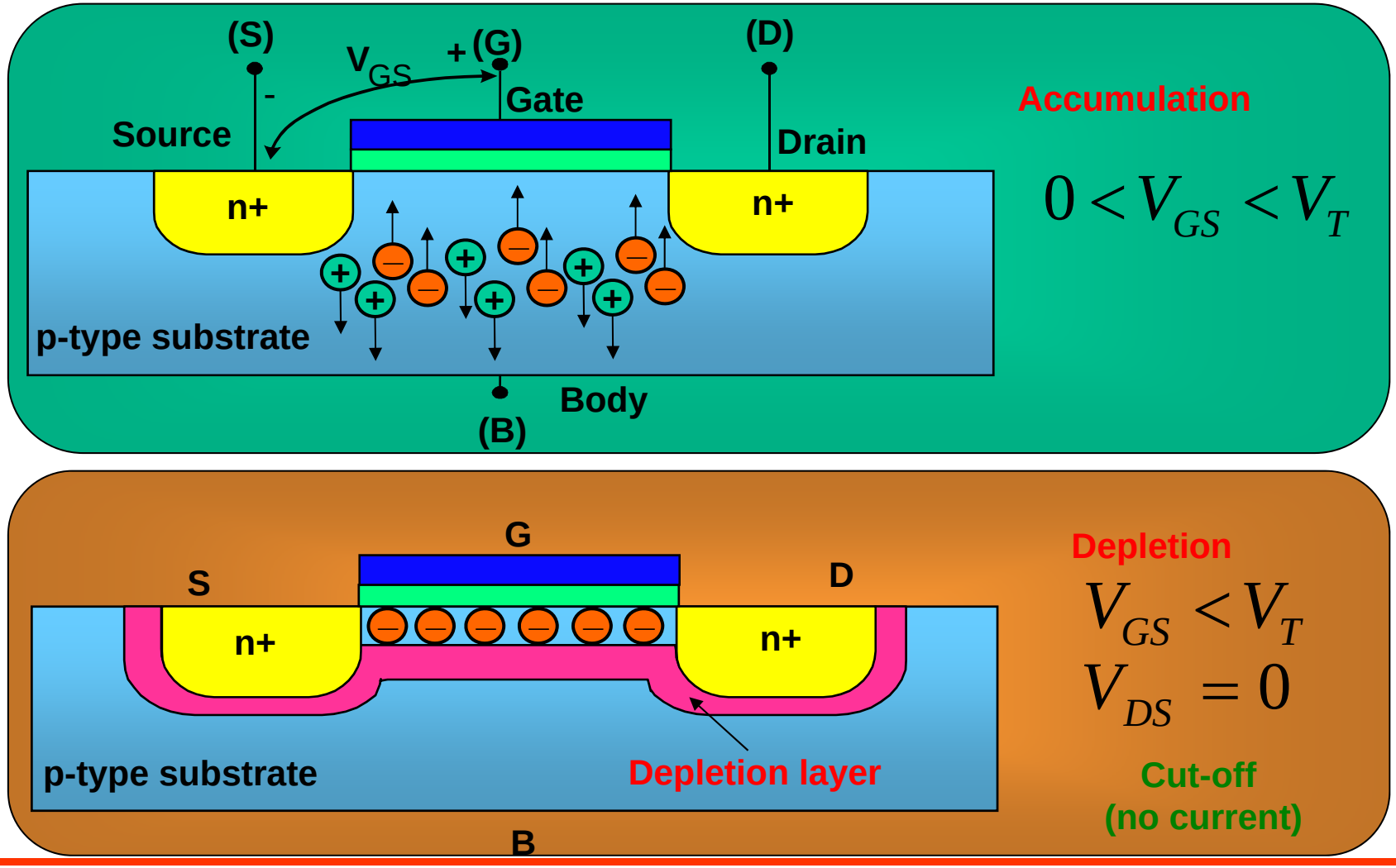
- V_{BS} is the substrate bias voltage (normally positive for n-channel devices with the body tied to ground)
- A negative bias causes V_T to increase from 0.45V to 0.85V



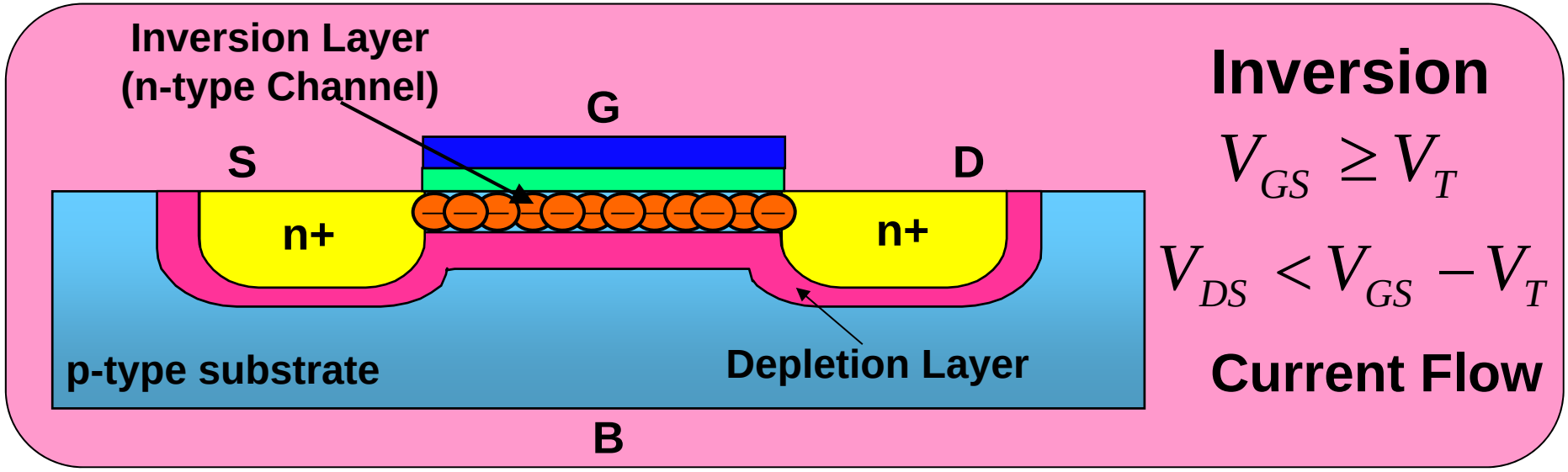
2.4 Threshold Voltage of the MOS Transistor added in Body-Effect



2.4 NMOS Theory of Operation



2.4 NMOS Operation (Triode Mode)

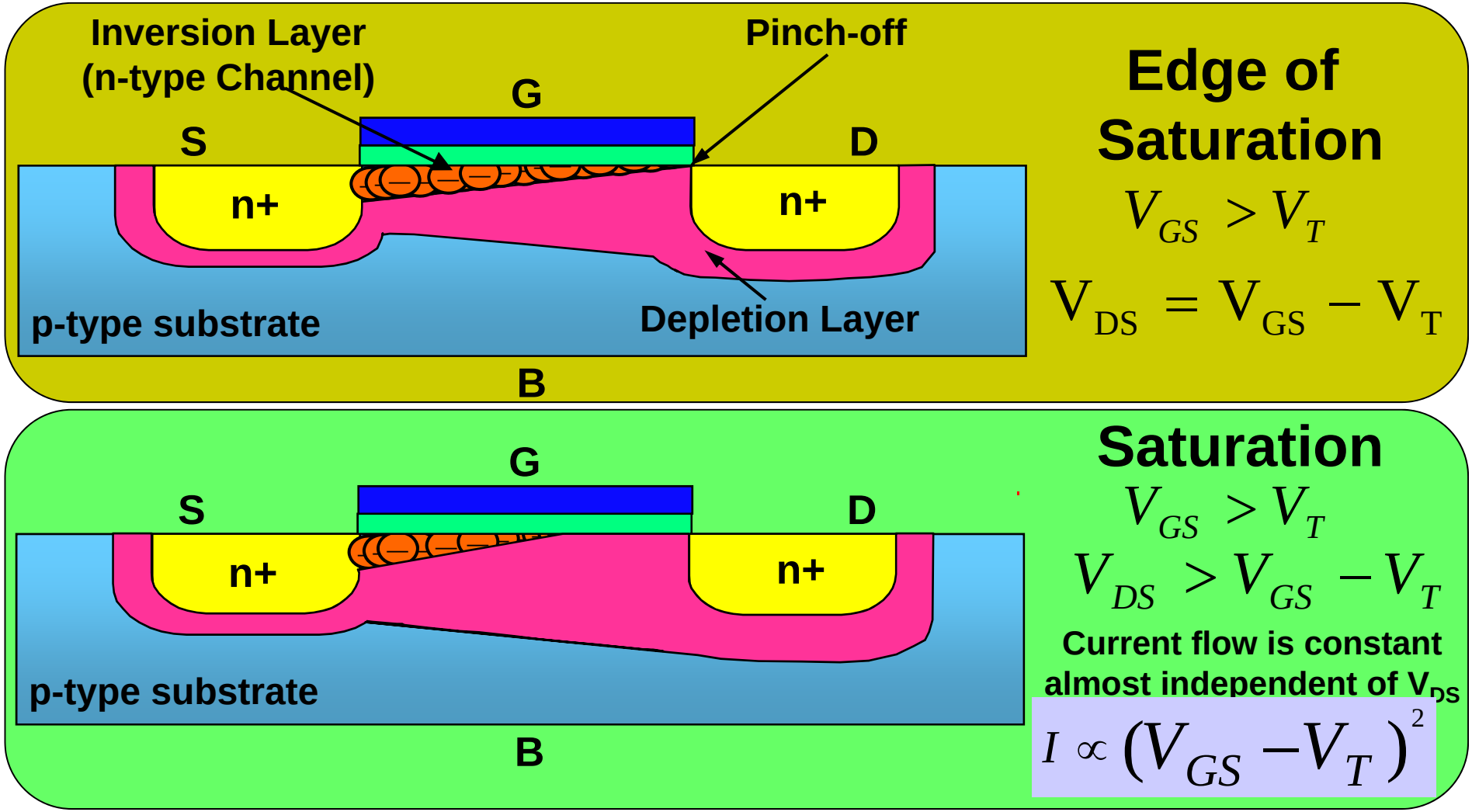


Threshold voltage, V_T, is the potential difference between gate and source, V_{GS}, just enough to invert the channel and let the current flow

In triode (also called linear) mode current flow increases by increasing V_{GS} and V_{DS}

$$I \propto (V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}$$

2.4 NMOS Operation (Saturation Mode)

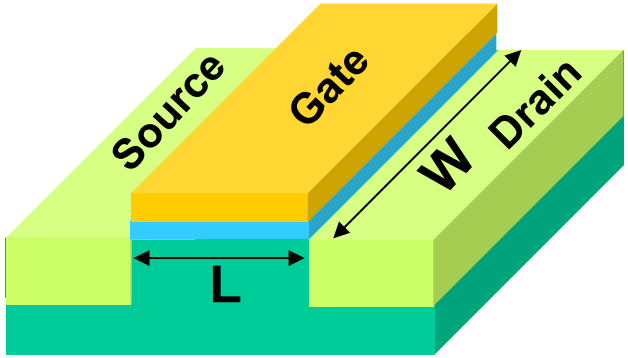


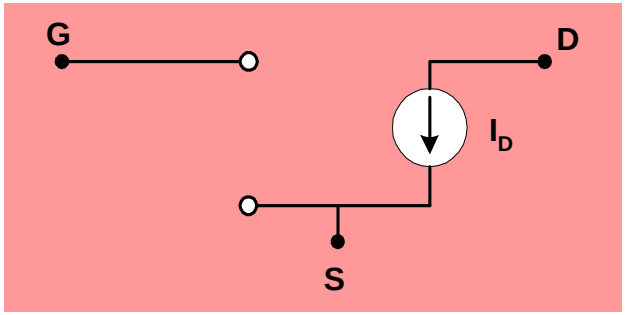
2.4 MOSFET Equations

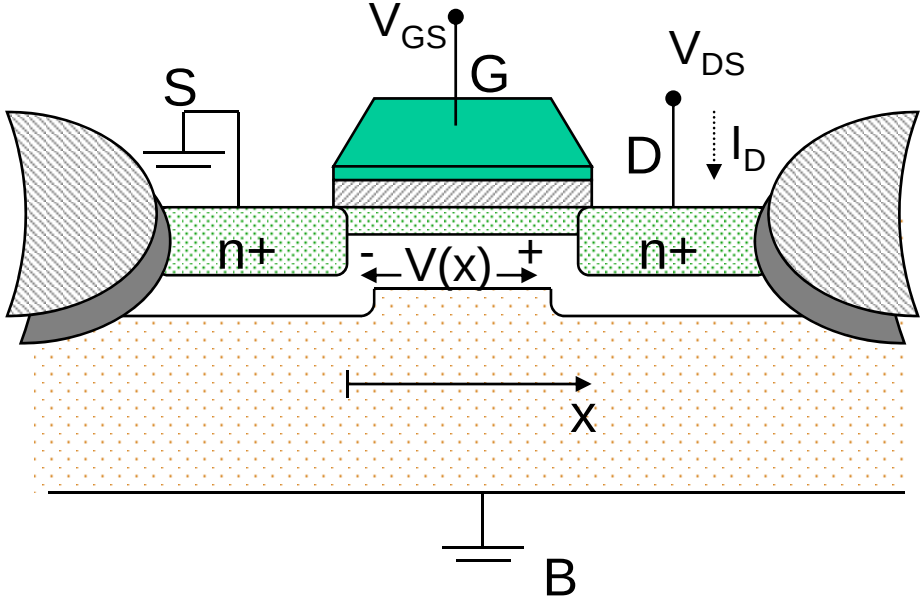
- Cut-off region
- Linear region
- Saturation
- Oxide capacitance
- Process “transconductance”

2.4 Transistor in Linear Mode—$0<V_{DS}<V_{GS}-V_T$

- $I_D = \beta\, W/L\, [(V_{GS} - V_T)V_{DS} - V_{DS}^2/2]$

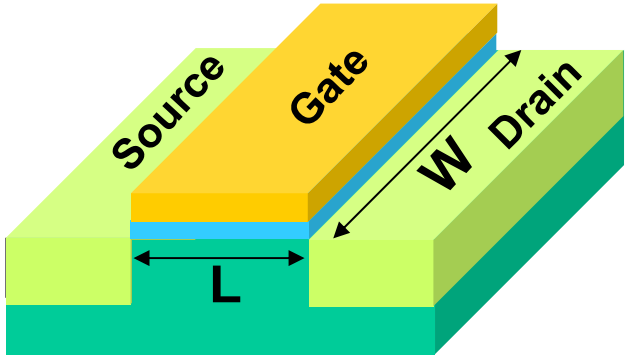


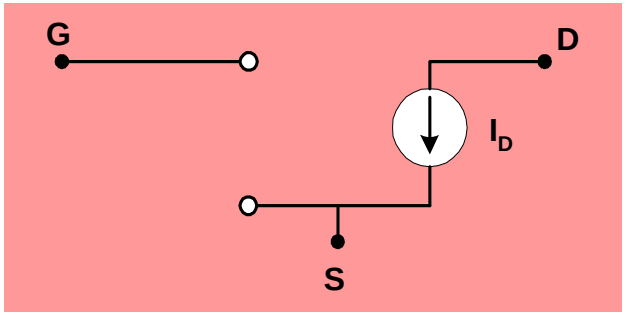


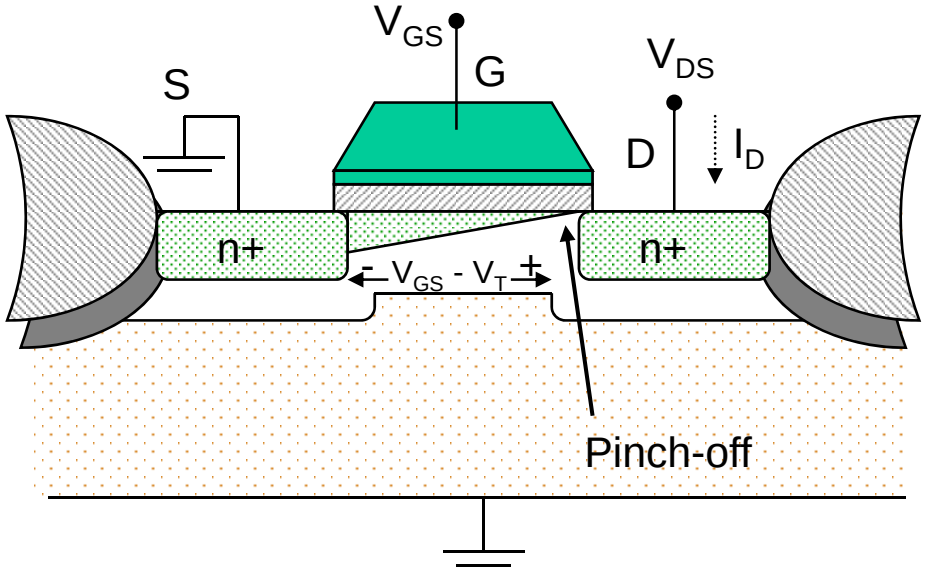


2.4 Transistor in Saturation Mode-- $V_{DS} > V_{GS} - V_T$

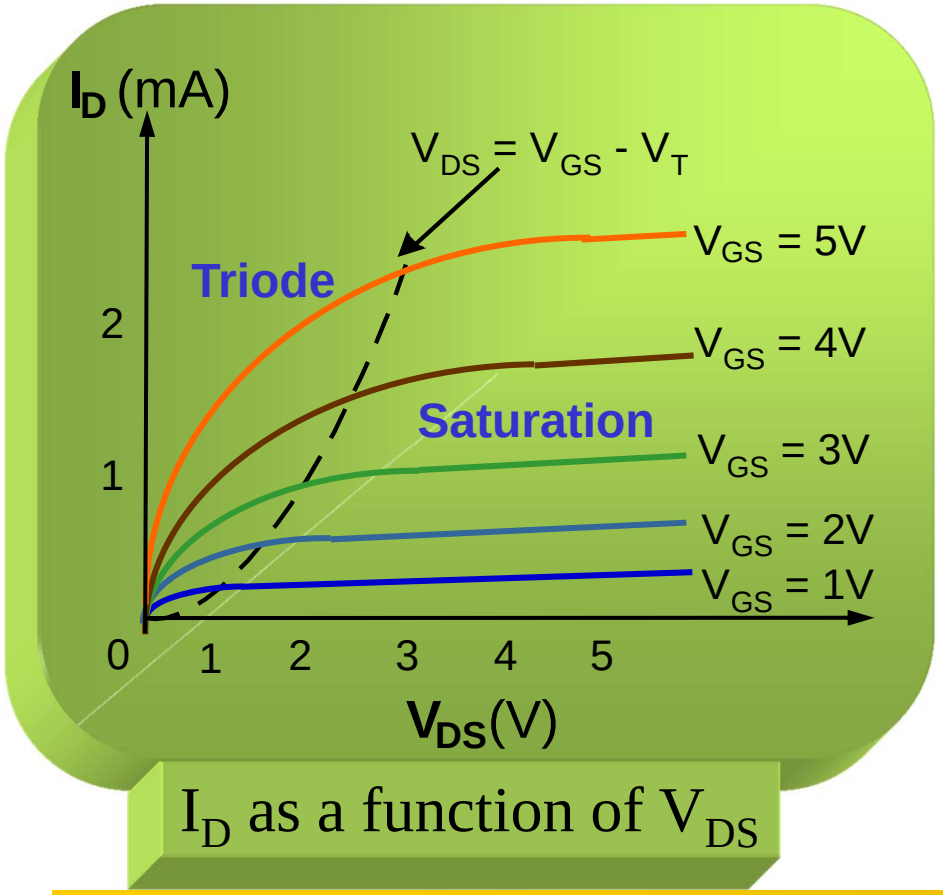
- $I_{DS} = \frac{\beta W}{2L}(V_{GS} - V_T)^2$



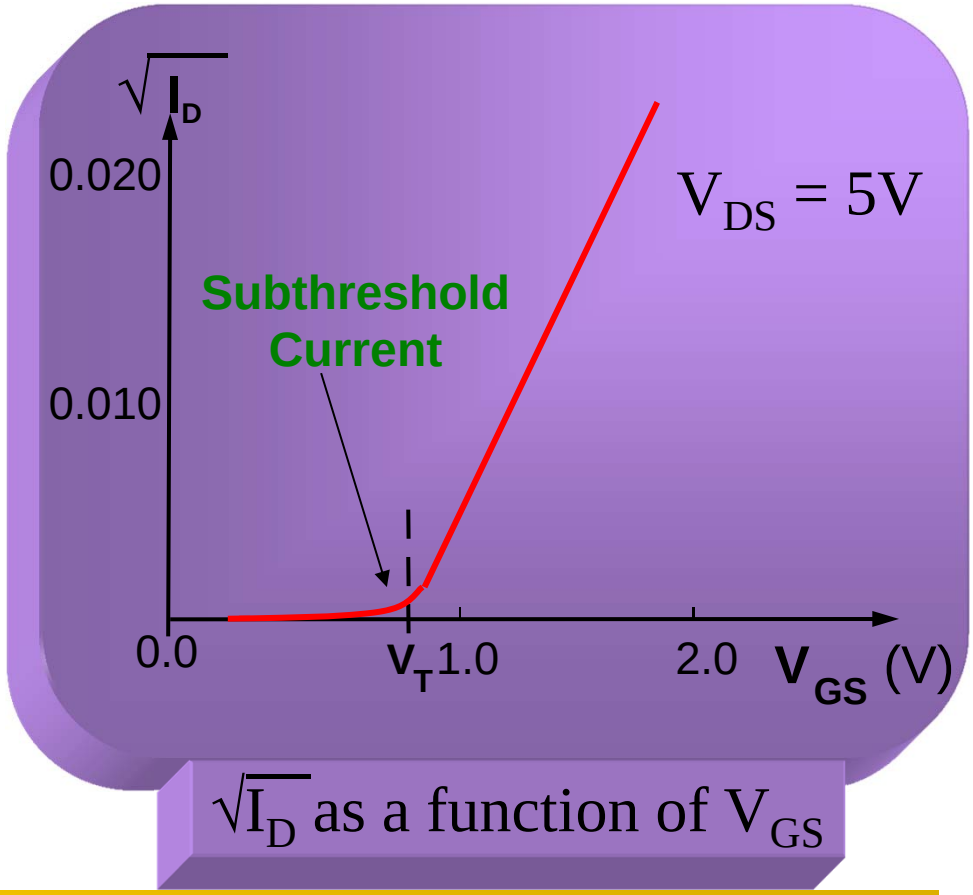




2.5 NMOS Current-Voltage Characteristic



I_D as a function of V_{DS}



$\sqrt{I_D}$ as a function of V_{GS}

Channel Length Modulation

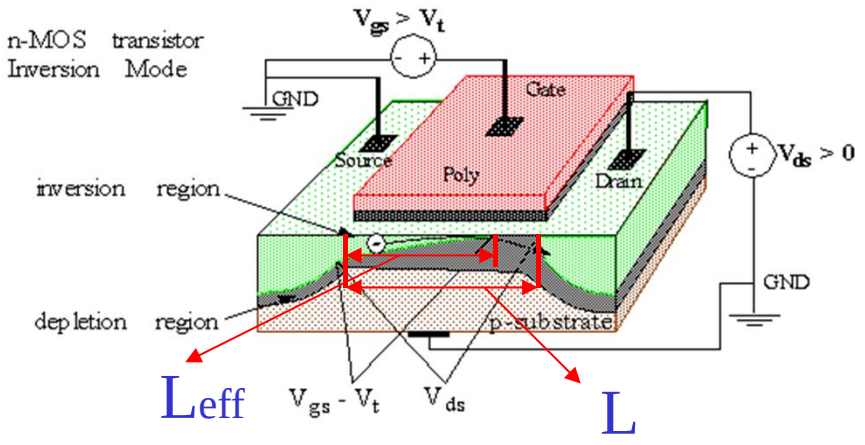
Refers to the fact that due to the enlargement of depletion layer on the drain side and, hence, reduction of channel length, I_D slightly increases as V_{DS} increases in saturation

2.5 NMOS Current-Voltage Characteristic added in Channel-Length Modulation

- In the saturation region conductance channel is pinched-off

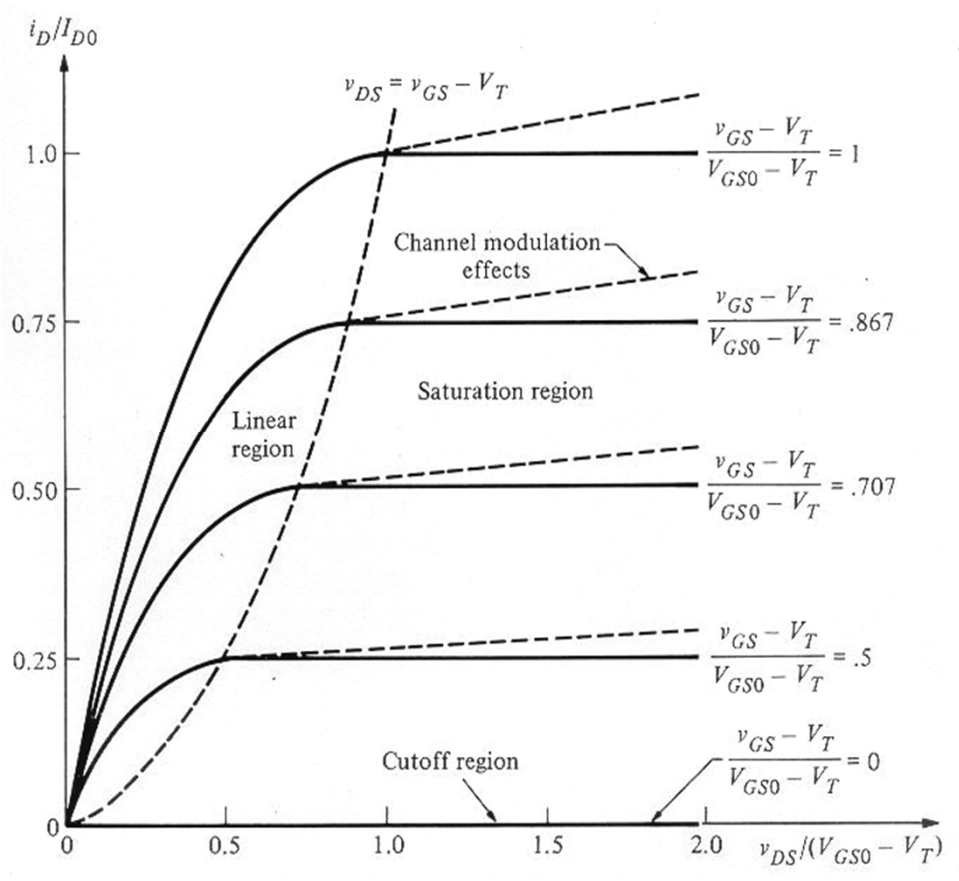
λ : channel-length modulation parameter

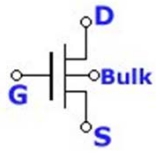
$\lambda \cong 0.1 \sim 0.001$ (/V)



2.5 NMOS Current-Voltage Characteristic

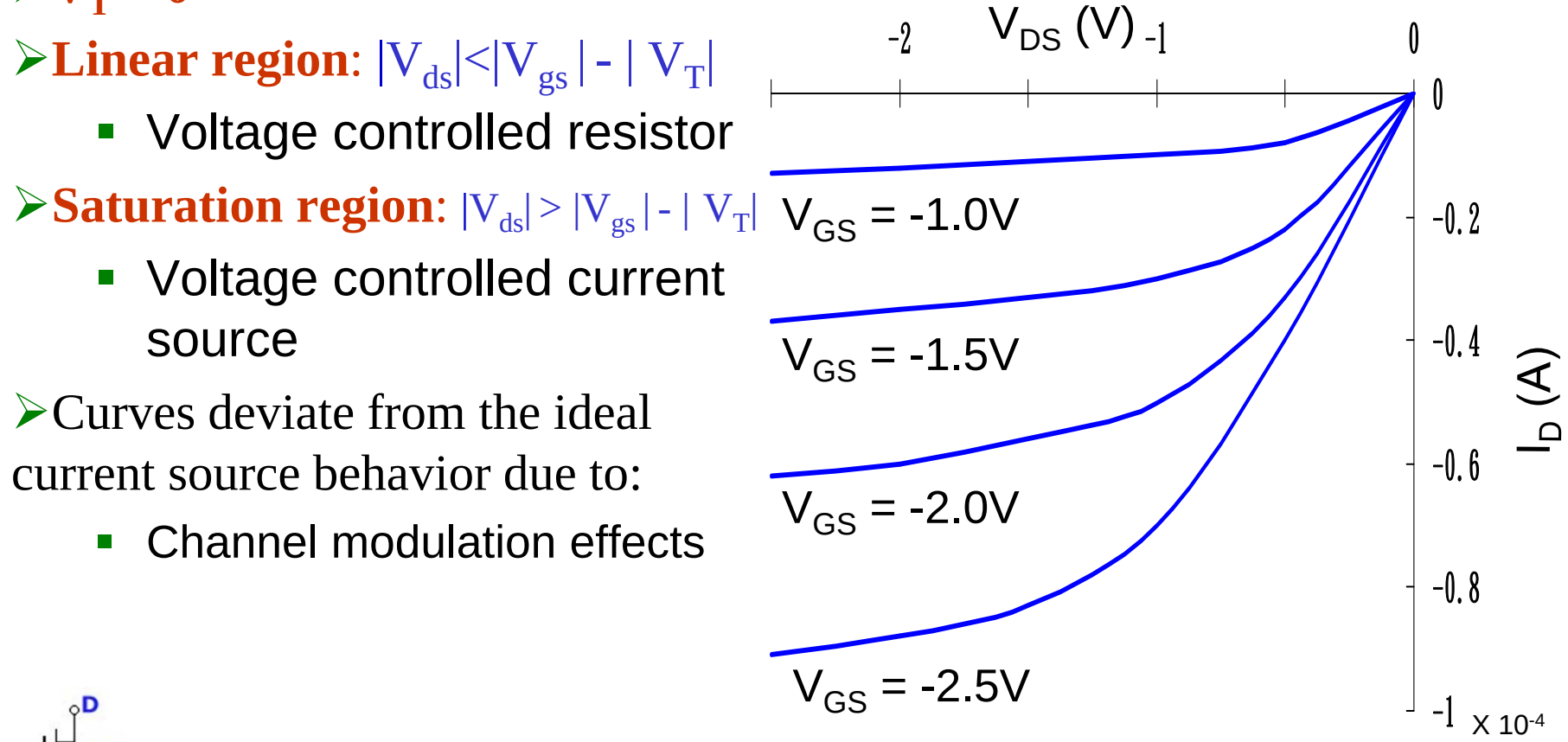
- **Linear region**: $V_{ds}<V_{gs}-V_T$
  - Voltage controlled resistor
- **Saturation region**: $V_{ds}>V_{gs}-V_T$
  - Voltage controlled current source
- Curves deviate from the ideal current source behavior due to:
  - Channel modulation effects

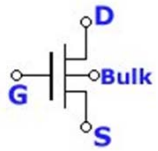




2.5 PMOS Current-Voltage Characteristic

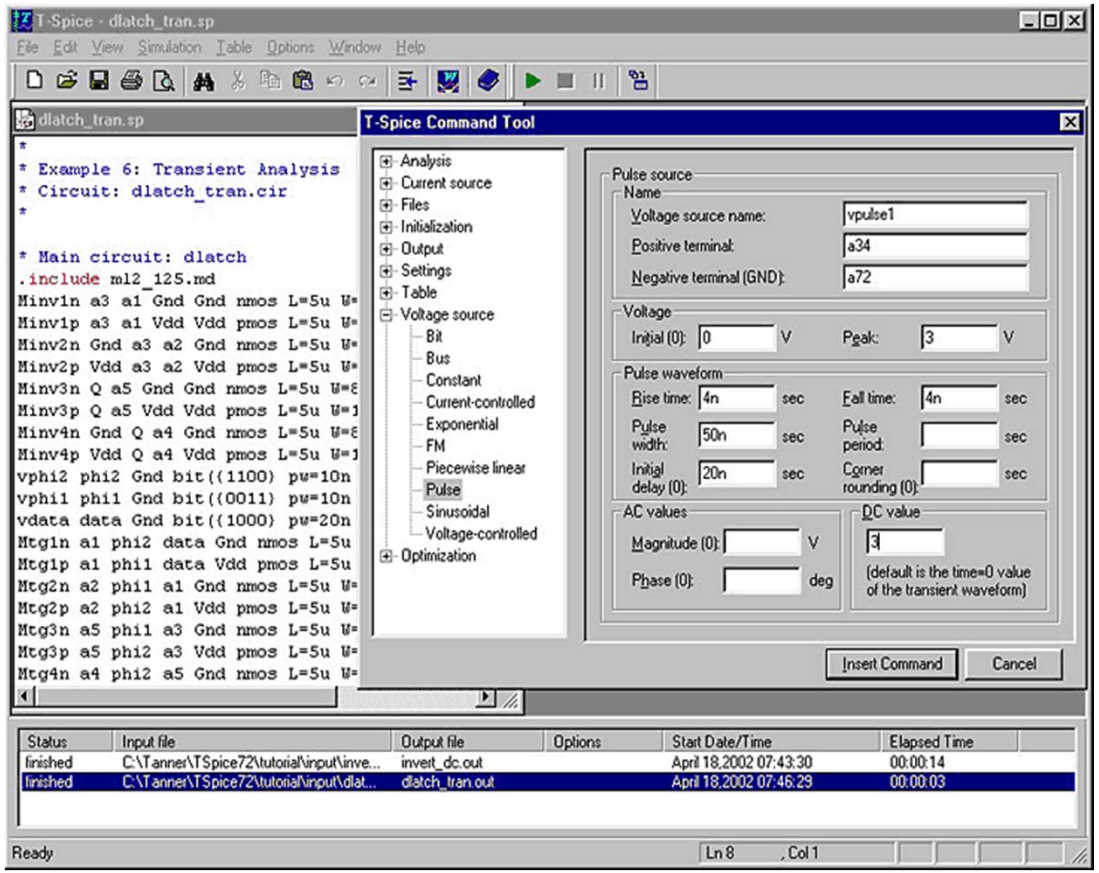
- **$V_T < 0$**
- **Linear region**: $|V_{ds}| < |V_{gs}| - |V_T|$
  - Voltage controlled resistor
- **Saturation region**: $|V_{ds}| > |V_{gs}| - |V_T|$
  - Voltage controlled current source
- Curves deviate from the ideal current source behavior due to:
  - Channel modulation effects





2.6 Modeling the MOS Transistor for Circuit Simulation

- SPICE
(Simulation Program, Integrated Circuit Emphasis) is widely used for IC simulation



2.6.1 SPICE MOSFET Model

- Level = 1 Schichman – Hodges Model
- Level = 2 Modified Grove – Frohman Model
- Level = 3 Empirical Model

The default value of level is 1

2.6.1 SPICE MOSFET Model

- The SPICE model of a MOSFET includes a variety of parasitic circuit elements and some process related parameters in addition to the elements previously discussed in this chapter. The syntax of a MOSFET incorporates the parameters a circuit designer can change as shown below:

MOSFET syntax

M <name> <drain node> <gate node> <source node> <bulk/substrate node>
+ [L=][W=][AD=][AS=]
+ [PD=][PS=][NRD=][NRS=]
+ [NRG=][NRB=]

where L is the gate length, W the gate width, AD the drain area, AS the source area
PD is the drain perimeter, PS is the source perimeter

2.6.1 SPICE MOSFET Model

Example:

M1 3 2 1 0 NMOS L=1u W=6u

.MODEL NFET NMOS (LEVEL=2 L=1u W=1u VTO=-1.44 KP=8.64E-6

+ NSUB=1E17 TOX=20n)

where M1 is one specific transistor in the circuit, while the transistor model "NFET" uses the built-in model NFET to specify the process and technology related parameters of the MOSFET.

2.6.1 SPICE MOSFET Model

SPICE variable	Equation
TOX	$TOX = t_{ox}$
KP	$KP = \mu C_{ox}$
VTO	$VTO = V_{FB} + 2\phi_F + \frac{\sqrt{2\varepsilon_S q N_a (2\phi_F)}}{C_{OX}}$
GAMMA	$GAMMA = \gamma = \frac{\sqrt{2\varepsilon_S q N_a}}{C_{OX}}$
NSUB	$NSUB = N_d$ or N_a
U0	$U0 = \mu$
LAMBDA	$LAMBDA = \lambda$
VMAX	$VMAX = v_{sat}$

SPICE parameters and corresponding equations

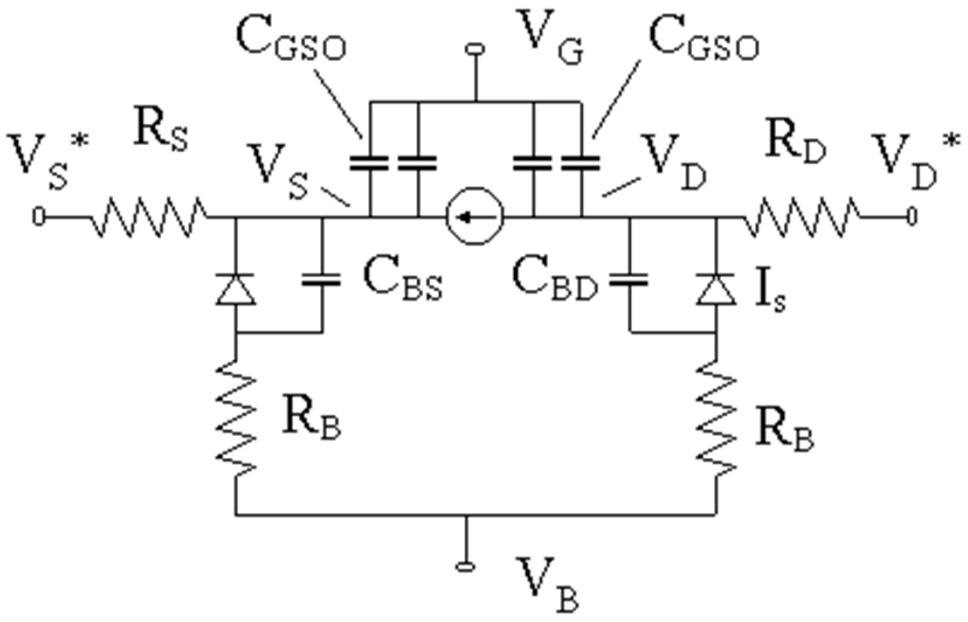
2.6.1 SPICE MOSFET Model

In addition there are additional parameters, which can be specified to further enhance the accuracy of the model, such as:

LD , lateral diffusion (length)
RD, drain ohmic resistance
RG, gate ohmic resistance
IS, bulk p-n saturation current
CBD, bulk-drain zero-bias p-n capacitance
CGSO/CGDO, gate-source/drain overlap capacitance/channel width
XJ, metallurgical junction depth
WD, lateral diffusion (width)
RS, source ohmic resistance
RB, bulk ohmic resistance
JS, bulk p-n saturation current/area
CBS, bulk-source zero-bias p-n capacitance

2.6.1 SPICE MOSFET Model

- Large signal model of a MOSFET



2.7 Limitations on the MOS Transistor

2.7.1 Voltage Limitations

- Punch through

  As $V_D \uparrow$ $\Rightarrow$ D-B PN junction width $\uparrow$

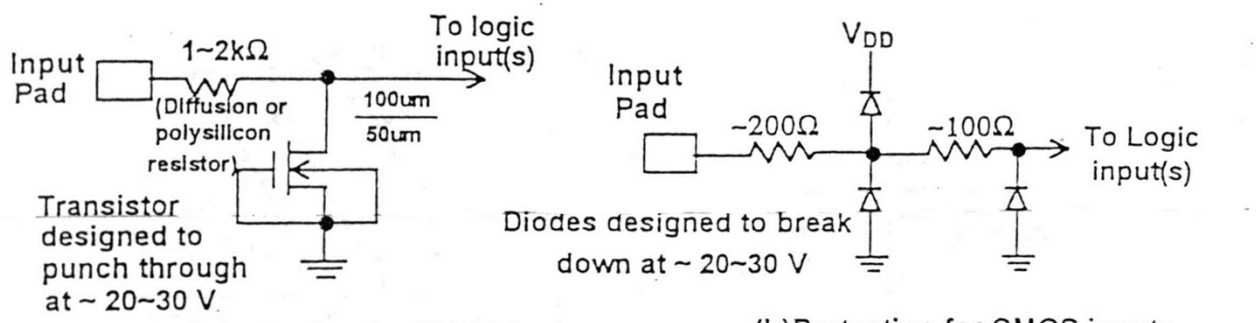
  $\Rightarrow$ extends to S-B depletion

  $\Rightarrow$ Punch through

※ Punch through occurs at VD in 15 to 20 V.

2.7.1 Voltage Limitations

- Static charge (come from I/O Pads)
  - will destroy the gate dielectric.
  - can overcome by protection ckt.

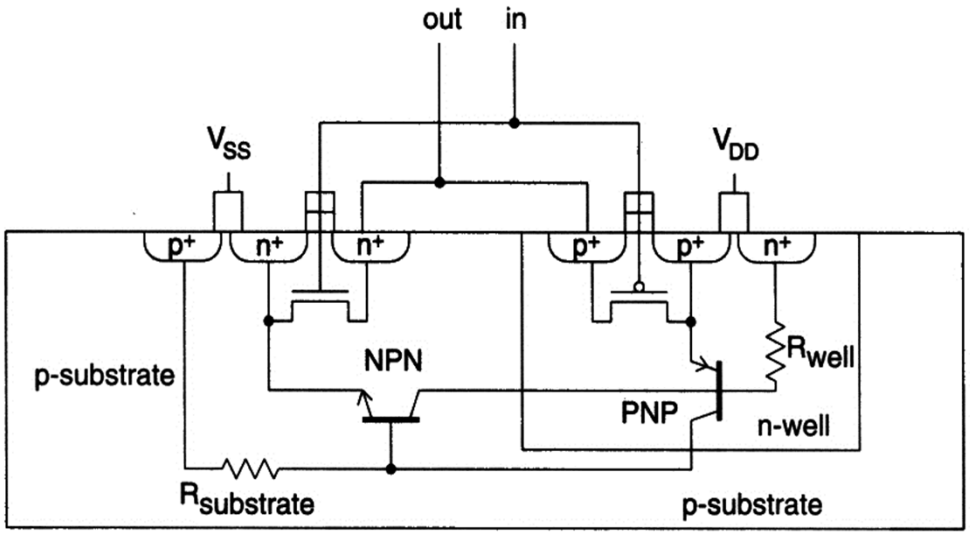


(a) Protection for NMOS inputs (b)Protection for CMOS inputs

FIGURE 1.10 Input protection for MOS circuits.

2.7.2 Parasitic Bipolar Transistors and Latch-up

- Sequence of events for latch-up to occur
  1. The initial (forward biasing of one xtor)
  2. The regeneration (forward biasing the other xtor, thus one driving the other)
  3. Self-sustaining (the power supply must be capable of sustaining the current flow), the amount of current is called the Holding Current



Equivalent Circuit

2.7.2 Parasitic Bipolar Transistors and Latch-up

- Common latchup suppression methods :

1. Bipolar spoiling : reduction βnpn or βpnp ➔ degrade VLSI device performance
   - Beta reduction
     - Life time (base) reduction : gold doping
     - Increase lateral spacing (base width) (vertical dimension are fixed by process) ie. NMOS to N-well or PMOS to P-well
   - guard-rings to reduce $R_{substrate}$ and R_{well}, increase the space between n-well & NMOS, …

2.7.2 Parasitic Bipolar Transistors and Latch-up

2. Bipolar Decoupling : prevent one transistor from turning on other-reduction of R_{well} and $R_{substrate}$

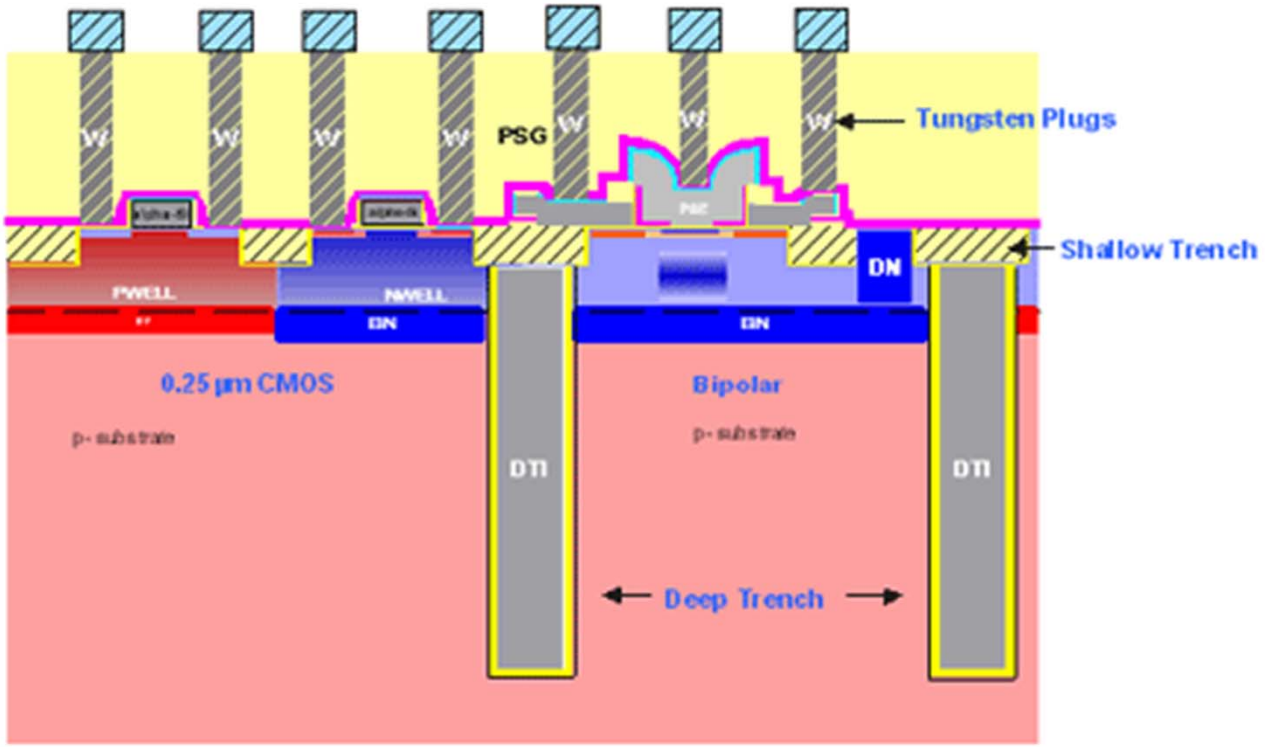
- R_{well} reduction
  - Using enough well plugs (ohmic connections from the well to, usually through metal)
  - Placing P+ (for P-well process) collar around the pexiphery of a well. This greatly reduced R_{well} (from several kΩ to less than 100Ω)and is most useful for I/O circuits, where latching disturbance are most serve.
- $R_{substrate}$ reduction
  - Using frequent substrate plugs (ohmic contacts connect to VDD)
  - Epi wafer

2.7.2 Parasitic Bipolar Transistors and Latch-up

3. Other process stricture
   - trench isolation
   - SOI (Silicon on Insulator)

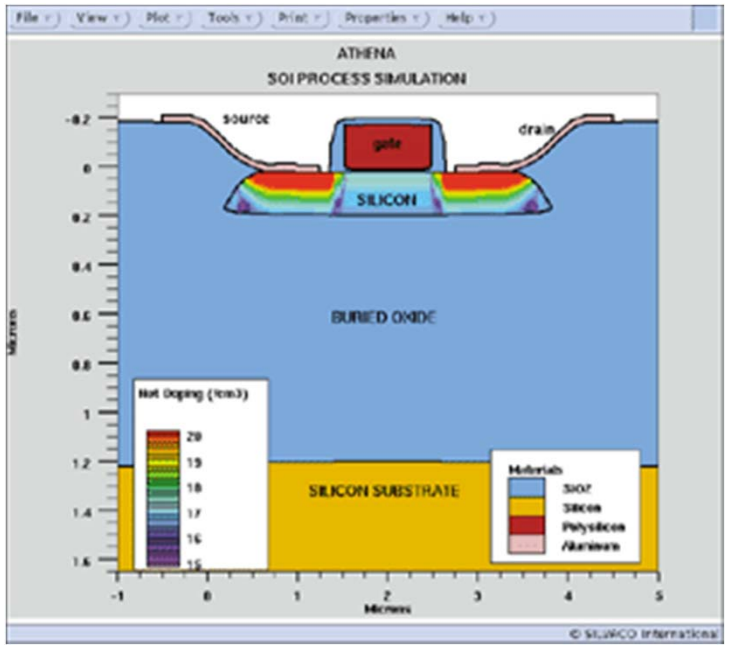
2.7.2 Parasitic Bipolar Transistors and Latch-up

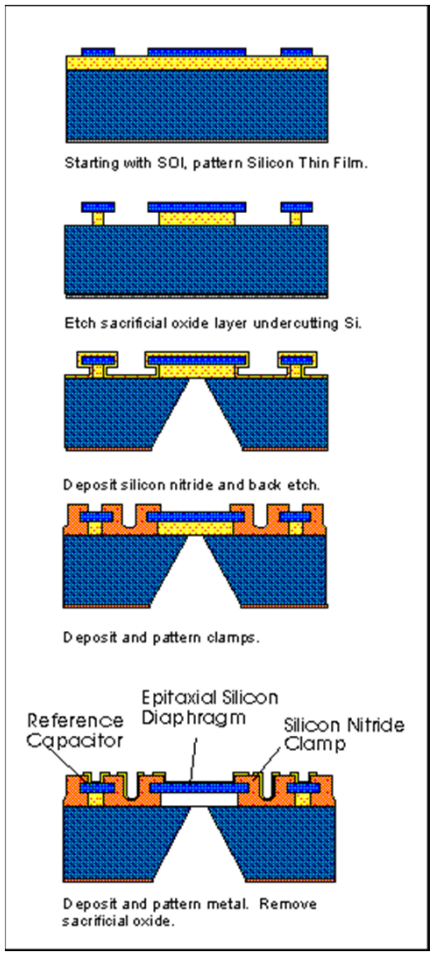
- Trench isolation



2.7.2 Parasitic Bipolar Transistors and Latch-up

- SOI (Silicon on Insulation)





Appendix

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