

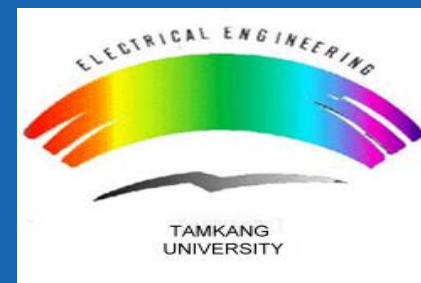
# 第06次組語實習課

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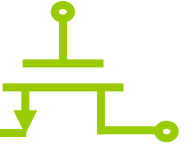
2023 Advanced Mixed-Operation System (AMOS) Lab.



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# p.90 EXAMPLE 5.4



## EXAMPLE 5.4

Consider a simple ARM7TDMI program that copies moves a string of characters from one memory location to another.

(C語言寫法)

#define SRAM\_BASE 0x40000000

Equal

0x40000000

->從這個位置以後能讓使用者存取。

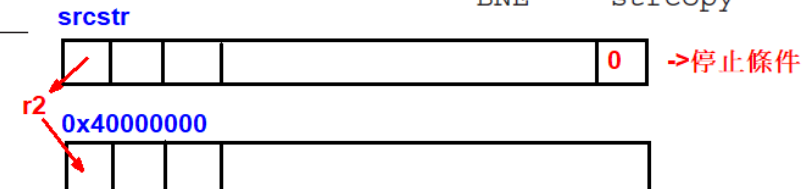
TABLE 4.2  
Frequently Used Directives

Keil Directive	CCS Directive	Uses
AREA	.sect	Defines a block of code or data
RN	.asg	Can be used to associate a register with a name
EQU	.equ	Equates a symbol to a numeric constant
ENTRY		Declares an entry point to your program
DCB, DCW, DCD	.byte, .half, .word	Allocates memory and specifies initial runtime contents
ALIGN	.align	Aligns data or code to a particular memory boundary
SPACE	.space	Reserves a zeroed block of memory of a particular size
LTORG		Assigns the starting point of a literal pool
END	.end	Designates the end of a source file

```

SRAM_BASE EQU 0x40000000 ; start of SRAM for STR910FM32
AREA StrCopy, CODE
ENTRY
Main ADR r1, srcstr ; mark the first instruction
      LDR r0, =SRAM_BASE ; pointer to the second string

strcpy
      LDRB r2, [r1], #1 ; load byte, update address
      STRB r2, [r0], #1 ; store byte, update address
      CMP r2, #0 ; check for zero terminator
      BNE strcpy ; keep going if not
    
```



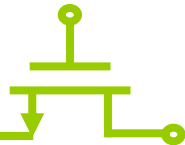
Loads, Stores, and Addressing

91

```

stop B stop ; terminate the program
srcstr DCB "This is my (source) string", 0
      END
    
```





2023/11/2

# p.90 EXAMPLE 5.4-補充題型1

## ❖ Reverse string

The screenshot displays a debugger interface with three main panels:

- Registers:** Shows the current state of registers. R0 is 0x3FFFFFFF, R1 is 0x0000003B, and R2 is 0x00000000. The PC register is at 0x0000001C.
- Disassembly:** Shows assembly code for 'ex5.4r.s'. Key instructions are highlighted:
  - Line 7: `ADD r0, #25` (highlighted with a red box)
  - Line 10: `CMP r2, #0` (highlighted with a red box)
  - Line 11: `STRBNE r2, [r0], #-1` (highlighted with a red box)
- Memory 1:** Two views of memory starting at address 0x40000000.
  - The top view shows the initial state of memory, with the string "This is my (source) string" stored in reverse order (starting with 'n' at offset 0).
  - The bottom view shows the memory after the reversal operation, where the string is now in its original order (starting with 'T' at offset 0).

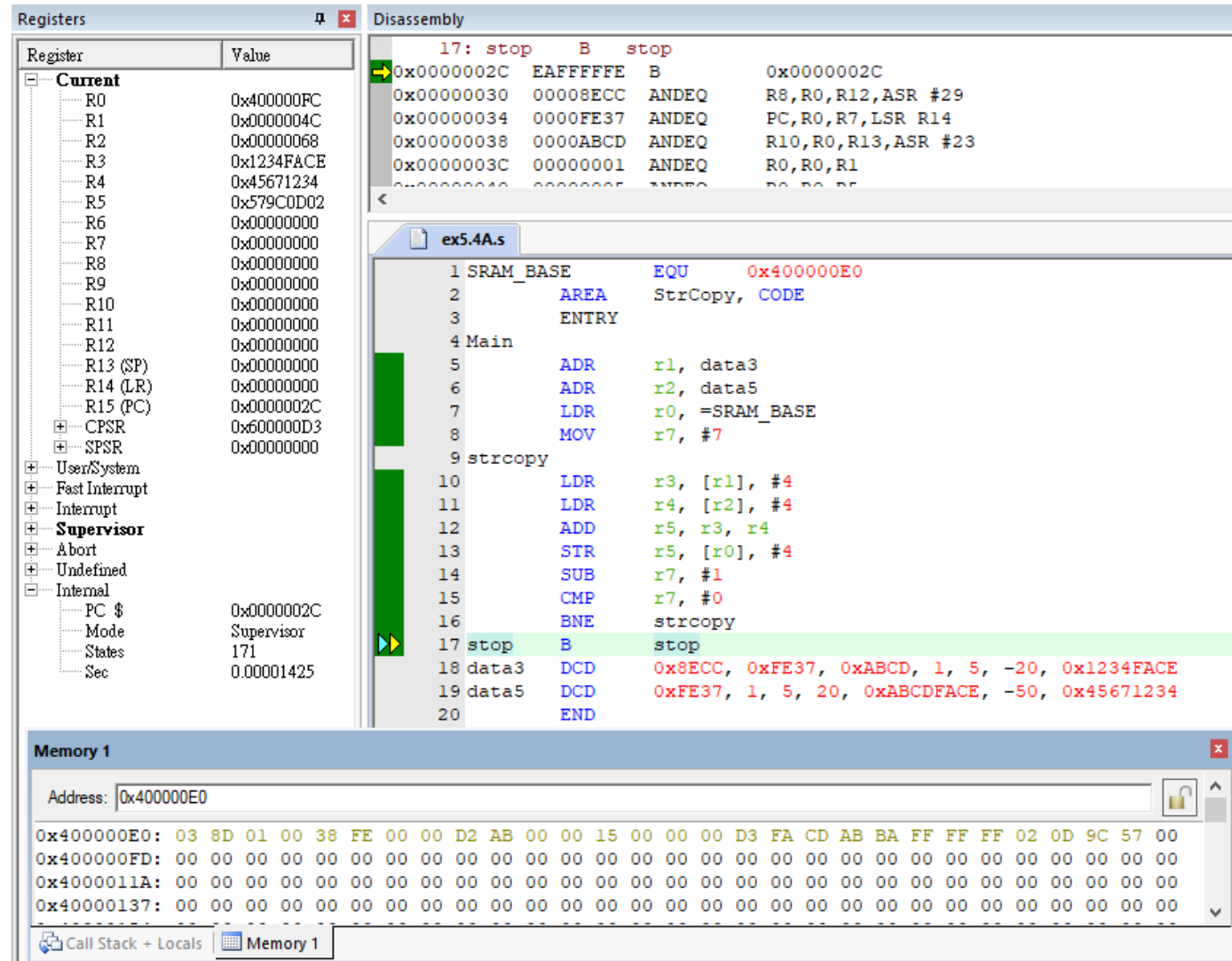
→ 字串總長度為26 bytes  
 → 先讓初始位置r0變為r0+25，  
 從字串總長度最後一個位置開始往前存。  
 (存完1個byte → r0 = r0 - 1)

→ 原本的

## p.90 EXAMPLE 5.4-補充題型2

- ❖ Word array(DCD) #4 #-4
- ❖ Halfword array(DCW) #2 #-2
- ❖ Add the corresponding words between data3 and data5 and put the sums one by one in memory started from address 0x400000E0.

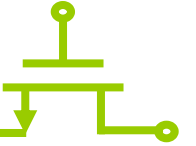
```
data3 DCD 0x8ECC, 0xFE37, 0xABCD, 1, 5, -20, 0x1234FACE
data4 DCB 0xCF, 23, 39, 0x54, 250, 0xFF, 0xAD, -20, -30
data5 DCD 0xFE37, 1, 5, 20, 0xABCDFACE, -50, 0x45671234
```



The screenshot displays three panels from an ARM development tool:

- Registers:** Shows the current state of registers. R0 is 0x400000FC, R1 is 0x0000004C, R2 is 0x00000068, R3 is 0x1234FACE, R4 is 0x45671234, R5 is 0x579CDD02, R6 is 0x00000000, R7 is 0x00000000, R8 is 0x00000000, R9 is 0x00000000, R10 is 0x00000000, R11 is 0x00000000, R12 is 0x00000000, R13 (SP) is 0x00000000, R14 (LR) is 0x00000000, R15 (PC) is 0x0000002C. CPSR is 0x600000D3, SPSR is 0x00000000.
- Disassembly:** Shows the assembly code for 'ex5.4A.s'. It includes a stop instruction at 17, followed by instructions to load data from data3 and data5 into registers R3, R4, R5, and R7, and then store the result back into R7. The code ends with a stop instruction at 17.
- Memory 1:** Shows the memory dump starting at address 0x400000E0. The first four words (0x400000E0 to 0x400000E3) contain the data from data3 and data5. The rest of the memory is filled with zeros.

# p.124 TST指令



Q : read bits(讀取某個bits)

A1 : AND (具破壞性，使暫存器數值發生變化)

A2 : TST (undestructive，暫存器數值不發生改變)

補充： CMP r0, r1 CPU實際會做 r0-r1  
= 0 -> EQ  
!= 0 -> NE

Ex :

```
TST  r0, #0b0100 ;read bit2 of r0
BNE  X1
```

bit2 = 0 -> EQ  
bit2 = 1 -> NE

; bit2 = 0

X1

用這個隔開  
B NEXT

; bit2 = 1

NEXT

Read multiple bits

EX :

```
TST  r0, #0b1111
TST  r1, #0x0000000F
```

All bits read = 0 -> EQ

otherwise -> NE



# p.124 TST指令-補充題型1



- ❖ Put the number of 1's of r0 into r1.(r0 = 0b11110000110011110011000100001111)    ANS : r1 = 17

Registers

Register	Value
<b>Current</b>	
R0	0xF0CF310F
R1	0x00000011
R2	0x00000000
R3	0x00000000
R4	0x00000000
R5	0x00000000
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000028
CPSR	0x600000D3
SPSR	0x00000000
<b>User/System</b>	
Fast Interrupt	
Interrupt	
<b>Supervisor</b>	
Abort	
Undefined	
<b>Internal</b>	
PC \$	0x00000028
Mode	Supervisor
States	308
Sec	0.00002567

Disassembly

```

0x00000020 E3530000 CMP R3,#0x00000000
13: BNE LOOP
14:
0x00000024 1AFFFFF9 BNE 0x00000010
15: STOP B STOP
0x00000028 EAF7FFFE B 0x00000028
0x0000002C F0CF310F (32)

```

TST1.s\*

```

1 AREA TST1, CODE, READONLY
2 ENTRY
3 LDR r0, =0xF0CF310F
4 LDR r1, =0
5 LDR r2, =0x1
6 LDR r3, =32
7 LOOP
8 TST r0, r2
9 ADDNE r1, r1, #1
10 LSL r2, r2, #1
11 SUB r3, #1
12 CMP r3, #0
13 BNE LOOP
14
15 aSTOP B STOP
16 END

```



## p.124 TST指令-補充題型2



- ❖ Put the number of different bits between r0 and r1 into r3.(r0 = 0x1010, r1 = 0101)      ANS : 4

**Registers**

Register	Value
<b>Current</b>	
R0	0x00001010
R1	0x00000101
R2	0x00000000
R3	0x00000004
R4	0x00000000
R5	0x00001111
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x00000000
R14 (LR)	0x00000000
R15 (PC)	0x00000030
CPSR	0x600000D3
SPSR	0x00000000
<b>User/System</b>	
Fast Interrupt	
Interrupt	
<b>Supervisor</b>	
Abort	
Undefined	
<b>Internal</b>	
PC \$	0x00000030
Mode	Supervisor
States	339
Sec	0.00002825

**Disassembly**

```

16:                                BNE        LOOP
17:                                0x0000002C 1AFFFFFF9 BNE        0x00000018
18: STOP        B        STOP
0x00000030  EFFFFFFE B        0x00000030
0x00000034  00001010 ANDEQ        R1, R0, R0, LSL R0
0x00000038  00000101 ANDEQ        R0, R0, R1, LSL #2

```

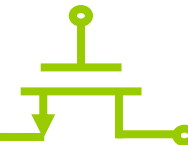
**TST2.s**

```

1  AREA    TST2, CODE, READONLY
2  ENTRY
3  LDR     r0, =0x1010
4  LDR     r1, =0x0101
5  LDR     r2, =0x1
6  LDR     r3, =0
7  LDR     r4, =32
8  EOR     r5, r0, r1
9
10 LOOP
11  TST     r5, r2
12  ADDNE   r3, r3, #1
13  LSL     r2, r2, #1
14  SUB     r4, #1
15  CMP     r4, #0
16  BNE     LOOP
17
18 STOP    B        STOP
19  END

```



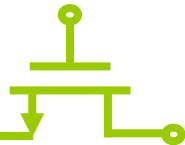


## 第一部分



- ▶ 將前面兩大題相關程式如上課時所示範的一樣，各打入一個program，並單步執行（F11），且截圖展示出題目所要求的結果，手算驗證部分用註解呈現在program中



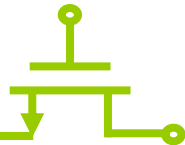


## 第二部分



- 如上課時所示範的一樣，將前一頁之宣稱寫入程式
- 在記憶體視窗中紅色標出每一個值儲存之位置並註明data1~data10每一變數的位址





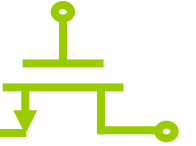
→ 第三部分1(1)、2.可以寫在同一個程式碼，每執行完一行程式碼截一張圖。

## 第三部分

- 1. (1) Assume  $r3 = 0x40000000$  and  $r4 = 0x60$ . What would  $r3$  contain after executing each of the following instructions?
- (a) `STR r6, [r3, #8]`
- (b) `STRB r7, [r3], #12`
- (c) `LDRH r5, [r3], #12`
- (d) `LDR r12, [r3, #4]!`
- (e) `LDR r6, [r3, r4, ROR #28]!`
- (f) `LDR r0, [r3, r4, LSL #2]`
- (2) What would register  $r4$  contain after executing the following instructions? Register  $r6$  holds the value `0xDEADBEEF` and register  $r3$  holds `0x40000000`.
- `STR r6, [r3]`
- `LDRB r4, [r3]`



## 作業2 注意事項(4/4)



→ 第三部分3.的每一小題獨立寫，避免因為前幾題結果錯，而導致後面也全錯。

### 第三部分



- ➔ 3. Assume  $r6 = 0xABCD8765$ . Write a sequence of instructions to
- ➔ (1) calculate the 2's complement of  $r6$  and put the result in  $r7$ .
- ➔ (2) set bits 1, 5, and 13 in register  $r6$  and leave the remaining bits unchanged.
- ➔ (3) clear bits 0, 4, and 12 in register  $r6$  and leave the remaining bits unchanged.
- ➔ (4) change bits 4, 8, and 11 of  $r6$ .
- ➔ (5) insert the value  $0x5555$  into the lower half of register  $r0$  so that the final value is  $0xBEEF5555$ , assuming register  $r0$  contains the value  $0xBEEFABCD$ .

# *Q&A*

***Thanks for your attention !!***