第08次實習課

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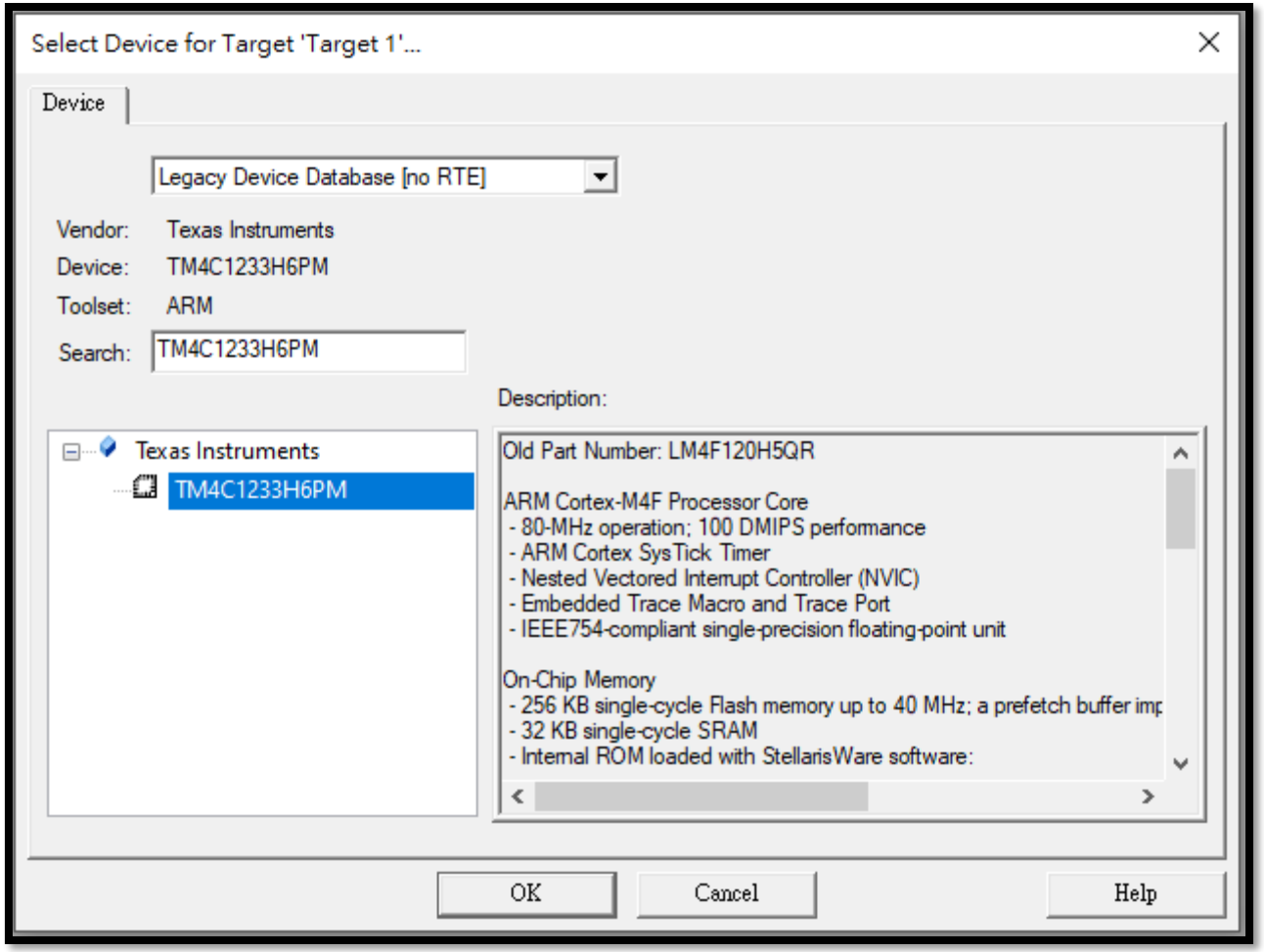
EXAMPLE 15.1


Select Device for Target 'Target 1'...
Device
Legacy Device Database [no RTE]
Vendor: Texas Instruments
Device: TM4C1233H6PM
Toolset: ARM
Search: TM4C1233H6PM
Description:
Texas Instruments
TM4C1233H6PM
Old Part Number: LM4F120H5QR
ARM Cortex-M4F Processor Core
- 80-MHz operation; 100 DMIPS performance
- ARM Cortex SysTick Timer
- Nested Vectored Interrupt Controller (NVIC)
- Embedded Trace Macro and Trace Port
- IEEE754-compliant single-precision floating-point unit
On-Chip Memory
- 256 KB single-cycle Flash memory up to 40 MHz; a prefetch buffer imp
- 32 KB single-cycle SRAM
- Internal ROM loaded with StellarisWare software:
OK
Cancel
Help

初始化NVIC

```
; enable the divide-by-zero trap
; located in the NVIC
; base: 0xE000E000
; offset: 0xD14
; bit: 4
LDR     r6, =NVICBase
LDR     r7, =DivbyZ
LDR     r1, [r6, r7]
ORR     r1, #0x10                   ; enable bit 4
STR     r1, [r6, r7]
; now turn on the usage fault exception
LDR     r7, =SYSHNDCTRL             ; p. 163
LDR     r1, [r6, r7]
ORR     r1, #0x40000
STR     r1, [r6, r7]
```

```
Reset_Handler
            ; 啟用除零陷阱
            ; 在 NVIC 中設置
            ; 基址: 0xE000E000
            ; 偏移: 0xD14
            ; 位: 4
            LDR     r6, =NVICBase           ; 將 NVIC 的基址載入 r6 中
            LDR     r7, =DivbyZ             ; 將 DivbyZ 的地址載入 r7 中
            LDR     r1, [r6, r7]            ; 將 NVICBase + DivbyZ 地址處的值讀入 r1 中
            ORR     r1, #0x10               ; 啟用第 4 位
            STR     r1, [r6, r7]            ; 將修改後的值寫入 NVICBase + DivbyZ 的地址處
            ; 現在啟用使用異常處理器
            LDR     r7, =SYSHNDCTRL         ; 參見第 163 頁
            LDR     r1, [r6, r7]            ; 將 SYSHNDCTRL 的地址載入 r7 中
            ORR     r1, #0x40000            ; 設置第 18 位以啟用使用異常處理器
            STR     r1, [r6, r7]            ; 將修改後的值寫入 SYSHNDCTRL 的地址處
```

參考NVIC技術手冊(0xE000ED14)

Configuration Control Register	Read/write	0xE000ED14	0x00000000	*Configuration Control Register*

Configuration Control Register

Use the Configuration Control Register to:

- enable NMI, Hard Fault and FAULTMASK to ignore bus fault
- trap divide by zero, and unaligned accesses
- enable user access to the Software Trigger Exception Register
- control entry to Thread Mode.

The register address, access type, and Reset state are:

Address

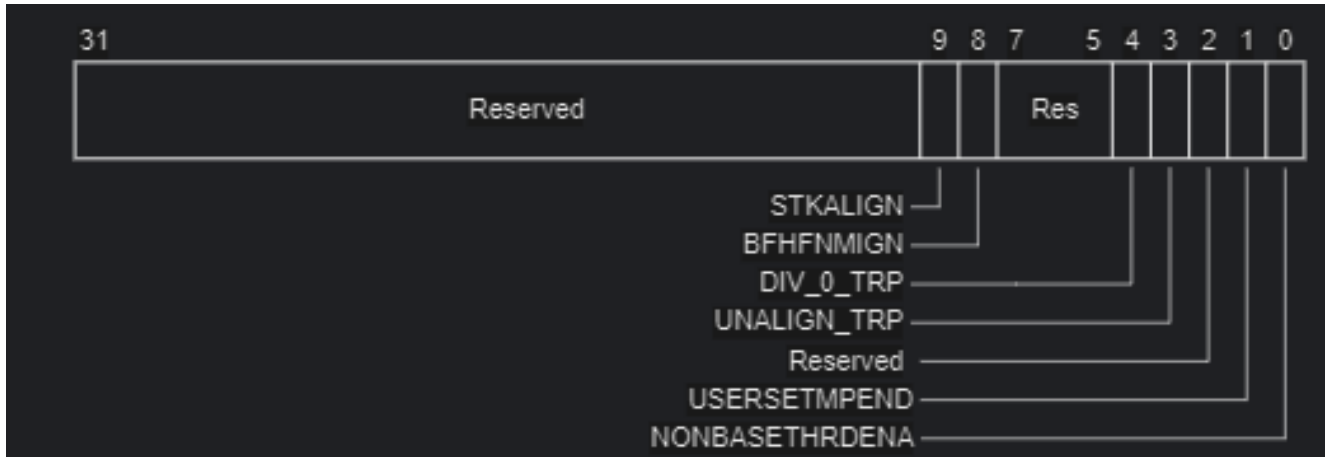
0xE000ED14

Access

Read/write

Reset state

0x00000000



[4]	DIV_0_TRP	Trap on Divide by 0. This enables faulting/halting when an attempt is made to divide by 0. The relevant Usage Fault Status Register bit is DIVBYZERO, see *Usage Fault Status Register*.

TABLE 15.1 Usage fault

TABLE 15.1
Exception Types and Vector Table

Exception Type	Exception Number	Priority	Vector Address	Caused by…
—	—	—	0x00000000	Top of stack
Reset	1	– 3 (highest)	0x00000004	Reset
NMI	2	– 2	0x00000008	Non-maskable interrupt
Hard fault	3	– 1	0x0000000C	All fault conditions if the corresponding fault is not enabled
Mem mgmt fault	4	Programmable	0x00000010	MPU violation or attempted access to illegal locations
Bus fault	5	Programmable	0x00000014	Bus error, which occurs during AHB transactions when fetching instructions or data
Usage fault	6	Programmable	0x00000018	Undefined instructions, invalid state on instruction execution, and errors on exception return
—	7–10	—		Reserved
SVcall	11	Programmable	0x0000002C	Supervisor Call
Debug monitor	12	Programmable	0x00000030	Debug monitor requests such as watchpoints or breakpoints
—	13	—		Reserved
PendSV	14	Programmable	0x00000038	Pendable Service Call
SysTick	15	Programmable	0x0000003C	System Tick Timer
Interrupts	16 and above	Programmable	0x00000040 and above	Interrupts

指令執行時錯誤的情形

參考NVIC技術手冊(0xE000ED24)

System Handler Control and State Register	Read/write	0xE000ED24	0x00000000	*System Handler Control and State Register*

System Handler Control and State Register

Use the System Handler Control and State Register to:

- enable or disable the system handlers
- determine the pending status of bus fault, mem manage fault, and SVC
- determine the active status of the system handlers.

If a fault condition occurs while its fault handler is disabled, the fault escalates to a Hard Fault.

The register address, access type, and Reset state are:

Address

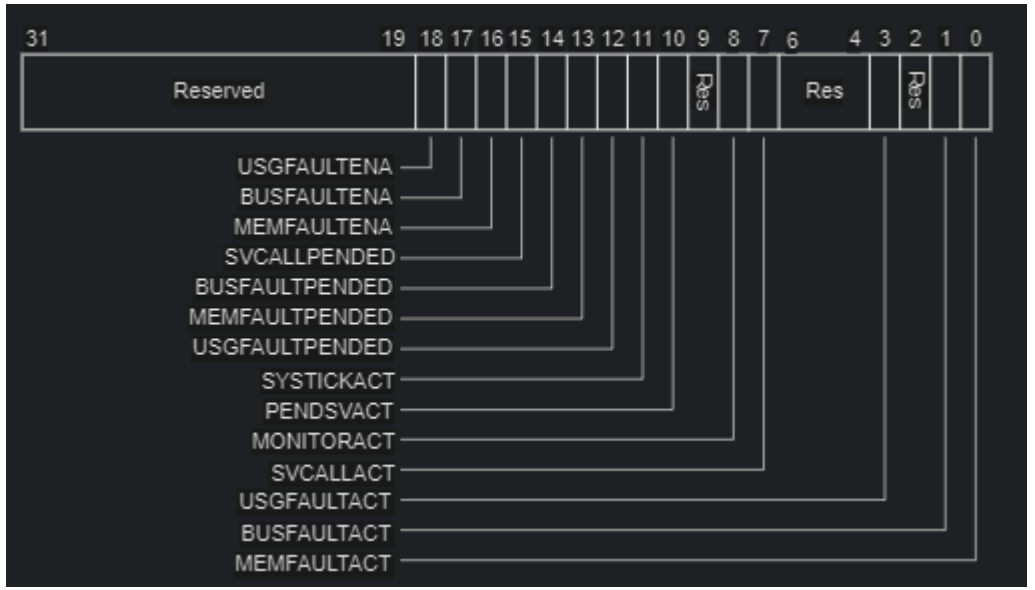
0xE000ED24

Access

Read/write

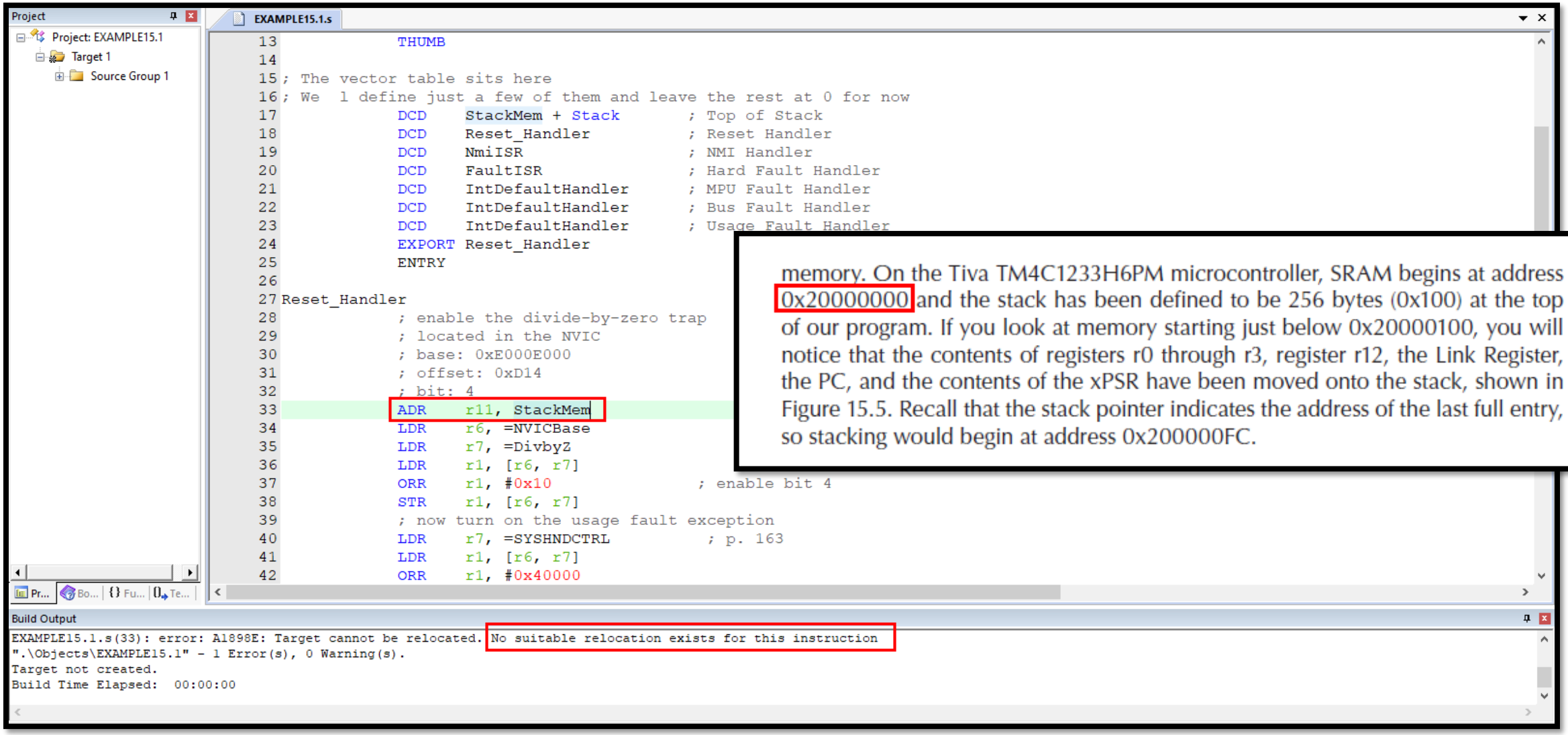
Reset state

0x00000000



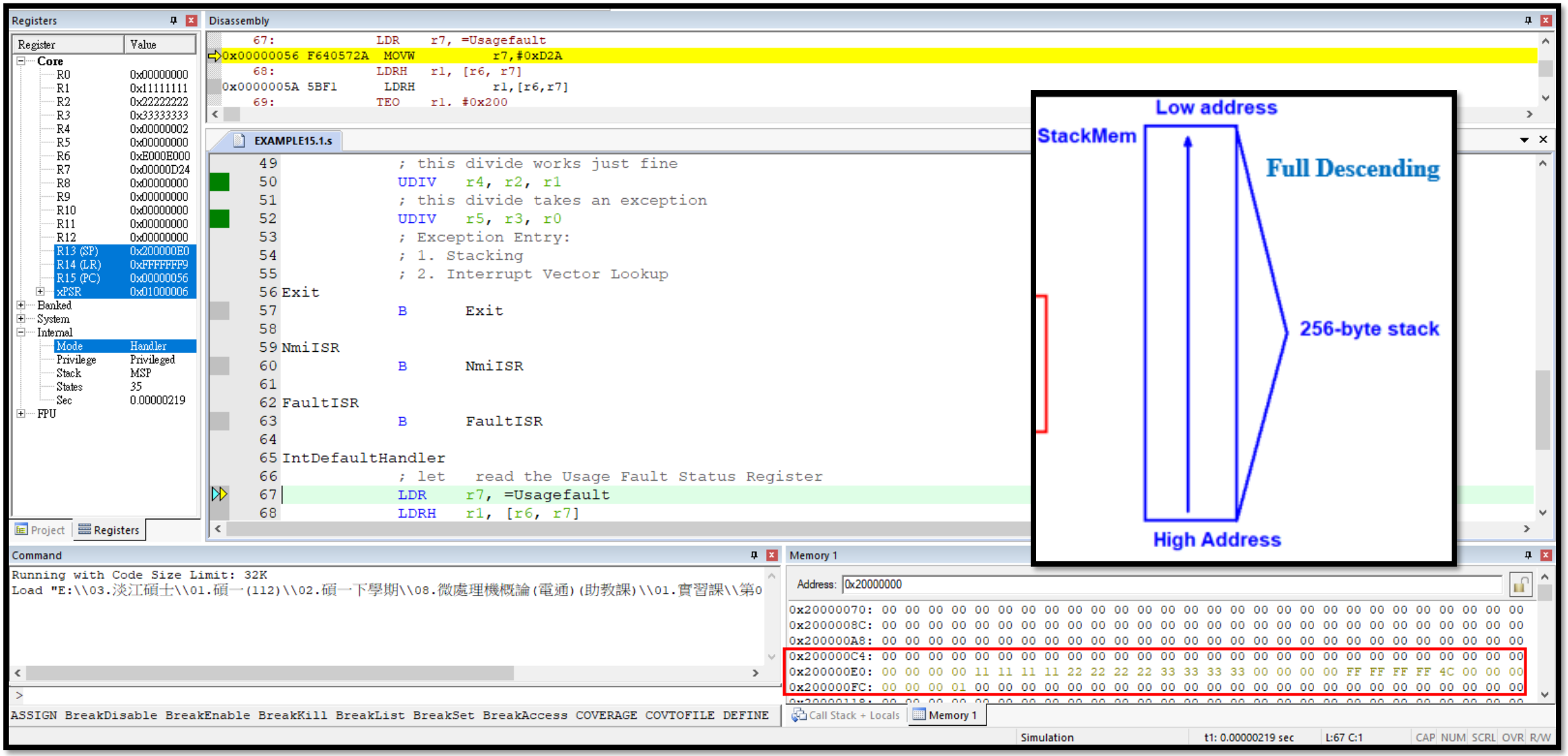
[18]	USGFAULTENA	Set to 0 to disable, else 1 for enabled.

P332 查找StackMem初始位置

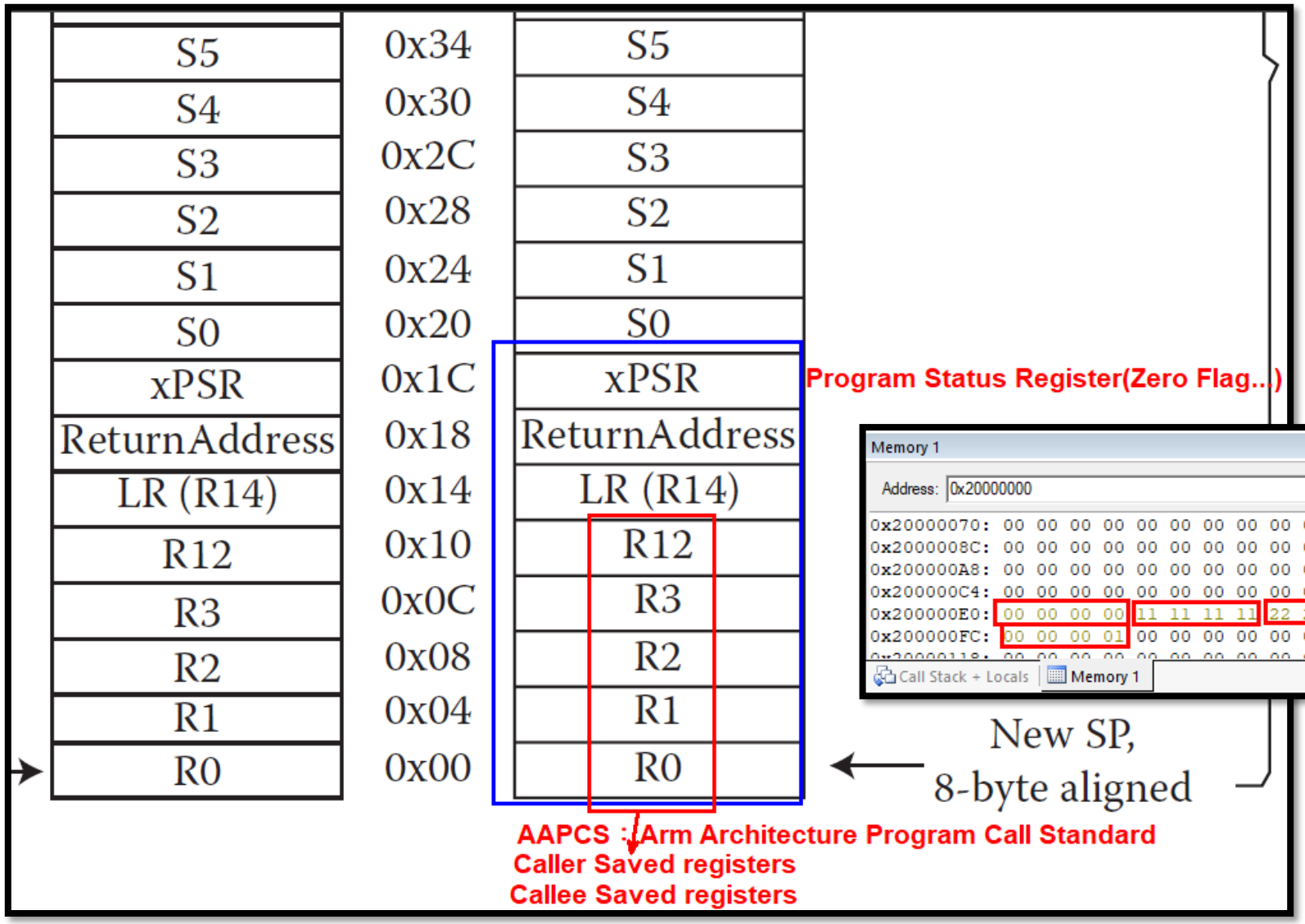


memory. On the Tiva TM4C1233H6PM microcontroller, SRAM begins at address 0x20000000 and the stack has been defined to be 256 bytes (0x100) at the top of our program. If you look at memory starting just below 0x20000100, you will notice that the contents of registers r0 through r3, register r12, the Link Register, the PC, and the contents of the xPSR have been moved onto the stack, shown in Figure 15.5. Recall that the stack pointer indicates the address of the last full entry, so stacking would begin at address 0x200000FC.

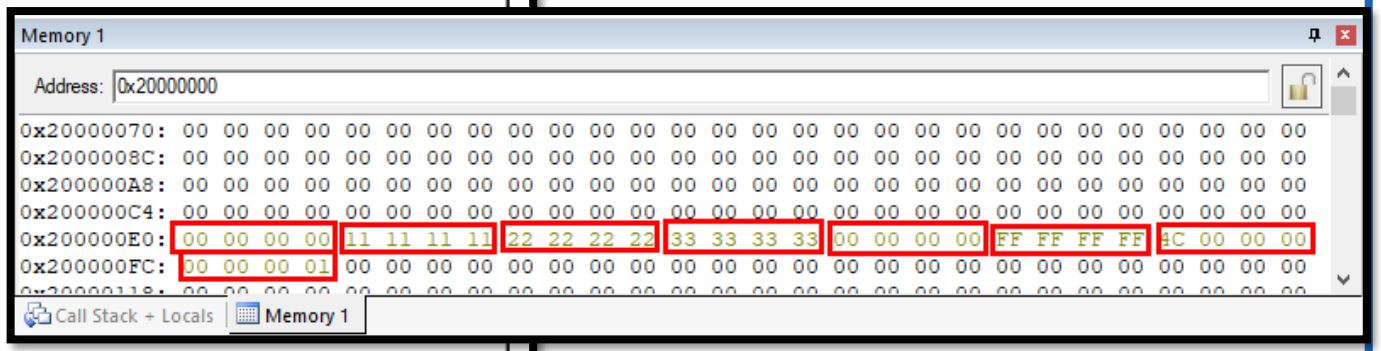
EXAMPLE15.1-Keil Tool-StackMem



P332 FIGURE 15.4對應到Keil Tool



R0	0x00000000
R1	0x11111111
R2	0x22222222
R3	0x33333333
R4	0x00000002
R5	0x00000000
R6	0xE000E000
R7	0x00000D24
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000



P336 TABLE15.4對照InDefaultHandler

TABLE 15.4
Usage Fault Status Register (Offset 0xD2A)

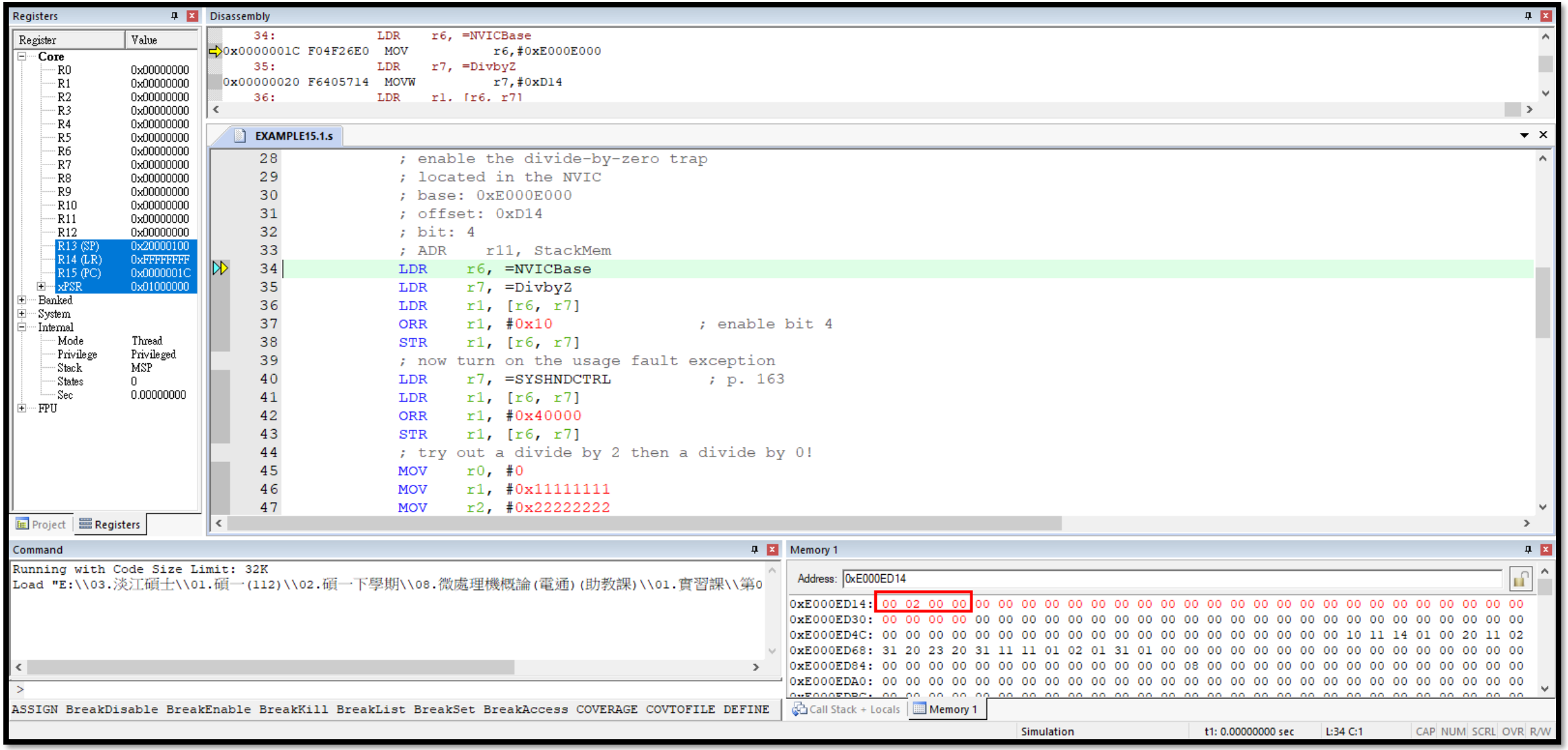
Bit	Name	Reset Value	Description
9	DIVBYZERO	0	Indicates a divide by zero has occurred (only if DIV_0_TRP is also set)
8	UNALIGNED	0	An unaligned access fault has occurred
7:4	—	—	—
3	NOCP	0	Indicates a coprocessor instruction was attempted
2	INVPC	0	An invalid EXC_RETURN value was used in an exception
1	INVSTATE	0	An attempt was made to switch to an invalid state
0	UNDEFINSTR	0	Processor tried to execute an undefined instruction

```
IntDefaultHandler
            ; let   read the Usage Fault Status Register
            LDR     r7, =Usagefault
            LDRH    r1, [r6, r7]
            TST     r1, #0x200
            IT      NE
            ; IT:If NE Then
            ; ITT
            ; ITTE
            ; ITTEE:If Then 2 Else 2
            LDRNE   r9, =0xDEADDEAD
            ; MOVNE r10, r9
            ; LDRNE r11, =FACEBEEF
            ; MOVEQ r12, r11
```

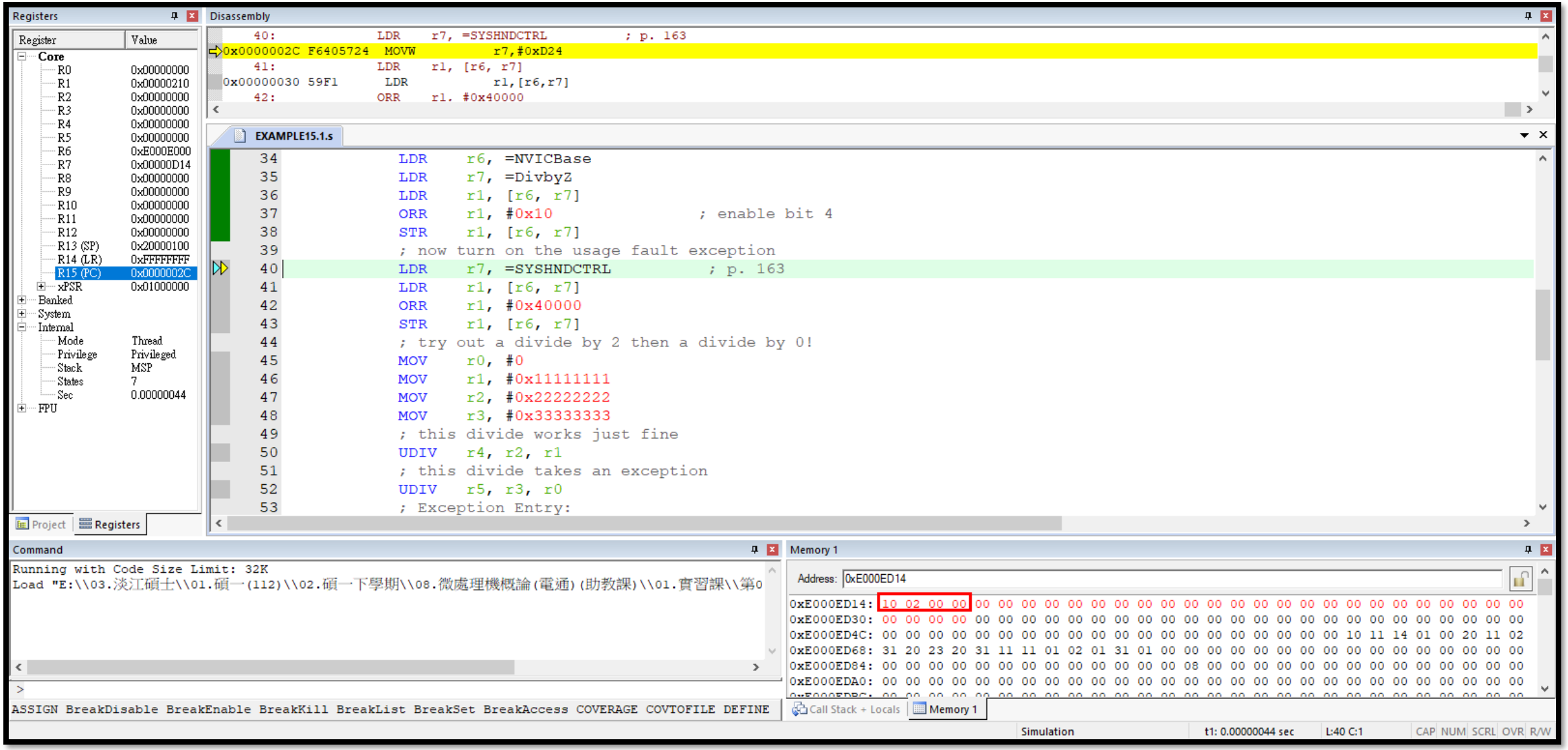
讓Assembler先知道後面的組織，
增加程式執行效率。(可有可無)

T：正面；E：負面
最多接4個

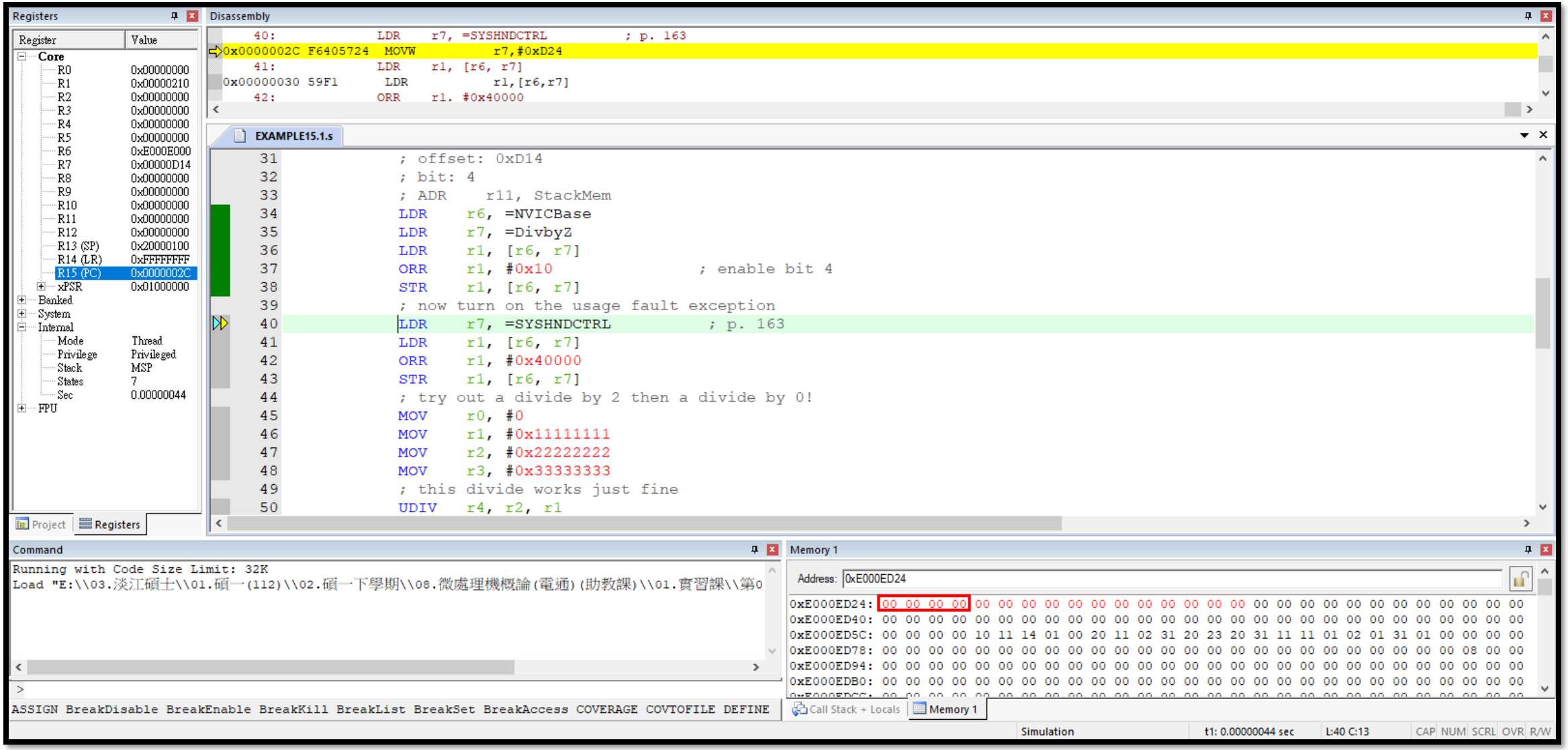
EXAMPLE 15.1-Enable the divide-by-zero trap



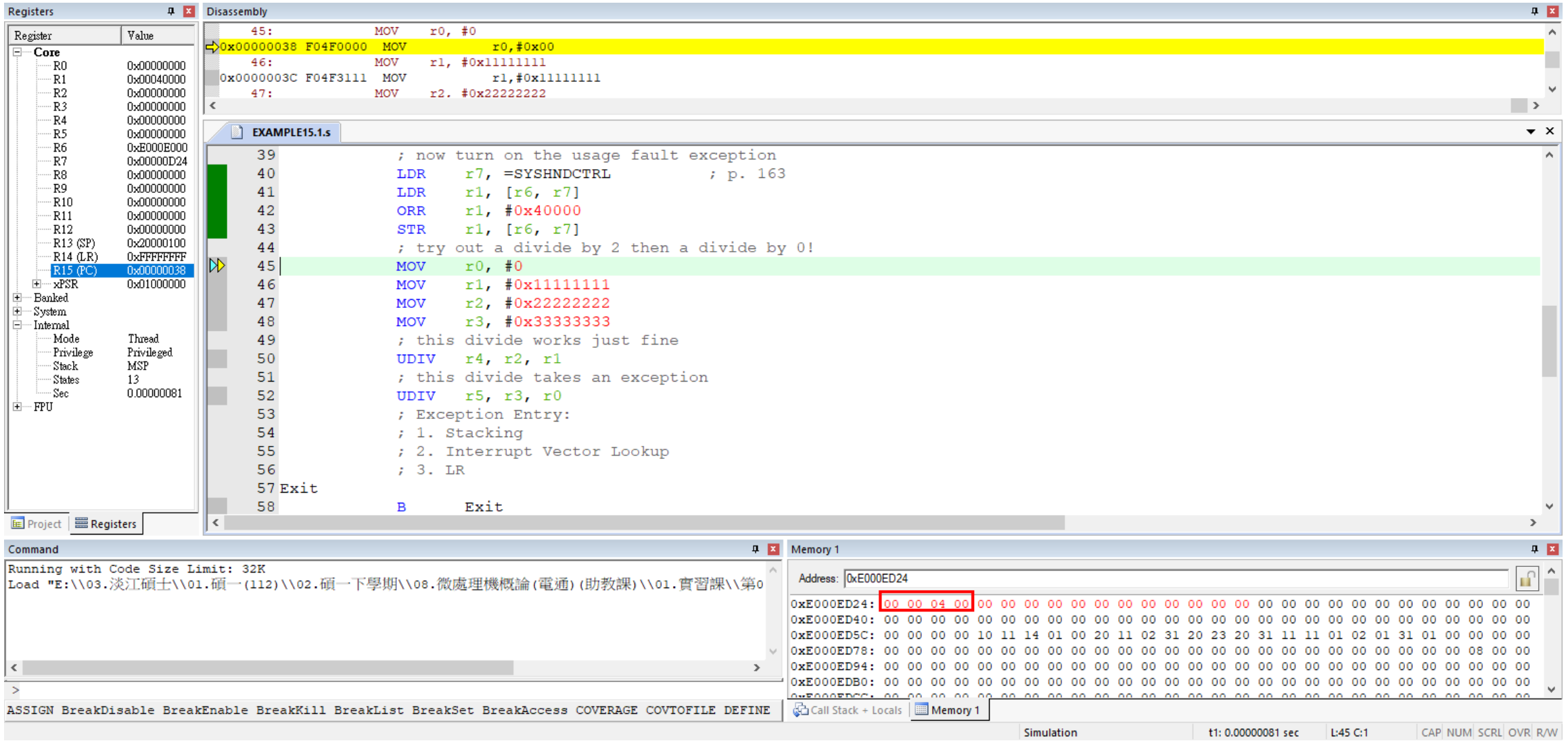
EXAMPLE 15.1-Enable the divide-by-zero trap



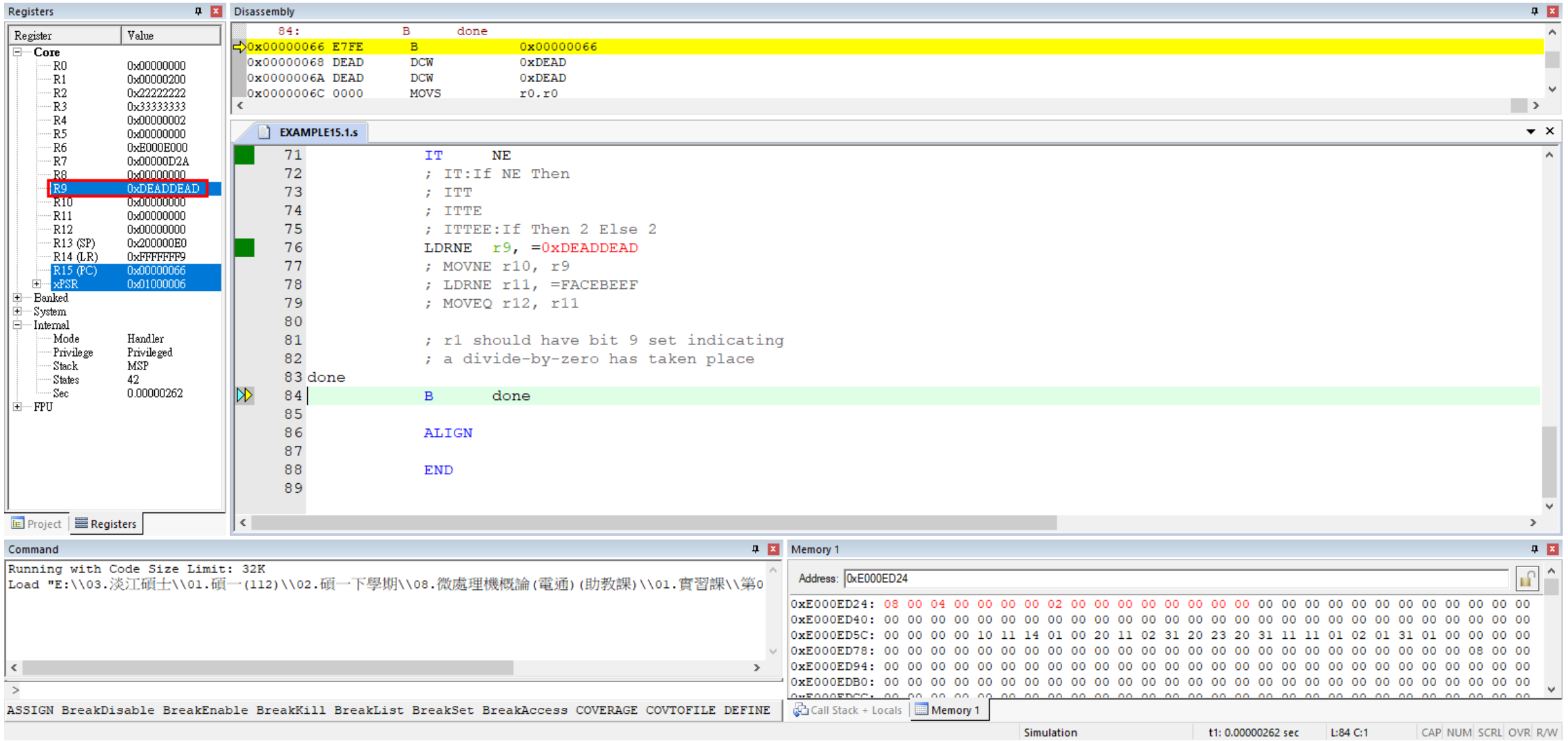
EXAMPLE 15.1-Turn on the usage fault exception



EXAMPLE 15.1-Turn on the usage fault exception



EXAMPLE 15.1-Final



EXAMPLE 15.3：Exception Entry→1. Stacking

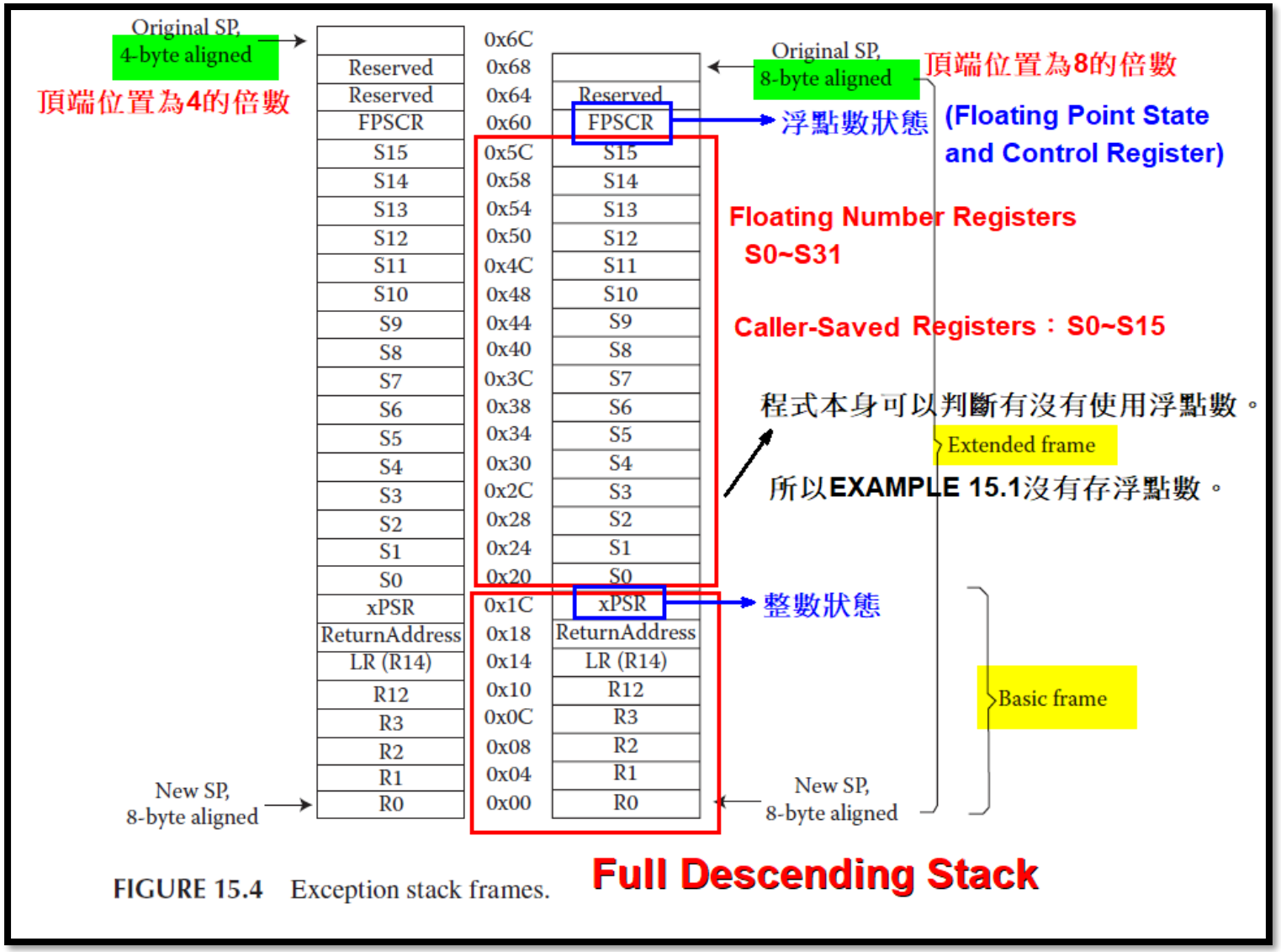


FIGURE 15.4 Exception stack frames.

EXAMPLE 15.2 Switch to user Thread mode

```
IntDefaultHandler

    ; let's read the Usage Fault Status Register

    LDR         r7, =Usagefault
    LDRH        r1, [r6, r7]
    TEQ         r1, #0x200
    IT          NE
    LDRNE       r9, =0xDEADDEAD
    ; r1 should have bit 9 set indicating
    ; a divide-by-zero has taken place

    ; switch to user Thread mode
    MRS (從S到R)    r8, CONTROL
    ORR         r8, r8, #1
    MSR (從R到S)    CONTROL, r8
    BX          LR

    ALIGN
```

原本使用MOV

因為有使用到系統暫存器，所以用MRS、MSR。

Register(一般暫存器)：r8...

Special register(系統暫存器)：CONTROL...

回到原來被中斷的地方
但意義與副函式不同。

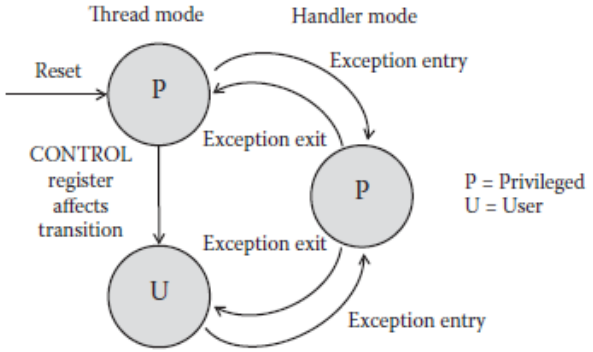
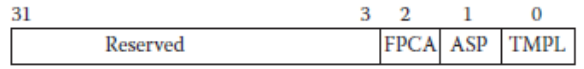


FIGURE 15.1 Cortex-M4 operation modes.



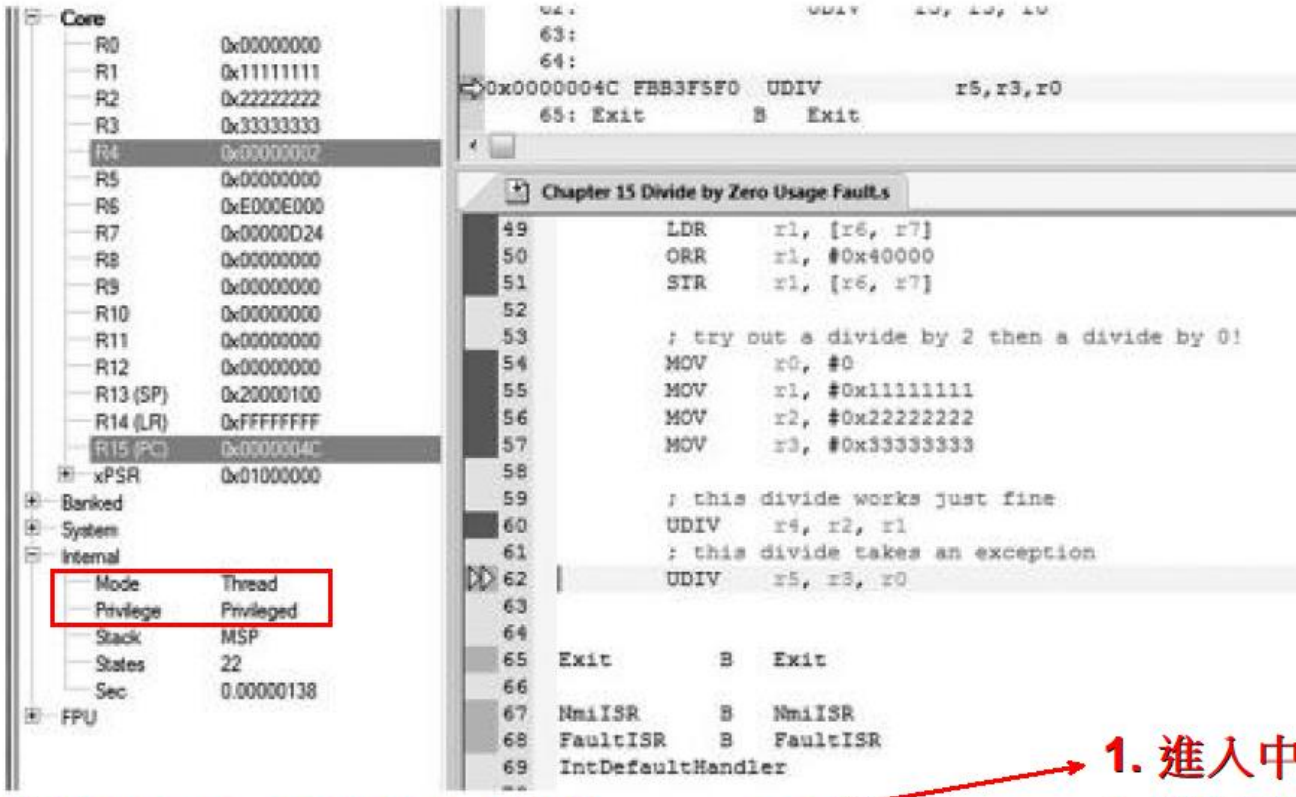
FPCA – Floating-point context active
- 1 – Preserve floating-point state when processing exception
- 0 – No floating-point context active

ASP - Active stack pointer
- 1 – PSP
- 0 – MSP

TMPL - Thread mode privilege level
- 1 – Unprivileged
- 0 – Privileged

FIGURE 15.2 CONTROL Register on the Cortex-M4.

觀察Keil Tool上Mode、Privilege變化



觀察Mode、Privileged變化。

1. 進入中斷程式後
2. 執行完EXAMPLE15.2回到主程式

(有可能會考)

FIGURE 15.3 Cortex-M4 operating in privileged Thread mode.

Q&A

Thanks for your attention !!