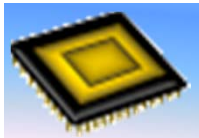
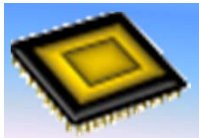


Chapter 4

Circuit Characterization and Performance Estimation



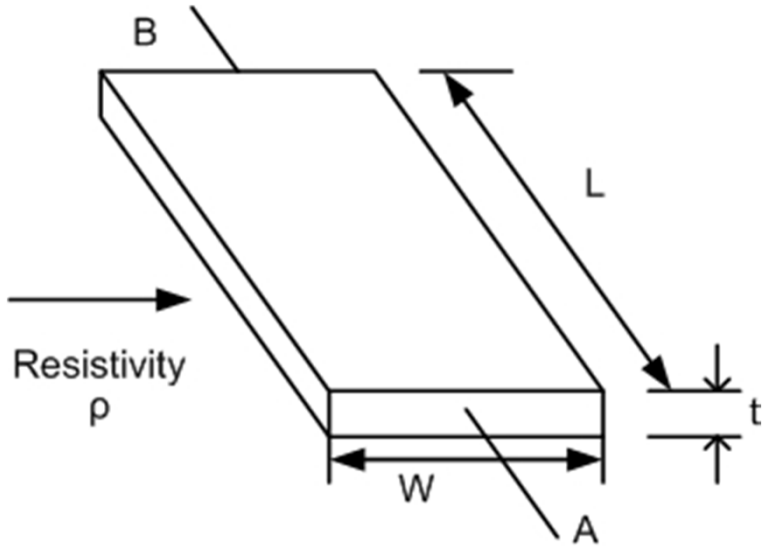
Chapter 4

Outline

- Resistance Estimation
- Electromigration
- Capacitance Estimation
- Switching Characteristics
- CMOS – Gate Transistor Sizing
- Power Dissipation

Resistance Estimation

- Rectangular shape Resistance (interconnection)



Wire Resistance

Material	ρ (Ω-m)
Silver (Ag)	1.6×10^{-8}
Copper (Cu)	1.7×10^{-8}
Gold (Au)	2.2×10^{-8}
Aluminum (Al)	2.7×10^{-8}
Tungsten (W)	5.5×10^{-8}

Resistance Estimation

- Typical sheet resistances for conductors

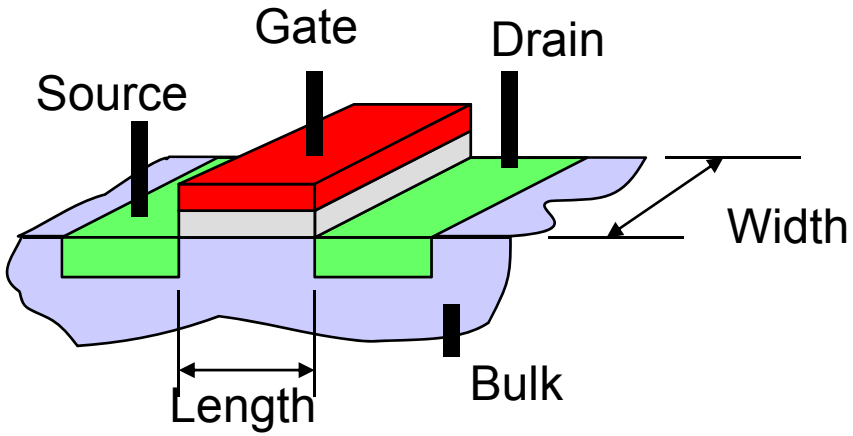
Material	Sheet Resistance OHM/SQ.		
	Min.	Typical	Max.
Metal(Al)	0.03	0.05	0.08
Silicides	2	3	6
Diffusion (n^+ and p^+)	10	25	50
Polysilicon	15	50	100

Resistance Estimation

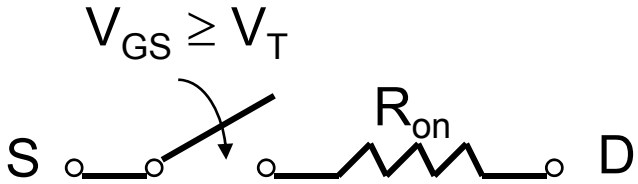
- MOS transistors:
  - Although the I-V characteristic of an MOS transistor is generally nonlinear, it is sometimes useful to approximate its behavior in term of a "channel resistance" to estimate performance.
  - Channel resistance in linear region

R_{on} of MOS Transistors

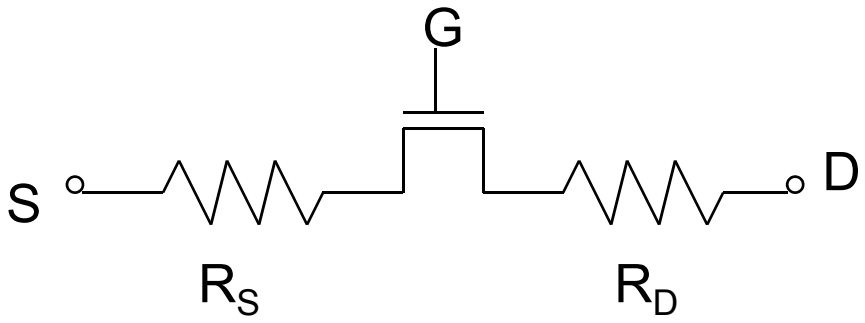
- MOS structure resistance - R_{on}
- Source and drain resistance
- Contact (via) resistance
- Wiring resistance



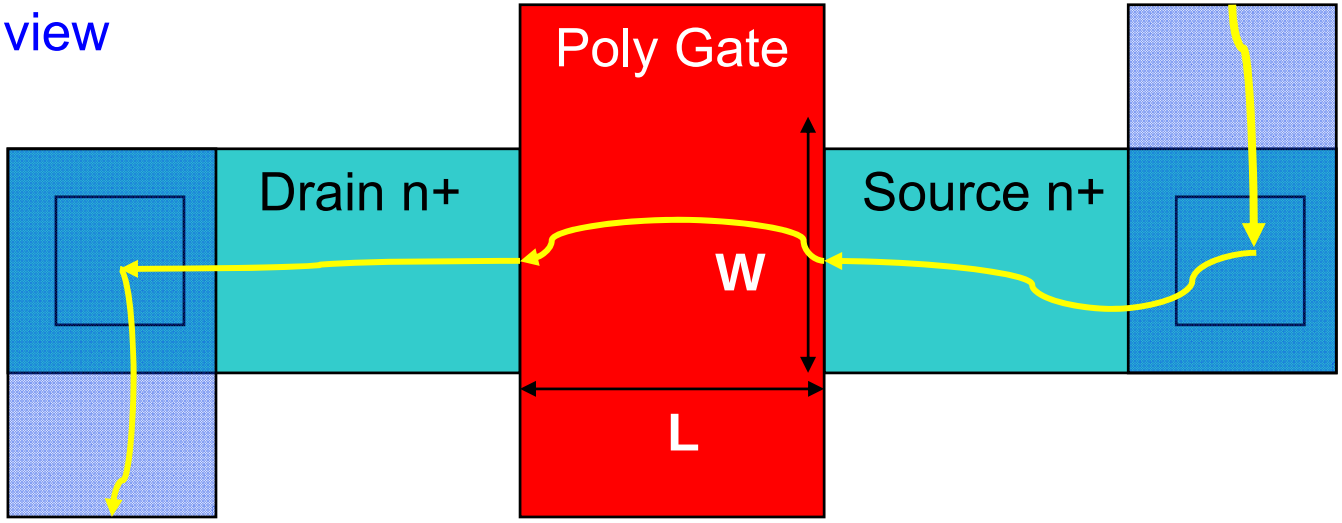
Cross-Section View



Source and Drain Resistance of MOS Transistors



Top view



Resistance Estimation

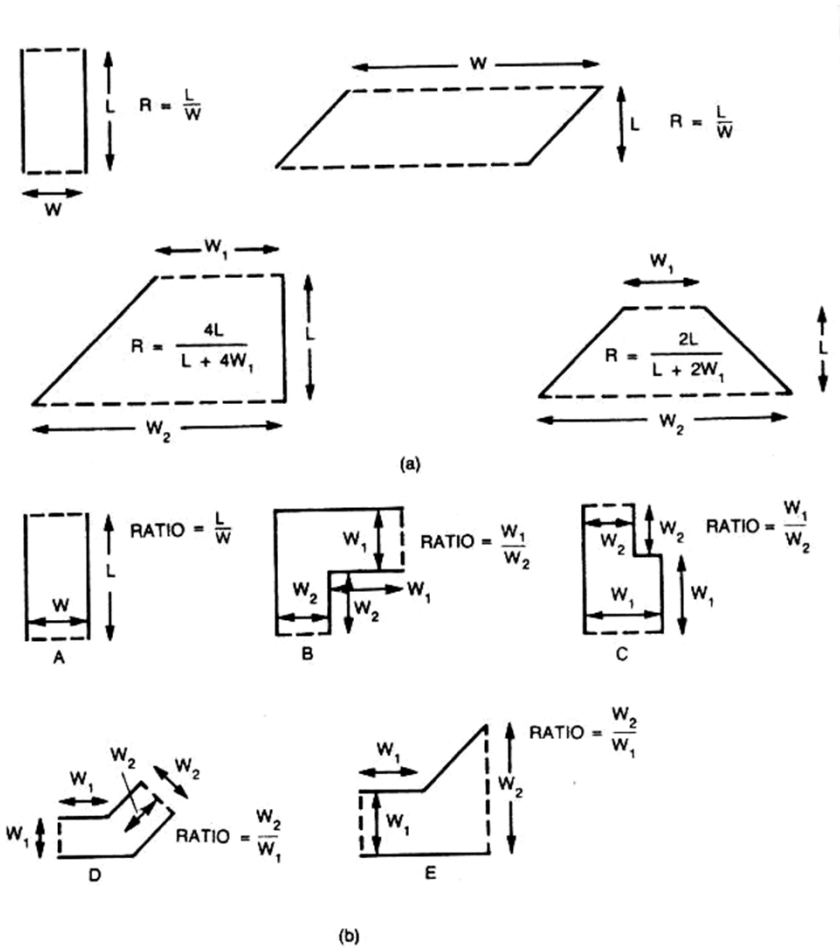
- Resistance of non-rectangular regions
  - One method of calculating the resistance of nonrectangular regions is to break the shape in question into simple regions.
- Ref:1. M Horowitz,R.W Dutton “Resistance Extraction from Mask Layout “IEEE Tran. CAD,Vol-CAD-2,No.3 P.P 145~150,1983.

  2. E.R.Girczyc,A.R.Boothroyd,”A 1-dimension DC model for nonrectangular IGFET “IEEE JSSC PP.778~784,DEC,1983.

Resistance Estimation

TABLE 4.2 Resistance of Non-Rectangular Shapes

SHAPE	RATIO	RESISTANCE
A	1	1
A	5	5
B	1	2.5
B	1.5	2.55
B	2	2.6
B	3	2.75
C	1.5	2.1
C	2	2.25
C	3	2.5
C	4	2.65
D	1	2.2
D	1.5	2.3
D	2	2.3
D	3	2.6
E	1.5	1.45
E	2	1.8
E	3	2.3
E	4	2.65



Resistance Estimation

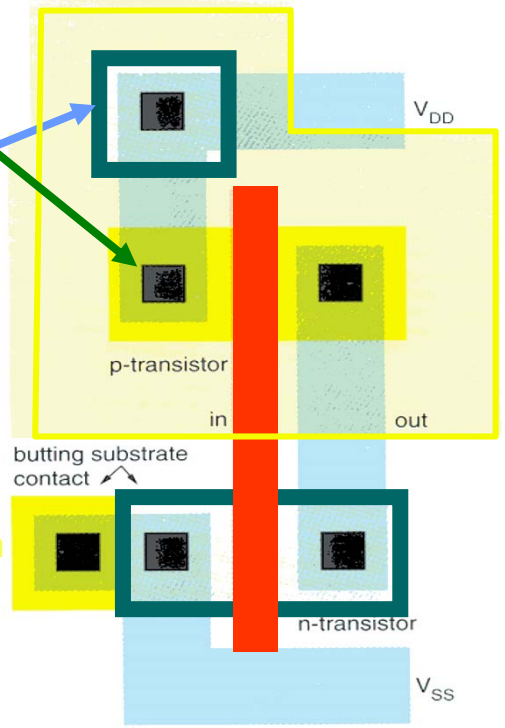
- Contact and Via resistance
  - Contact and via resistance associated with the contacted materials and the area of contact
  - Typical values are from .25Ω(Via) to a few tens of Ωs
  - For low resistance interlayer connections,multiple contacts are used.

Contact Resistance

Source & Drain Contacts:
- **surrounded by p+ region in the n-well**
- **surrounded by n+ region in the p-substrate**

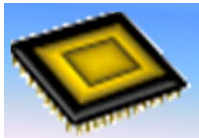
N-well Contacts:
- **surrounded by n+ region in the n-well**
- **connect n-well to VDD**

Substrate Contacts:
- **surrounded by p+ region in the p-substrate**
- **connect p-substrate to GND**



Many substrate & well contacts are needed to avoid latch-up problem, sometimes form a guard-ring

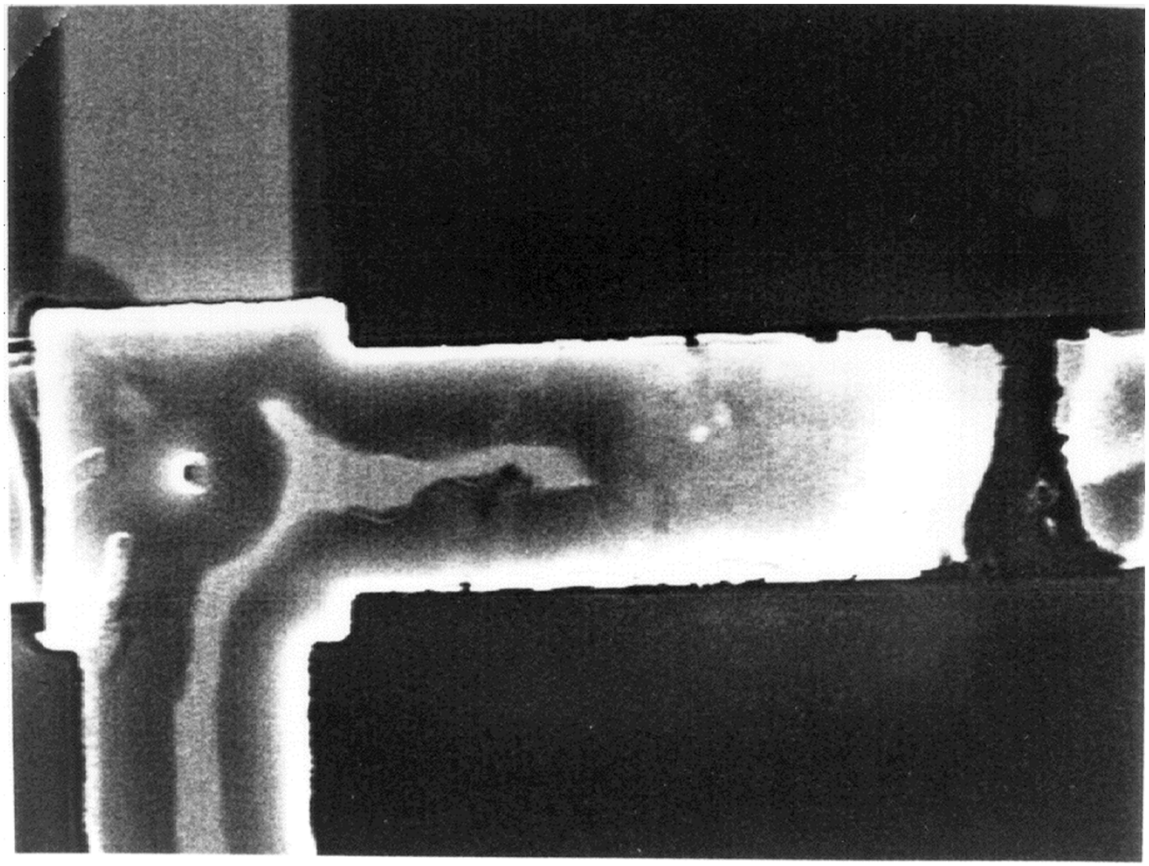
Source: Prof. syhuang's note



Electromigration

- Electromigration set limit in determining the conductor size.
- The term electronmigration refers to the transfer of mass in metals under the influence of current .It occurs by the transfer of momentum from the electrons to the positive mental ions.
- This can result in deformation of conductors.
  - a. cause wire to _____
  - b. cause wire _____

Wire Open–circuit



Electromigration

- The mean time to failure(MTF) of a conductor due to electromigration is

Electromigration

- For IC using Al as the connection, J must less than 1 mA/um^2
  - For Example:a 0.5um thick Al, J must be less than 0.5 mA/um^2 of metal width, for a Al connection line carriers width 10mA current, the metal width must be large than 20um.

Electromigration

- According to the scaling …

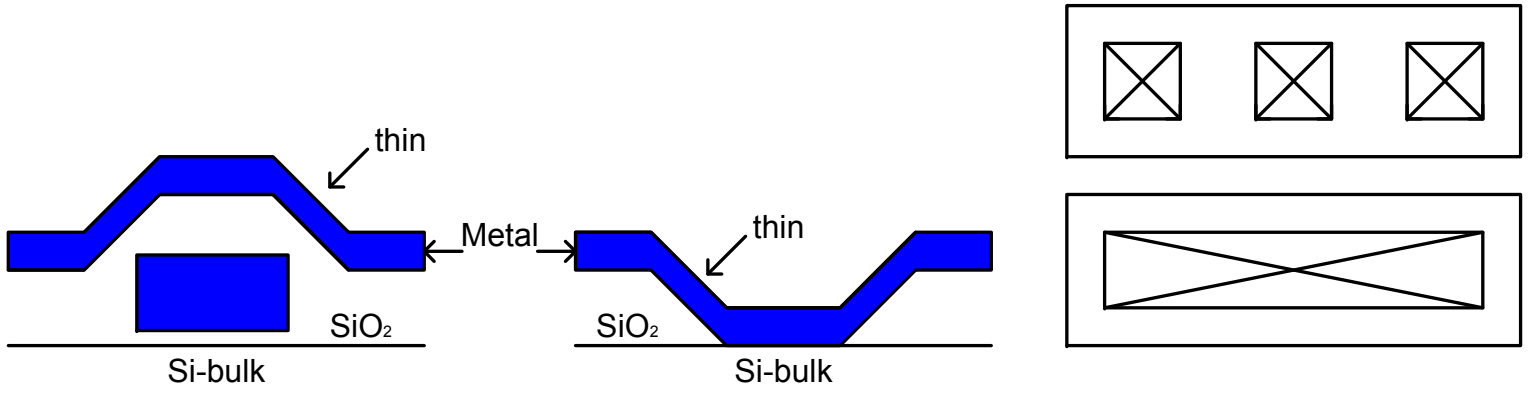
$$\mathrm{MTF} \propto \frac{\mathrm{WT}}{\mathrm{J}^2} \propto (\mathrm{WT})^3 \quad \left(\because \mathrm{J} \propto (\mathrm{WT})^{-1}\right)$$

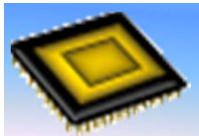
$$\therefore \quad \mathrm{WT} \downarrow \Rightarrow \mathrm{MTF} \downarrow$$

- Set a serious problem as device scaled down.

Electromigration

- Thin metal at the peripheral edge } open failure
  - A set of small contacts can provide much current than a single long narrow contact.



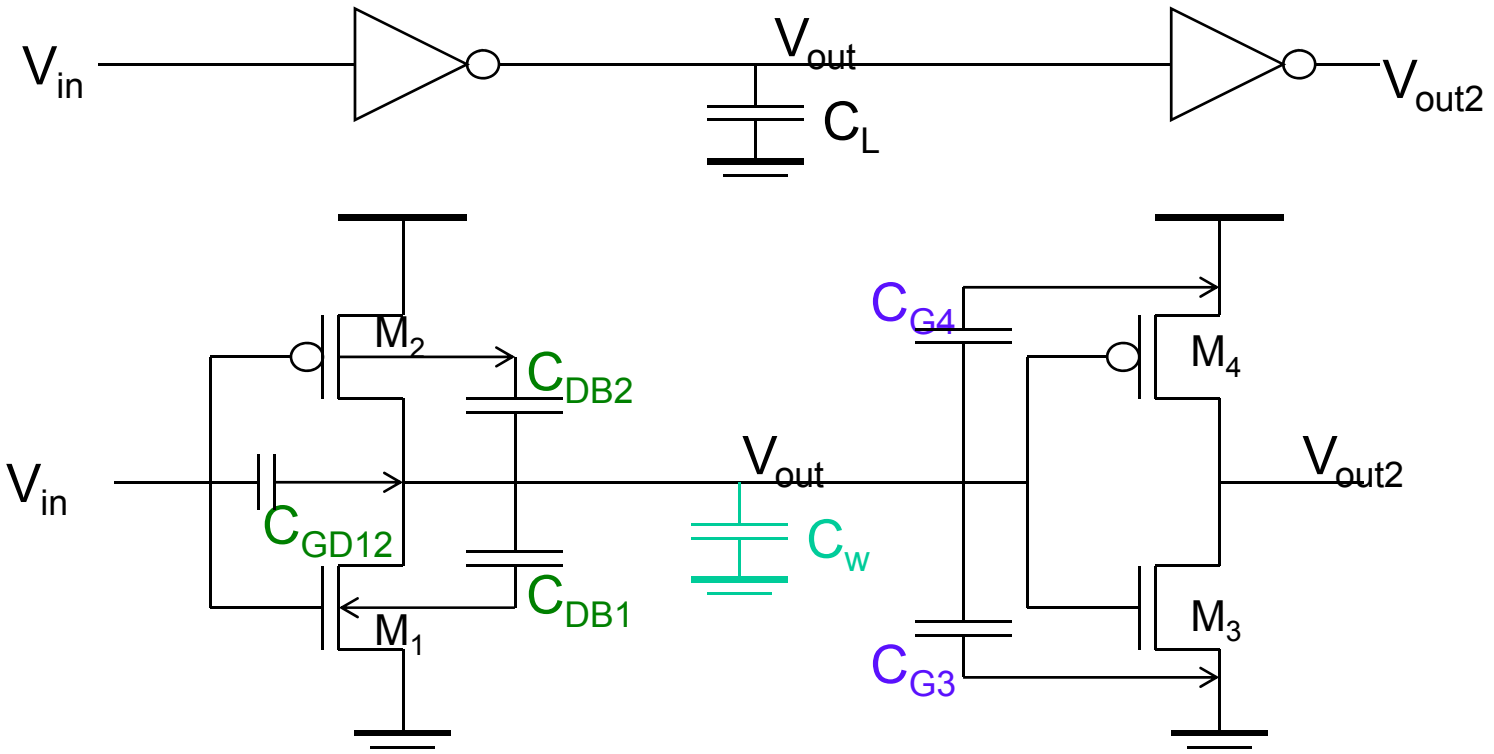


Capacitance Estimation

- Gate Capacitance
- (Source/Drain) Junction Capacitance
- Routing Capacitance (Interconnection)
- Distributed RC effects

Sources of Capacitance

- intrinsic MOS transistor capacitances
- extrinsic MOS transistor (fanout) capacitances
- wiring (interconnect) capacitance



Gate Capacitance

Gate to Bulk Capacitance

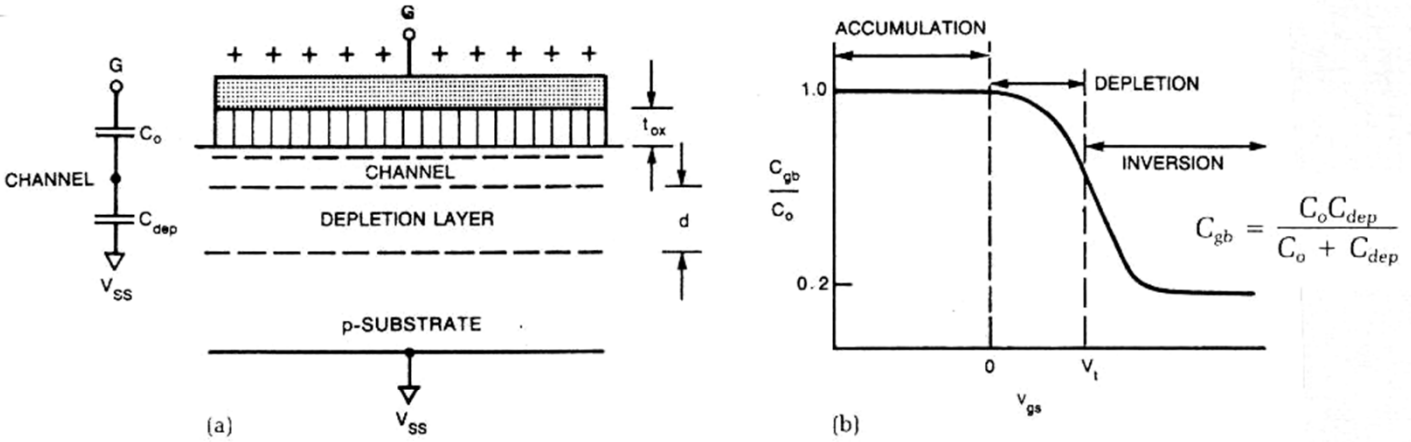


FIGURE 4.3. MOS capacitance (a) physical structure and (b) variation as a function of V_{gs}

$$C_o = \left(\frac{\varepsilon_{SiO_2}\varepsilon_o}{t_{ox}}\right) \cdot A, \qquad \textbf{(4.5)}$$

where

A = area of gate

ε_{SiO_2} = dielectric constant (or relative permittivity of SiO_2 taken as 3.9).

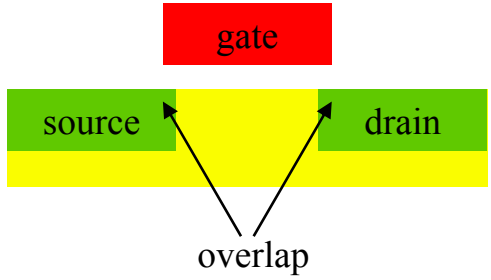
$$C_{dep} = \left(\frac{\varepsilon_o \varepsilon_{Si}}{d}\right) \cdot A,$$

where

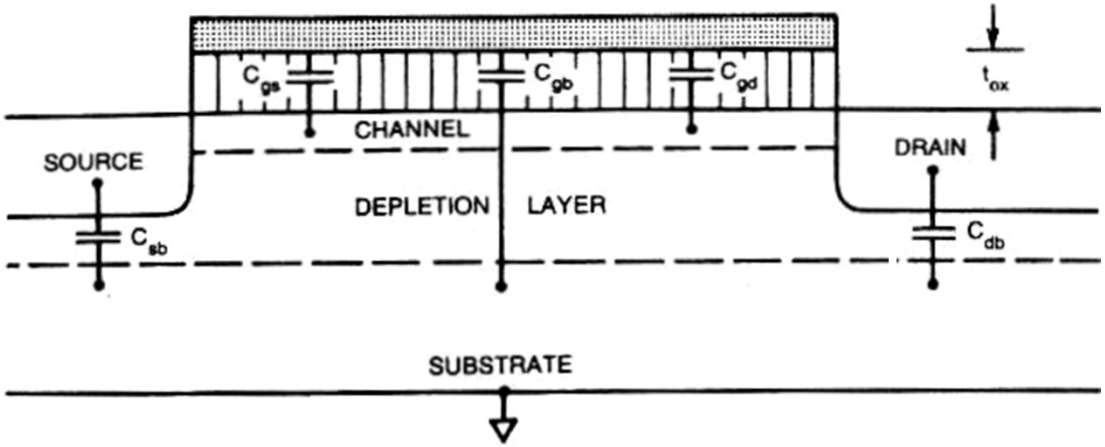
d = depletion layer depth

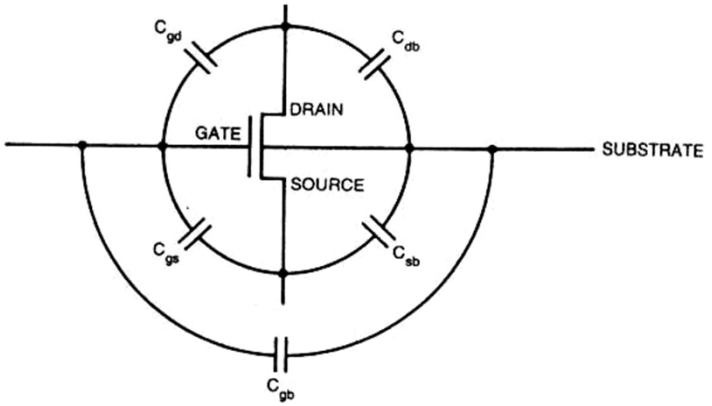
ε_{Si} = dielectric constant of silicon

Gate Capacitance



- Total Gate Capacitance C_g





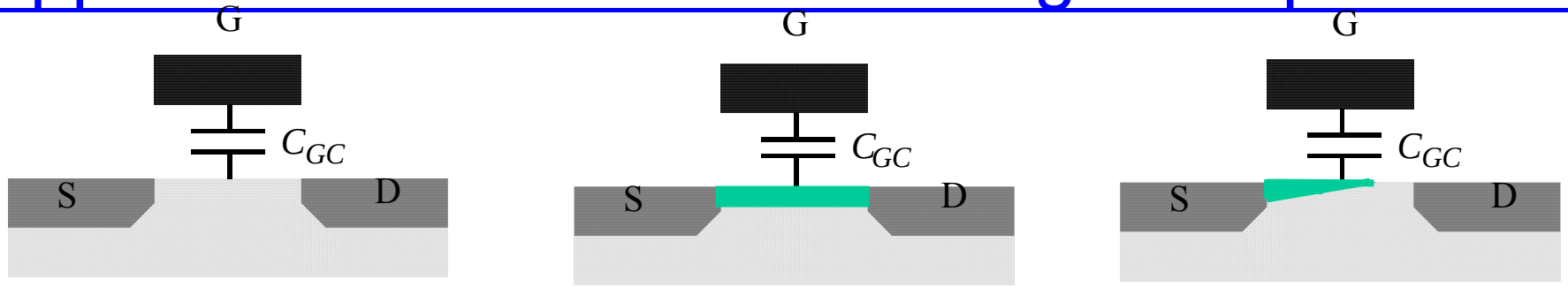
C_{gs},C_{gd} : gate to channel capacitance,which are lumped at source and drain regions of channel, respectively.

C_{sb},C_{db} : source and drain diffusion capacitance to bulk (or substrate).

C_{gb} : gate to bulk capacitance.

$$C_g = C_{gb} + C_{gs} + C_{gd}$$

Approximation of intrinsic MOS gate capacitance



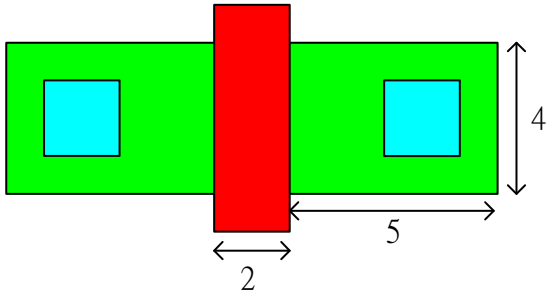
PARAMETER	CAPACITANCE		
	Off	Linear	Saturation
C_{gb}			
C_{gs}			
C_{gd}			
$C_g = C_{gb} + C_{gs} + C_{gd}$			

Note: $\varepsilon = \varepsilon_0 \cdot \varepsilon_{SiO_2}$ where $C_0 = \dfrac{\varepsilon A}{t_{OX}}$

- We can conservatively approximate $C_g = C_0$

Approximation of intrinsic MOS gate capacitance

Example



(a) $\lambda = 2\text{um}, t_{OX} = 1000\,\text{Å}$ find C_g

(b) $\lambda = 0.5\text{um}, t_{OX} = 150\,\text{Å}$ find C_g

$$\text{Sol}:(\text{a})\ C_{OX} = \frac{4\times 8.85\times 10^{-14}}{1000\times 10^{-8}} = 3.5\times 10^{-4}\ \text{pF}/\text{um}^2$$

$$C_g = 3.5\times 10^{-4}\times 8\lambda^2\text{pF} = 11.2\text{fF}$$

$$(\text{b})\ C_{OX} = \frac{4\times 8.85\times 10^{-14}}{150\times 10^{-8}} = 25.5\times 10^{-4}\ \text{pF}/\text{um}^2$$

$$C_g = 25.5\times 10^{-4}\times 8\lambda^2\text{pF} = 5.1\text{fF}$$

S/D Junction Capacitance

- The S/D junction capacitance C_d is proportional to the total diffusion-to-substrate junction area and the area of "sidewalk" peripheral.

Total C_d can be represented by

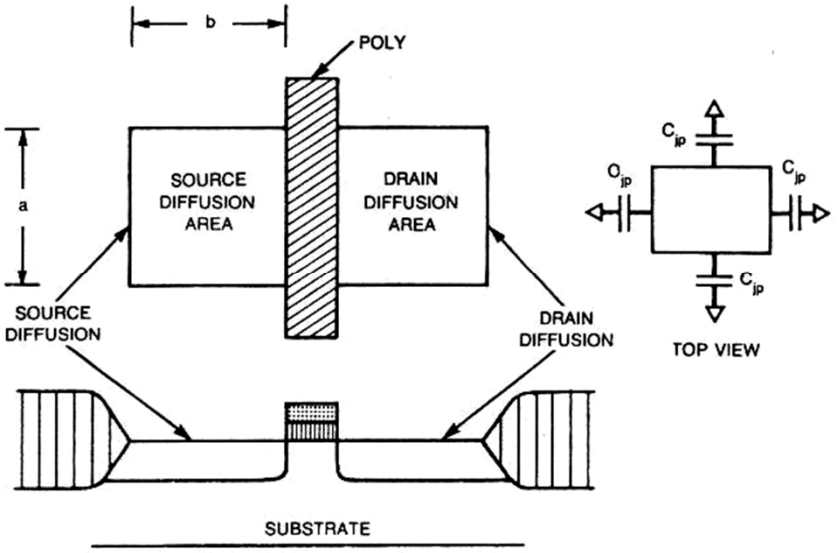
$$C_d = C_{ja} * (ab) + C_{jp} * (2a + 2b),$$

C_{ja} = junction capacitance per sq. μm

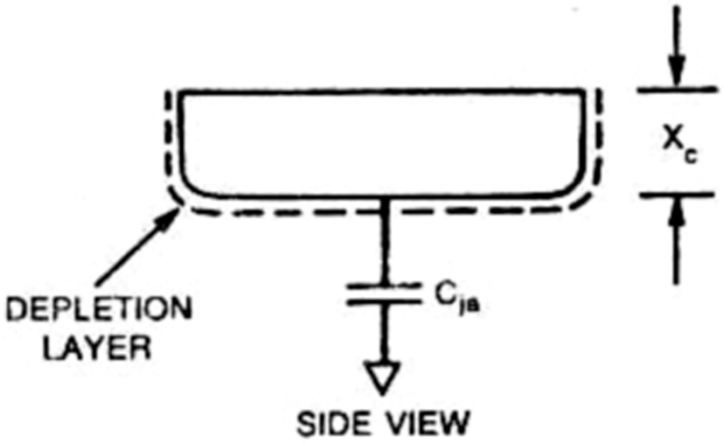
C_{jp} = periphery capacitance per μm

a = width of diffusion region

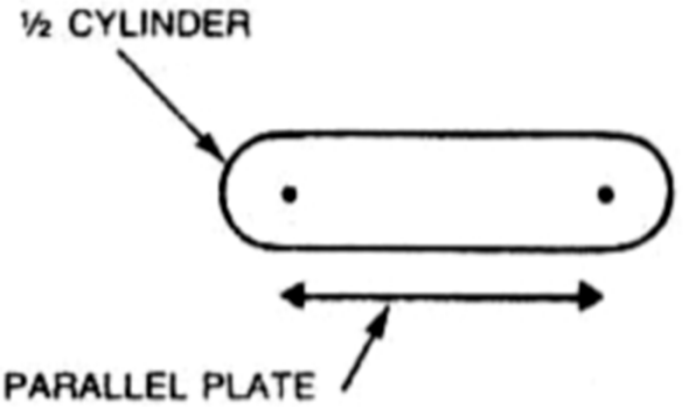
b = extent of diffusion region.



S/D Junction Capacitance



(b) CAPACITANCE REPRESENTATION

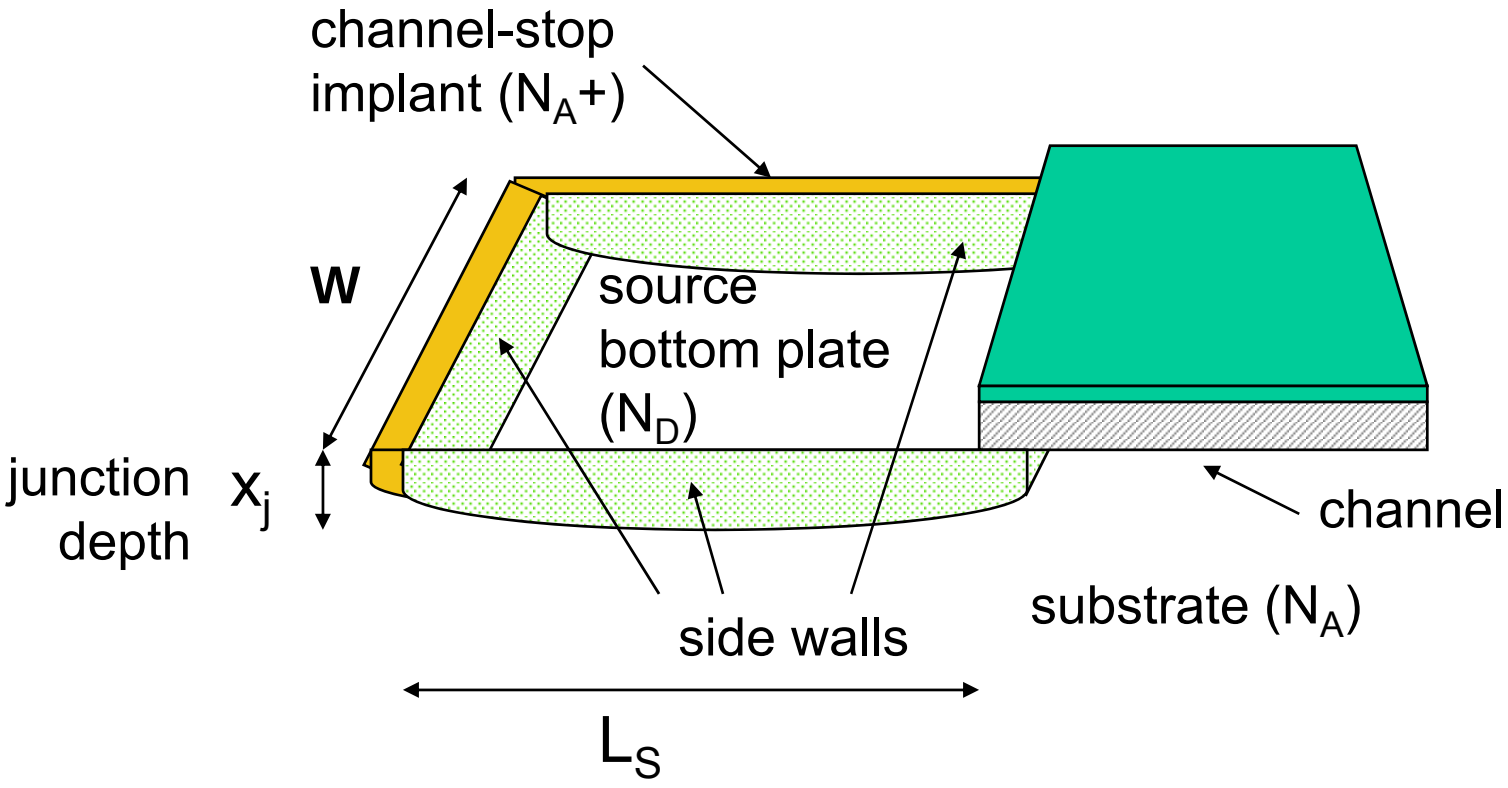


(c) CAPACITANCE MODEL

	n-DEVICE(OR WIRE)	p-DEVICE(OR WIRE)
C_{ja}	1×10^{-4}pF/um^2	1×10^{-4}pF/um^2
C_{jp}	9×10^{-4}pF/um	8×10^{-4}pF/um

Typical diffusion capacitance value

S/D Junction Capacitance



Example

- Find C_d for a n-device with a=10um, b=8um

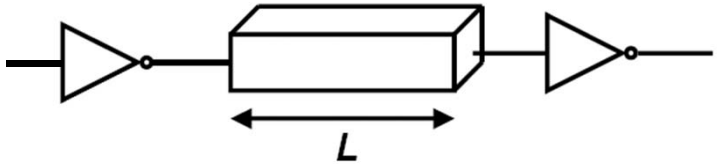
$C_d = 1\times10^{-4} \times (10\times8) + 9\times10^{-4} \times (20+16)$

$= 40\times10^{-3}pF$

$= 40\ fF$

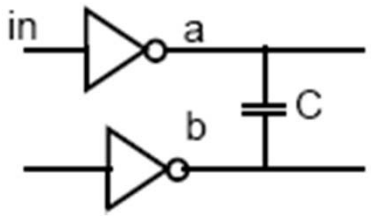
* C_d has the same as C_s value

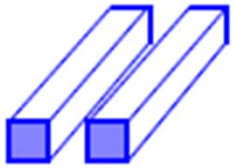
Interconnect



- Wires are not ideal interconnections
- They may have non-negligible capacitance, resistance, inductance
- Can dominate performance of chip
- Using approximate models
- Detailed post-layout verification also necessary

Coupling Capacitance

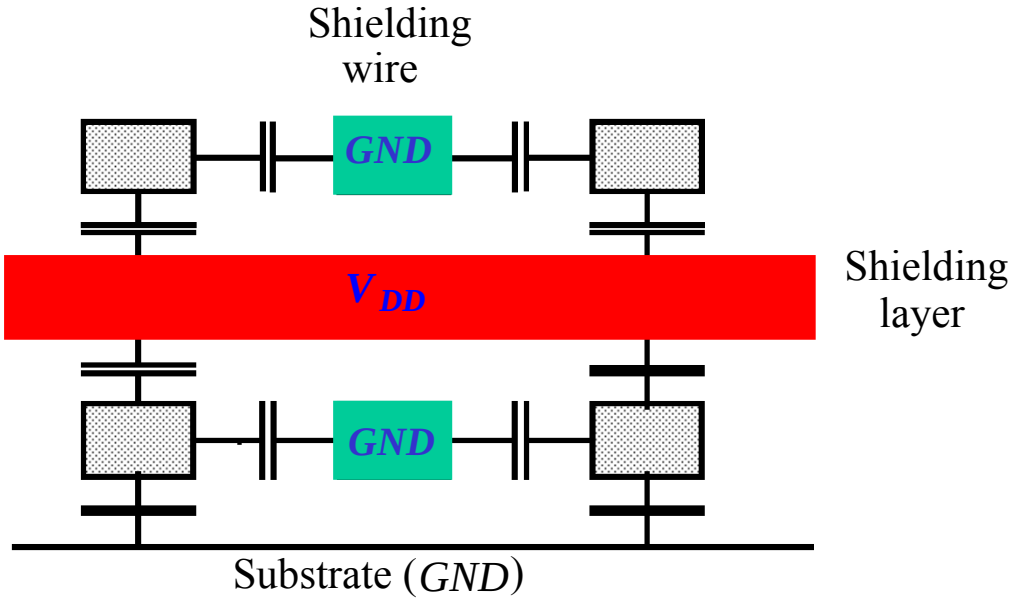




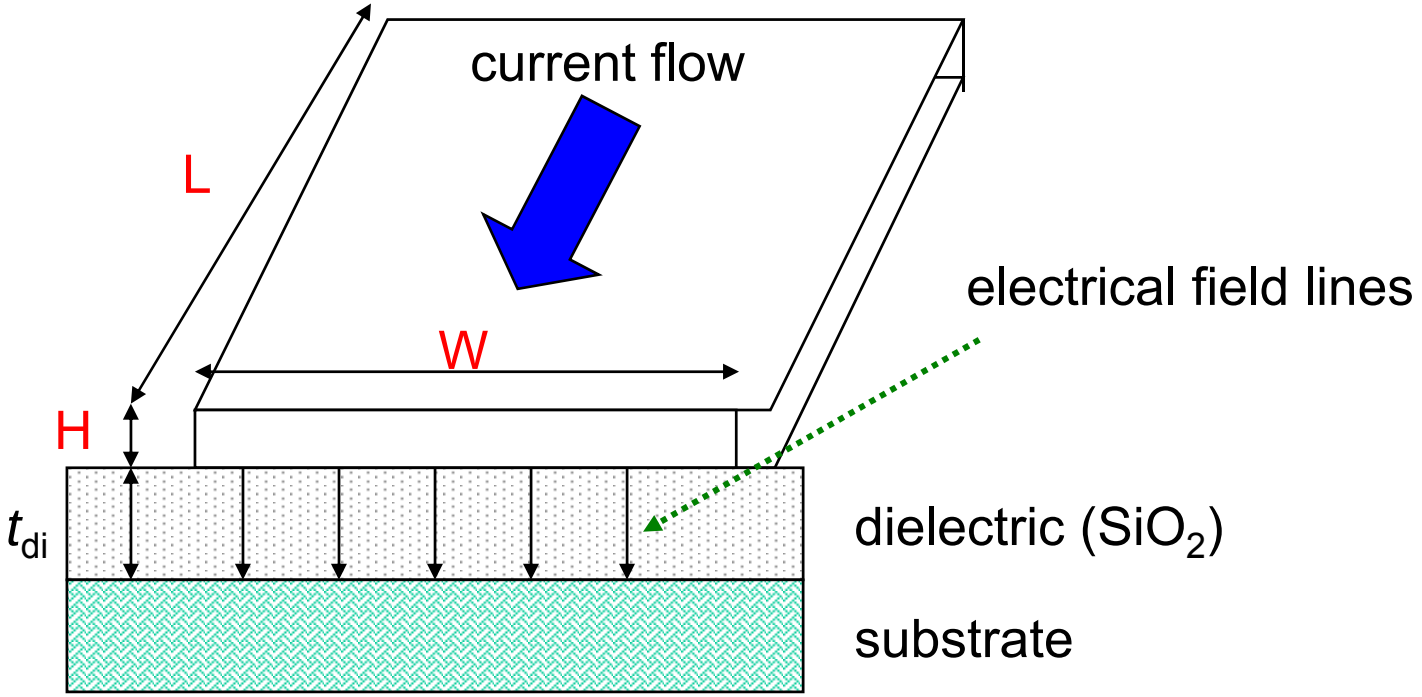
- It creates noise issues
  - a' changing will cause noise on 'b'
- If 'a' and 'b' transition at the same time in same direction
  - ΔV across the cap will be zero, and it won't affect the delay
- If 'a' and 'b' transition at the same time in opposite direction
  - ΔV across the cap will be ___, and it will look like a grounded cap of ___

Reduced Capacitive Crosstalk

- Avoid parallel wires
- Shielding



Parallel Plate Wiring Capacitance



permittivity constant (SiO_2= 3.9)

$$C_{pp} = (\varepsilon_{di}/t_{di})\ WL$$

Interconnect capacitances

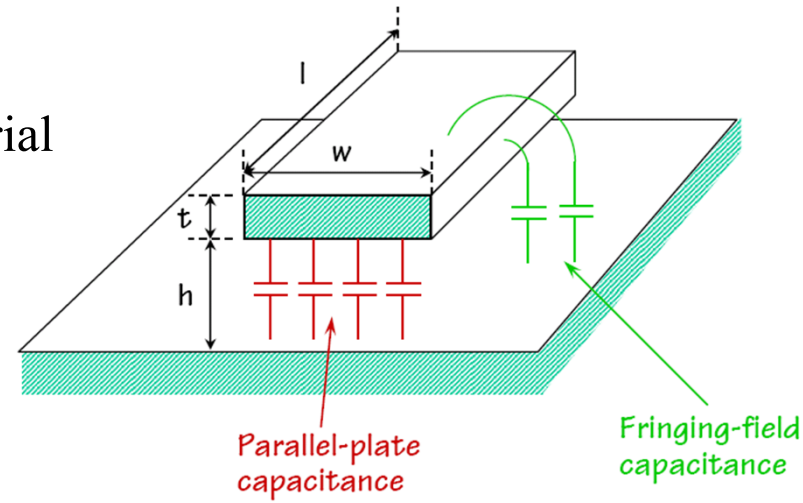
Parallel Plate Model

$C = (\varepsilon/h) \times A$

where A : area of the parallel plate

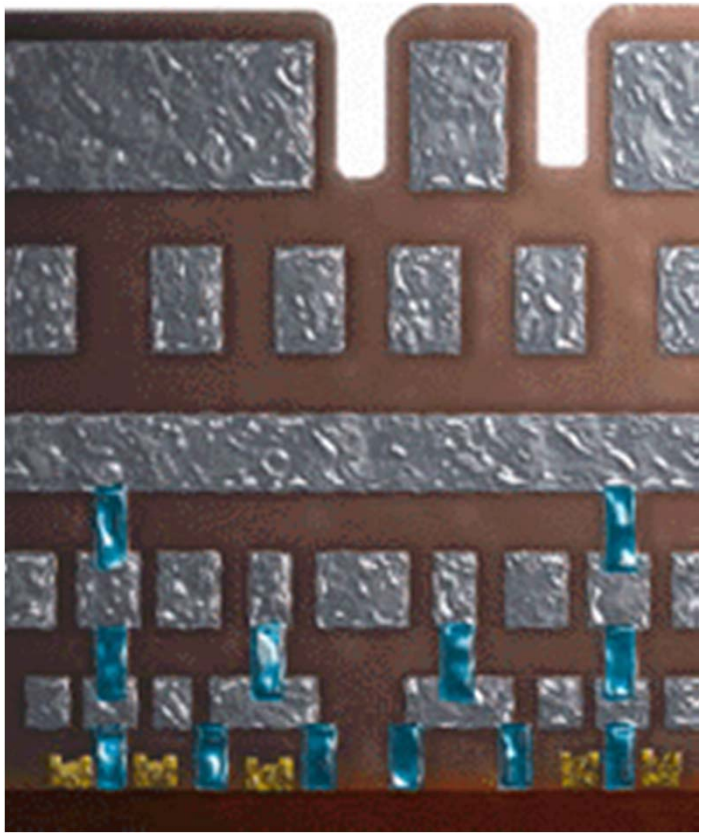
ε : dielectric constant of the insulator material

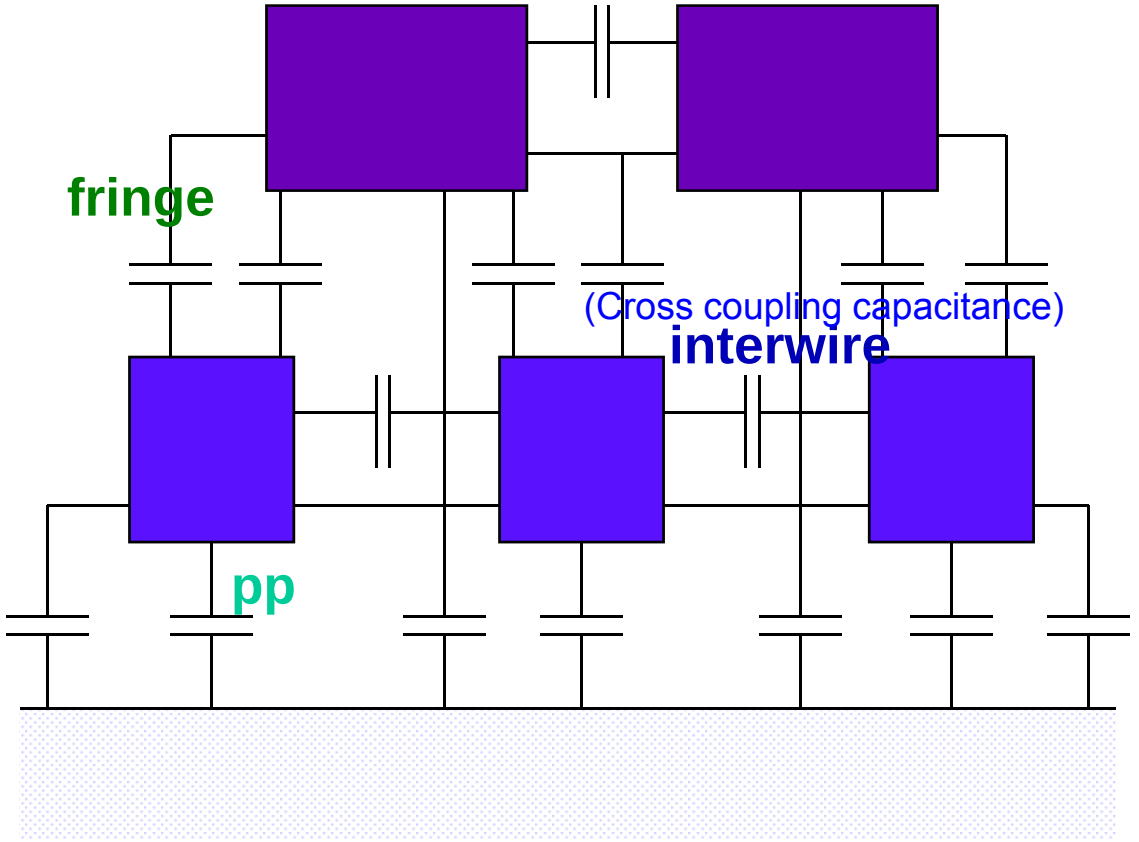
h : the insulator thickness.



- This approximation ignores fringing fields.
- The effect of fringing fields is to increase the effective area of the plate.
- Routing capacitances between metal and poly layers and the substrate can be approximated using the parallel plate model.

Interwire capacitances





Wiring Capacitances (0.25 μm CMOS)

	Field	Active	Poly	Al1	Al2	Al3	Al4
Poly	88						
	54						
Al1	30	41	57				
	40	47	54				
Al2	13	15	17	36			
	25	27	29	45			
Al3	8.9	9.4	10	15	41		
	18	19	20	27	49		
Al4	6.5	6.8	7	8.9	15	35	
	14	15	15	18	27	45	
Al5	5.2	5.4	5.4	6.6	9.1	14	38
	12	12	12	14	19	27	52

pp in aF/μm^2

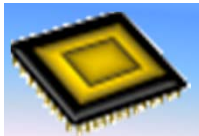
fringe in aF/μm

	Poly	Al1	Al2	Al3	Al4	Al5
Interwire Cap	40	95	85	85	85	115

per unit wire length in aF/μm for minimally-spaced wires

Dealing with Capacitance

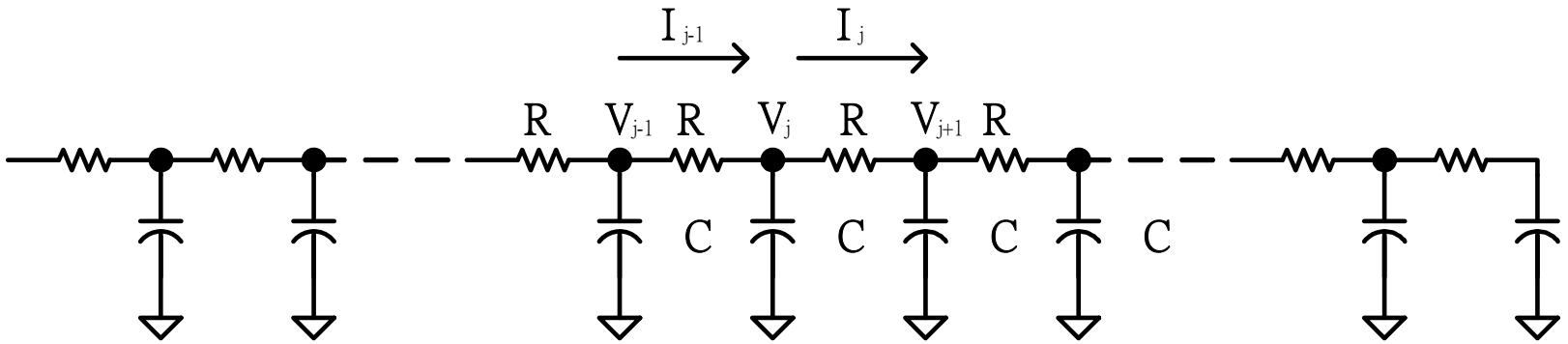
- Low capacitance (low-k) dielectrics (insulators) such as polymide or even air instead of SiO_2
  - family of materials that are low-k dielectrics
- Copper interconnect allows wires to be thinner without increasing their resistance, thereby decreasing interwire capacitance
- SOI (silicon on insulator) to reduce junction capacitance



Distributed RC effects

- For very long wires propagation delays caused by distributed R-C in the wiring layer tend to dominate
- A long wire can be represented in terms of several RC section.

Distributed RC effects



- Equivalent circuit: Distributed RC Network
- Diffusion equation

$$C\frac{dV_j}{dt} = (I_{j-1} - I_j) = \frac{(V_{j-1} - V_j)}{R} - \frac{(V_j - V_{j+1})}{R}$$

$$rc\frac{dV}{dt} = \frac{d^2V}{dx^2}$$

x=distance from input

r=resistance per unit length

c=capacitance per unit length

Distributed RC effects

- Solution:
- V(0,t)=Vs ; Voltage source at input
- V(x,0)=0 ; initial condition

$$\Rightarrow V(x,t) = V_S \cdot erfc \cdot \frac{x}{2\sqrt{RCt}}$$

- For Example, the time t_1 required for a wire with length l to reach a voltage $V(l,t_1)=kV_s$ is

$$\frac{V(l,\, t_1)}{V_S} = \text{erfc} \cdot \frac{l}{2\sqrt{RCt_1}} = \text{constant}$$

$$\Rightarrow \frac{l}{2\sqrt{RCt_1}} = \text{constant} \;\Rightarrow\; t_1 \propto RCl^2$$

The time required for a transient to propagate a distance l is proportional to x^2

Distributed RC effects

- Define R-C delay

$$T_d = \sum_{j=1}^{N} C_j \sum_{i=1}^{j} R_i \qquad \text{for } R_i = R, C_j = C \quad \text{for all i, j}$$

$$T_d = RC \cdot \frac{N(N+1)}{2}$$

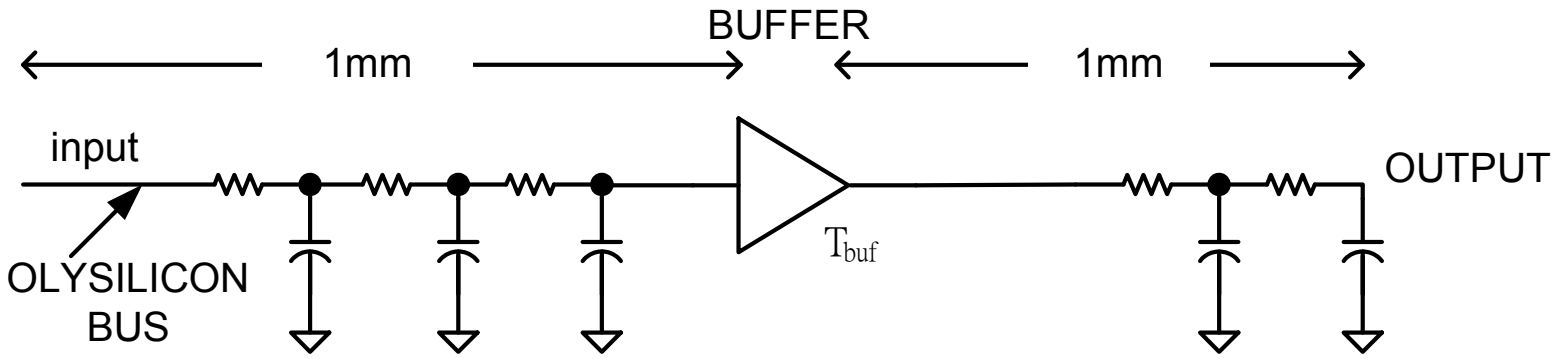
$$\text{As } N \to \infty \quad T_d = \frac{R_L C_L}{2}$$

where R_L : total line resistance

C_L : total line capacitance

Distributed RC effects

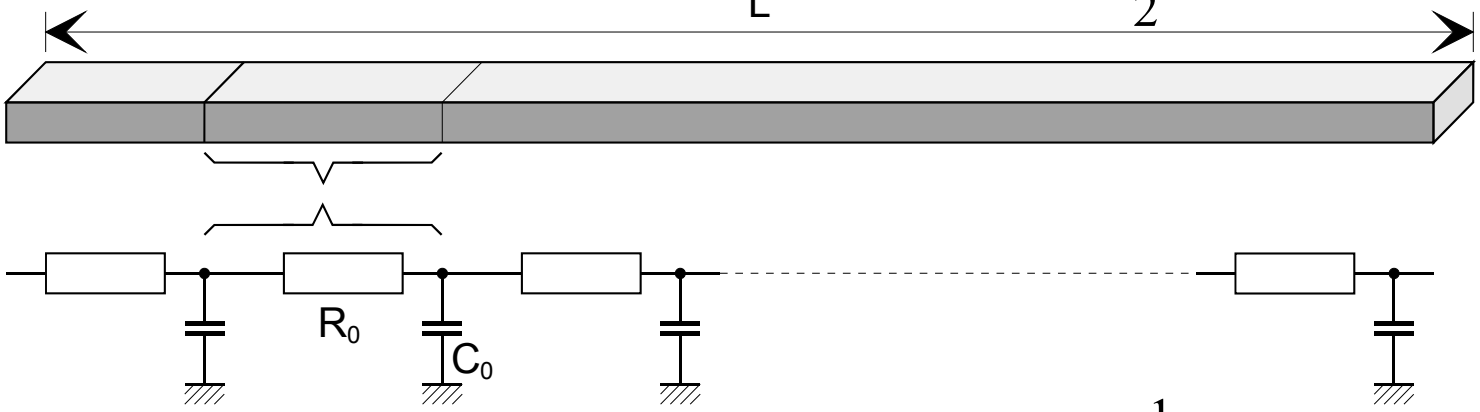
- In order to optimize speed in a long poly line, one possible strategy is to segment the line into several sections and insert buffers within theses sections.



Reduction RC effects

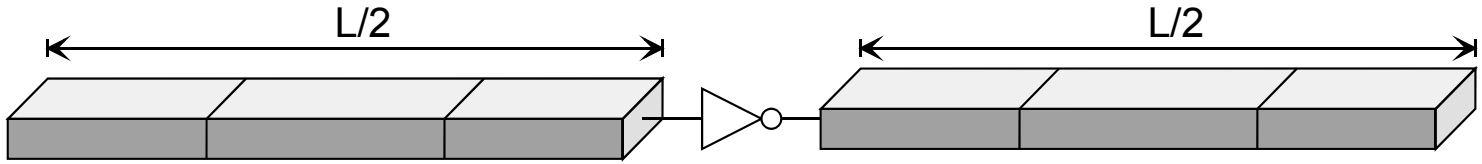
Long line

$$t_d = \frac{1}{2} \cdot R_0 \cdot C_0 \cdot L^2$$



Delay optimization

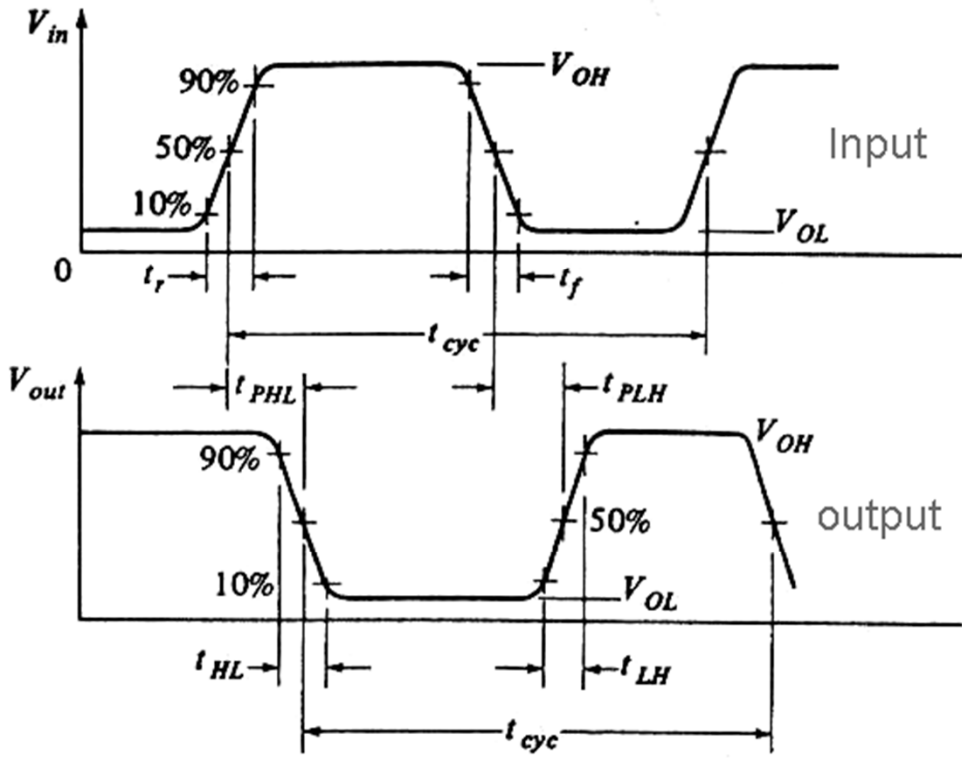
$$t_d' = \frac{1}{2} t_d + t_{buf}$$



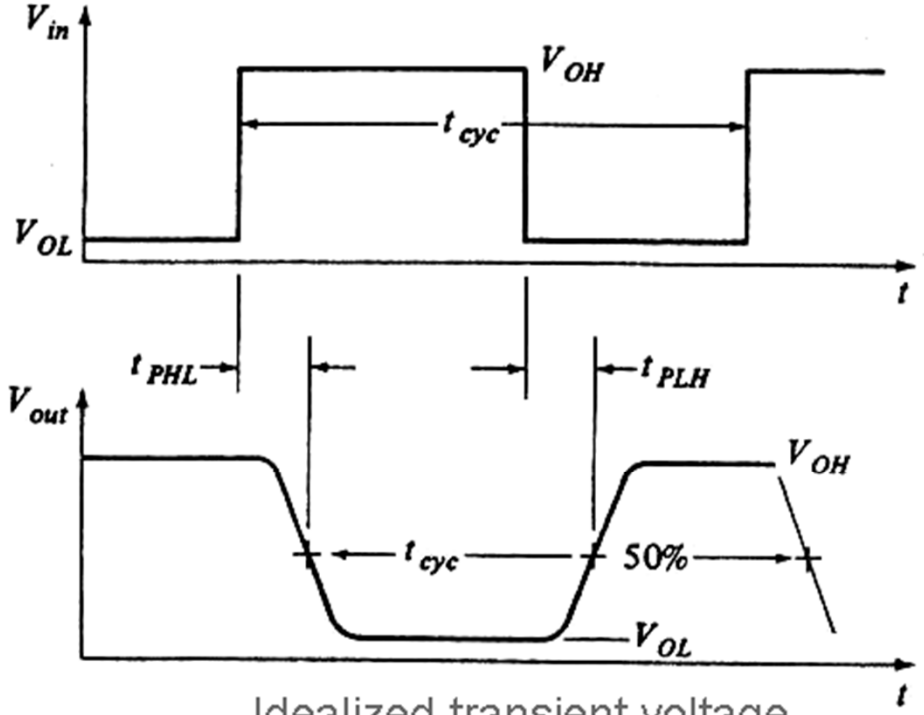
Switching Characteristics

- Measures time quality of digital circuit .
- Consider “_____”, “_____”, “_____”and “_____”.

Switching Characteristics



Actual trasient voltage

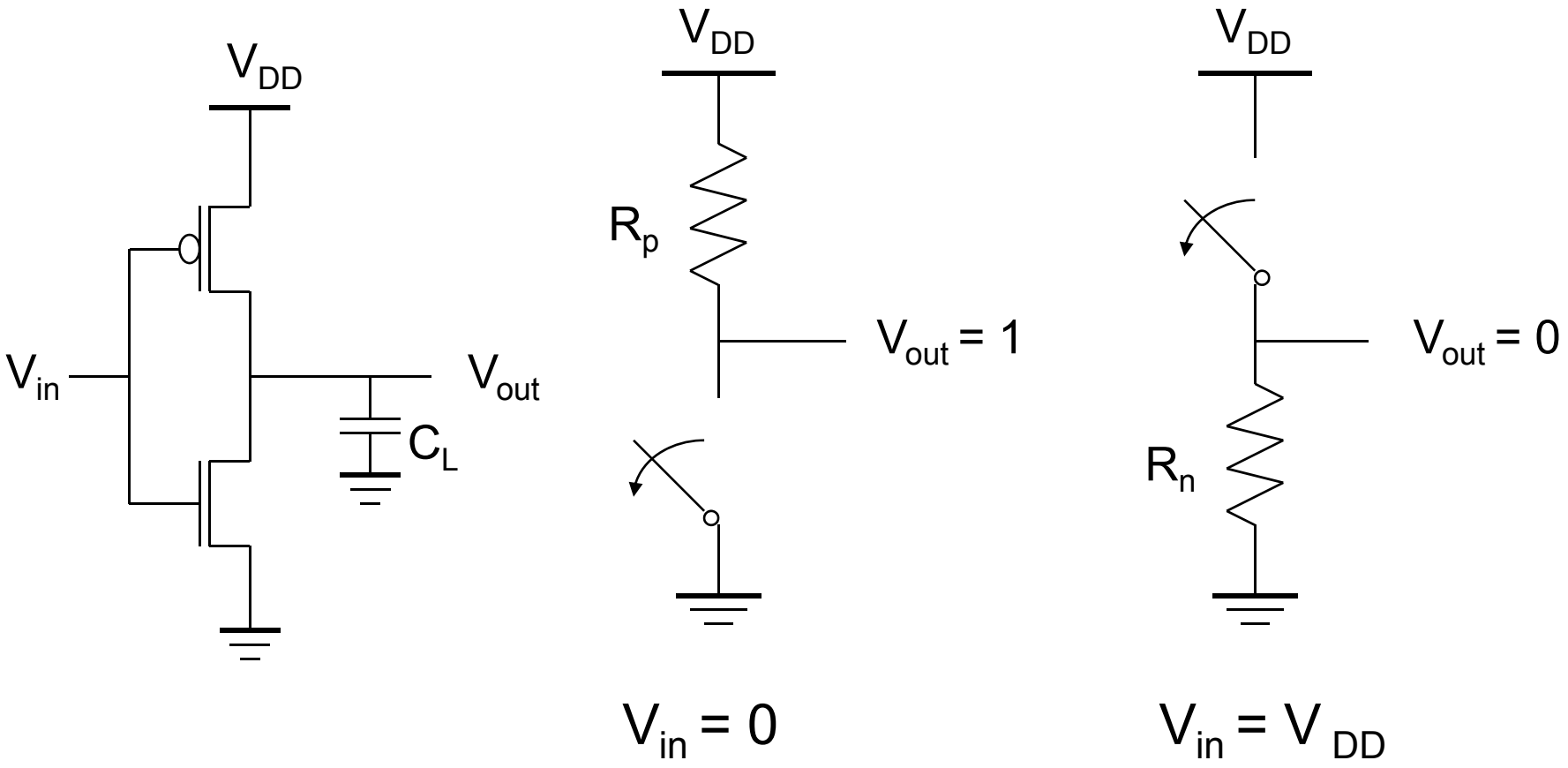


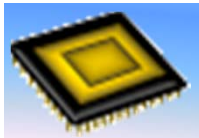
Idealized transient voltage

Switching Characteristics

- RISE and FALL times tr and tf : The ___ and ___ points of the total voltage transition at the input.
- High-low and low-high transition time at the output t_{HL}, t_{LH} : between the ___ and ___ points.
- Propagation delay times from input to output t_{PHL},t_{PLH} : between the points of the input and output pulse waveforms.
- Cycle time t_{CYC} : the time between identical points of successive cycle in the signal waveform.

CMOS Inverter: Steady State Response

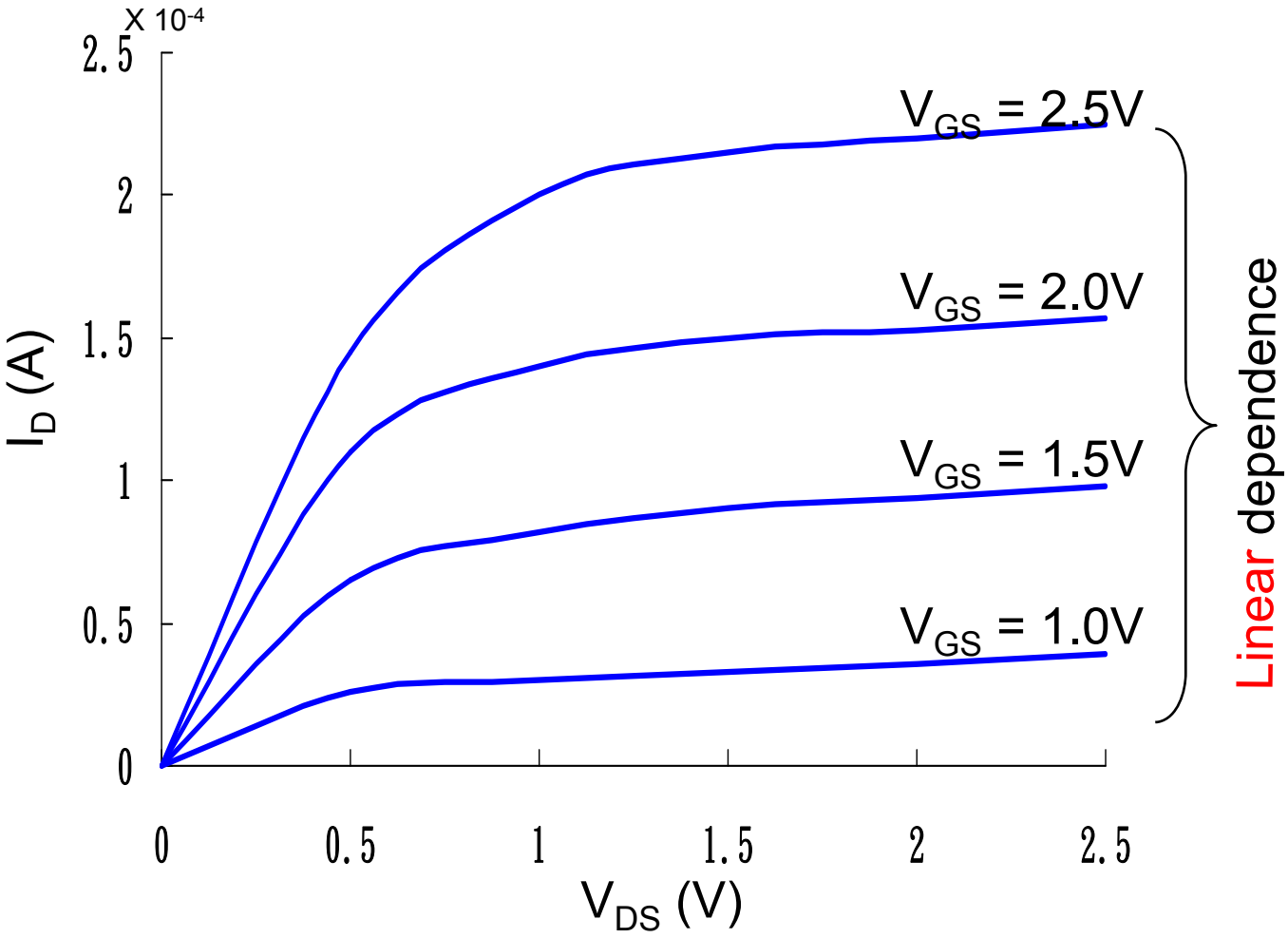




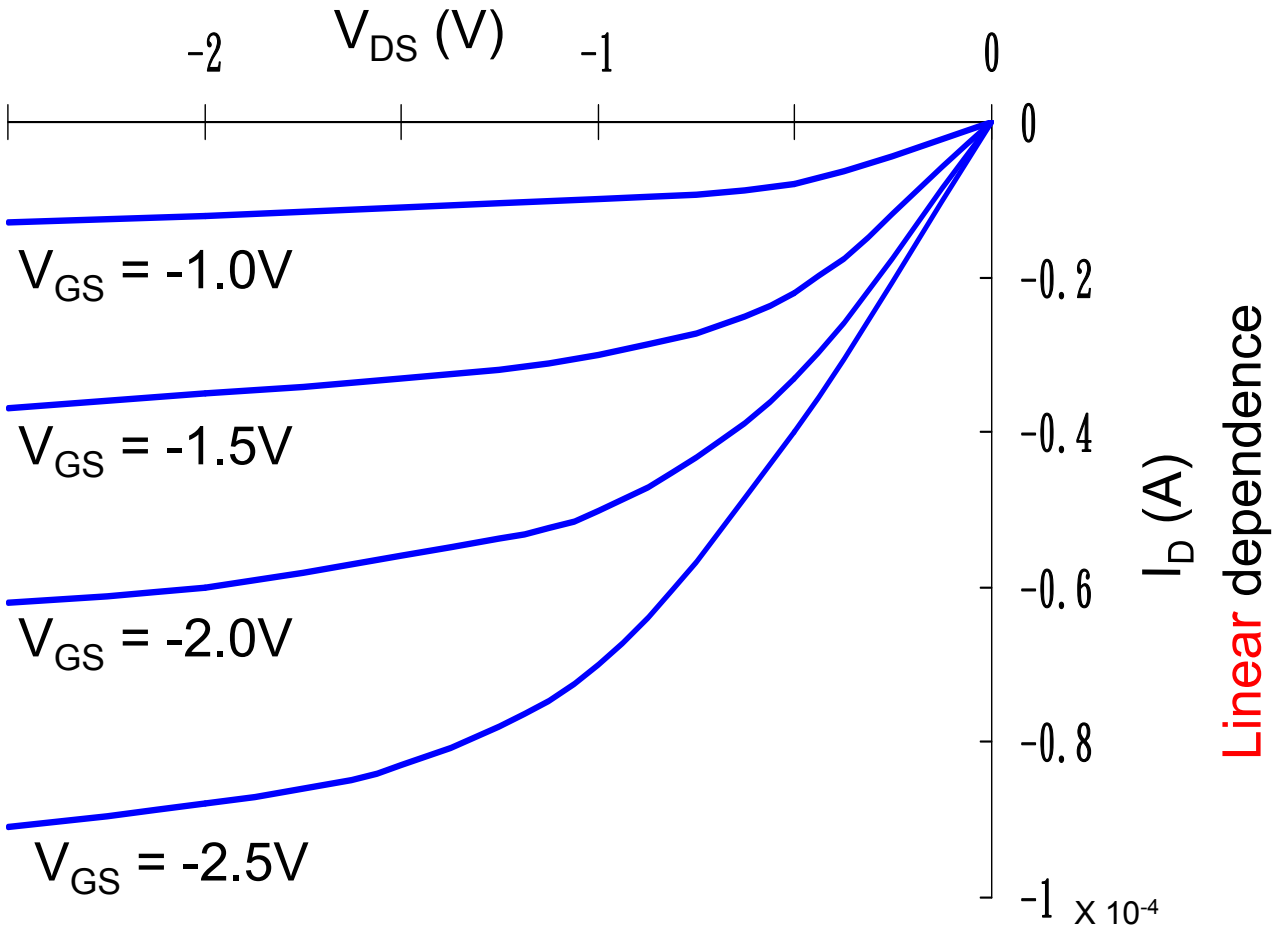
CMOS Properties

- Full rail-to-rail swing ⇒ high noise margins
  - Logic levels not dependent upon the relative device sizes ⇒ transistors can be minimum size ⇒ _____
- Always a path to V_{dd} or GND in steady state ⇒ low output impedance (output resistance in kΩ range) ⇒ large fan-out (albeit with degraded performance)
- Extremely high input resistance (gate of MOS transistor is near perfect insulator) ⇒ _____
- No direct path steady-state between power and ground ⇒ _____
- Propagation delay function of load capacitance and resistance of transistors

NMOS I-V Characteristic



PMOS I-V Characteristic



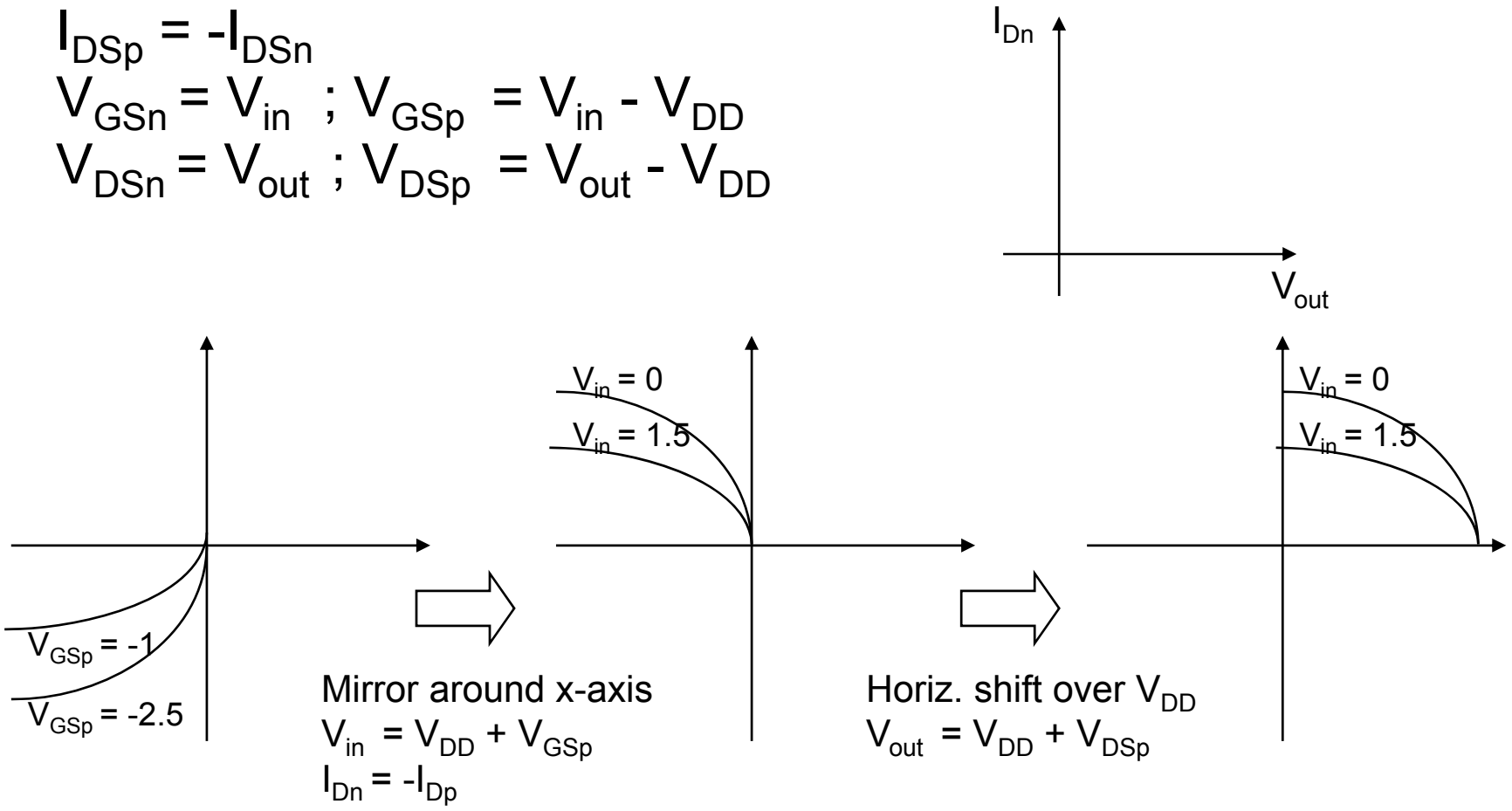
Transforming PMOS I-V Lines

- Want common coordinate set V_{in}, V_{out}, and I_{Dn}

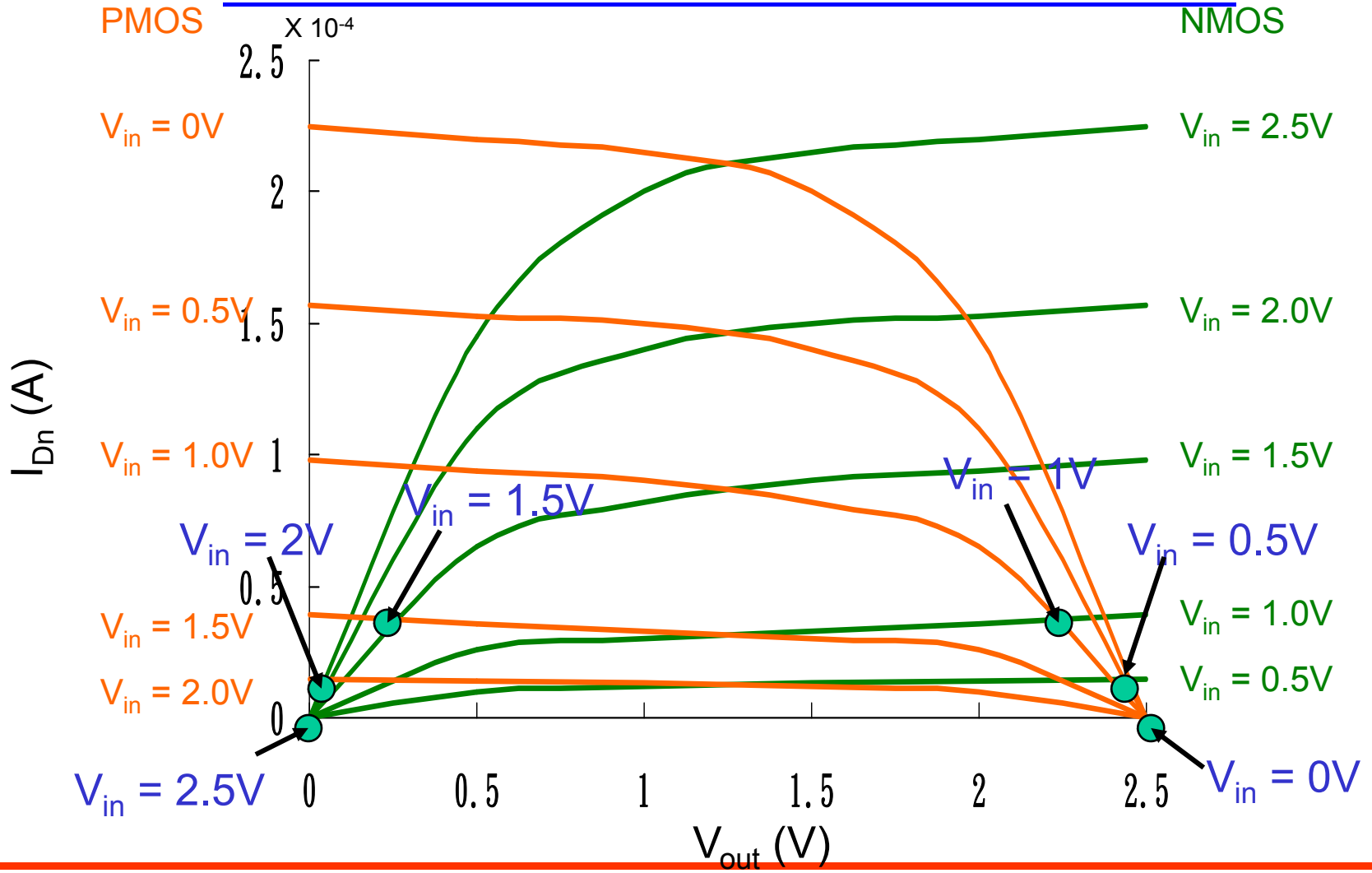
$I_{DSp} = -I_{DSn}$

$V_{GSn} = V_{in}$; $V_{GSp} = V_{in} - V_{DD}$

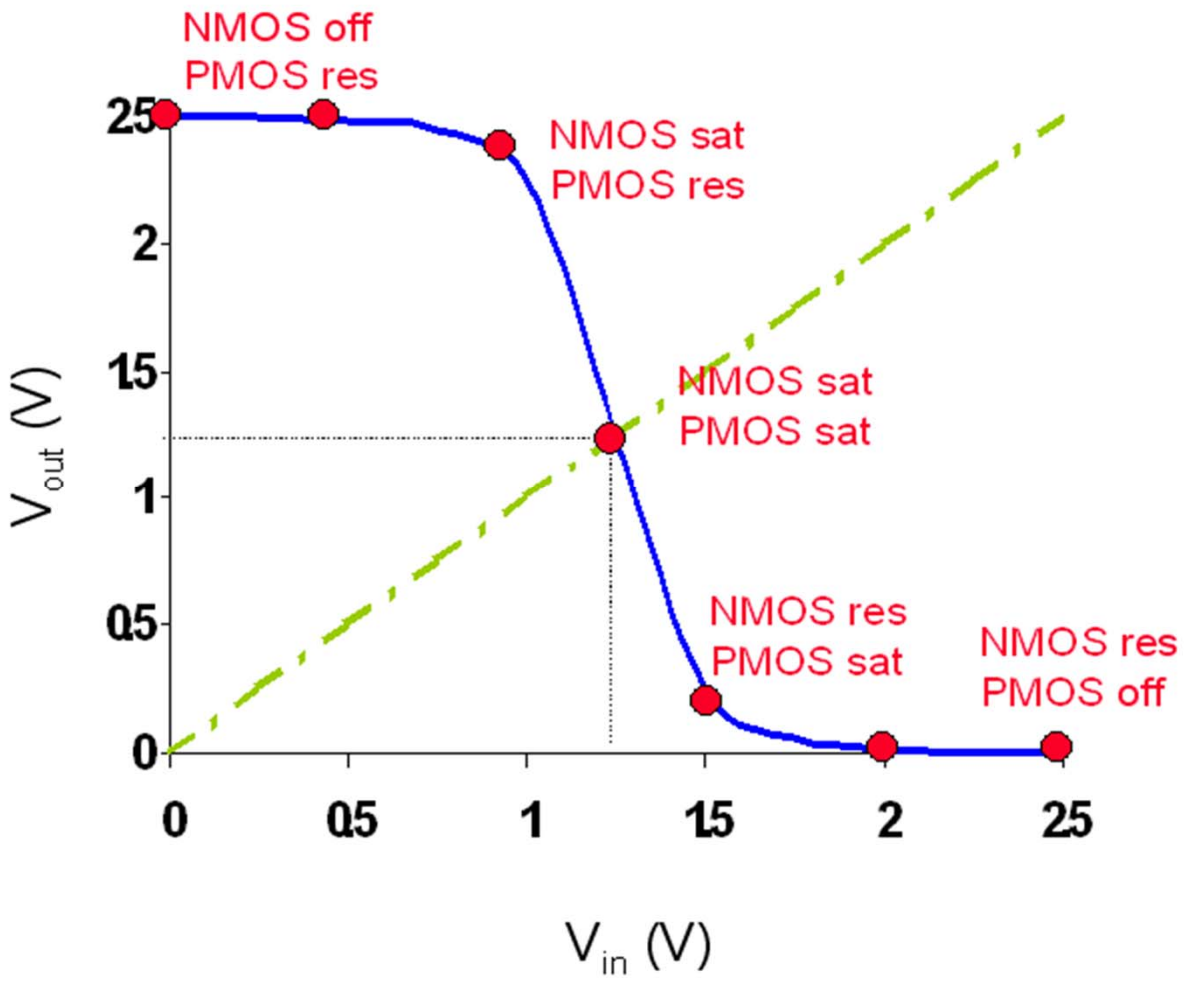
$V_{DSn} = V_{out}$; $V_{DSp} = V_{out} - V_{DD}$



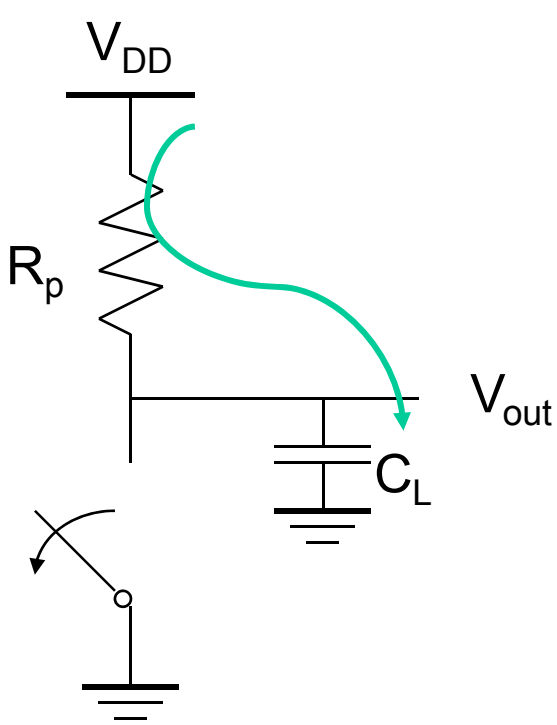
CMOS Inverter Transform Curve



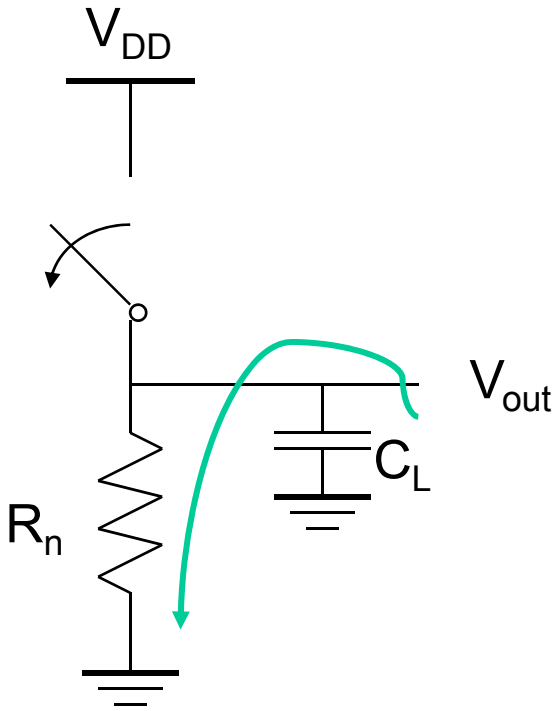
CMOS Inverter VTC



CMOS Inverter: Switch Model of Dynamic Behavior



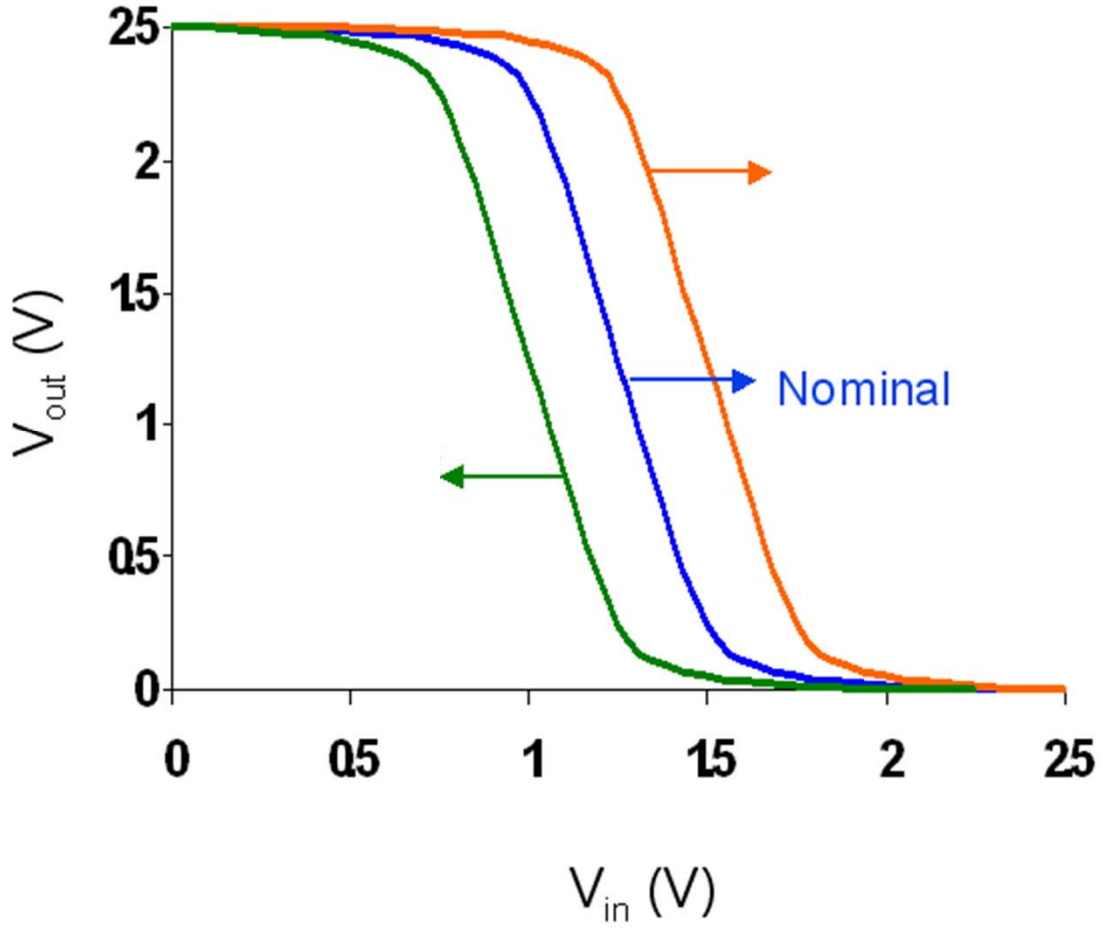
$V_{in} = 0$



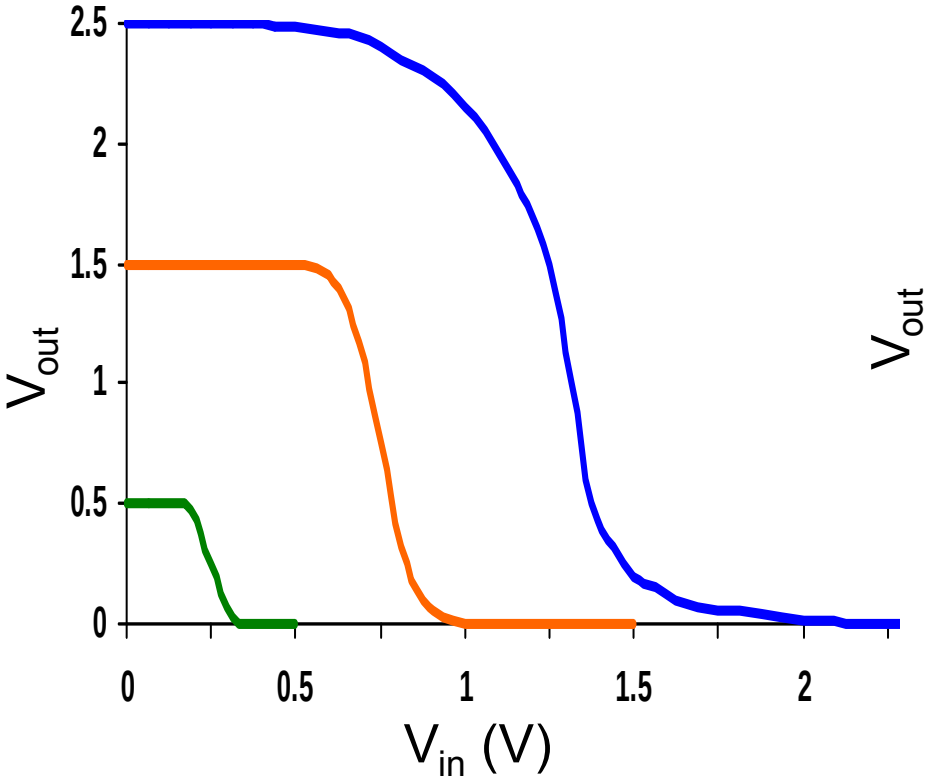
$V_{in} = V_{DD}$

- Gate response time is determined by the time to charge C_L through R_p (discharge C_L through R_n)

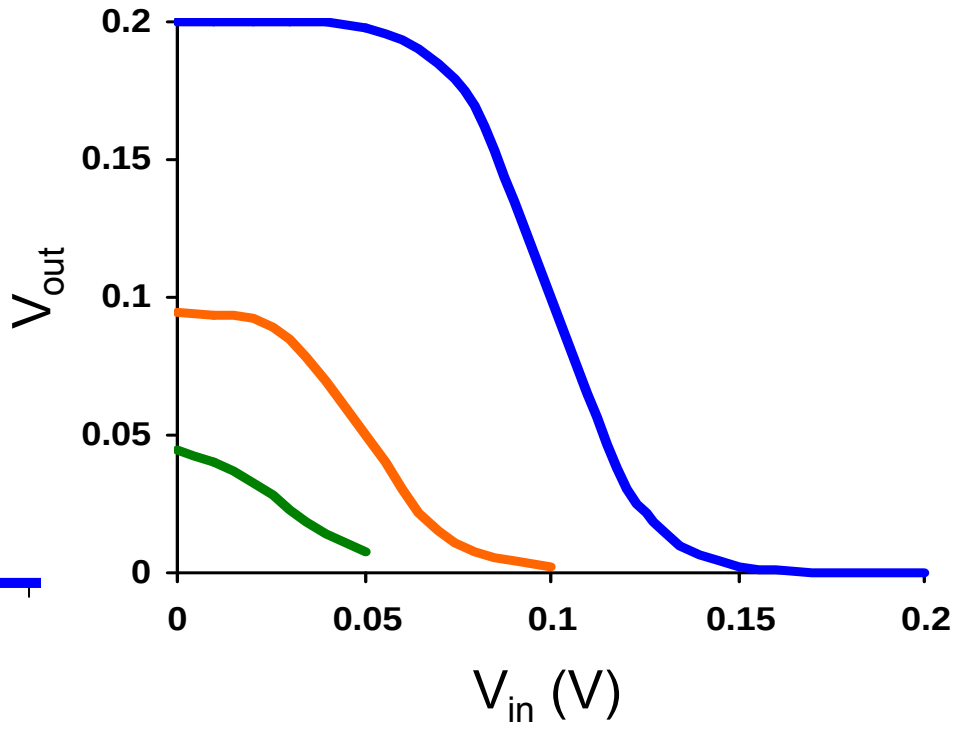
Impact of Process Variation on VTC Curve



Scaling the Supply Voltage



Device threshold voltages are kept (virtually) constant



Device threshold voltages are kept (virtually) constant

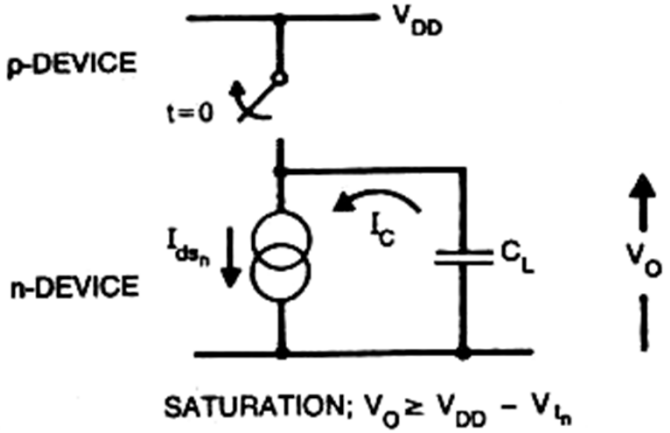
Analytic Delay Models

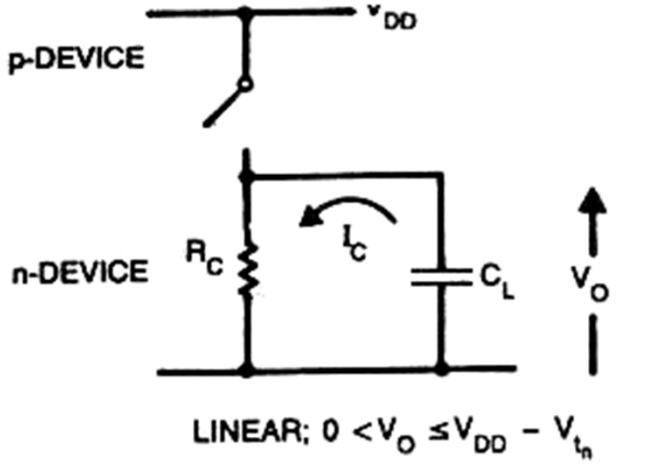
- (A) Fall Time($V_{IN}=V_{DD}=V_{GSN}$)
- Saturation

$$I_{DN}=\beta_n(V_{GS}-V_{TN})^2$$
$$=\beta_n(V_{DD}-V_{TN})^2$$

- Linear

$$I_{DN}=\beta_n(V_{gs}-V_{TN}-V_{DS}/2)\,V_{DS}$$
$$=\beta_n(V_{gs}-V_{TN}-V_O/2)\,V_O$$





Analytic Delay Models

- the Fall Time $t_f=t_{f1}+t_{f2}$

  t_{f1}:Vo drops from 0.9*Vdd to (V_{DD}-V_{TN})

  t_{f2}:Vo drops from (V_{DD}-V_{TN}) to 0.1*V_{DD}

$$C_L * \frac{dV_O}{dt} = I_{DN}$$

$$\Rightarrow \frac{C_L}{I_{DN}} dV_O = dt \Rightarrow \int dt = \int \frac{C_L}{I_{DN}} dV_O$$

Analytic Delay Models

t_{f1} : NMOS in saturation

$$t_{f1} = \int dt = \int_{V_{DD}-V_{TN}}^{0.9V_{DD}} \frac{C_L}{I_{DN}} dVo = \frac{2C_L}{\beta_n (V_{DD} - V_{TN})^2} \int_{V_{DD}-V_{TN}}^{0.9V_{DD}} dVo$$

$$= \frac{2C_L (Vth - 0.1V_{DD})}{\beta n (V_{DD} - V_{TN})^2}$$

t_{f2} : NMOS in linear

$$t_{f2} = \int_{0.1V_{DD}}^{V_{DD}-V_{TN}} \frac{C_L}{I_{DN}} dVo = \frac{C_L}{\beta_n V_{DD} (1-n)} \ln(19 - 20n)$$

where $n = V_{TN}/V_{DD}$

Analytic Delay Models

$$t_f = t_{f1} + t_{f2} = 2\frac{C_L}{\beta_n V_{DD}(1-n)}\left[\frac{(n-0.1)}{1-n} + \frac{1}{2}\ln(19-20n)\right]$$

$$\approx K \times \frac{C_L}{\beta_n V_{DD}} \qquad K \approx 3 \text{ to } 4 \qquad \text{for } V_{DD} = 3 \text{ to } 5 \text{ volts}$$

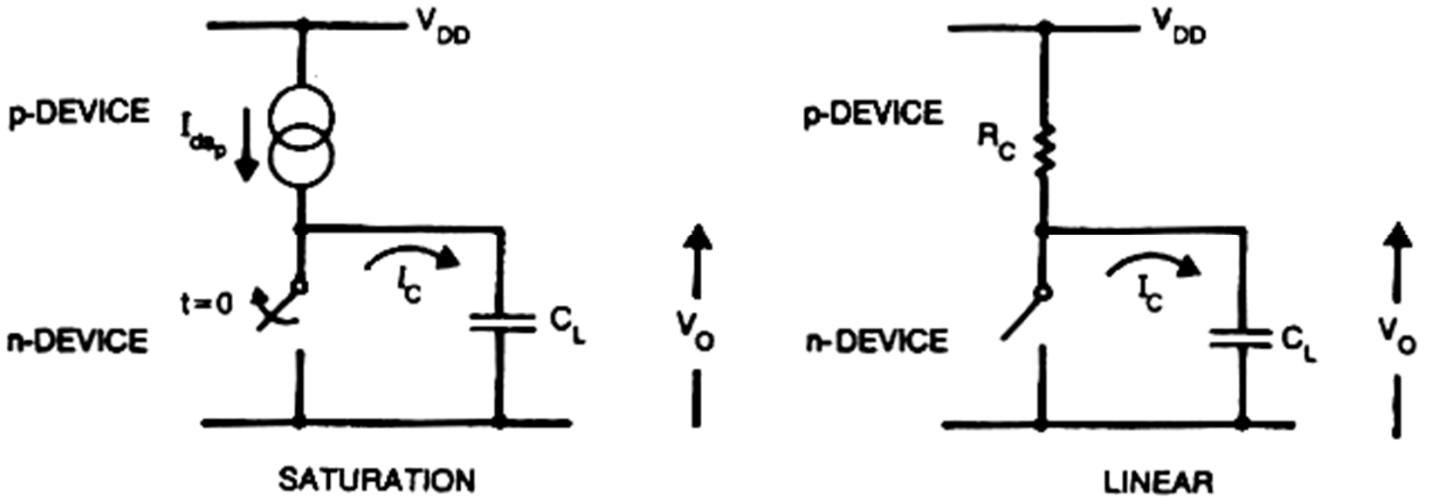
$$t_f \propto C_L ; t_f \propto \frac{1}{V_{DD}} \quad ; t_f \propto \beta_n^{-1} \propto \left(\frac{W}{L}\right)^{-1} = \left(\frac{L}{W}\right)$$

- t_f can be effective decreased by
  - _____
  - _____
  - _____

Analytic Delay Models

- (B) Rise Time(V_{IN}=0)

  Similar as the t_f, we can find the Rise Time t_r of the CMOS inverter



Analytic Delay Models

$$t_r = 2\frac{C_L}{\beta_p V_{DD}(1-p)}\left[\frac{(p-0.1)}{1-p}+\frac{1}{2}\ln(19-20n)\right]$$

$$\approx 3 \rightarrow 4\ \frac{C_L}{\beta_p V_{DD}} \qquad \text{where } p=\frac{|V_{TP}|}{V_{DD}}$$

**If we want to $t_r = t_f$

Analytic Delay Models

- (C) Delay Time

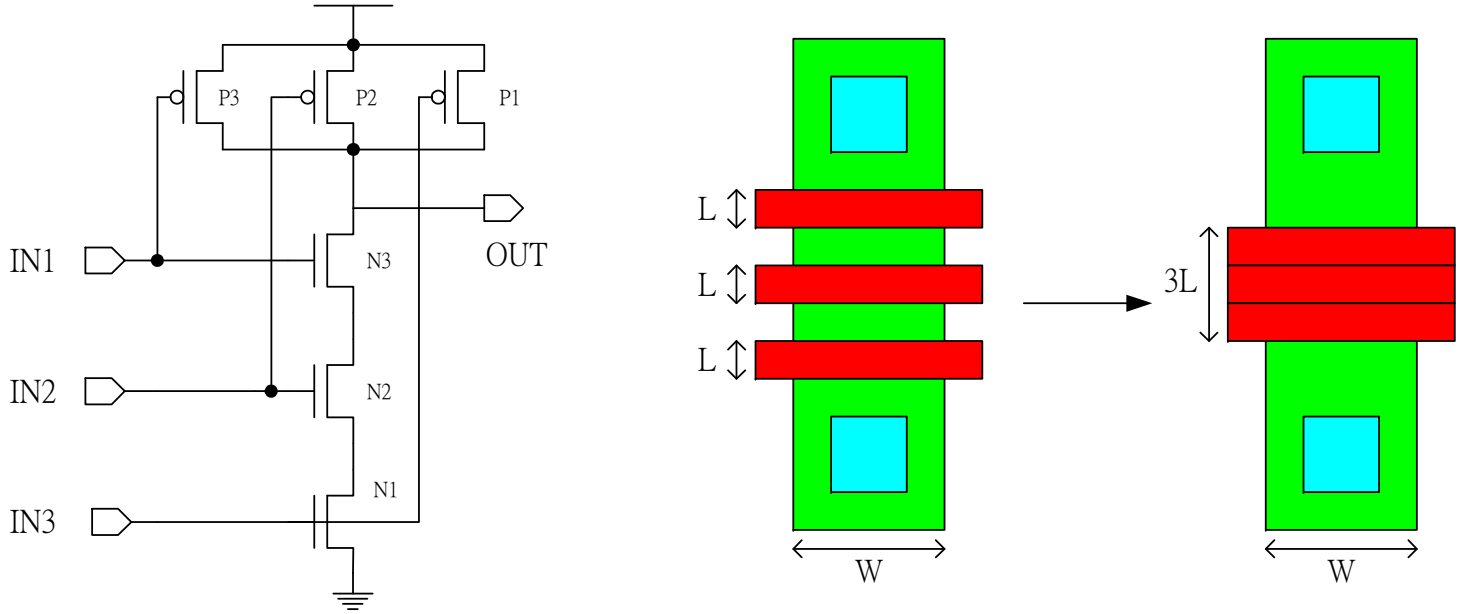
  The average gate delay for rising and falling transitions is

$$t_{av} = \frac{t_{df} + t_{dr}}{2} \qquad \text{where} \begin{cases} t_{df} = \dfrac{t_f}{2} \\ t_{dr} = \dfrac{t_r}{2} \end{cases}$$

$$\therefore \quad \text{if } t_r = t_f \Rightarrow t_{av} = \frac{t_r}{2} = \frac{t_f}{2}$$

Gate Delays

- The delay of simple gate may be approximated by constructing an “equivalent”inverter.
- For Example, in the 3-input NAND



Example (3-input NAND)

$$\beta_{neff} = \frac{1}{\frac{1}{\beta_{n1}} + \frac{1}{\beta_{n2}} + \frac{1}{\beta_{n3}}}$$

For $\beta_{n1} = \beta_{n2} = \beta_{n3} = \beta_n$

$$\beta_{neff} = \frac{\beta_n}{3} = \beta_{series}$$

(Summation of series conductance) $\therefore \tau_{series} = K\frac{C_L}{\frac{\beta_n}{3}V_{DD}} = 3K \times \frac{C_L}{\beta_n V_{DD}}$

Assume $\mu_p = \frac{1}{2}\mu_n$, want $t_r = t_f$ as an inverter.

Design the W_p and W_n of the 3-input NAND.

$\Rightarrow$ 3-input NAND

$L_p = L_n = L_{min}$, $W_n = 3W_{min}$, $W_p = 2W_{min}$

"equilvalen t" inverter

$L_p = L_n = L_{min}$, $W_n = W_{min}$, $W_p = 2W_{min}$

CMOS – Gate Transistor Sizing

- Want to determine the CMOS channel width
  - Minimum-Sized Inverter and “Equivalent” Simple Gate
  - Tapered Buffer Stage Ratio

Minimum-Sized Inverter and "Equivalent" Simple Gate

Set $t_r = t_f$, we have $\beta_n = \beta_p$

- A minimum size inverter is

$L = L_p = L_n = L_{min}$

$W_p = 3W_{min}$

$W_n = W_{min}$ ($Assume\ \mu_n = 3\mu_p$)

- m-input NAND

$L = L_{min}$

$W_p = 3W_{min}$

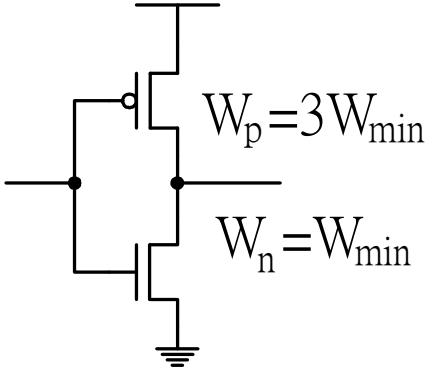
$W_n =$

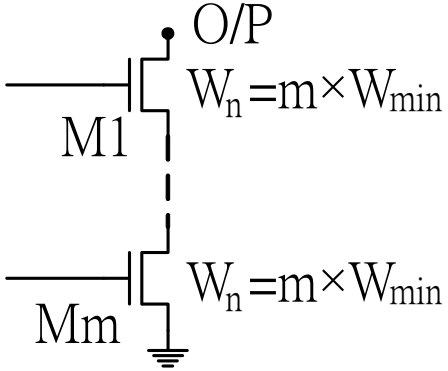
- m-input NOR

$L = L_{min}$

$W_p =$

$W_n = W_{min}$





- **In static CMOS Logic design, NAND using fewer MOS gate area than NOR gate**
- **=> NAND gate constructing faster logic operation.**

Tapered Buffer Stage Ratio

- How to drive large capacitive load?

  Eq. (1)output Buffer and output pad ~20pf

  (2)internal data bus ~5pf

  (3)Clock drivers ~10pf ~50pf

  ---Dynamic Logic & Memory

Tapered Buffer Stage Ratio

C_L: load capacitance

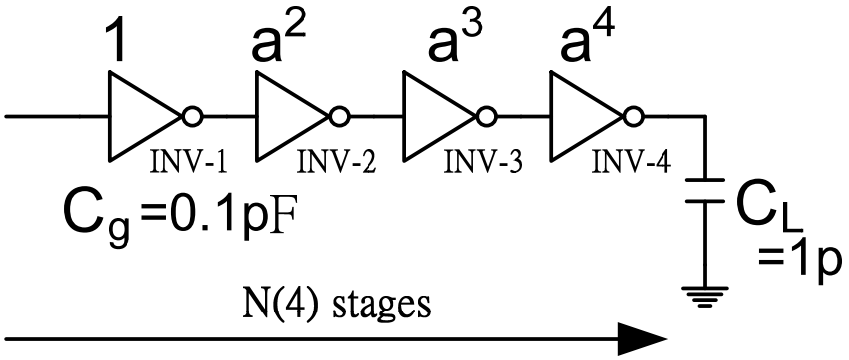
C_g: cap. of a minimum inverter

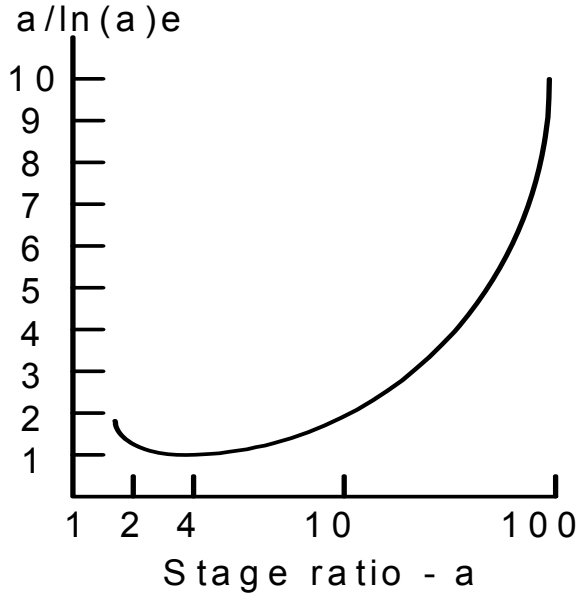
td: the average delay of a min-sized inverter driving another min-sized inverter.

(1) Using a minimum inverter to drive the C_L .

Total delay =R × td = 100 td ($R=(C_L/C_g)$)

(2) Multi Stage Tapered Buffer.





Tapered Buffer Stage Ratio

- Consider a cascade of enlarged inverter, each scaled by a^i relative to the minimum inverter.
- Using n cascade inverter let $a^n = R$

  =>ln R =n ln a =>n=ln(R) /ln(a)

  total delay =_____

Tapered Buffer Stage Ratio

- Want to optimize total delay (min delay)

$$\frac{\partial(\text{Total delay})}{\partial \text{a}} = (\ln \text{R})td\left[\frac{1}{\ln \text{a}} + a\frac{\partial}{\partial \text{a}}\left(\frac{1}{\ln \text{a}}\right)\right]$$

$$= (\ln \text{R})td\left[\frac{1}{\ln \text{a}} + a\left(-\frac{1}{(\ln \text{a})^2}\right)\frac{1}{\text{a}}\right]$$

$$= \frac{\ln \text{R}}{\ln \text{a}} \cdot td\left[1 - \frac{1}{\ln \text{a}}\right] = 0 \qquad \Rightarrow \ln(a_{\min}) = 1$$

- In practical a $\fallingdotseq$ _____ for area consideration

Power Dissipation

- There are two components of power dissipation in a CMOS gate.

1. _____ due to leakage current or other current drawn continuously from the power supply.
2. _____ due to
   - switching transient current
   - charge & discharge of load cap

Power Dissipation

A. Static Power Dissipation

Ps=

where

Ps = total static power dissipation

n = number of devices

Power Dissipation

B. Dynamic Power Dissipation

- Charging and discharging of load capacitance
- As P and N alternately switch ON and OFF, C_L is charged to V_{DD} and the discharged to GND.

Power Dissipation

- Charge:

$$E_C = \int i_p(t)[V_{DD} - Vo(t)]dt$$

$$= V_{DD}\int i_p(t)dt - \int i_p(t)Vo(t)dt$$

$$= C_L V_{DD}\int_0^{V_{DD}} dv - C_L\int_0^{V_{DD}} Vdv$$

$$= C_L {V_{DD}}^2 - \frac{1}{2}C_L {V_{DD}}^2$$

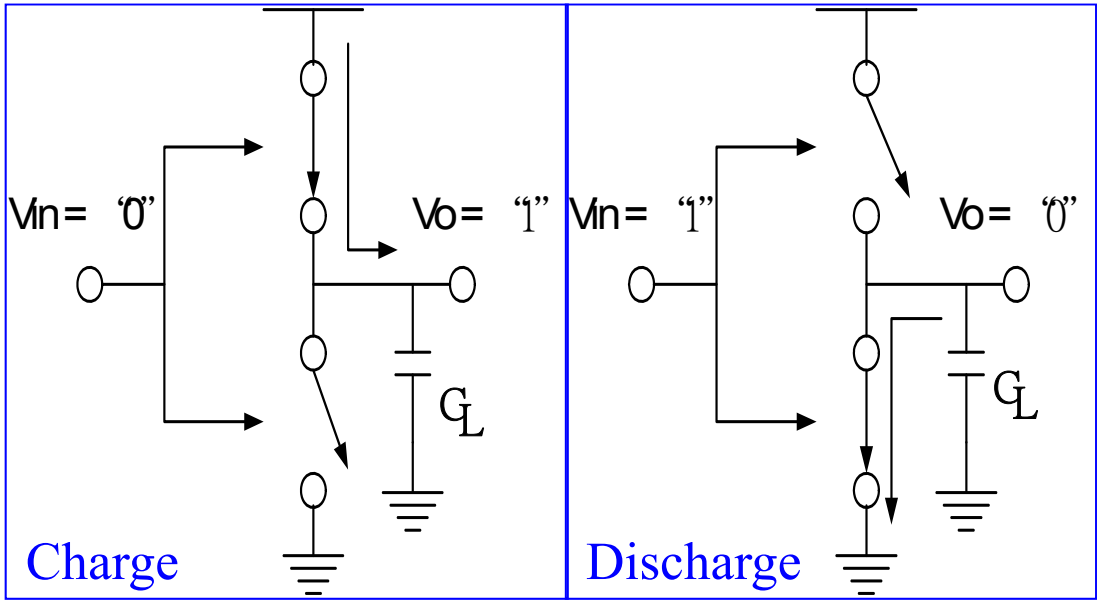
$$= \frac{1}{2}C_L {V_{DD}}^2$$

- Discharge:

$$E_D = \int i_n(t)V(t)dt$$

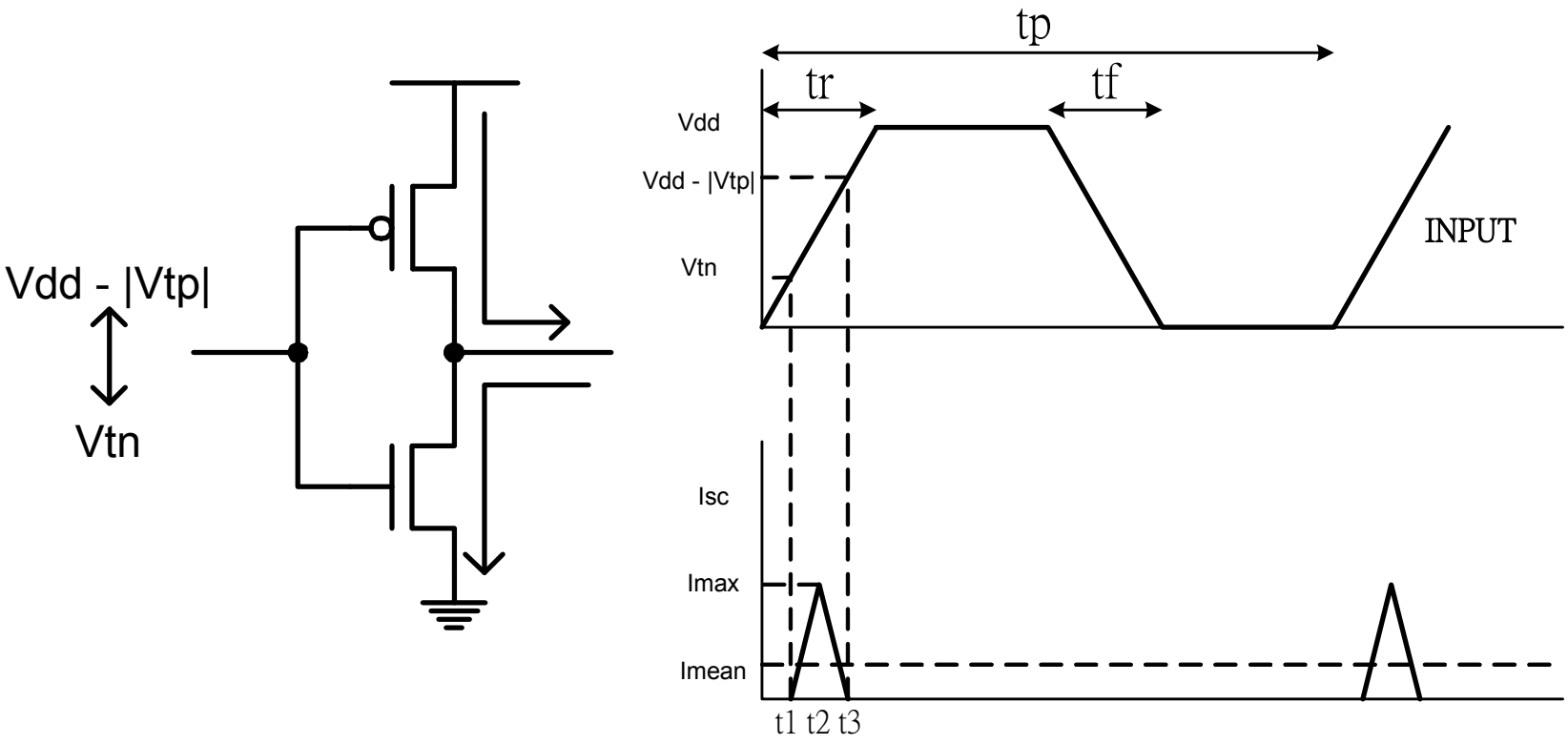
$$= -\int_{V_{DD}}^{0} C_L Vodv$$

$$= \frac{1}{2}C_L {V_{DD}}^2$$



Power Dissipation

C. Short – Circuit Dissipation



Power Dissipation

$$P_{SC} = I_{mean} \times V_{DD}$$

$$I_{mean} = 2 \times \left[\frac{1}{T} \int_{t1}^{t2} I(t)dt + \frac{1}{T} \int_{t2}^{t3} I(t)dt \right]$$

$$\text{Assume } V_{TN} = -V_{TP} \ , \ \beta_n = \beta_p = \beta \ , \ t_r = t_f \ , \ Vin(t) = \frac{V_{DD}}{t_r} \times t$$

$$\text{We have } P_{SC} = \frac{\beta}{12}(V_{DD} - 2V_t)^3 \left(\frac{t_{rf}}{t_p} \right)$$

where t_p : the period of the input waveform.

$$P_{SC} \propto \frac{t_{rf}}{t_p} \Rightarrow \text{small } t_{rf} \Rightarrow \text{small } P_{SC}$$

* Slow rise times can result in significant short - circuit dissipation.

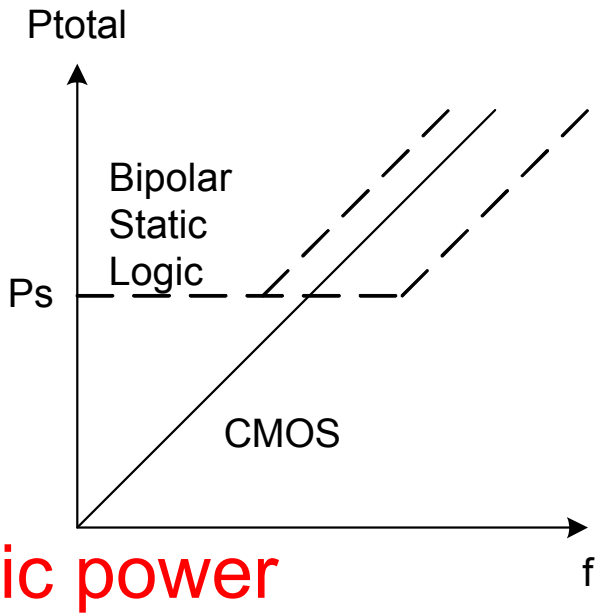
Power Dissipation

D. Total Power Dissipation

$P_{total} = P_s + P_d + P_{sc}$

P_s : Static dissipation

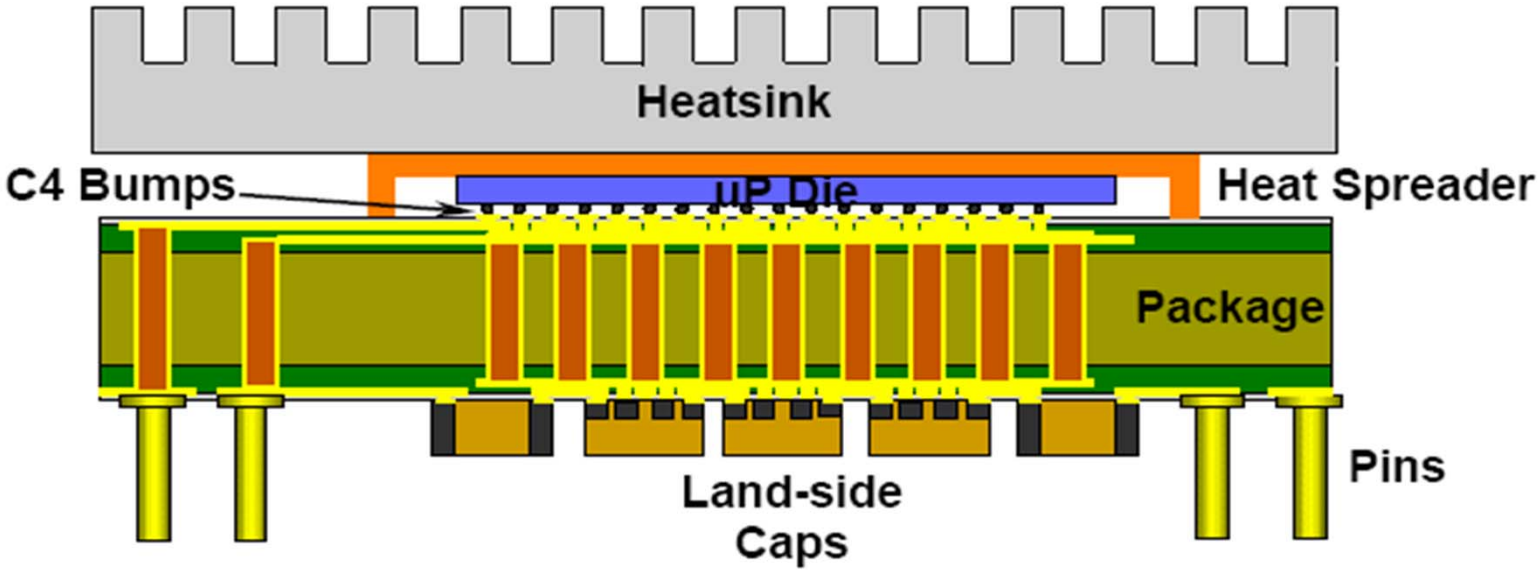
P_d , P_{sc}: Dynamic dissipation



- As frequency increased, dynamic power dissipation is dominated.

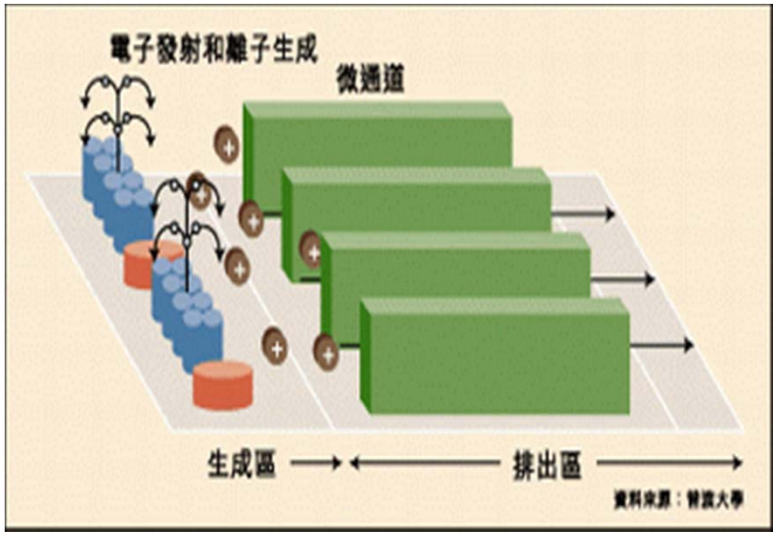
Packaging Cross-Section

- A sample processor cross-section is shown below
  - May or may not have a heat spreader
  - May have die side capacitors as well as land side
  - Package may have 4-14 layers depending on number of signals and cost structure of market (low-end desktop to high-end server)
  - May have an additional layer of package (interposer) for space transformation and for housing additional components
- Power must penetrate through the socket and package

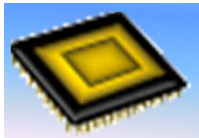


奈米技術將創造自我冷卻晶片

- 美國普渡大學(Purdue University)
- 桶式(bucket brigade)、類似電荷耦合的元件，它可以將熱量從處理電子訊號的晶片中排出
- 離子風:當離子向前運動時，它們與中性的分子發生重覆碰撞，因而形成離子風。



Source:電子工程專輯



Chapter 4

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