AROR UNIVERSITY
OF ART, ARCHITECTURE,
DESIGN & HERITAGE,
SUKKUR, SINDH

Faculty of Artificial Intelligence & Multimedia Gamming

BS – Artificial Intelligence (Section A and B)

Digital Logic Design Lab

Lab # 11: Flip Flops

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Submission Profile

Name: Submission date (dd/mm/yy):

Marks obtained:

Comments:

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Instructor

Background Theory:

Flip-flops

- Flip-flops are the fundamental building blocks of sequential circuits.
- They are 1-bit storage devices that, unlike latches (which are level sensitive devices) are edge-triggered.
- Data gets stored into a flip-flop at one of the edges of the clock signal, i.e. when the clock input makes a transition from 0 to 1 or from 1 to 0.

The timing diagram of a clock pulse is shown below:

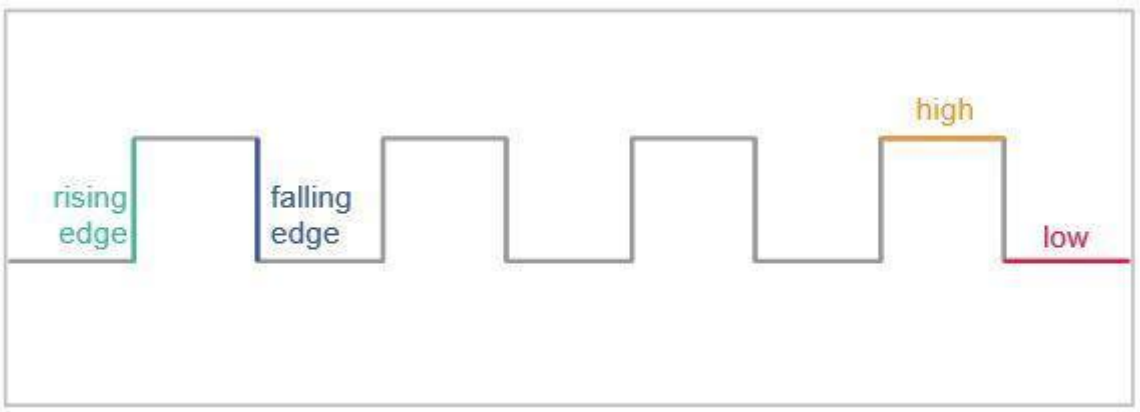


Figure 1-2 Timing diagram of a clock pulse

Latch Feedback

- The state transitions of the latches start in the moment the clock changes to 1 and can continue for the entire period while it is active.
- Because of this, the output of a latch cannot be applied through combinational circuits to the inputs of other latches triggered by the same clock signal.
- This fact represents a serious drawback when using latches as storage elements.
- Flip-flops overcome this problem by triggering only during signal conditions.

Latch feedback is illustrated in the figure below.

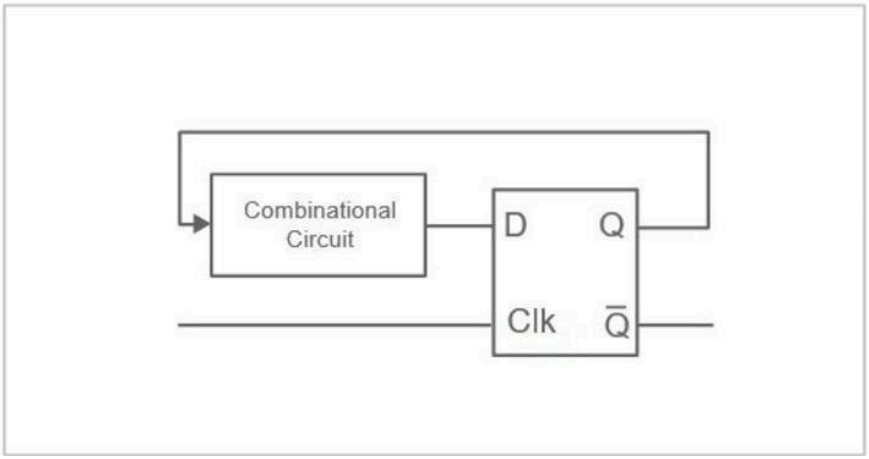


Figure 1-3 Latch feedback

D Flip-flops (DFFs)

D flip-flops (DFFs) are very commonly used because they are perfectly suited for the construction of sequential circuits.

- If the DFF transfers the input to the output on the rising edge of the clock signal then it is said to be a *positive-edge triggered* D flip-flop or positive-edge DFF.
- If the DFF transfers the input to the output on the falling edge of the clock signal then it is said to be a *negative-edge triggered* D flip-flop or negative-edge DFF.
- This mode of operation is signaled through the use of a circle on the clock input. The image below shows the symbol for a positive-edge DFF (left) and a negative-edge DFF (right).
- For both DFF circuits shown below, the small triangle on the clock input indicates that the flip-flop will trigger only on one of the clock edges.
- The complemented output, Q is omitted in the graphical symbol when it is not needed.

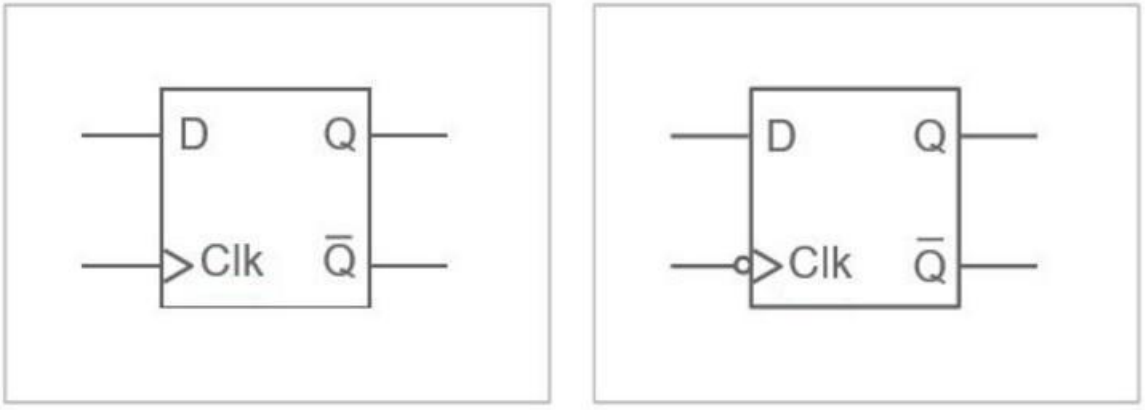


Figure 1-4 Positive edge DFF (left) and negative edge DFF (right)

The operation of the positive-triggered D flip-flop is very simple:

- The output **Q** will go to the present state of the **D** input when the clock signal changes from **0** to **1**.
- The level present at the input will be stored in the flip-flop on the rising transition of the **Clk** signal.

The figures below present the functionality of a positive-edge DFF:

Clk	Q(t +1)
0	Q
1	Q
↑	D
↓	Q

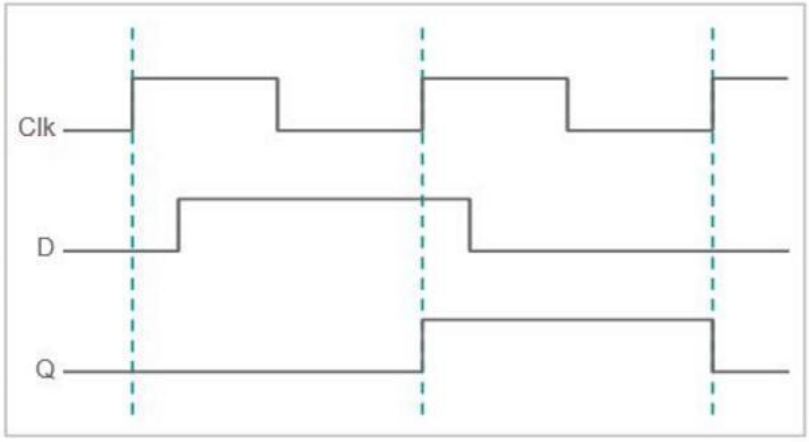


Figure 1-5 Characteristic table (left) and diagram (right) for a positive-edge DFF

A flip-flop can be built using the following methods:

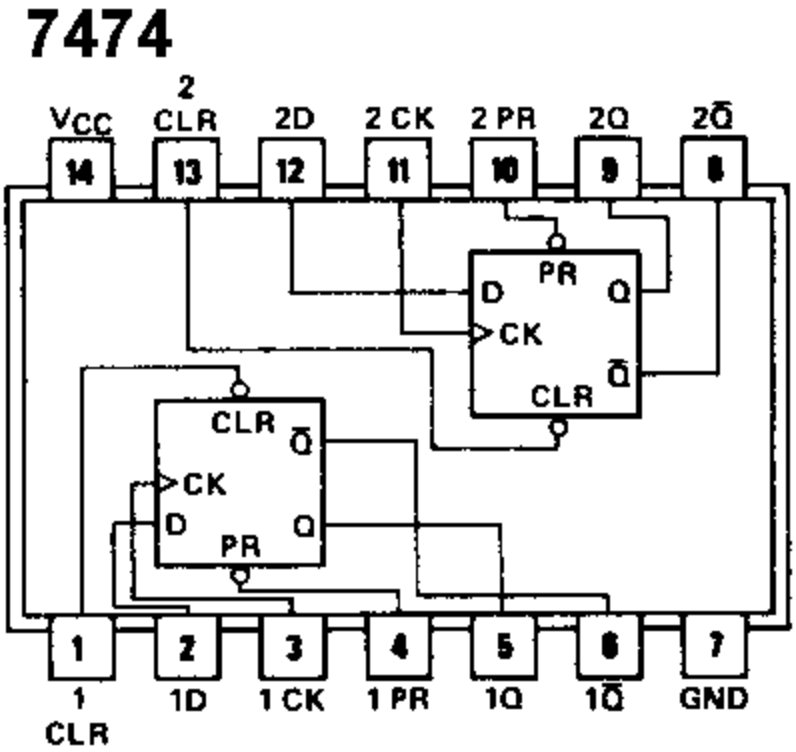
- Using two D latches arranged in a master-slave configuration, where one of them is transparent during one semi-period of the clock period and the other transparent during the other semi-period.

Note: another circuit having the same operation, but implemented using fewer gates, can be built from three SR latches.

- Using of a single D latch and short pulses derived from the clock signal, which cause of the latch to be transparent for only a brief moment. These circuits are called pulsed latches or pulse-based flip-flops.

The timing characteristics of flip-flops include:

- the propagation delay from **Clk** to **D** (the time needed for a value present on the input to reach the output when the clock changes from **0** to **1**)
- the setup time
- the hold time
- the maximum frequency that can be applied to the clock signal and still have correct operation



The J K Flip-flop (JKFF)

Another type of flip-flop, one that is not as widely used as the DFF, but a more versatile one, is the *J K flip-flop (JKFF)*.

- The J K flip-flop is referred to as the *universal* bi-stable because it can easily behave like any one of the others.
- It has two data inputs, (**J** and **K**), a clock input, and two outputs (**Q** and $\bar{\mathbf{Q}}$)
- **J** acts as a **SET** input and **K** acts as a **RESET** input.
- The output changes only on one of the clock edges.
- When both **J** and **K** are **1**, the flip-flop toggles between opposite logic states each time the clock signal changes from **0** to **1** from **1** to **0**.
- This circuit is like the one of a gated SR latch with an edge detector, with the difference that the *forbidden* state (when both **S** and **R** are set to **1**) is replaced by the *toggle* state.

The golden rules of JKFFs are:

1. If **J** and **K** are different, then **Q** is always the same as **J**.
2. If **J** and **K** are **0**, nothing happens.
3. If **J** and **K** are **1**, **Q** toggles.

The figures below present the way in which a J K flip-flop can be built using a DFF and logic gates. The graphical symbol of the JKFF is also shown below, and its operation is described by the characteristic table.

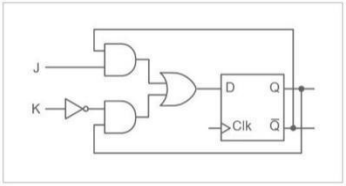


Figure 1-6 J K flip-flop built using a DFF and logic gates

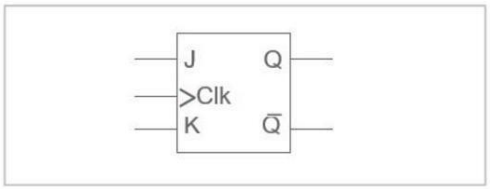


Figure 1-7 Graphical symbol of the JKFF

J	K	Q(t +1)	
0	0	Q(t)	no change
0	1	0	reset
1	0	1	set
1	1	Q(t)	toggle

Figure 1-8 (a) JKFF characteristic table

Lab Activities:

1.2 Simulate: Building a JK Flip Flop Using a DFF and Logic Gates

- Launch Multisim
- Connect the following circuit:

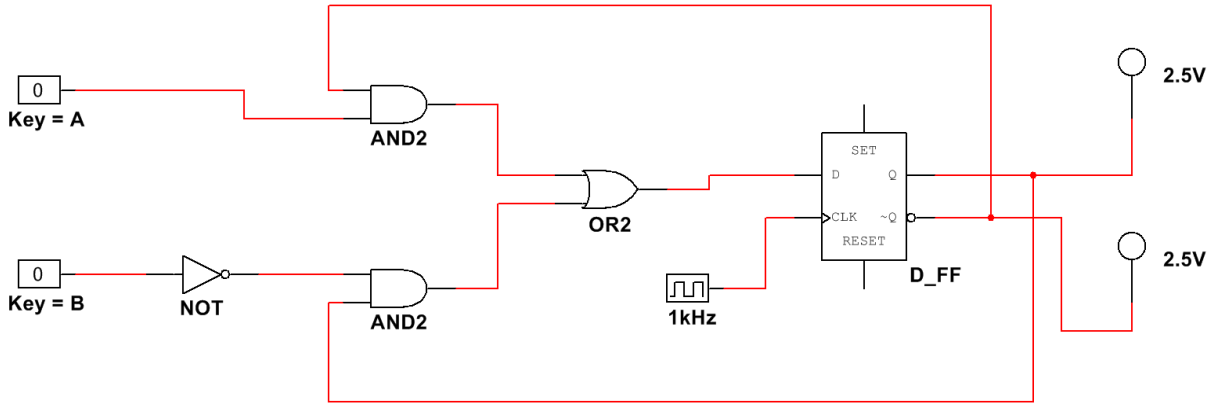


Figure 1-13 Circuit diagram

- **Start** the simulation
- Vary the two inputs and observe what happens

1-3 Compare your results with the following characteristic table:

J	K	Q(t +1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q(t)

Figure 1-14 JFKK characteristic table

Lab Activities:

1.3 Simulate: Building a D Flip-Flop

- Launch Multisim
- Connect the following circuit:
- Search d_ff for d flop flop
- Search DIPSWI for switch (S1 and S2)

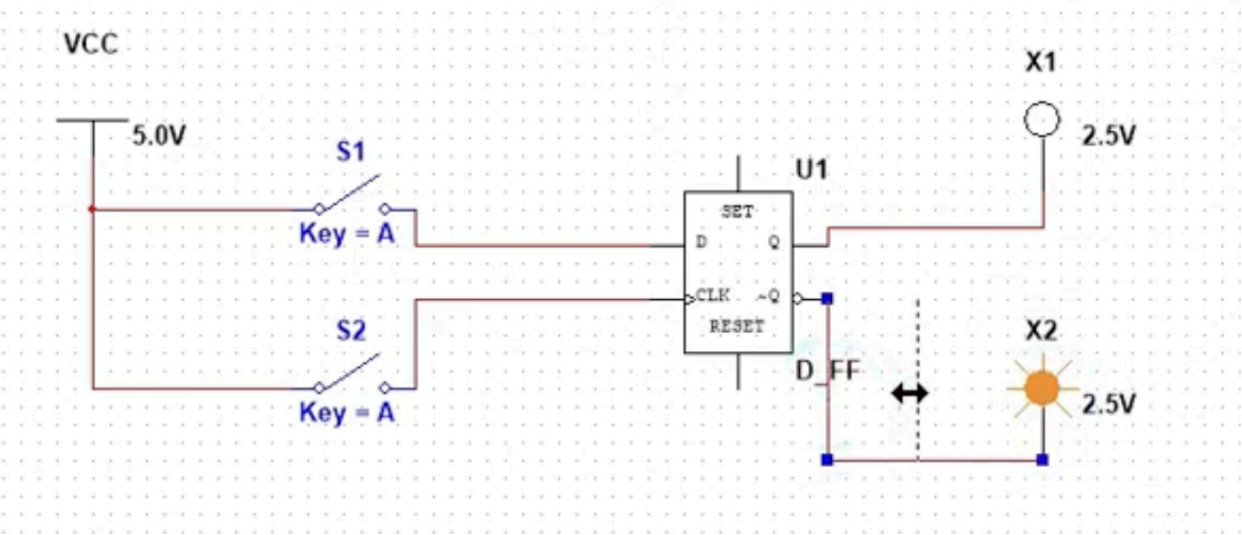


Figure 1-15 Circuit diagram

- **Start** the simulation
- Vary the input and observe the probes

1-5 What happens when the input is high?

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1-6 What happens when the input is low?

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1-7 How is this different than the other flip-flops?

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- **Stop** the simulation when you are done