



AROR UNIVERSITY  
OF ART, ARCHITECTURE,  
DESIGN & HERITAGE,  
SUKKUR, SINDH

## Faculty of Artificial Intelligence & Multimedia Gamming

BS – Artificial Intelligence (Section A)

Digital Logic Design Lab

### Lab # 02: NAND, NOR, XOR, and XNOR Gate

Instructor: Abdul Ghafoor

#### Submission Profile

Name:

Submission date (dd/mm/yy):

Marks obtained:

Comments:

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Instructor

## Lab Learning Objectives:

Upon successful completion of this experiment, the student will be able:

- To explore the function of various different logic gates
- To create circuits with varying logic gates in theory and in practice

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Platform: NI ELVIS III

- ✓ View User Manual:

<http://www.ni.com/en-us/support/manual.ni-elvis-iii.html>

- ✓ View Tutorials:

[https://www.youtube.com/playlist?list=PLvcPIuVaUMIWm8ziaSxv0gwts\\_hBA2dh\\_M](https://www.youtube.com/playlist?list=PLvcPIuVaUMIWm8ziaSxv0gwts_hBA2dh_M)

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Hardware: Digilent Digital Electronics Board for NI ELVIS III

- ✓ View NI DSDB Board Manual:

[http://www.ni.com/pdf/manuals/376\\_627b.pdf](http://www.ni.com/pdf/manuals/376_627b.pdf)

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Software: NI Multisim 14.0.1 Education Version or newer

- ✓ Install Multisim:

[http://www.ni.com/gate/gb/GB\\_AC\\_ADEMICEVALMULTISIM/US](http://www.ni.com/gate/gb/GB_AC_ADEMICEVALMULTISIM/US)

- ✓ View Help:

<http://www.ni.com/multisim/technical-resources/>

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Software: NI LabVIEW FPGA Vivado 2014.4

- ✓ Install:

<http://www.ni.com/download/labview-fpga-module-2015-sp1/5920/en/>

**Note:** Digilent Driver (The installer above automatically downloads the installer below onto your computer)

- ✓ Navigate to:

C:\NIFPGA\programs\Vivado2014\_4\data\xicom\cable\_drivers\nt64\digilent

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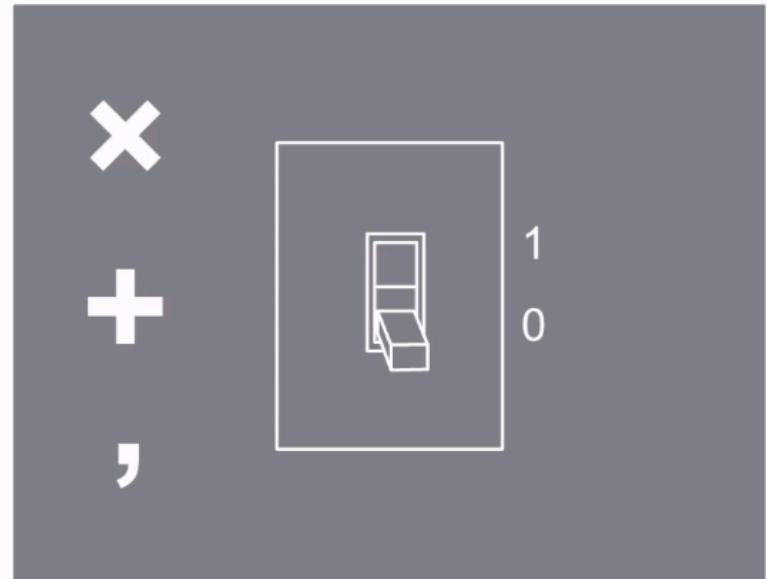
✓ Install: install\_digilent.exe

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### Lab Hardware and Software Required:

### Background Theory:

## Boolean Algebra



The diagram shows a dark gray square containing three white symbols: a multiplication sign (×), a plus sign (+), and a comma (,). To the right of the square is a white rectangle containing a logic gate symbol (an AND gate) and two vertical numbers: 1 at the top and 0 at the bottom.

Algebraic System

- Two value system
- ON and OFF

Creates Equations

- Multiplication
- Addition
- Complement

Figure 1-1 Video. View the video here: <https://youtu.be/IwnztS6et0w>



### Video Summary

- NAND, NOR, XOR, and XNOR gates have at least two inputs, one output, and a unique truth table
- NOT gate output is the inverse of the input

### List of Logic Gate ICs

The [7400 series](#) has several ICs for basic logic gates in TTL family.

| IC No. | Gate               |
|--------|--------------------|
| 7400   | NAND               |
| 7402   | NOR                |
| 7404   | NOT                |
| 7408   | AND                |
| 7432   | OR                 |
| 7486   | EX-OR              |
| 4077   | XNOT (CMOS family) |

## Inverters

- Inverters are also known as *NOT* gates.
- They have only one input and one output.
- The truth table for an inverter is simple. The output is always the *opposite* of the input.
- For example, if the input is 1, the output will be 0 and vice versa. Visually this is depicted by a circle at the input and/or output ends of the logic gates.
- In this situation, the circle is at the output, which means that the output is inverted. If it was at the input, then it is the input that would be inverted.
- Circuits with more than one input can use NAND or NOR logic gates which we will explore next.

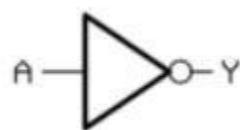


Figure 1-2 Inverter

## NAND Logic Gates

- *NAND* gates invert the output of the AND gate.
- The inputs do not change from those of the AND truth table, but the output is the opposite.
- As a rule, if any of the inputs are 0, the output will always be 1.
- See below for the truth table and the symbol.

| A | B | O |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |



Figure 1-3 NAND gate truth table and symbol

## NOR Logic Gates

- The *NOR* logic gate inverts the output of the OR gate.
- The inputs of the truth table for the OR gate do not change, but the output is the opposite.
- As a rule, if any of the inputs are 1, the output will always be 0.
- See below for the truth table and symbol.

| A | B | O |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

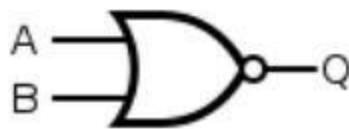


Figure 1-4 NOR gate truth table and symbol

### XOR Logic Gates

- An XOR gate is also known as an exclusive OR gate.
- The output will be 1 if only one of the inputs is 1. The output will be 0 if both inputs are 0 or both are 1.
- See below for the truth table and symbol.

| A | B | O |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |



Figure 1-5 XOR gate truth table and symbol

## XNOR Logic Gates

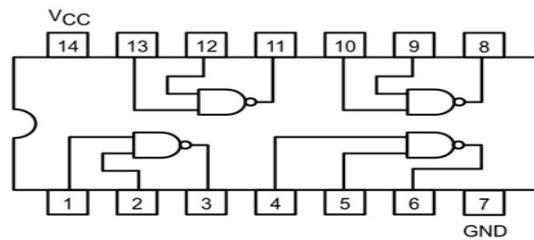
- The *XNOR* gate does the opposite of the XOR gate.
- The output will be 1 if the inputs are the same and the output will be 0 if the inputs are not the same.
- See below for the truth table.

| A | B | O |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

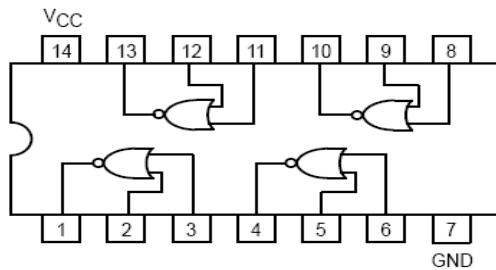
Figure 1-6 XNOR gate truth table

Exercise 1: Implementation of following ICs' on NI Elvis kit using Digital Reader and Digital Writer

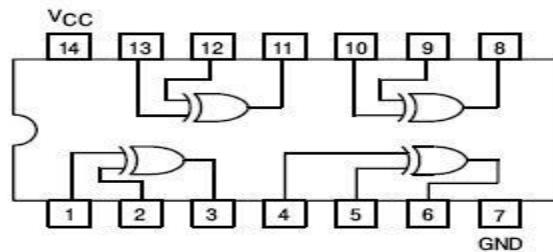
74LS00 2-input NAND gate IC:



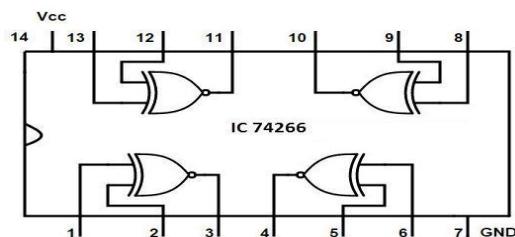
74LS02 2-Input NOR Gate IC:



### 74LS86 2-Input XOR Gate IC:



### 74LS266 2-Input XNOR Gate IC:



## Exercise 2: Building an XOR Logic Gate in Multisim

### XOR Gate Circuit

Build the following circuit using an XOR gate:

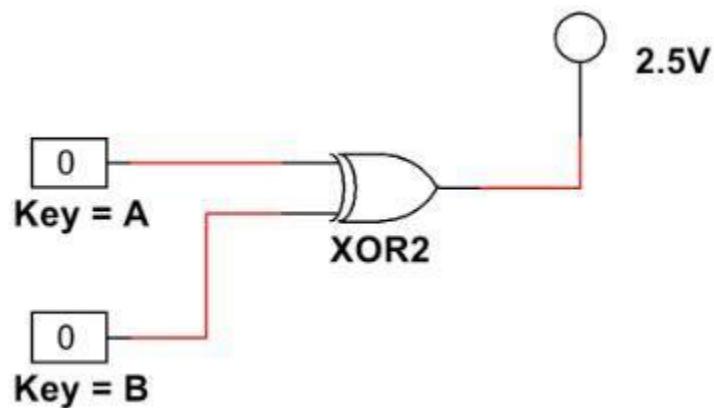


Figure 1-18 XOR gate circuit

Configure the Digital Constants:

- Double-click the top **Digital Constant**.
- In the window that appears, select ‘A’ from the Key for toggle dropdown.
- Change the second constant to toggle with the ‘B’ key.
- Click the **Run** to begin simulating the circuit.



Figure 1-19 Run button

- Press the ‘A’ key on the keyboard to change the value of that input to **1**.

2-1 Does the probe turn on?

- A. Yes
- B. No

- Press the ‘A’ key again to change the top input back to **0**.
- Press the ‘B’ key to change the second input to **1**.

2-2 Does the probe turn on?

- A. Yes
- B. No

- Press the ‘A’ key, so that both inputs are equal to **1**.

2-3 Does the probe turn on?

- A. Yes
- B. No

2-4 How would you describe the behavior of this gate?

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- When you're done, stop the simulation by clicking the **Stop** button.



Figure 1-20 Stop button

### Exercise 3: Building a NOR Logic Gate on the Digital Electronics Board

Using the switches, LEDs, and logic gates, create the following circuit:

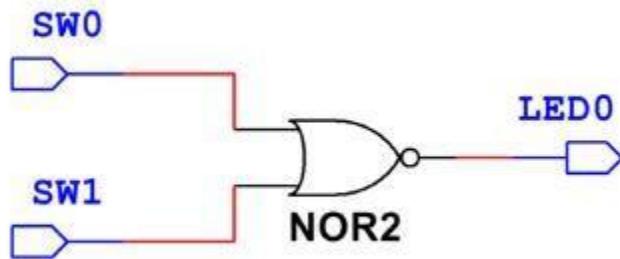


Figure 1-21 PLD design

Configure the Digital Constants:

- Double-click the top **Digital Constant**.
- In the window that appears, select '**A**' from the Key for toggle dropdown.
- Change the second constant to toggle with the '**B**' key.
- Click the **Run** to begin simulating the circuit.



Figure 1-22 Run button

- Press the '**A**' key on the keyboard to change the value of that input to **1**.

3-1 Does the probe turn on?

- C. Yes
- D. No

- Press the '**A**' key again to change the top input back to **0**.

- Press the 'B' key to change the second input to 1.

3-2 Does the probe turn on?

- C. Yes
- D. No

- Press the 'A' key, so that both inputs are equal to 1.

3-3 Does the probe turn on?

- C. Yes
- D. No

3-4 How would you describe the behavior of this gate?

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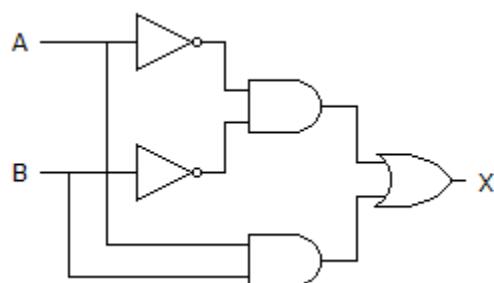
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- When you're done, stop the simulation by clicking the **Stop** button.



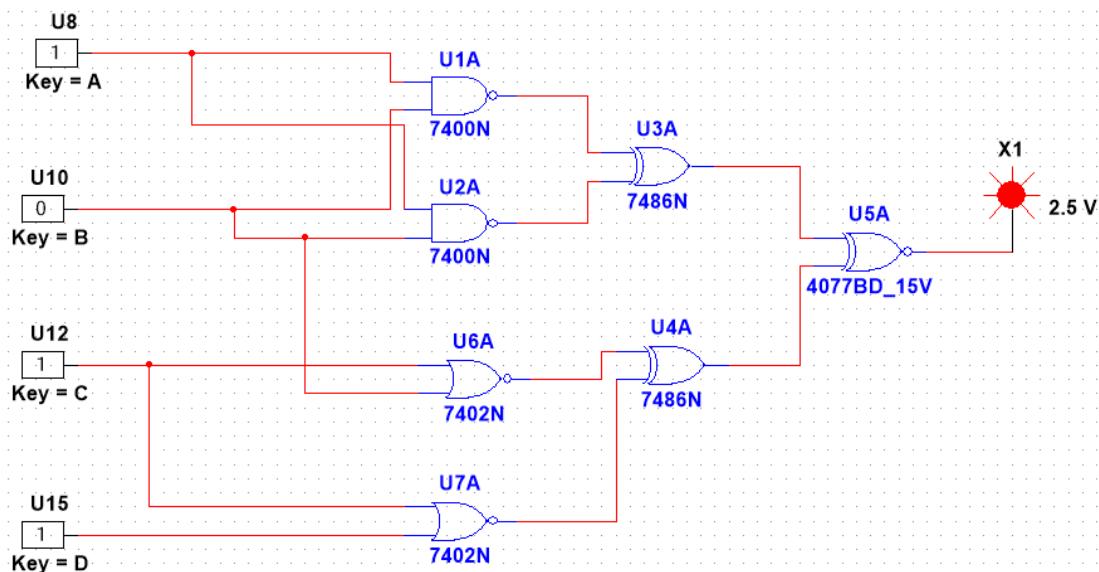
Figure 1-23 Stop button

**Exercise 4:** Design the following circuit on multisim and show the results with truth table.



| A | B | Output |
|---|---|--------|
| 0 | 0 |        |
| 0 | 1 |        |
| 1 | 1 |        |
| 1 | 0 |        |

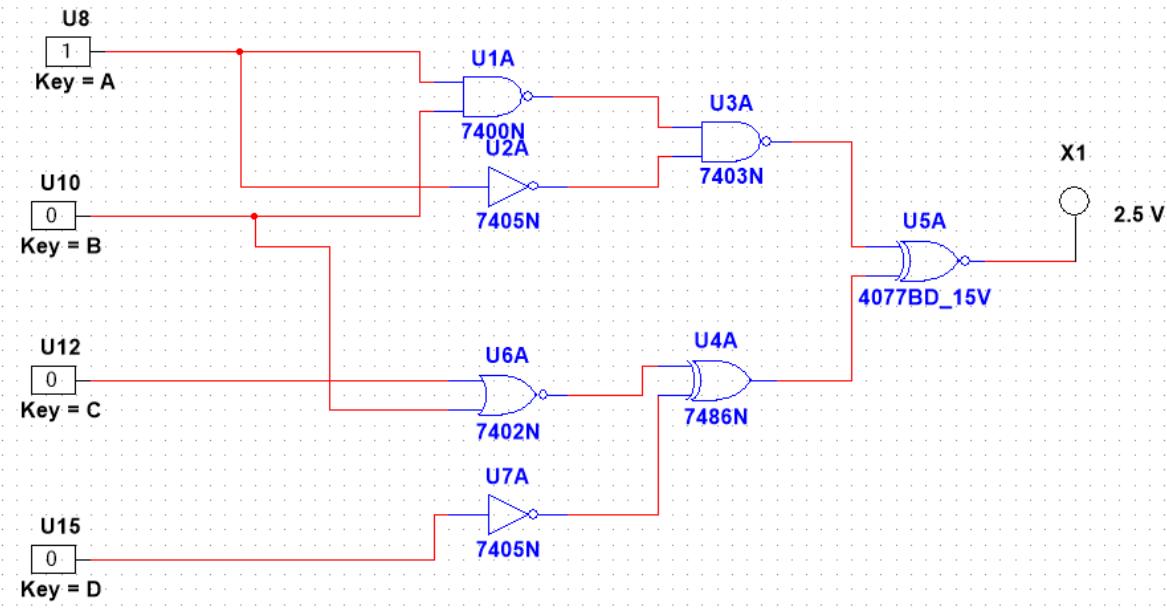
Exercise 5: Design the following circuit on multisim and show the results with truth table.



| A | B | C | D | Output |
|---|---|---|---|--------|
| 0 | 0 | 0 | 1 |        |
| 0 | 0 | 0 | 1 |        |
| 0 | 1 | 0 | 1 |        |
| 0 | 1 | 0 | 1 |        |
| 1 | 0 | 1 | 0 |        |

|   |   |   |   |  |
|---|---|---|---|--|
| 1 | 0 | 1 | 0 |  |
| 1 | 1 | 1 | 0 |  |
| 1 | 1 | 1 | 0 |  |

Exercise 6: Design the following circuit on multisim and show the results with truth table.



| A | B | C | D | Output |
|---|---|---|---|--------|
| 0 | 0 | 0 | 1 |        |
| 0 | 0 | 0 | 1 |        |
| 0 | 1 | 0 | 1 |        |
| 0 | 1 | 0 | 1 |        |
| 1 | 0 | 1 | 0 |        |
| 1 | 0 | 1 | 0 |        |
| 1 | 1 | 1 | 0 |        |
| 1 | 1 | 1 | 0 |        |