# CMOS

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Introduction and physical properties

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## 1- Cell Description

This cell consists of a CMOS inverter. They are extremely common and one of the most used circuity. Cmos inverters are used in every digital device that exists. It takes whatever the input may be ,and it inverts it. For example, if the input is a logic 1, the inverter will take that input and transform it into a logic 0.

## 2- Cell Symbols

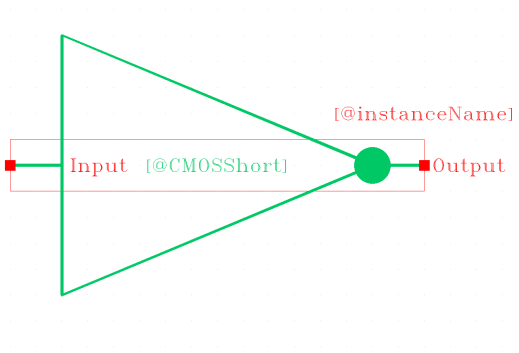


*Figure 1: CMOS inverter (normal)*

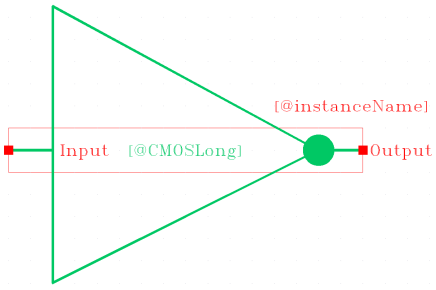


*Figure 2: CMOS inverter (long)*

### 3- Cell Truth Table (for both cmos inverters)

| Cell input | Cell output |
|---|---|
| **A** | **Y** |
| **0** | **1** |
| **1** | **0** |

### 4- Cell schematic

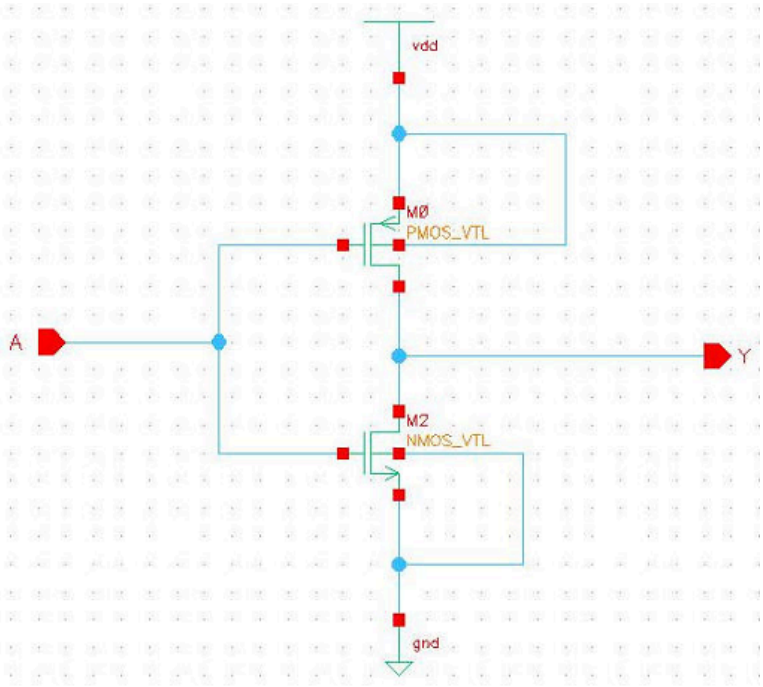


*Figure 3: CMOS inverter (short)*

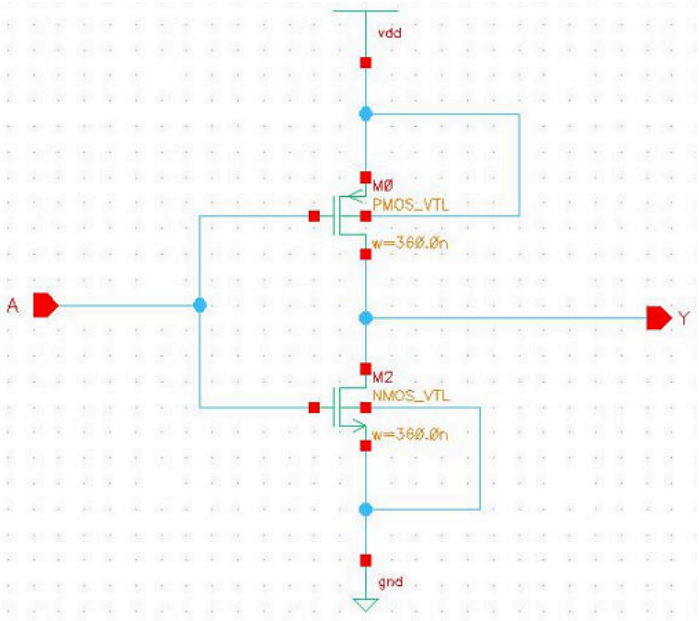


*Figure 4: CMOS inverter (long)*

**5- Cell Dimensions**

**CMOS**

| transistor instance number | Width (nm) | Length (nm) |
|---|---|---|
| PMOS (M0) | 90 | 50 |
| NMOS (M2) | 90 | 50 |

**CMOS Long**

| transistor instance number | Width (nm) | Length (nm) |
|---|---|---|
| PMOS(M0) | 360 | 50 |
| NMOS(M2) | 360 | 50 |

**6- Input X: output rise time data**

**CMOS**

| Input rise/fall time (ps) | FO0 | FO1 | FO2 | FO4 | FO8 |
|---|---|---|---|---|---|
| 40 | —----- | —---- | —----- | 391.1 | —------ |

**CMOS Long**

| Input rise/fall time (ps) | FO0 | FO1 | FO2 | FO4 | FO8 |
|---|---|---|---|---|---|
| 40 | —----- | —---- | —----- | 94.56 | —------ |

**7- Input X: output fall time data**

**CMOS**

| Input rise/fall time (ps) | FO0 | FO1 | FO2 | FO4 | FO8 |
|---|---|---|---|---|---|
| 40 | —----- | —---- | —----- | 116.6 | —------ |

**CMOS Long**

| Input rise/fall time (ps) | FO0 | FO1 | FO2 | FO4 | FO8 |
|---|---|---|---|---|---|
| 40 | —----- | —---- | —----- | 32.14 | —------ |

**8- Data worst case Low to High propagation delay $t_{plh}$**

**CMOS**

| Input rise/fall time (ps) | FO0 | FO1 | FO2 | FO4 | FO8 |
|---|---|---|---|---|---|
| 40 | —----- | —---- | —----- | 275.404 | —------ |

**CMOS Long**

| Input rise/fall time (ps) | FO0 | FO1 | FO2 | FO4 | FO8 |
|---|---|---|---|---|---|
| 40 | —----- | —---- | —----- | 75.756 | —------ |

**9- Data worst case High to Low propagation delay $t_{phl}$**

**CMOS**

| Input rise/fall time (ps) | FO0 | FO1 | FO2 | FO4 | FO8 |
|---|---|---|---|---|---|
| 40 | —----- | —---- | —----- | 96.995 | —------ |

**CMOS Long**

| Input rise/fall time (ps) | FO0 | FO1 | FO2 | FO4 | FO8 |
|---|---|---|---|---|---|
| 40 | —----- | —---- | —----- | 31.985 | —------ |

## 10- Transient analysis

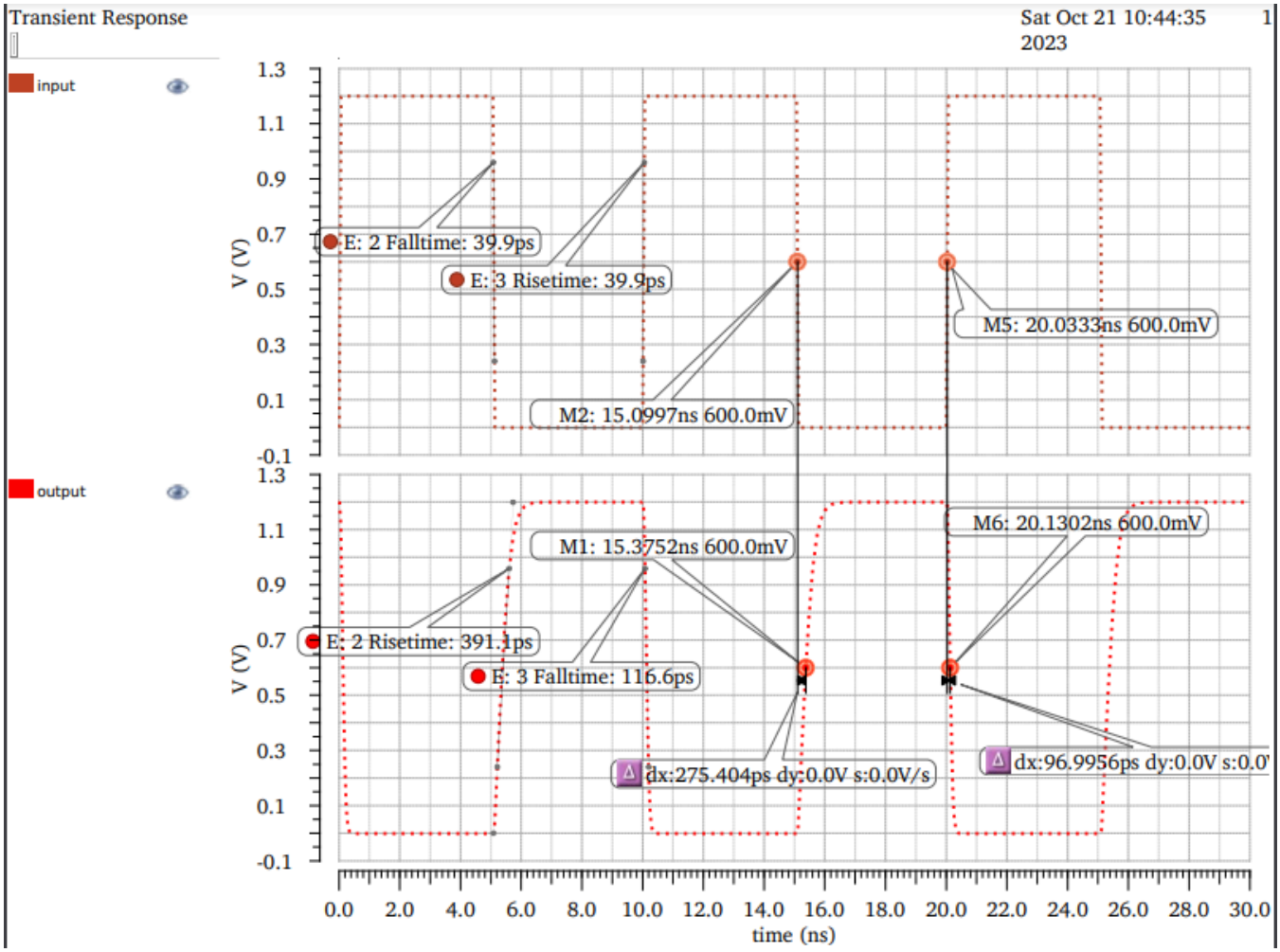


*Figure 5: Transient analysis on the normal CMOS circuitry*

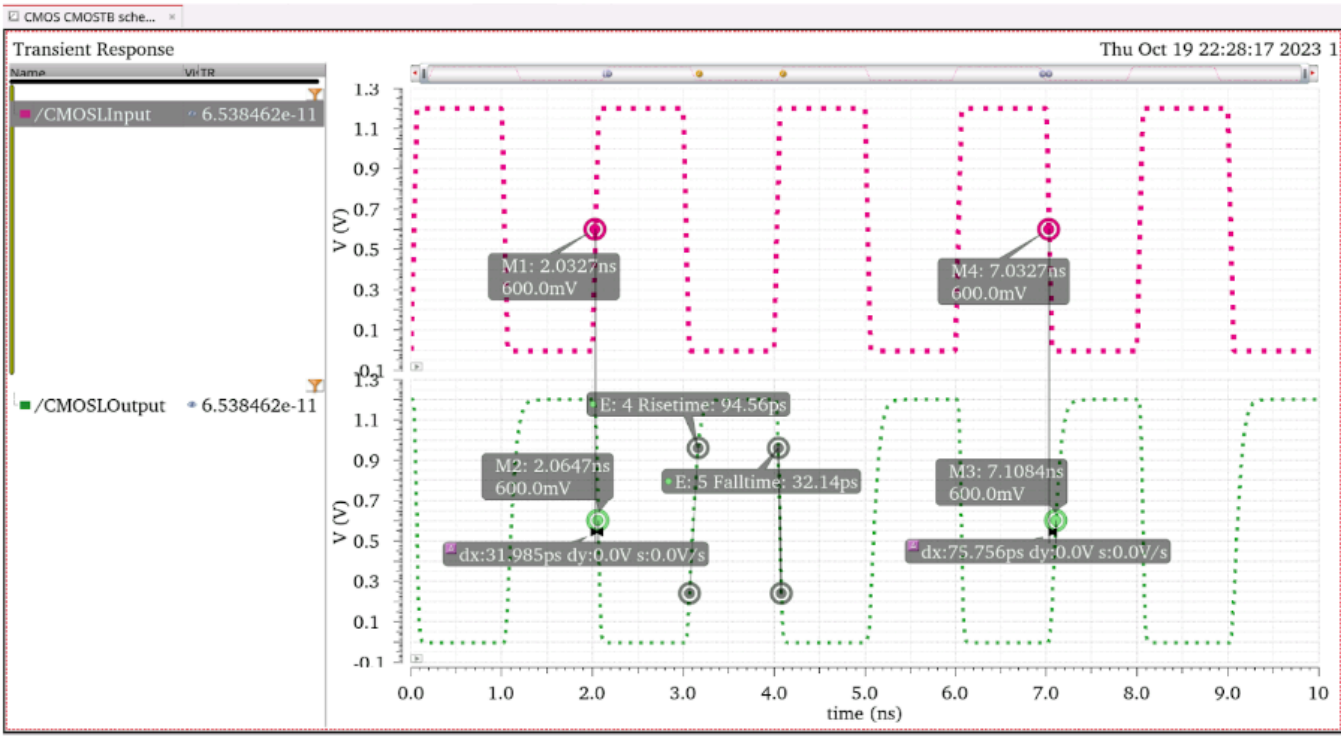


*Figure 6: Transient analysis on the CMOS Long circuitry*

**Table 1: Transient analysis table**

| TYPE | $t_{plh}$ (ps) | $t_{phl}$ (ps) | $t_r$ (ps) | $t_f$ (ps) |
|---|---|---|---|---|
| CMOS | 275.404 | 96.995 | 391.1 | 116.6 |
| CMOS_LONG | 75.756 | 31.985 | 94.56 | 32.14 |
| Enhancement mode NFET | 323.892 | 72.1549 | 1560 | 74.74 |
| Enhancement mode NFET Long | 1034.43 | 62.3649 | 4724 | 77.4 |
| Resistive load | 590.613 | 100.105 | 880.5 | 118.2 |
| Resistive load Long | 2082.7 | 90.7394 | 2925 | 105.8 |

## 11- DC analysis

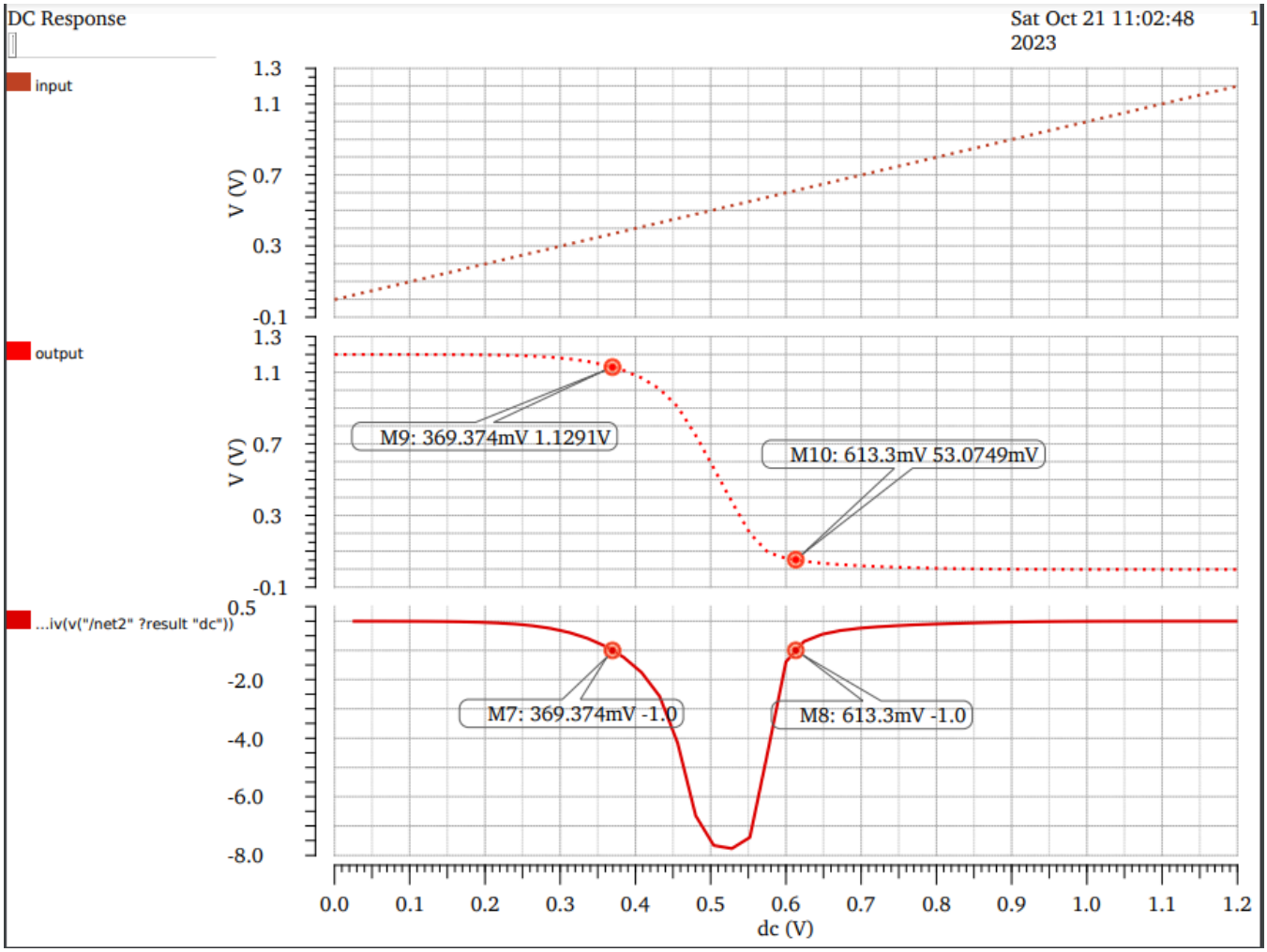


*Figure 7: DC analysis on the normal CMOS circuitry*

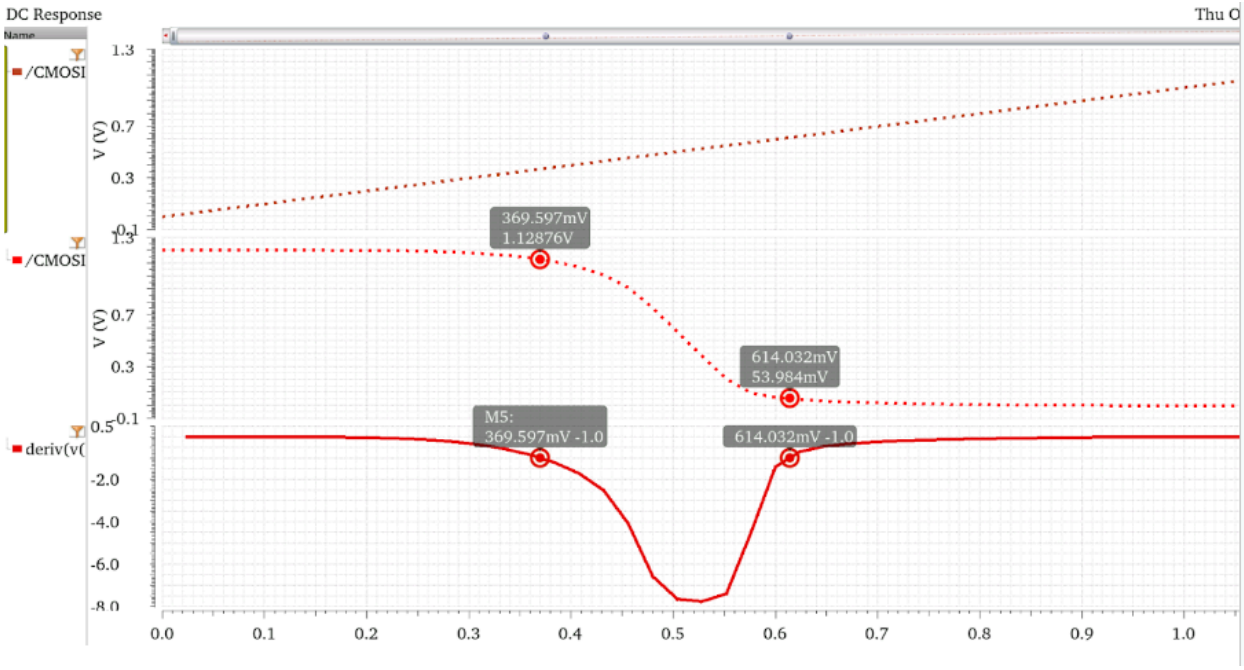


*Figure 8: DC analysis on the CMOS Long circuitry*

*Table 2: DC Analysis table*

| TYPE | $V_{IH\_DC}$ (mV) | $V_{IL\_DC}$ (mV) | $V_{OH\_DC}$ (mV) | $V_{OL\_DC}$ (mV) |
|---|---|---|---|---|
| CMOS | 613.3 | 369.374 | 1129.1 | 53.0749 |
| CMOS_LONG | 614.032 | 369.597 | 1128.76 | 53.984 |
| Enhancement mode NFET | 344.75 | 624.697 | 508.485 | 117.365 |
| Enhancement mode NFET Long | 270.272 | 550.588 | 528.809 | 66.047 |
| Resistive load | 677.123 | 307.049 | 1126.49 | 115.919 |
| Resistive load Long | 558.172 | 239.854 | 1132.73 | 56.047 |