Enhancement

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Introduction and physical properties

1- Cell Description

This cell consists of a NMOS and pull up resistor as a load bearing component, vs a typical Enhancement inverter. These resistive load inverters may be used in place of enhancement inverters for various reasons, including but not limited too:

- Simplicity of technology
- Higher output voltage when compared to enhancement
- Availability with older technologies

2- Cell Symbols

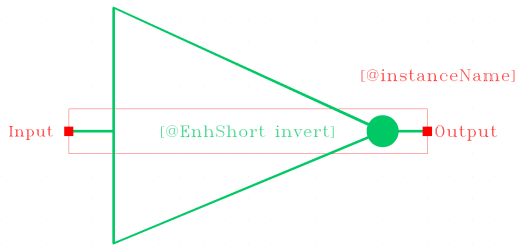

Figure 1: Enhancement inverter (Short)

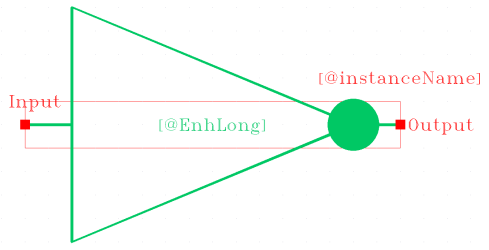

Figure 2: Enhancement inverter (long)

3- Cell Truth Table (for both enhancement inverters)

Cell input	Cell output
A	**Y**
0	**1**
1	**0**

4- Cell schematic

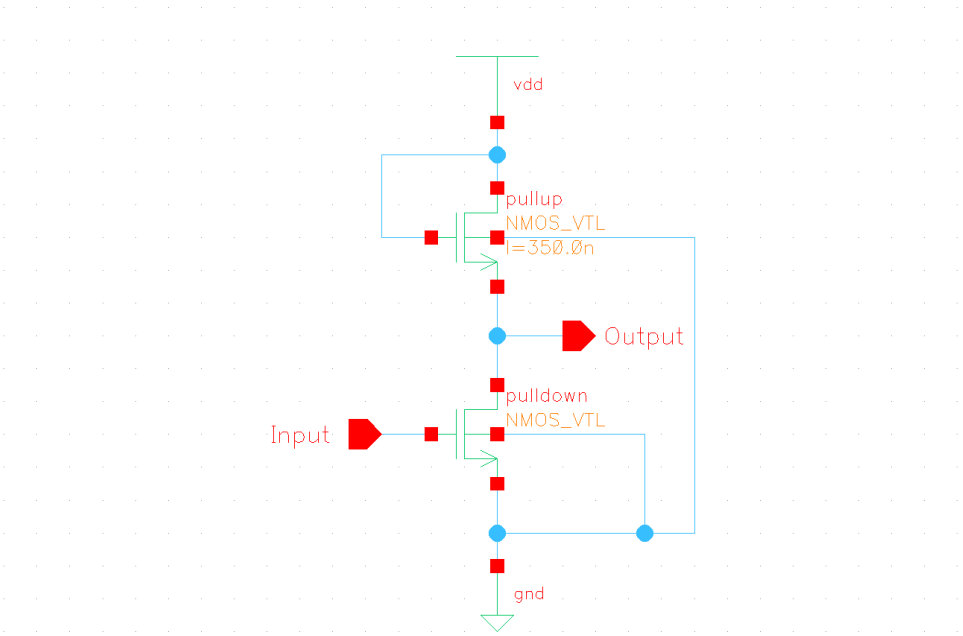

Figure 3: Enhancement inverter (short)

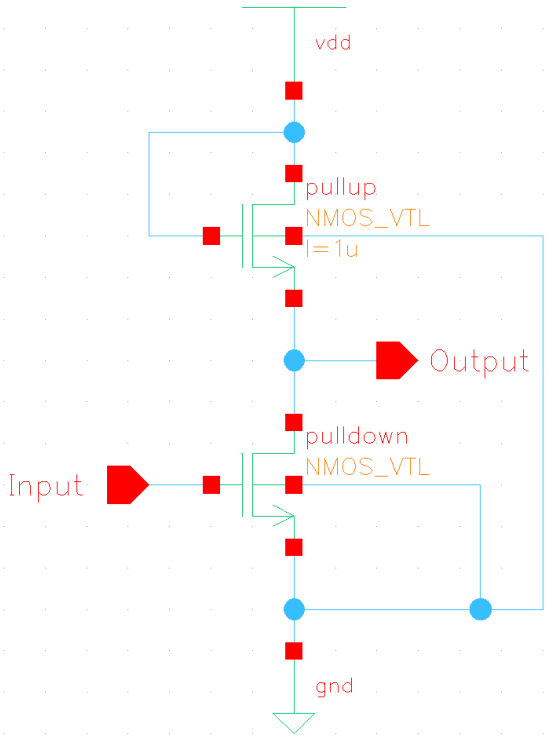

Figure 4: Enhancement inverter (long length l=1u)

5- Cell Dimensions

Enhancement

transistor instance number	Width (nm)	Length (nm)
NMOS (Pullup)	90	350
NMOS (pulldown)	90	50

Enhancement Long

transistor instance number	Width (nm)	Length (nm)
NMOS (Pullup)	90	1000
NMOS (pulldown)	90	50

6- Input X: output rise time data

Enhancement

Input rise/fall time (ps)	FO0	FO1	FO2	FO4	FO8
40	—-----	—----	—-----	1560	—------

Enhancement Long

Input rise/fall time (ps)	FO0	FO1	FO2	FO4	FO8
40	—-----	—----	—-----	4724	—------

7- Input X: output fall time data

Enhancement

Input rise/fall time (ps)	FO0	FO1	FO2	FO4	FO8
40	—-----	—----	—-----	74.74	—------

Enhancement Long

Input rise/fall time (ps)	FO0	FO1	FO2	FO4	FO8
40	—-----	—----	—-----	77.4	—------

8- Data worst case Low to High propagation delay t_{plh}

Enhancement

Input rise/fall time (ps)	FO0	FO1	FO2	FO4	FO8
40	—-----	—----	—-----	323.892	—------

Enhancement Long

Input rise/fall time (ps)	FO0	FO1	FO2	FO4	FO8
40	—-----	—----	—-----	1034.43	—------

9- Data worst case High to Low propagation delay t_{phl}

Enhancement

Input rise/fall time (ps)	FO0	FO1	FO2	FO4	FO8
40	—-----	—----	—-----	72.1549	—------

Enhancement Long

Input rise/fall time (ps)	FO0	FO1	FO2	FO4	FO8
40	—-----	—----	—-----	62.3649	—------

10- Transient analysis

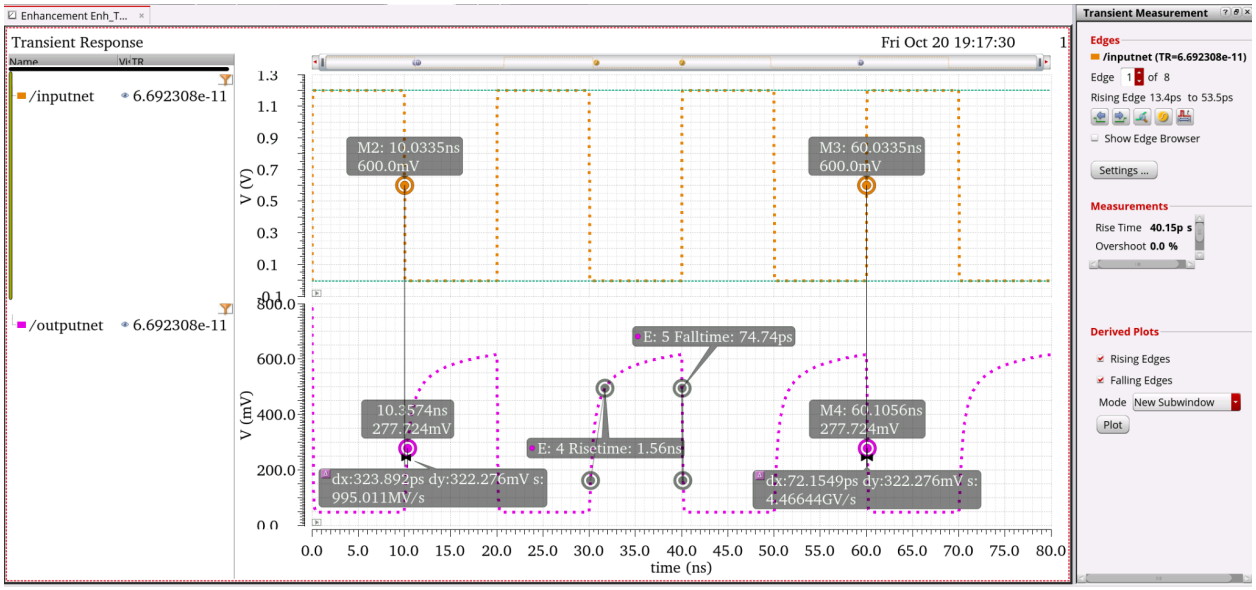

Figure 5: Transient analysis on Enhancement Short circuitry

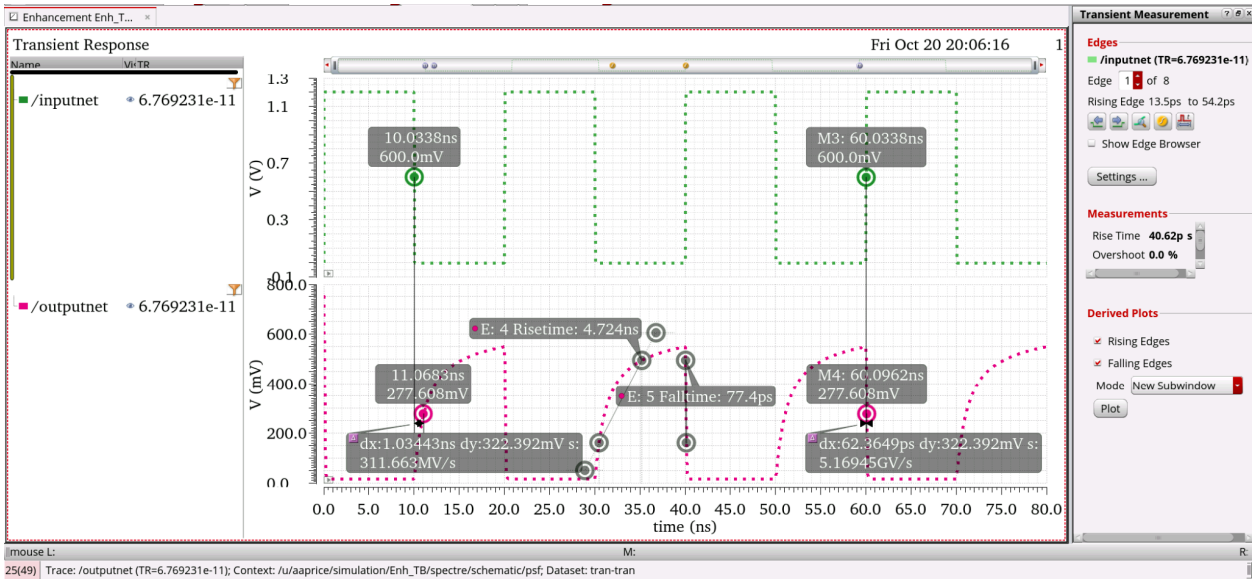

Figure 6: Transient analysis on Enhancement Long circuitry

Table of Transient Analysis

TYPE	t_{plh} (ps)	t_{phl} (ps)	t_r (ps)	t_f (ps)
CMOS	275.404	96.995	391.1	116.6
CMOS_LONG	75.756	31.985	94.56	32.14
Enhancement mode NFET	323.892	72.1549	1560	74.74
Enhancement mode NFET Long	1034.43	62.3649	4724	77.4
Resistive load	590.613	100.105	880.5	118.2
Resistive load Long	2082.7	90.7394	2925	105.8

11- DC analysis

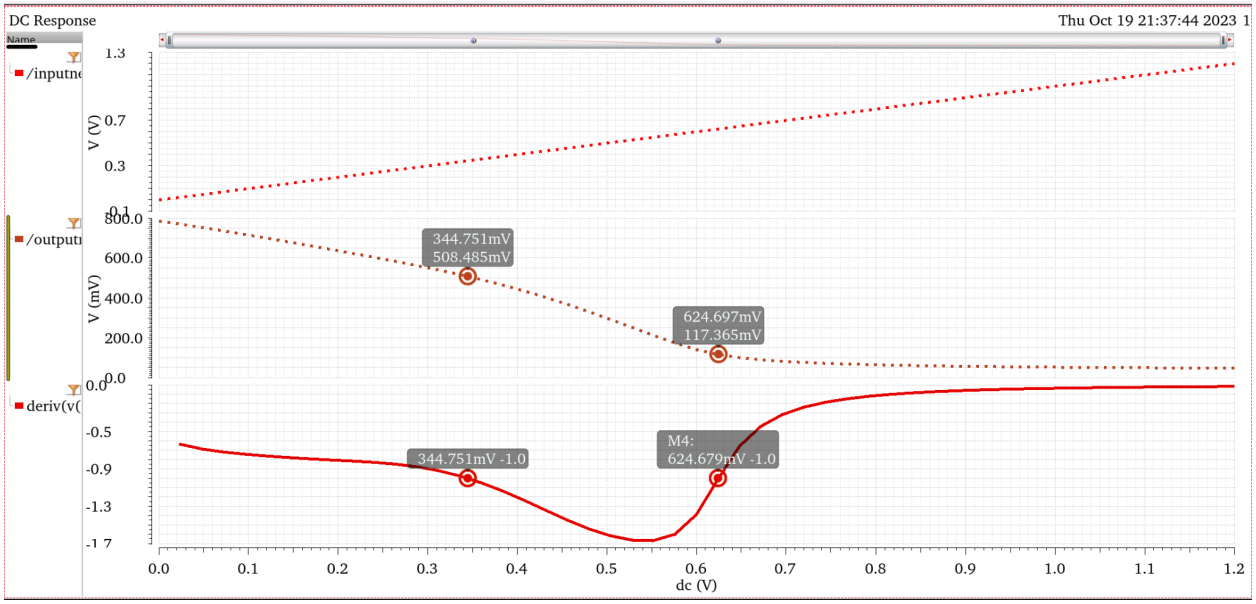

Figure 7: DC analysis on Enhancement Short circuitry

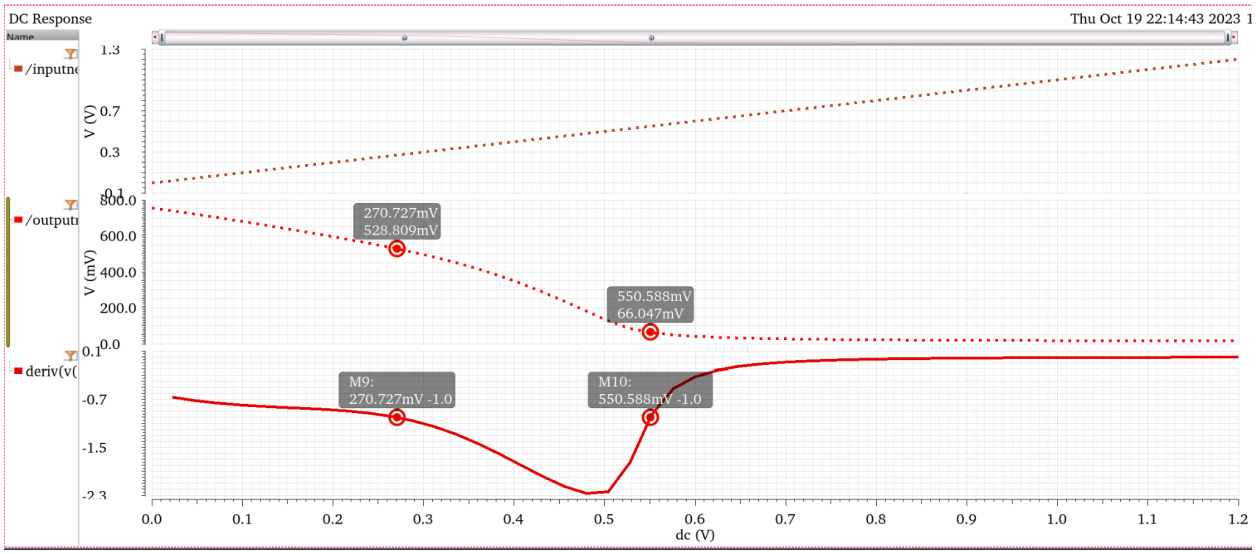

Figure 8: DC analysis on Enhancement Long circuitry

Table of DC Analysis

TYPE	V_{IH_DC} (mV)	V_{IL_DC} (mV)	V_{OH_DC} (mV)	V_{OL_DC} (mV)
CMOS	613.3	369.374	1129.1	53.0749
CMOS_LONG	614.032	369.597	1128.76	53.984
Enhancement mode NFET	344.75	624.697	508.485	117.365
Enhancement mode NFET Long	270.272	550.588	528.809	66.047
Resistive load	677.123	307.049	1126.49	115.919
Resistive load Long	558.172	239.854	1132.73	56.047