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Maseeh College of Engineering and Computer Science
Electrical and Computer Engineering Department
Digital IC Design - ECE 425/525
Fall 2023

2nd Laboratory Assignment

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1. CMOS Inverter

1.1. Cell description

Complementary Metal-Oxide Semiconductor (CMOS) inverter gate primary function is to invert the input signal: a logic high (1) input results in a logic low (0) output and vice versa. The inverter's Boolean function can be represented as:

$$Y = \overline{A} \quad (1)$$

A CMOS inverter is typically constructed using a pair of complementary MOS transistors: a p-channel MOS (PMOS) transistor and an n-channel MOS (NMOS) transistor. The PMOS transistor is connected in series between the power supply (VDD) and the output, with its source connected to VDD and its drain connected to the output node. The NMOS transistor is connected in parallel to the PMOS transistor, with its source connected to the output, drain connected to ground (VSS), and its gate tied to the input signal. When the input signal is low (0), the PMOS transistor turns on, providing a path from Vdd to the output, making it a logic high (1). Conversely, when the input signal is high (1), the NMOS transistor is ON and the PMOS is OFF, which connects the output to GND, making it a logic low (0).

1.2. Cell Symbol

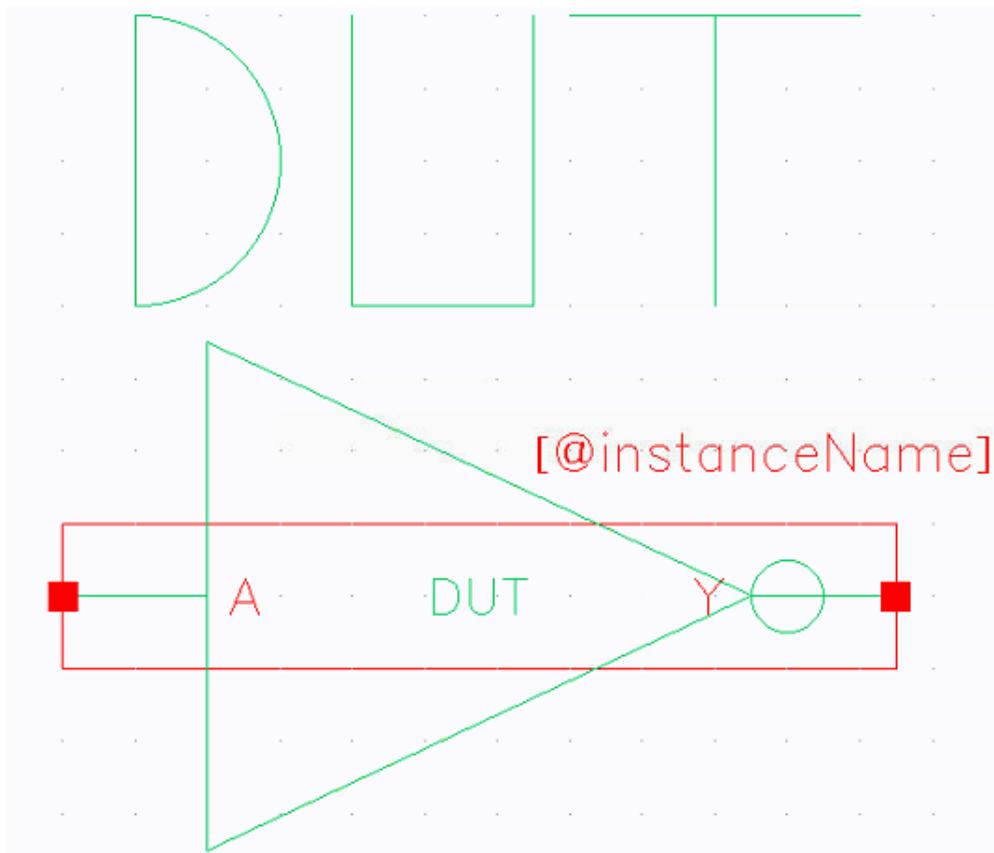


Figure 1: Device under test cell symbol

1.3. Cell Truth Table

Table 1: CMOS Inverter truth table

Cell input	Cell output
A	Y
0	1
1	0

1.4. Schematic diagram (DUT)

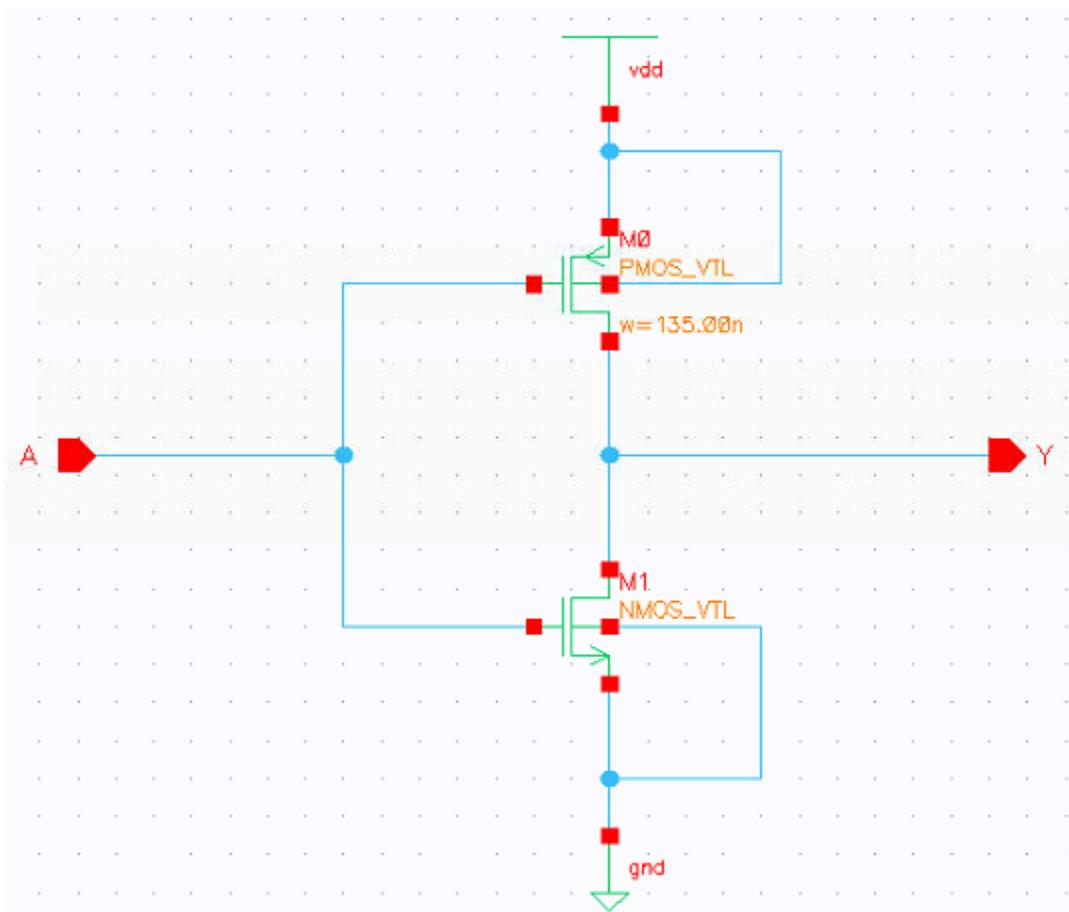


Figure 2: Device under test schematic

1.5. Cell Layout Diagram and Dimensions

1.5.1. Testbenches

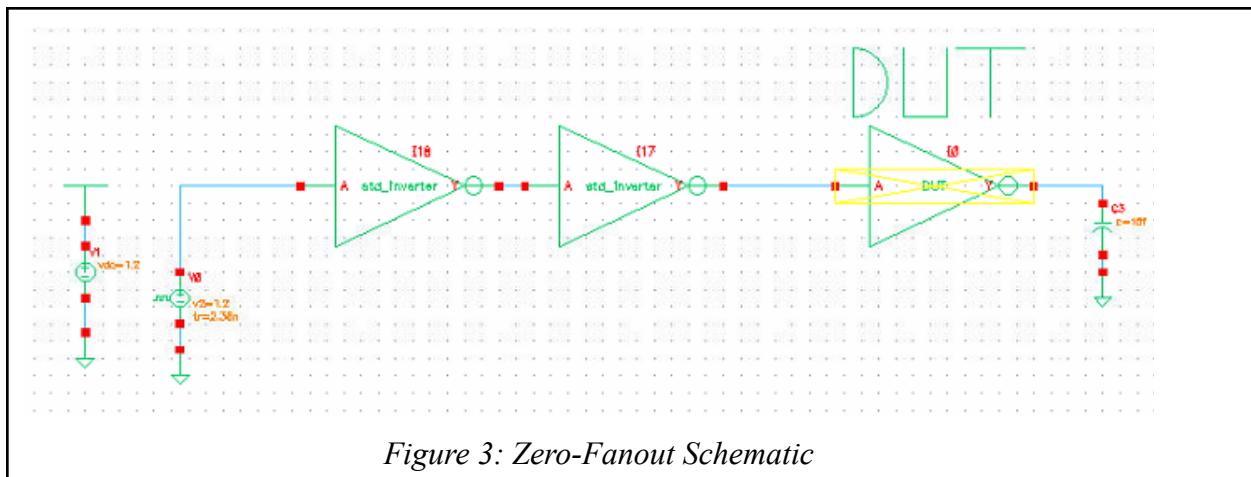


Figure 3: Zero-Fanout Schematic

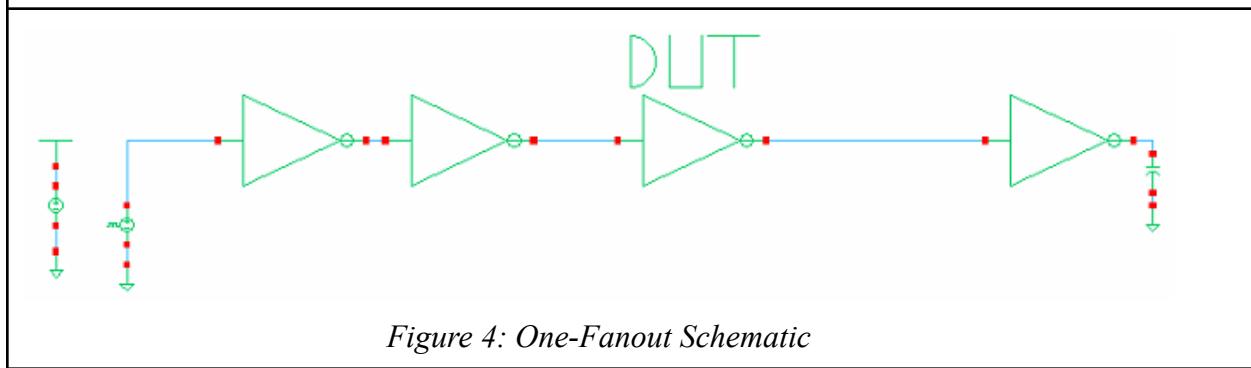


Figure 4: One-Fanout Schematic

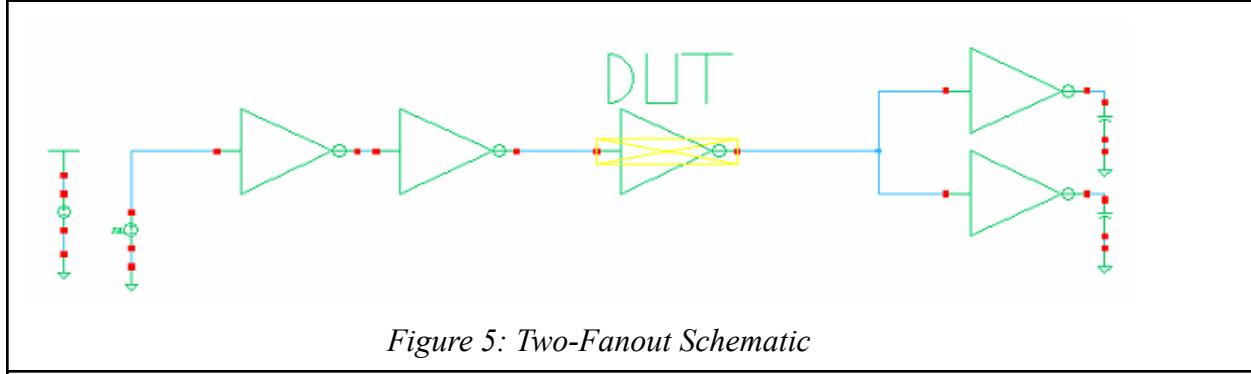


Figure 5: Two-Fanout Schematic

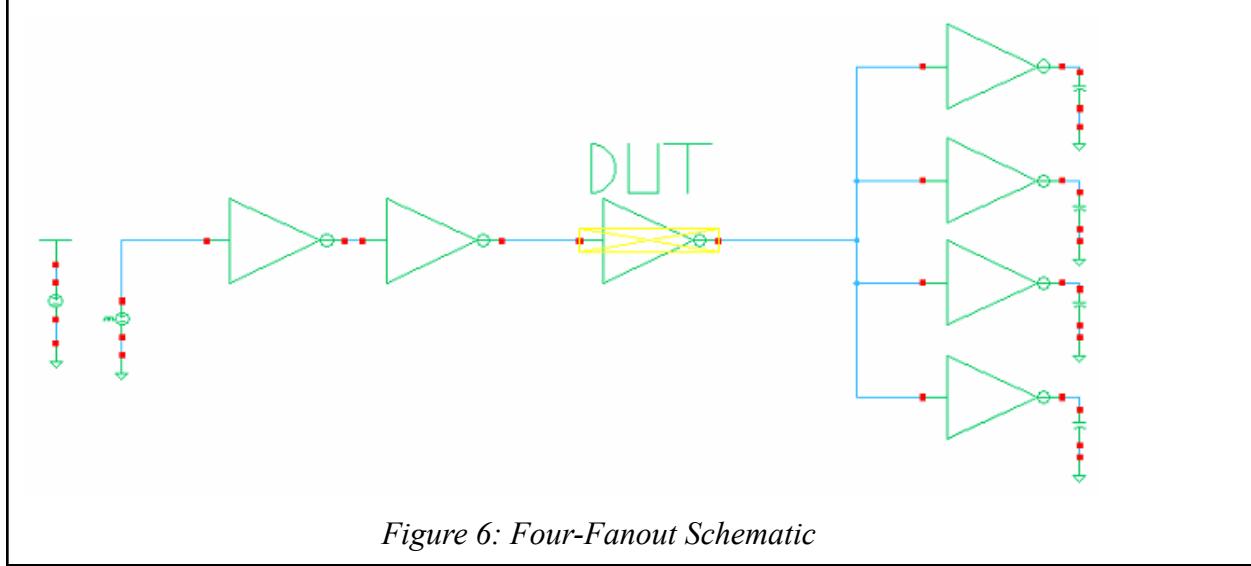
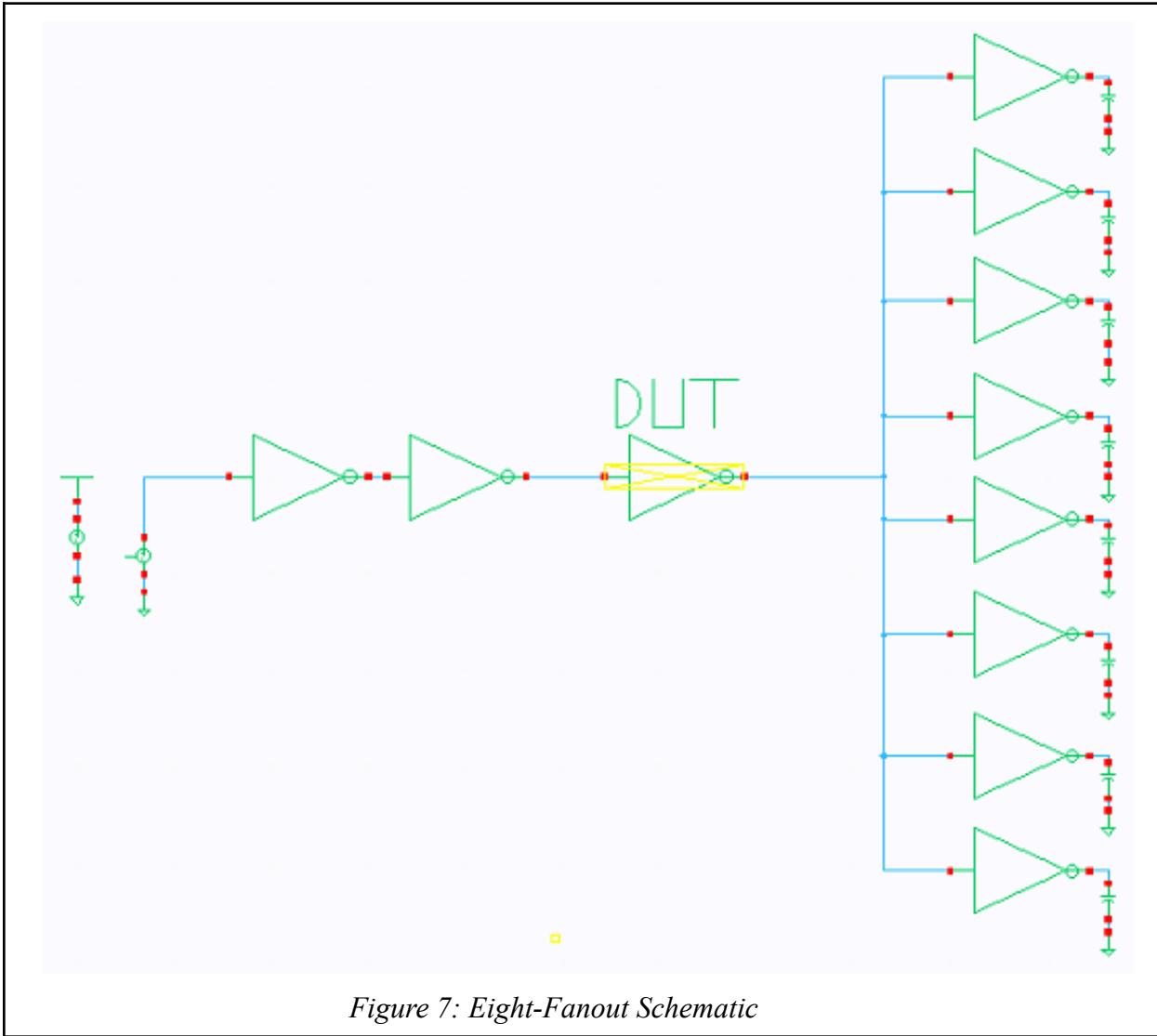


Figure 6: Four-Fanout Schematic



1.5.2. Dimensions

Table 2: CMOS Inverter dimension

Transistor Dimensions		
Transistor Instance Number	Length (nm)	Width (nm)
M1	50	90
M0	50	135

1.6. Performance Analysis

As *Figure 8 to Figure 12* shows, the rise time of Vpulse for the input A (at DUT) was set to 2.38 nanoseconds, yielding input rise times of 50.08. The fall time from VPulse, measured at 2.695 nanoseconds for input A, resulted in an input fall time of 50.11.

1.6.1. Transient Response graphs

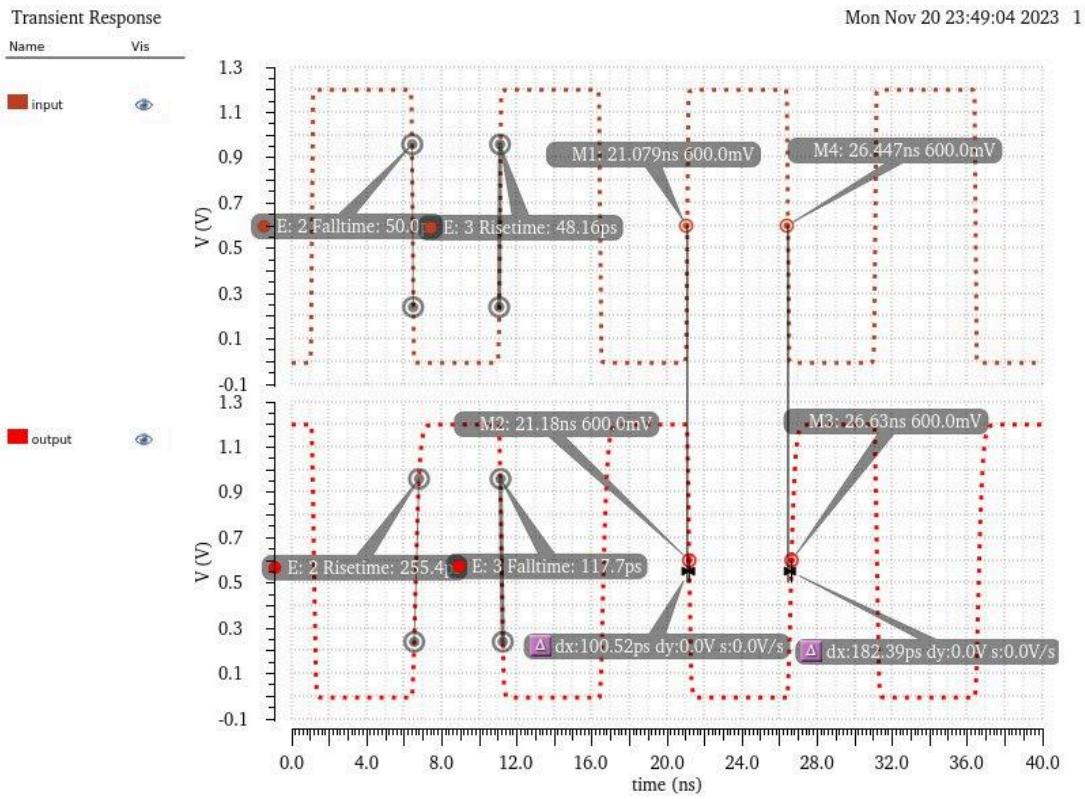


Figure 8: Zero-Fanout transient responses

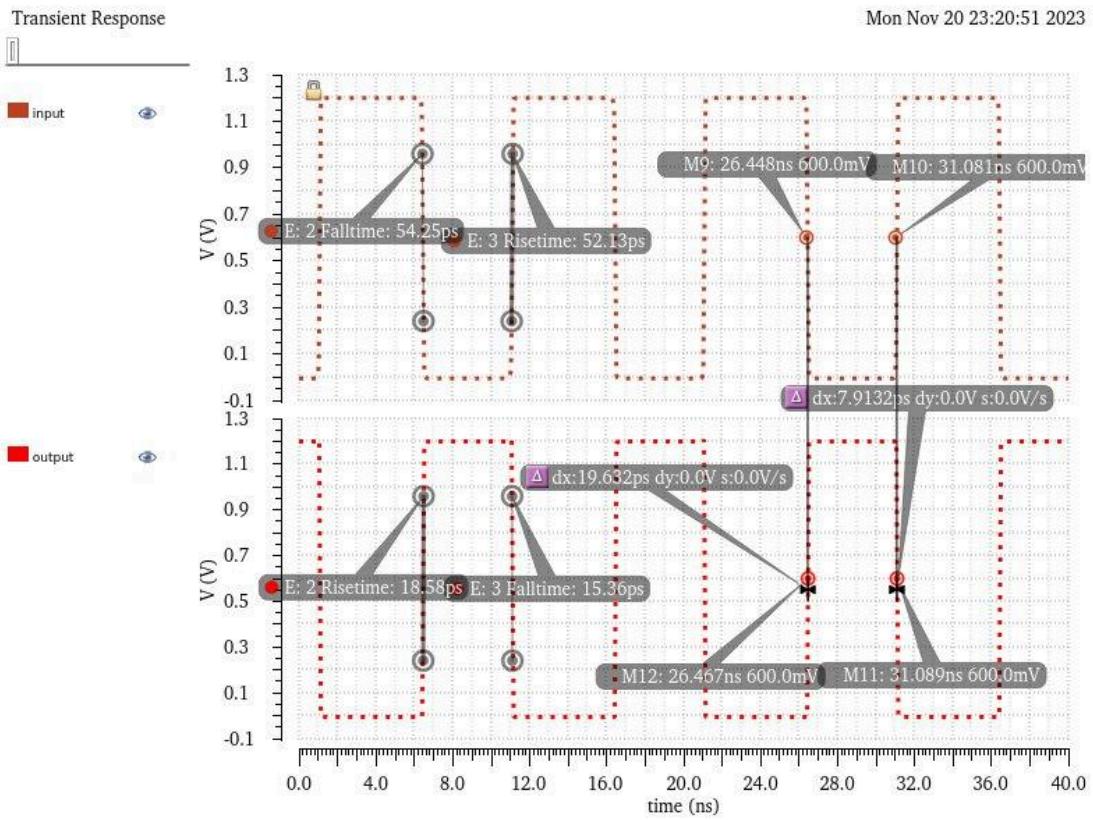


Figure 9: One-Fanout transient responses

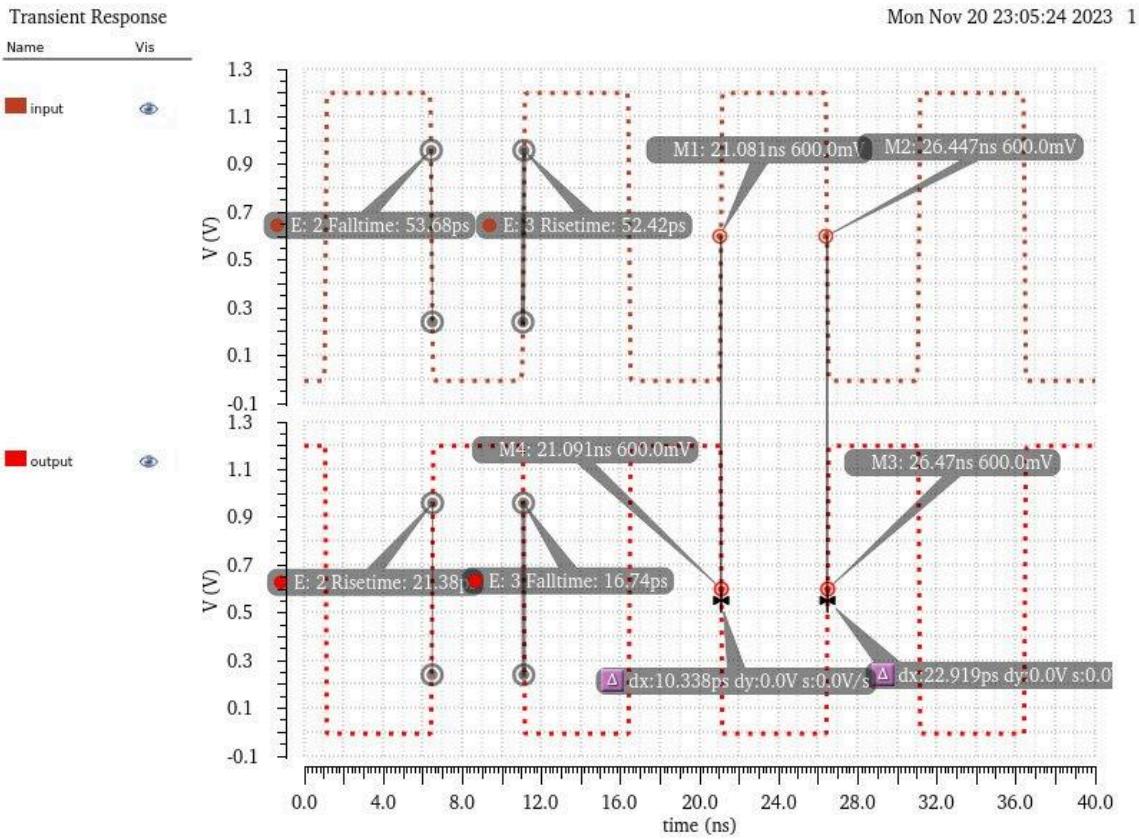


Figure 10: Two-Fanout transient responses

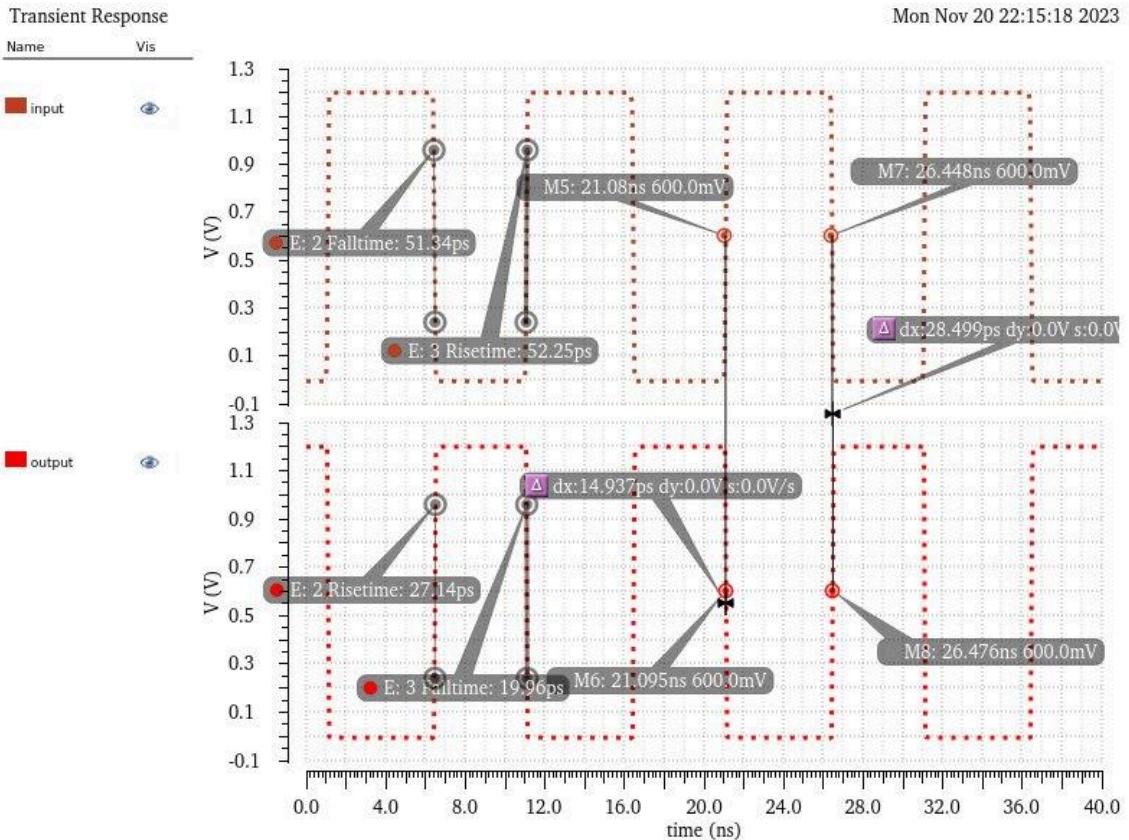


Figure 11: Four-Fanout transient responses

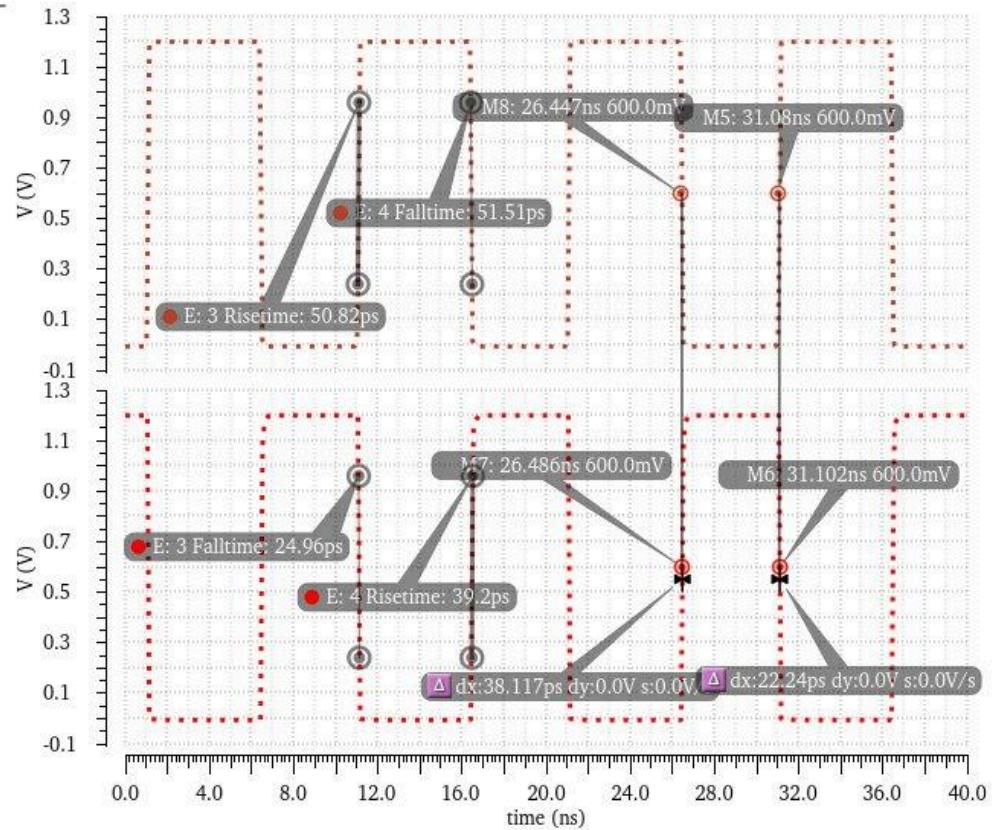


Figure 12: Eight-Fanout transient responses

1.6.2. Rise and Fall Times

Input X: Output Rise Time Data t_r (ps)					
Input rise/fall time (ns)	Output Load (FO _X)				
	0	1	2	4	8
0.05	255.4	18.58	21.38	27.14	39.2

Stack Input Combination: *Replace with Boolean Product*

Stack S, Input X: Output Fall Time Data t_f (ps)					
Input rise/fall time (ns)	Output Load (FO _X)				
	0	1	2	4	8
0.05	177.7	15.36	16.74	19.96	24.96

Stack Input Combination: *Replace with Boolean Product*

1.6.3. Propagation Delays

Table 3: CMOS Inverter dimension Low-to-High propagation

Data Worst Case Low to High Propagation Delay Data t_{ph} (ps)					
Input rise/fall time (ns)	Output Load (FO _X)				
	0	1	2	4	8
0.05	100.52	19.632	22.919	28.499	38.117

Worse Case Input Combination: *Replace with Boolean Product*

Table 4: CMOS Inverter dimension High-to-Low propagation

Input rise/fall time (ns)	Data Worst Case High to Low Propagation Delay Data t_{phl} (ps)				
	Output Load (FOx)				
	0	1	2	4	8
0.05	182.39	7.9132	10.338	14.9379	22.24

Worse Case Input Combination: *Replace with Boolean Product*

1.7. Conclusion

Based on our observation, we were able to detect a very interesting pattern in our data. We found out that Having a fanout of 0 is the worst propagation delay overall. It is very compared to all the other Fanouts. In addition, we also observed that Fanout of 1 is the best case ,because it has the lowest propagation delay overall which includes output rise, fall , t_{phl} and t_{plh} . Furthermore, we also found out that as we increase the fanout load, the propagation delay increases which makes it worse overall. It's very interesting to see that fanout of 1 is way better than fanout of 0. Intuitively, at first, we were expecting to see fanout of 0 to be the best case ,but the data clearly shows that fanout of 1 is MUCH better.

2. Compound CMOS Gate

2.1. Cell description

This section presents the results from the analysis of the rise and fall times for 3 input NAND compound gate, along with Tphl and Tplh timings and the variances between them. Exact VS TR and TF times are simulated, such that the resulting AIn, BIn, and CIn inputs have a slew rate of ~50ps for a FO4 testbench. From this, the PMOS and NMOS transistor widths are adjusted, to keep the TR and TF times from each VPulse input static. From this, Tphl and Tplh and TR and TF are designed within customer specifications. Troubleshooting and design steps taken are described during this process.

2.2. Cell Symbol

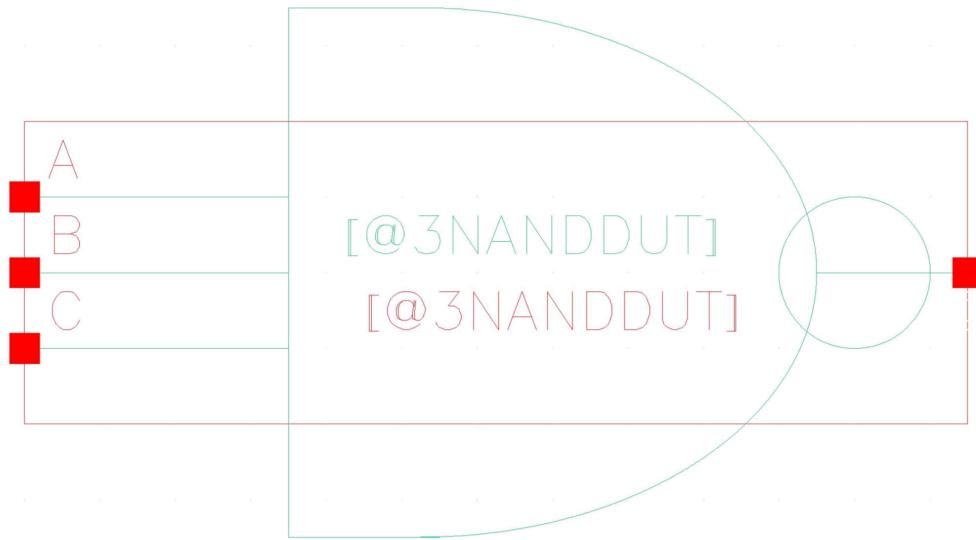


Figure 13: Compound CMOS symbol

2.3. Cell Truth Table

3 input NAND gate		
Cell Inputs {A,B,C}		Cell Outputs {net1}
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

2.4. Schematic diagram

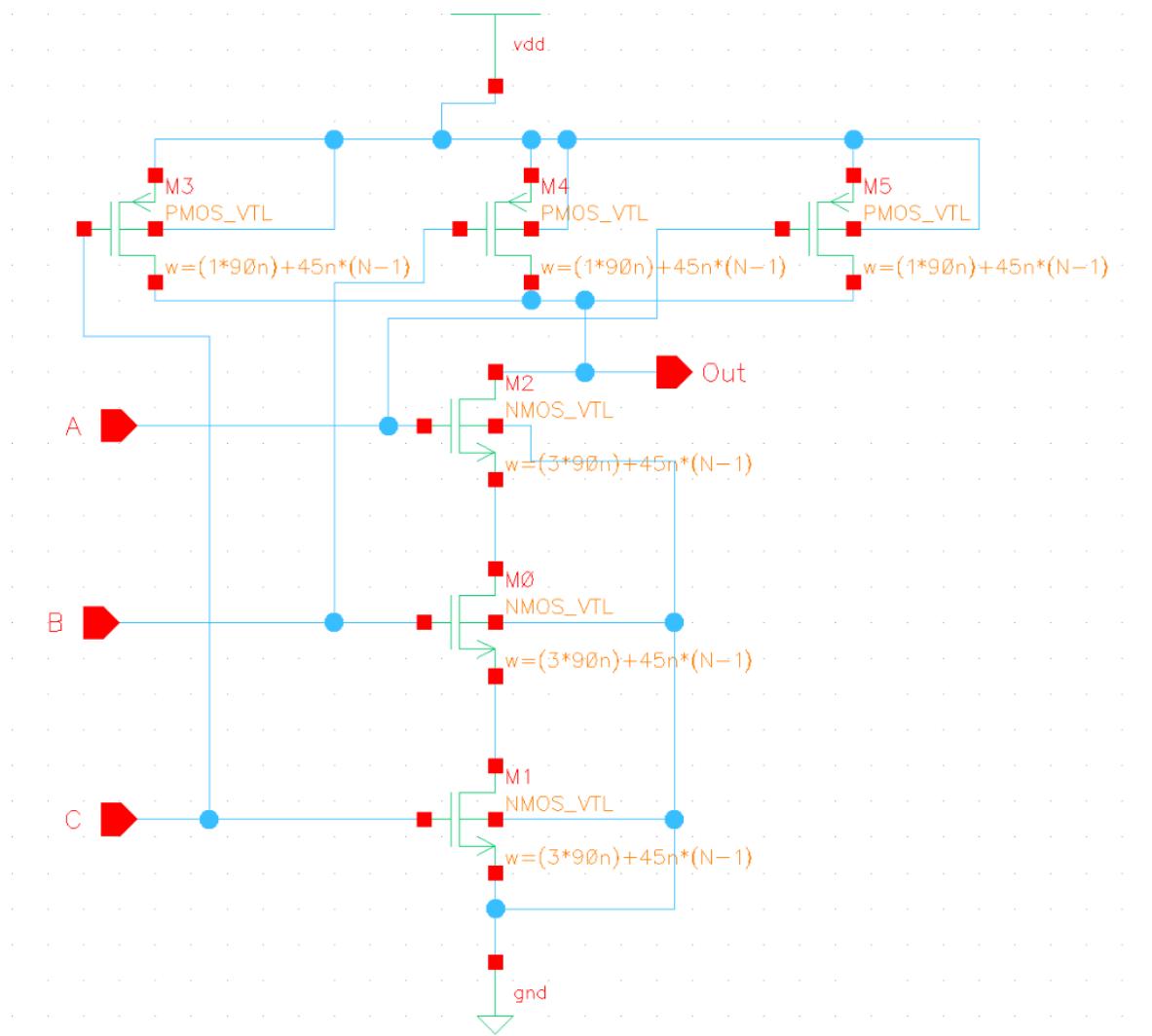


Figure 14: Compound CMOS schematic

2.5. Cell Layout Diagram and Dimensions

Initial sizing for the compound gate was based on the scaling factors applied to the dimensions of the inverter PMOS and NMOS. The PMOS width was determined by multiplying the inverter PMOS size by PMAX, and the NMOS width by multiplying the inverter NMOS size by NMAX. This can be represented as $(1 \times \text{PMOSwidth})$ and $(3 \times \text{NMOSwidth})$.

For an NMOS stack, the width calculation was (3×90) nm + $45 \times (N-1)$ nm, and for a PMOS stack, it was (1×90) nm + $45 \times (N-1)$ nm. With N being optimized at 3 for an FO4 inverter, the resulting widths were 360 nm for NMOS and 180 nm for PMOS.

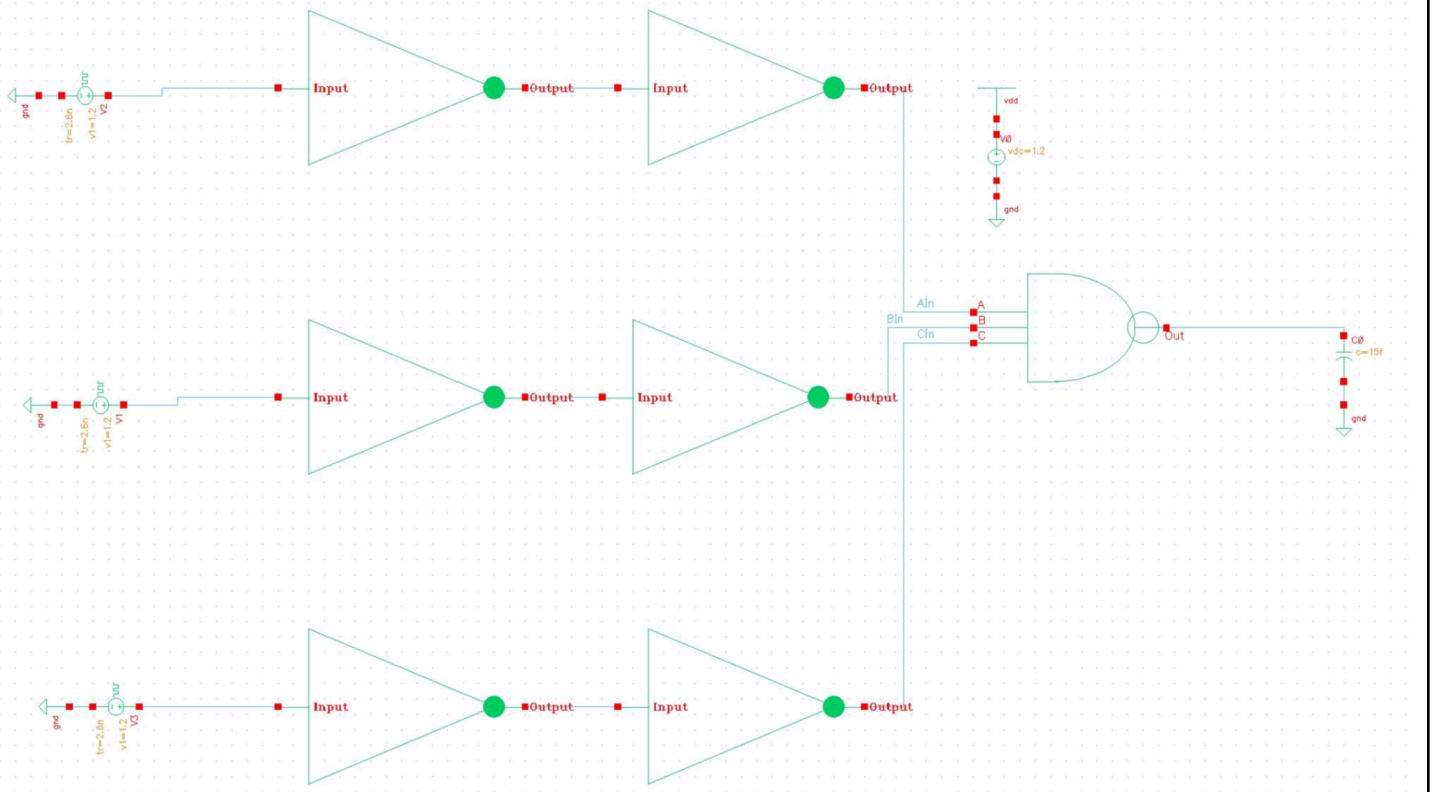


Figure 15: Zero-Fanout Schematic

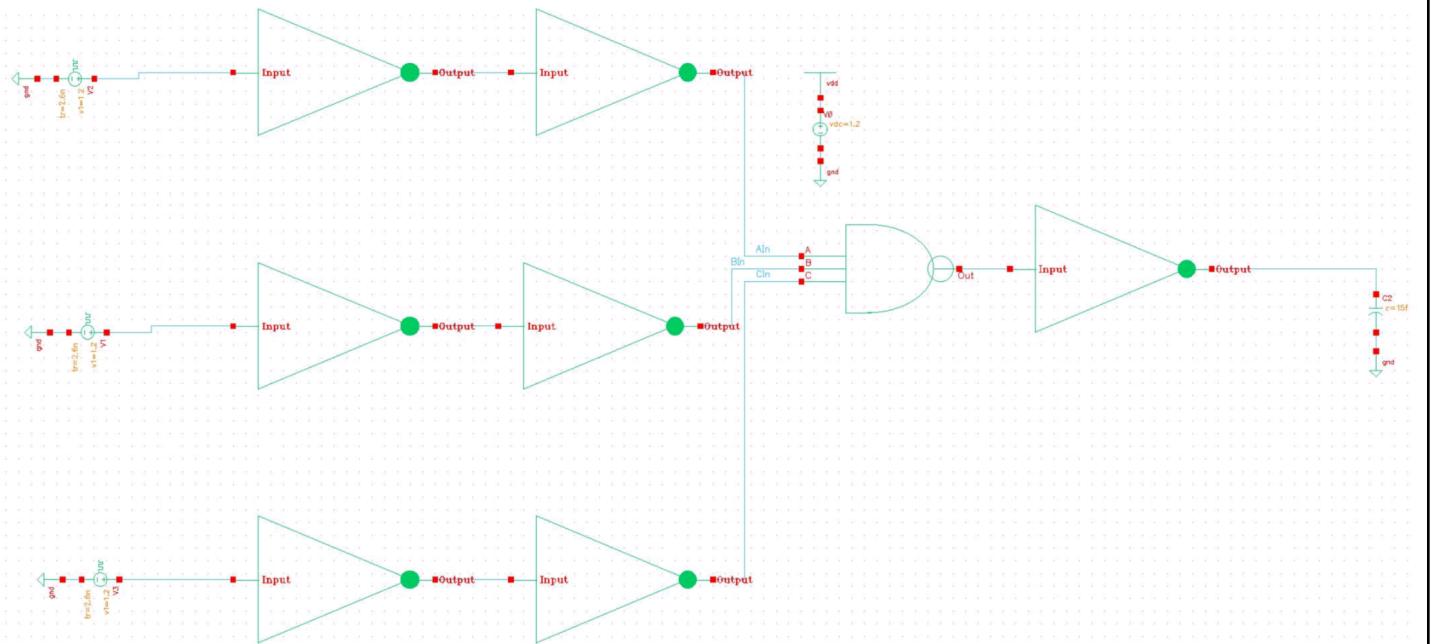


Figure 16: One-Fanout Schematic

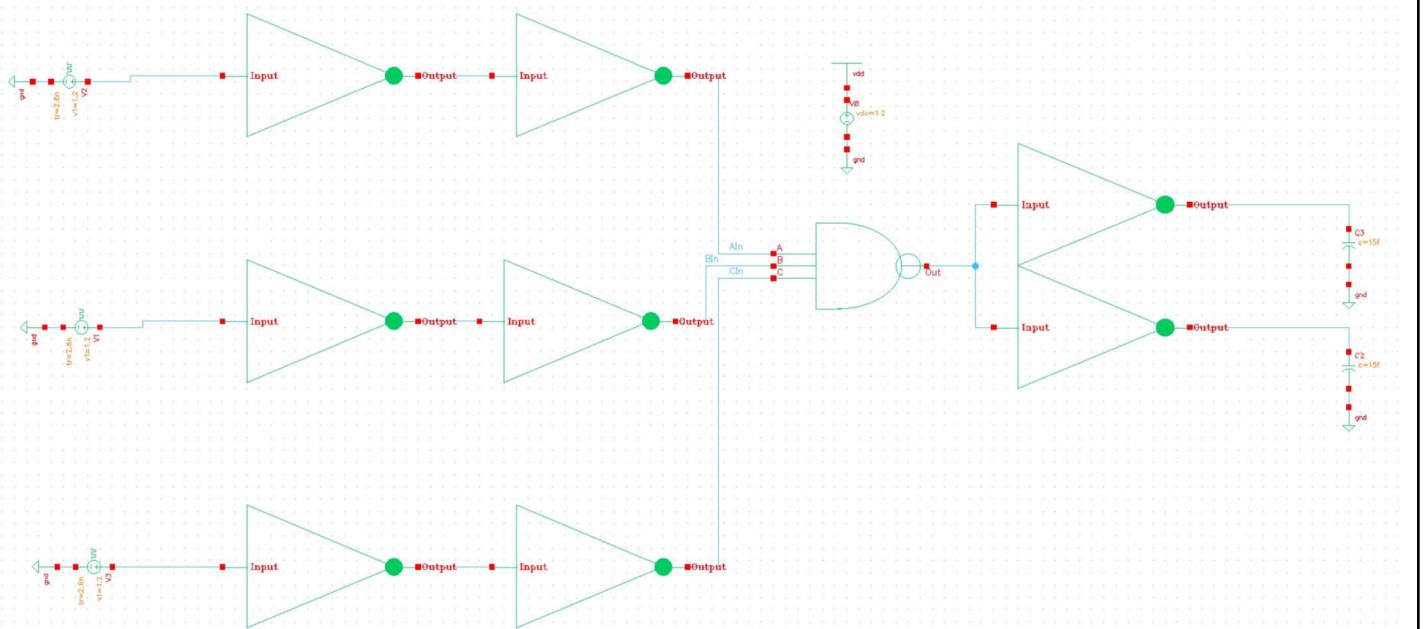


Figure 17: Two-Fanout Schematic

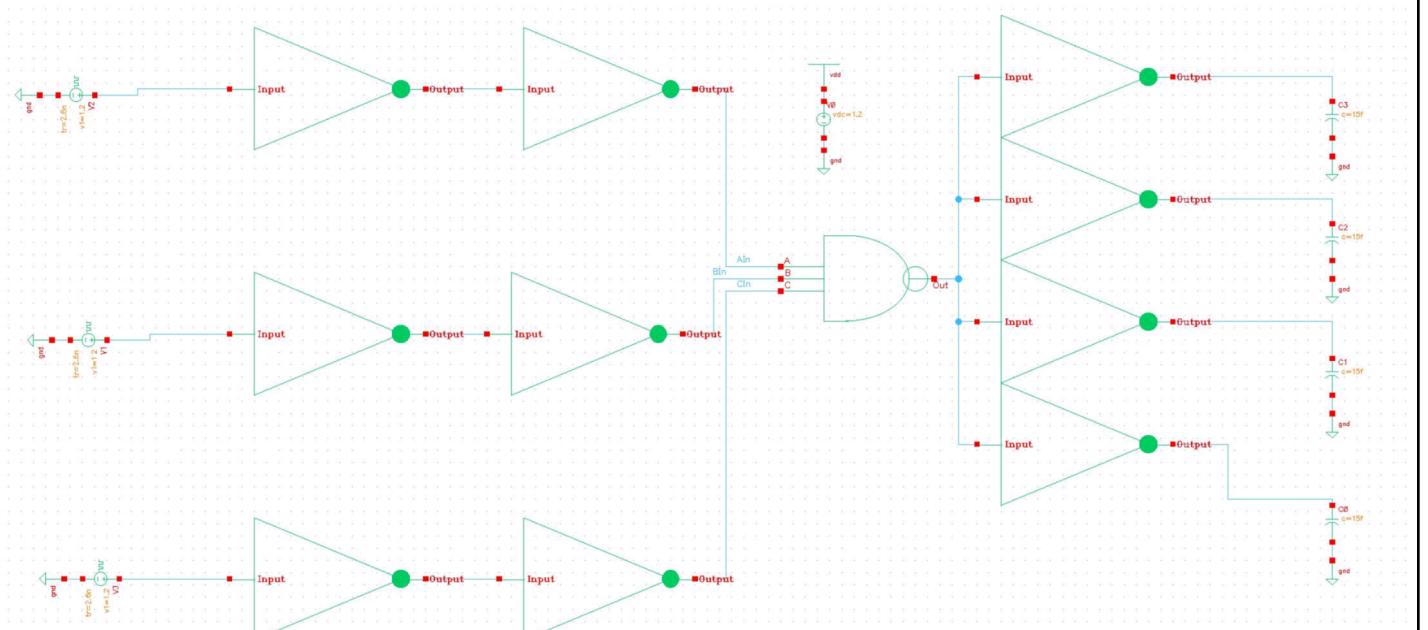


Figure 18: Four-Fanout Schematic

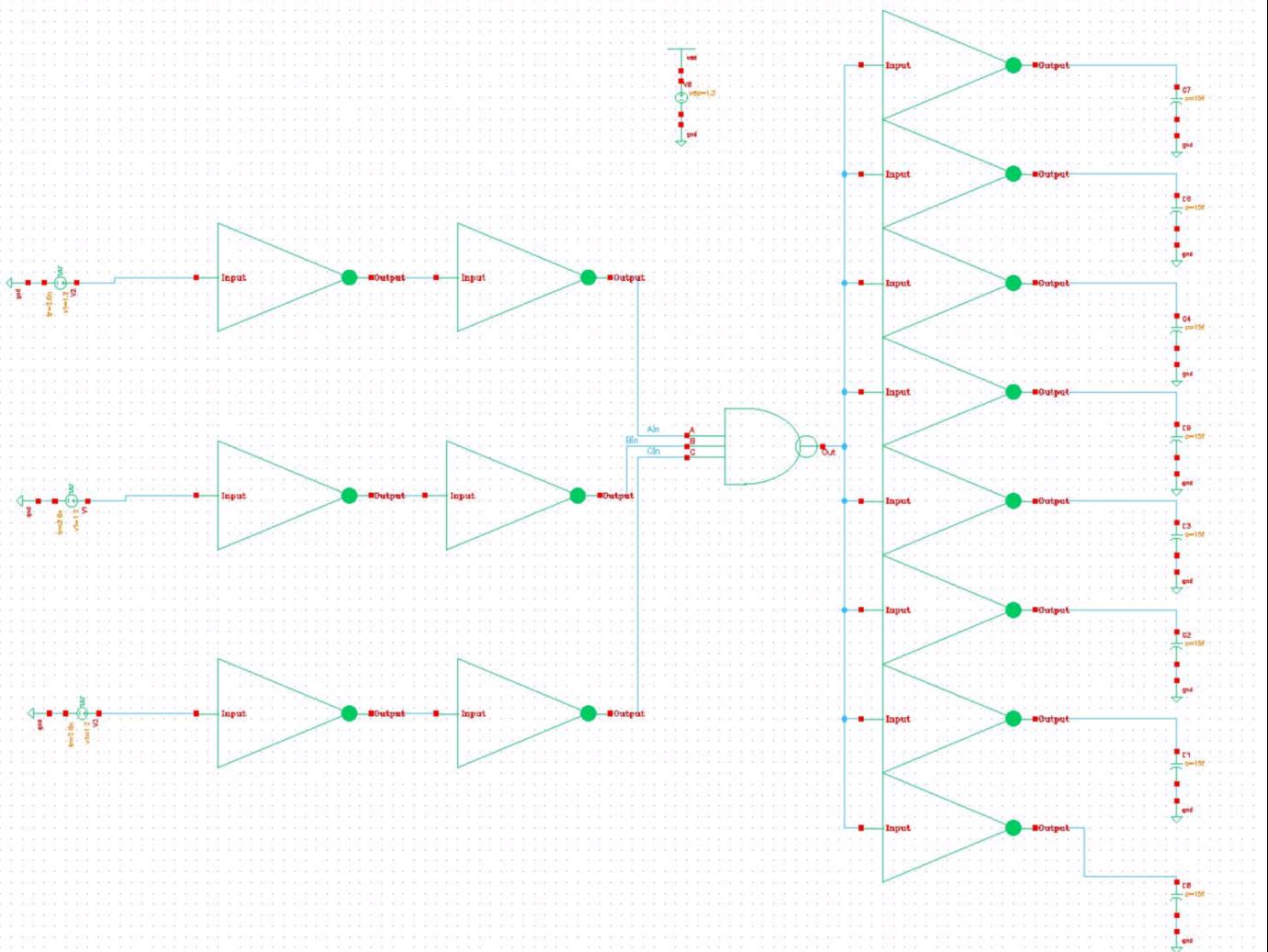


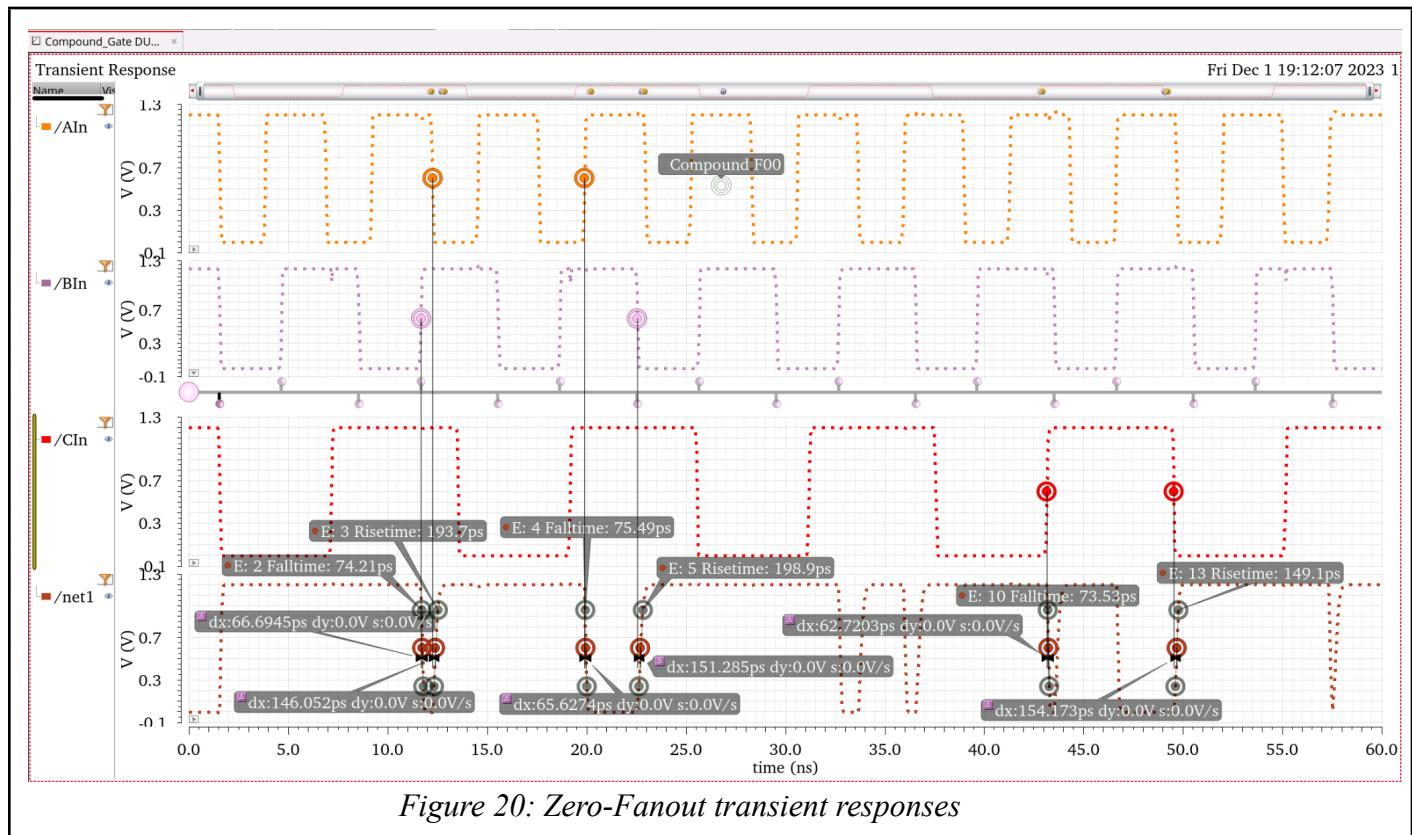
Figure 19: Eight-Fanout Schematic

Transistor Dimensions - 3 input NAND gate		
Transistor Instance Number	Length (nm)	Width (nm)
NMOS M0	50	360
NMOS M1	50	360
NMOS M2	50	360
PMOS M3	50	180
PMOS M4	50	180
PMOS M5	50	180

2.6. Performance Analysis

As Figure 20 to Figure 24 shows, the rise time for all three inputs from VPulse into (A, B, and C) were set to 2.6 nanoseconds, yielding input rise times as follows: AIn approximately 51 ps, BIn approximately 51 ps, and CIn approximately 49 ps. Additionally, The fall time from VPulse, measured at 2.75 nanoseconds for all inputs, resulted in the following input fall times: AIn approximately 51.21 ps, BIn approximately 50.13 ps, and CIn approximately 50.13 ps.

2.6.1. Transient Responses



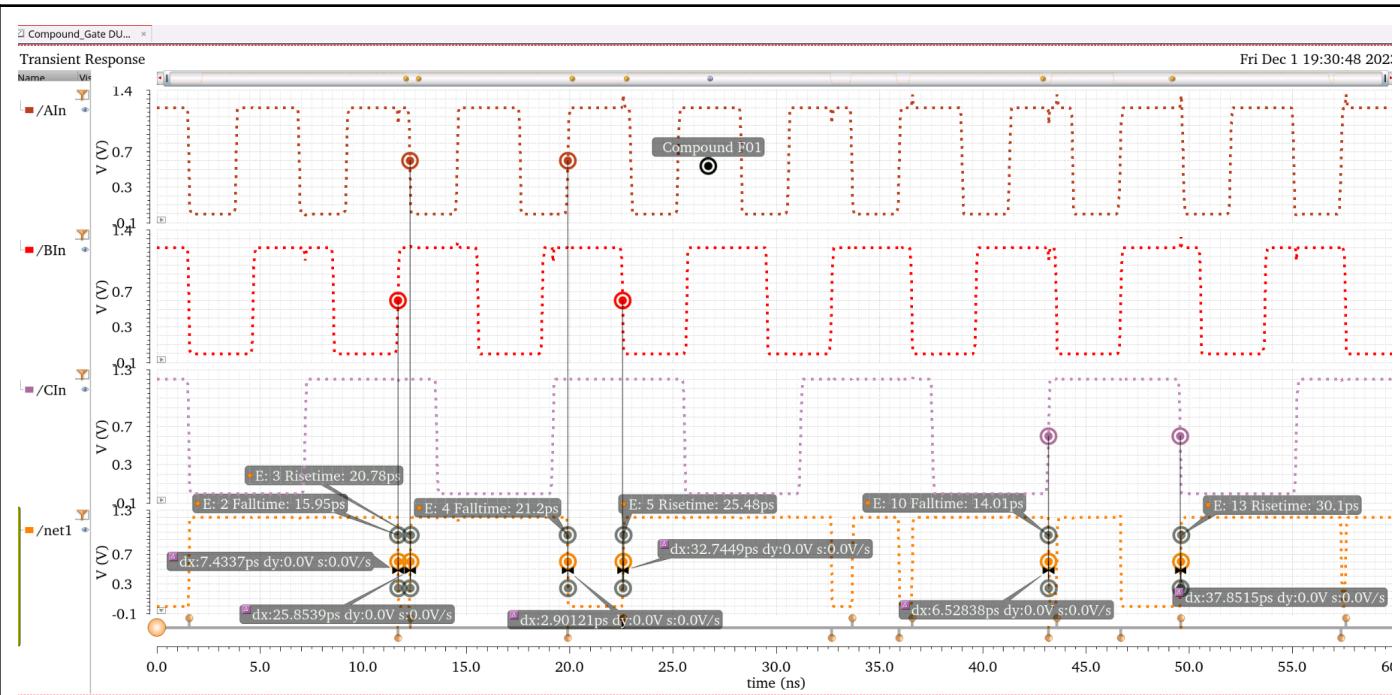


Figure 21: One-Fanout transient responses

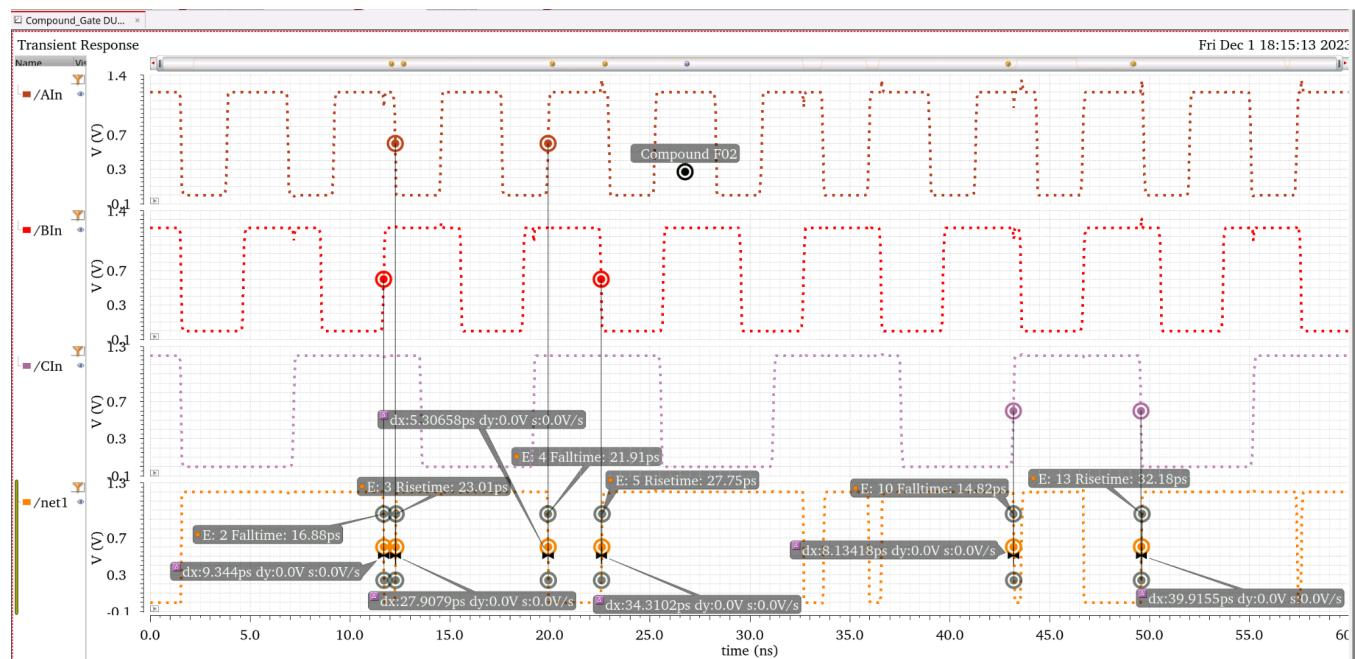


Figure 22: Two-Fanout transient responses

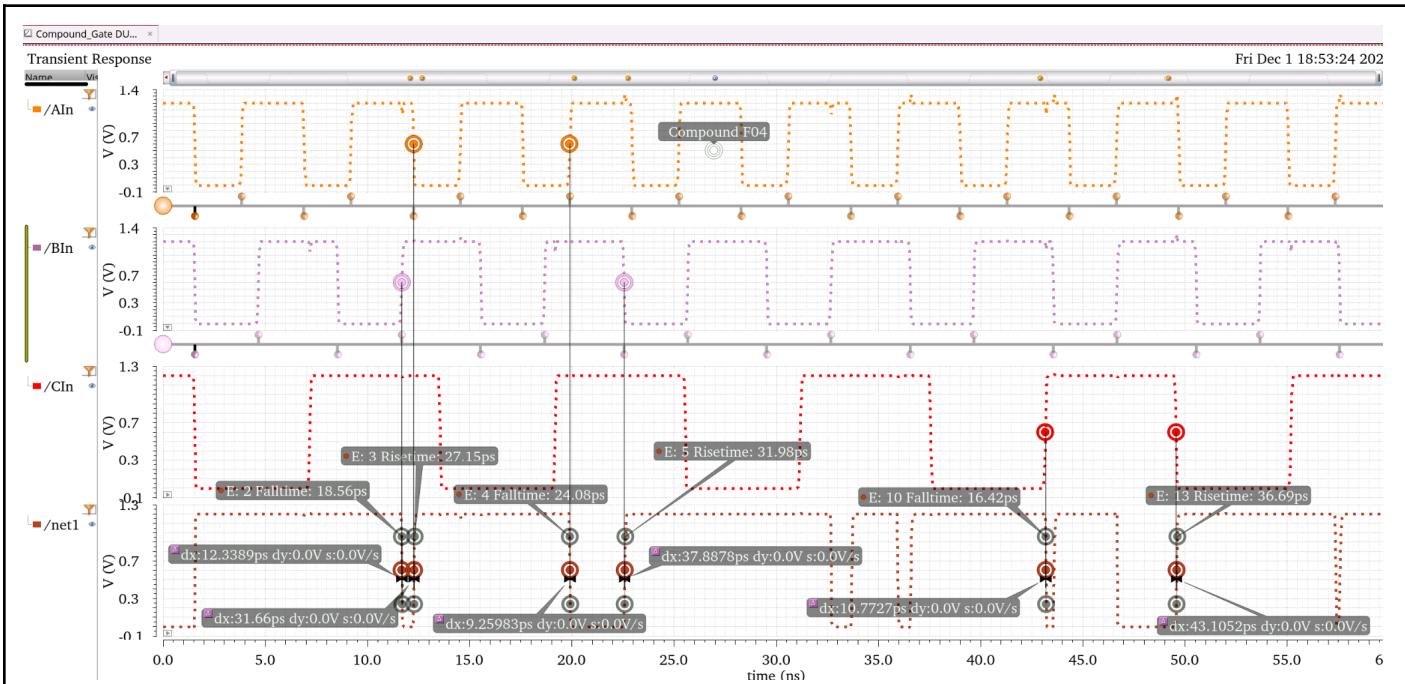


Figure 23: Four-Fanout transient responses

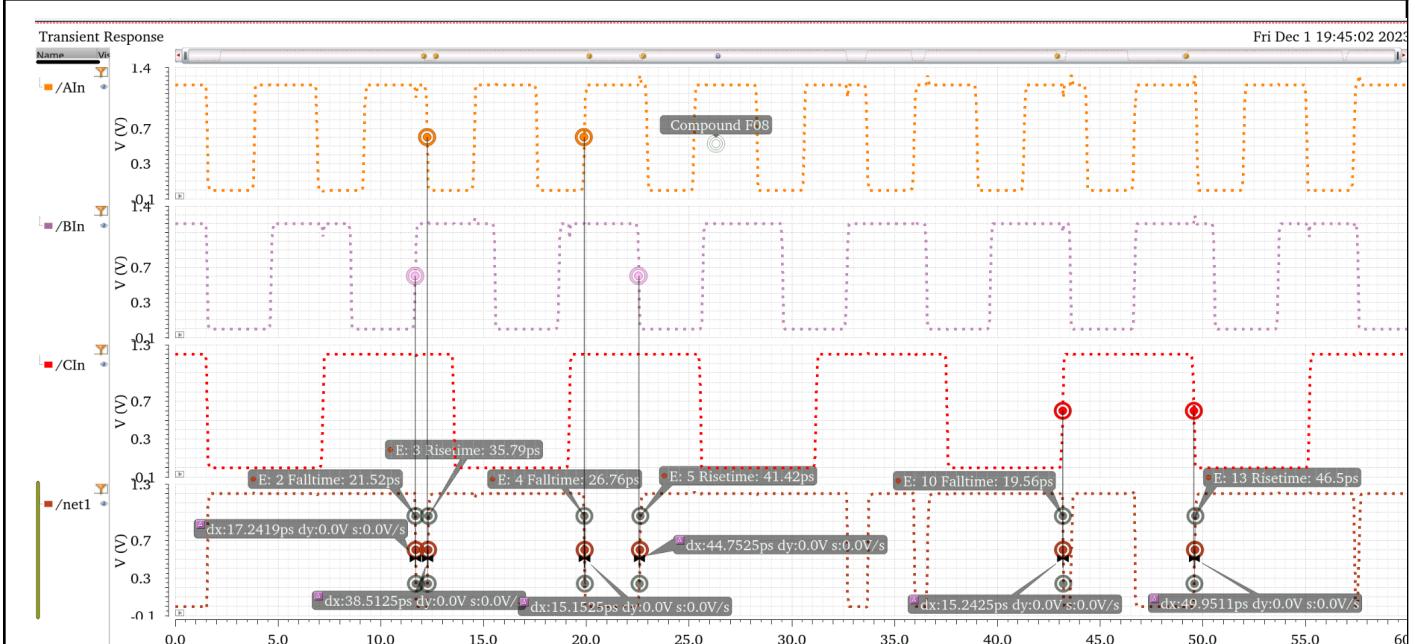


Figure 24: Eight-Fanout transient responses

2.6.2. Rise and Fall Times

Input A: Output Rise Time Data t_r (ps)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.05	193.7	20.78	23.01	27.15	35.79

Stack Input Combination: *Replace with Boolean Product*

Input A: Output Fall Time Data t_f (ps)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.05	75.49	21.2	21.91	24.08	26.76

Input B: Output Rise Time Data t_r (ps)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.05	198.9	25.48	27.75	31.98	41.42

Stack Input Combination: *Replace with Boolean Product*

Input B: Output Fall Time Data t_f (ps)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.05	74.21	15.95	16.88	18.56	21.52

Input C: Output Rise Time Data t_r (ps)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.05	149.1	30.1	32.18	36.69	46.5

Stack Input Combination: *Replace with Boolean Product*

Input C: Output Fall Time Data t_f (ps)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.05	73.53	14.01	14.82	16.42	19.56

2.6.3. Propagation Delays

Data Worst Case Low to High Propagation Delay Data t_{plh} (ps)					
AIn					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.05	65.6274	2.90121	5.30658	9.25983	15.1525
BIn					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.05	66.6945	7.4337	9.344	12.3389	17.2419
CIn					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.05	62.7203	6.52838	8.13418	10.7727	15.2425

Worse Case Input Combination: *Replace with Boolean Product*

Data Worst Case High to Low Propagation Delay Data t_{phl} (ps)					
AIn					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.05	146.052	25.8539	27.9079	31.66	38.5125
BIn					
Input rise/fall time (ns)	Output Load (FOx) -				
	0	1	2	4	8
0.05	151.285	32.7449	34.3102	37.8878	44.7525
CIn					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.05	154.173	37.8515	39.9155	43.1052	49.9511

Worse Case Input Combination: *Replace with Boolean Product*

2.7. Troubleshooting and Optimization

During NAND gate DUT creation, Virtuoso encountered errors when attempting to place two nodes directly on top of each other. This issue was exacerbated by a node overlapping a pass-through wire, which falsely suggested a connection between the NMOS and PMOS networks. There was initial confusion utilizing fall times with variable VS inputs. Once the concept was fully understood, we were able to align the FO4 inverter's rise and fall times with the standard sizing for a 90nm process, to match a ~ 50 ns slew rate. Also, it was misunderstood that each input, A, B, and C, needed their own independent Tphl, Tplh, Tr, and Tf times simulated. The aforementioned issues resulted in a re-simulation of every circuit to guarantee the precision of our results. We noticed that due to the re-simulation, FO4 BIn and CIn fell slightly out of SPEC. Unfortunately, due to time constraints, we could not redo sizing and simulations. Therefore the data shown is all we have to compare.

2.8. Conclusion

Through careful analysis and troubleshooting, we were able to optimize the FO4 compound gate sizing and correct simulation errors, leading to accurate modeling of the timing characteristics for the FO4 inverter using a 90nm technology node. After adjusting sizing to $N = 3$, TR, and TF times for inputs from VS, several test benches were utilized and added to the test bench output. These fanouts consisted of inverters ranging from 0, 1, 2, 4, and 8 inverters. After analyzing simulation results, see from the data that using a FO0 (fanout of 0), the TR and TF, along with Tphl and Tplh, are drastically higher than every subsequent circuit. Even by adding a FO8, Tphl, Tplh, TR, and TF times all improve vastly, with the best timings coming from a fanout of 1 (FO1). This suggests that simply adding a buffer to the output of a circuit (such as a 3-input NAND gate) can greatly improve performance. Design choices then must be considered by the engineering team, if adding a buffer to output logic is beneficial to a project.

3. Overall summary

In summary, It is very interesting that both the CMOS inverter and the CMOS compound gate have extremely similar results. The fanout of 1 is the best case because it has the least propagation delay, the fanout of 0 is the worst case, and as we increase the fanout load, the propagation delay gets bigger and bigger. Maybe an important question to ask is, is that the case for all CMOS devices, or is this merely a coincidence?

4. Team roles and responsibilities

- Aaron Price
 - Simulated compound CMOS Inverter gates (second section)
 - Contributed to report data and discussion write-up
- Wa'el Alkalbani
 - Worked on the lab report layout and data documentation
 - Assisted in troubleshooting Compound and CMOS gates
- Mosiah Beal
 - Assisted in troubleshooting CMOS and Compound Inverter gates
 - Contributed to report data and discussion write up
- Mohammad Hasan
 - Simulated CMOS Inverter (first section)
 - Contributed to report data and discussion write up