

EE6094
CAD for VLSI Design
Programming Assignment 3 Report

Student Name: 阮品紘

Student ID: 106502013

Abstract

using Quine-McCluskey and Petrick_Method to minimize logic.

I. Problem Description

Given a logic minimize it by Quine-McCluskey and Petrick_Method.

II. Program Structure

1. Read input

```
void read_file(ifstream &ifile, ofstream &ofile);
```

2. do Quine-McCluskey algorithm

```
void QMAlgo();
```

3. create table(for Petrick_Method)

```
void createTable();
```

4. do Petrick_Method

```
void Petrick_Method();
```

5. transform POS to SOP

```
void POS2SOP();
```

6. get min SOP

```
void getMinLogic();
```

III. Data Structures / Algorithms Used

Data Structures : map, vector, set

Algorithms : Quine-McCluskey and Petrick_Method

IV. How to Execute

```
$ make
```

```
$ ./PA3_106502013
```

V. Difficulty Encountered

Consider what data structures to use.

VI. Experimental Results

以 test2 為例：

Round1：

```
round1
implicants:
0101000 40
1001000 72
merged boolean:
-010000 16 80 0-00100 4 36 000-001 1 9 0000-01 1 5 00000-1 1 3 000010- 4 5 001-000 16 24
0-00101 5 37 00-0011 3 19 000-101 5 13 0001-01 9 13 00110-0 24 26 01001-0 36 38 010010- 36 37
-100101 37 101 00-1101 13 29 00-1110 14 30 00011-1 13 15 000111- 14 15 001-110 22 30 0011-10 26 30
-001111 15 79 -011110 30 94 00-1111 15 31 00111-1 29 31 001111- 30 31 10-1011 75 91 1001-11 75 79 10101-1 85 87
```

Round2：

```
round2
implicants:
0101000 40
1001000 72
-010000 16 80
00000-1 1 3
001-000 16 24
00-0011 3 19
00110-0 24 26
01001-0 36 38
-100101 37 101
001-110 22 30
0011-10 26 30
-001111 15 79
-011110 30 94
10-1011 75 91
1001-11 75 79
10101-1 85 87
merged boolean:
0-0010- 4 5 36 37 000--01 1 5 9 13
00-11-1 13 15 29 31 00-111- 14 15 30 31
```

Round3：

```
round3
implicants:
0101000 40
1001000 72
-010000 16 80
00000-1 1 3
001-000 16 24
00-0011 3 19
00110-0 24 26
01001-0 36 38
-100101 37 101
001-110 22 30
0011-10 26 30
-001111 15 79
-011110 30 94
10-1011 75 91
1001-11 75 79
10101-1 85 87
0-0010- 4 5 36 37
000--01 1 5 9 13
00-11-1 13 15 29 31
00-111- 14 15 30 31
```

3 round 即合併完畢

Create tabel :

```
1 00000-1 000--01
3 00000-1 00-0011
4 0-0010-
5 0-0010- 000--01
9 000--01
13 000--01 00-11-1
14 00-111-
15 -001111 00-11-1 00-111-
16 -010000 001-000
19 00-0011
22 001-110
24 001-000 00110-0
26 00110-0 0011-10
29 00-11-1
30 001-110 0011-10 -011110 00-111-
31 00-11-1 00-111-
36 01001-0 0-0010-
37 -100101 0-0010-
38 01001-0
40 0101000
72 1001000
75 10-1011 1001-11
79 -001111 1001-11
80 -010000
85 10101-1
87 10101-1
91 10-1011
94 -011110
101 -100101
```