

¹ A Design for a Deep Underground Single-Phase
² Liquid Argon Time Projection Chamber for
³ Neutrino Physics and Astrophysics

⁴ March 12, 2015

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⁹ Chapter 1

¹⁰ Cold Electronics

ch:ce

¹¹ 1.1 Introduction

¹² The TPC read-out electronics are referred to as the “Cold Electronics” (CE) because
¹³ they will reside in LAr, mounted directly on the APA front-end. This will minimize
¹⁴ channel capacitance and noise by keeping the length of the connection between an
¹⁵ anode wire and its corresponding electronics input to an absolute minimum. The
¹⁶ CE will be implemented as ASIC chips using CMOS technology, which performs
¹⁷ well at cryogenic temperatures, and will provide amplification, shaping, digitization,
¹⁸ buffering and multiplexing (Mux) of the signals. Because it is not possible to form
¹⁹ a trigger for some important measurements, such as proton decay and supernova
¹ bursts, the CE will be continuously read out, with a digitized ADC sample from
¹ each APA channel (wire) every 500 ns. For each of the 104 APAs in a ten-kton
² cryostat, one cable bundle will connect to the outside of the cryostat through a
³ feedthrough, with one feedthrough servicing two APAs. Each of these cable bundles
⁴ consists of wires for low-voltage power, TPC wire-bias voltages, data-out, clock-in,
¹ and digital-control IOs.

¹ The scope of the CE subsystem includes the design, procurement, fabrication,
² testing, delivery and installation of the CE:

- ³ • Front-end cards installed on the APAs
- ⁴ • All electronics on those cards
- ⁵ • Feedthroughs (a single type, henceforth “signal feedthroughs”) which handle
⁶ the signal, low-voltage power, TPC bias voltage, and control lines
- ⁷ • External interface crates

- 1 ● Power supplies, including low-voltage supplies for the CE and bias-voltage sup-
- 2 plies for the TPCs
- 3 ● Signal, control, and power cabling between the front-end cards and the feedthroughs,
- 4 and between the feedthroughs and external power supplies and interface crates

5 **1.2 Design Considerations**

- e_reqs_n_specs
- 6 The requirements for the CE can be found in the requirements documentation [?].
7 The most significant ones are the following:

8 ● Provide the means to read out the TPCs and transmit their data in a useful
9 format to the Data Acquisition System (DAQ).

10 ● Operate for the life of the facility without significant loss of function.

11 ● Record the channel waveforms continuously without dead time. Twelve bits
12 of ADC data per APA channel every 500 ns yields a single-channel bit rate of
13 0.024 Gbps. With 8B10B encoding this increases to 0.03 Gbps, plus some over-
14 head for frame data. Assuming a conservative serial-link transmission speed of
15 1 Gbps, a single link can therefore handle 32 channels. If a speed of 2 Gbps
16 can be achieved, which is possible but not yet demonstrated, the number of
17 serial links for data transmission will be cut in half.

18 ● Use only materials that are compatible with high-purity liquid argon.

19 ● Provide sufficient precision and range in the digitization to:

20 – Discriminate electrons from photon conversions;
21 – Optimize for high- and low-energy tracks from accelerator-neutrino inter-
22 actions;
23 – Distinguish a Minimum Ionizing Particle (MIP) from noise with a signal-
24 to-noise ratio > 9:1;

1 – Measure the ionization up to 15 times that of a MIP particle, so that
2 stopping kaons from proton decay can be identified.

3 ● All power supplies will have:

4 – Local monitoring and control;
- lar-fd-req

- 5 – Remote monitoring and control through DAQ;
- 6 – Over-current and over-voltage protection circuits;
- 7 • The low-voltage (signal) feedthroughs must be able to withstand twice their
8 nominal operating voltages with a maximum specified leakage current in 1-atm
9 argon gas.

10 The responsibility and authority for the design, installation and use of the detector
11 quiet-power distribution and detector-grounding system is held by the subproject
12 electrical engineer. This engineer has oversight responsibility for all electrical and
13 electronics design and installation tasks, including all attachments to the detector
14 that create an electrical connection.

15 1.3 Architecture

16 The CE architecture is manifested in the Cold Mother Board assembly (CMB), which
17 consists of an analog mother board with a digital ASIC mezzanine (Fig. 1.1). Each
18 APA is instrumented with 20 CMBs, for a total of 2,560 channels per APA.

19 The analog mother board is instrumented as a 128-channel board which uses eight
20 16-channel FE ASICs, eight 16-channel ADC ASICs, low voltage regulators, and
21 input-signal protection. The 16-channel FE ASIC provides amplification and pulse
22 shaping. The 16-channel ADC ASIC comprises a 12-bit digitizer, local buffering, and
23 an 8:1 Mux stage with two pairs of serial readout lines in parallel. This has already
24 been prototyped and tested, using a commercial FPGA to perform the rôle of the
25 digital ASIC (Fig. 1.2).

26 The Cold Digital Data (COLDATA) ASIC and its voltage regulators are mounted
27 on the digital ASIC mezzanine. The COLDATA ASIC provides:

- 28 • The communication protocol with the data acquisition system (DAQ);
- 1 • The control required to program and read out the FE and ADC ASICs;
- 2 • The system clock interface;
- 3 • Four 4:1 Muxs that combine 16 serial lines from the ADCs of eight channels
4 each into four serial lines of 32 channels each;
- 5 • Four 1-Gbps serial drivers that form the data link to DAQ.

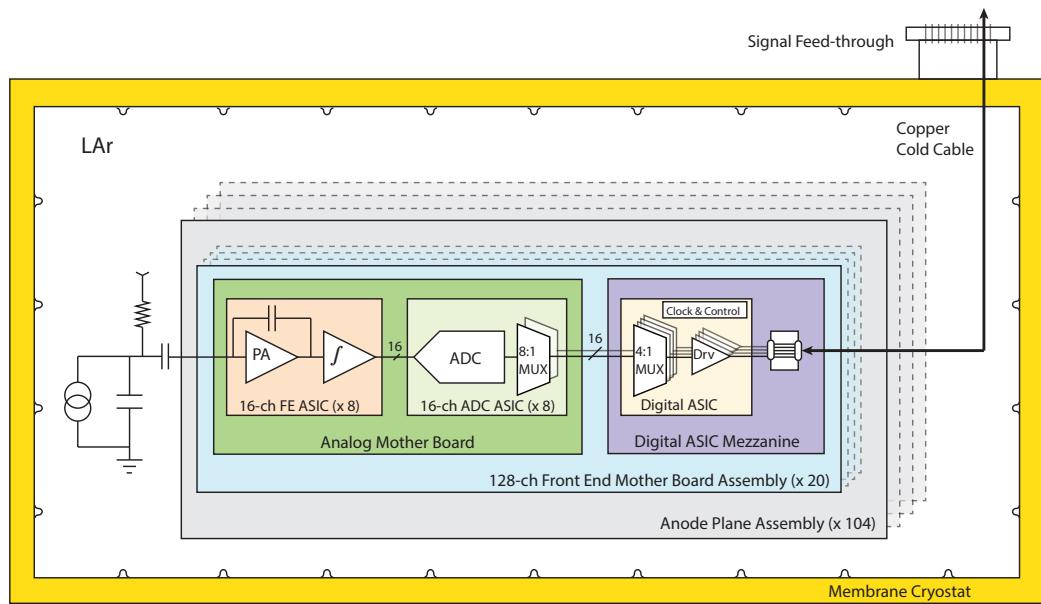


Figure 1.1: The CE Architecture. The basic unit is the 128-channel CMB

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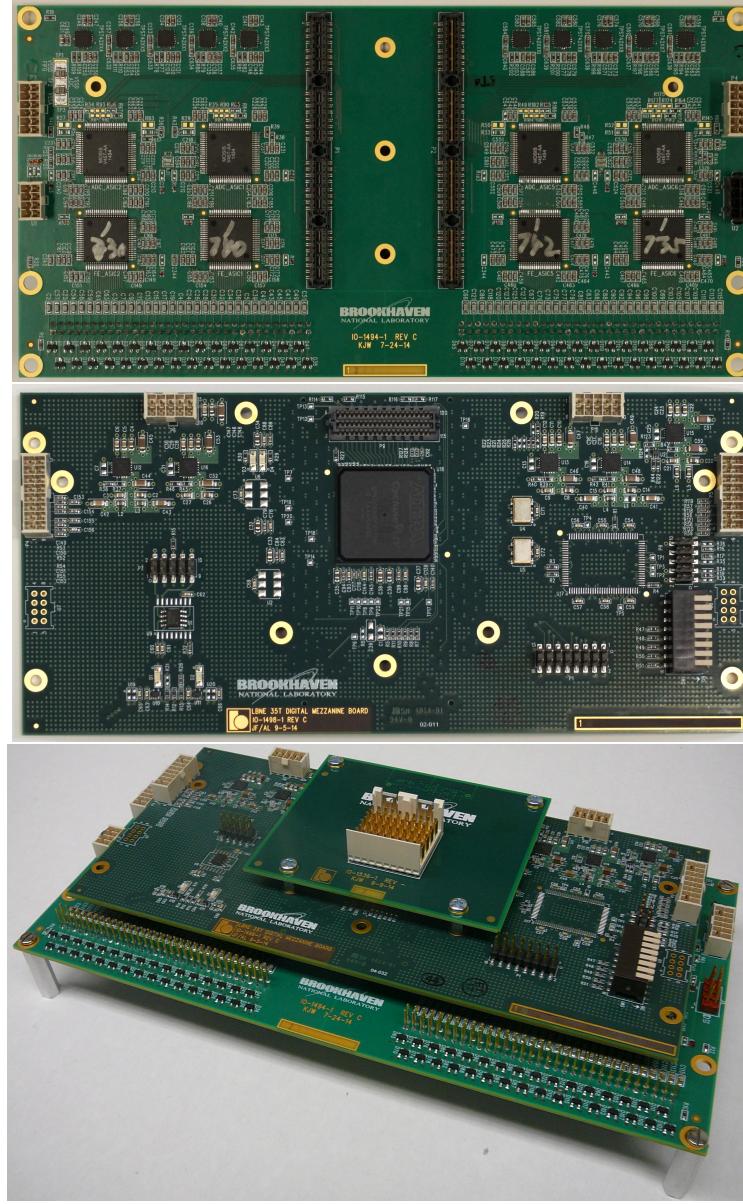


Figure 1.2: The Cold Mother Board (CMB), as used in the early set of tests. **Top:** The analog mother board, showing four ADC ASICs and four FE ASICs surface mounted. The other side of the board has another four ADC and FE ASICs. Except for anticipated small modifications, this board is essentially the final version. **Middle:** The FPGA mezzanine, used in place of the digital ASIC mezzanine for the early set of tests. **Bottom:** The complete CMB assembly as used in the early set of tests. The uppermost mezzanine board is the cable connection.

fig:elec_CMBpi

If it is demonstrated that the COLDATA ASIC can achieve 2 Gbps, then the 4:1 Mux will be increased to 8:1 and only two serial drivers will be implemented, with a subsequent reduction in cabling, etc. In either case, the data rates will not be high enough to require the use of optical fibers in the cold, nor is there a need for zero-suppression or data compression. This greatly reduces the complexity of the COLDATA ASIC, with a corresponding decrease in overall risk, including risk of failure-to-implement (within a fixed schedule and budget) and risk of device-failure during long-term operation. Data will be driven to DAQ through copper cable utilizing low-voltage differential signaling (LVDS). Output data cables will go to a signal feedthrough and from there to an external crate mounted nearby. Under DAQ scope, further data processing is done in the external crate and data is transmitted via optical fiber to front-end computers.

The analog FE ASIC has 16 channels. Each channel includes a charge amplifier with a gain selectable from one of 4.7, 7.8, 14 and 25 mV/fC (full scale charge of 55, 100, 180 and 300 fC), a high-order anti-aliasing filter with adjustable time constant (peaking time 0.5, 1, 2, and 3 μ s), an option to enable AC coupling, and a baseline adjustment for operation with either the collecting or the non-collecting wires. The 16-channel FE ASICs then transmit the shaped pulse to a 16-channel 12-bit 2 MS/s ADC ASIC. Shared among the 16 channels in the FE ASIC are the bias circuits, programming registers, a temperature monitor, an analog buffer for signal monitoring, and the digital interface. The estimated power dissipation of FE ASIC is about 6 mW per channel at 1.8 V supply. Shared among the 16 channels in the ADC ASIC are the bias circuits, programming registers, an 8:1 Mux, and the digital interface. The estimated power dissipation of FE ASIC is below 5 mW per channel at 1.8 V supply.

1.4 CMOS Circuit Design

To successfully design CMOS circuits that will operate at cryogenic temperatures, two critical issues must be addressed and resolved. The first issue is the need for realistic models at the operating temperature of all active and passive components in order to reliably predict operating points, signal response, and noise during the design process. The second issue is that the design must ensure a long operational lifetime, since once the TPC is filled with LAr the detector must operate for about 15 years without any access to the electronics for repair or replacement. Concerning the availability of realistic models, our preliminary results from the cryogenic characterization (down to 40 K) of a complete mixed-signal ASIC [?] in a commercial CMOS 0.25 μ m technology, originally developed for room-temperature applications,

13 indicates that the models are useful to first order. To refine these models, several
14 single-transistor test structures were fabricated on the first prototype of the $0.18\ \mu\text{m}$
15 device. Measurements of the properties of these structures at cryogenic temperatures
16 have been used to refine the device models at 89 K.

17 The lifetime of CMOS circuits is limited by several mechanisms which degrade
18 the performance over time, eventually causing the circuit to fail to perform as speci-
19 fied. The rates of most degradation mechanisms in CMOS, such as electro-migration
20 (EM), stress migration (SM), time-dependent dielectric breakdown (TDDB), ther-
21 mal cycling (TC), and negative bias-temperature instability (NBTI), all scale with
22 temperature such that cryogenic operation is favored [?][?]. The only mechanism
23 that could affect the lifetime at cryogenic temperature is the degradation due to
24 impact ionization, which causes charge trapping in the MOSFET gate oxide at large
25 drain-current densities (the “Hot Carrier” effect). Results from a CMOS reliability
26 study [?] provide general design guidelines (for device geometry, bias and current
27 density) that should guarantee a lifetime well in excess of 15 years for continuous
28 cryogenic operation. These design guidelines also provide information for design-
29 ing test conditions to observe the deterioration mechanism and to extrapolate from
30 accelerated deterioration rates, measured under stressed conditions within practical
31 times, to the ultimate lifetime under normal operation.

32 A monitor of the impact ionization is the bulk current, which reaches a maximum
33 at $V_{DS} = V_{DD}$ and at $V_{GS} = 0.5V_{DD}$. When operating constantly in this condition at
34 room temperature, a properly designed device will typically have a lifetime (defined
35 as a 10% degradation in g_m) of about 10 years. The bulk current (i.e. the impact
36 ionization) increases by roughly a factor of four from 300 K to 77 K [?] and a circuit
1 designed for operation at room temperature would have a proportionately shorter
2 useful life at cryogenic temperature. As stated above, in order to guarantee the
3 required lifetime at cryogenic temperatures, design guidelines must be modified for
4 both analog and digital circuits. For analog circuits, this is done by operating the
5 devices at moderate-to-low drain current densities, where impact ionization becomes
6 negligible. For digital circuits, operating the devices with reduced V_{DD} (about 20%)
7 and using non-minimum channel length L, which is easily accommodated since at
8 cryogenic temperature the speed of the digital circuit increases, compensating for
9 the increased L. These guidelines will be verified with accelerated aging tests, at
10 increasing values of V_{DD} , on dedicated structures. Such tests also will be conducted
11 on prototype samples throughout the development process to verify the long-term
12 reliability of the final ASICs.

1.4.1 Cold Analog ASICs

The development of the readout ASIC has begun by designing and fabricating in a commercial CMOS process ($0.18\text{ }\mu\text{m}$ and 1.8V) a 16-channel ASIC implementing the complete analog front-end section. The layout out the FE ASIC is shown in fig. 1.3. This process is expected to be available for at least another 10 years. The charge amplifier input MOSFET is a p-channel biased at 2 mA with a L/W (channel length/width) ratio of $0.27\text{ }\mu\text{m} / 10\text{ }\mu\text{m}$, followed by dual cascade stages. The charge amplification and shaping filter have digitally programmable gain and peaking time as described above. Each channel also implements a high-performance output driver, which is used to drive a long cable when it is used in a standalone mode, as it is in MicroBooNE. The buffer can be disabled when it is interfaced to an ADC ASIC, to reduce the power consumption. The ASIC integrates a band-gap reference (BGR) to generate all the internal bias voltages and currents. This guarantees a high stability of the operating point over a wide range of temperatures, including cryogenic. The ASIC is packaged in a commercial, fully encapsulated plastic QFP 80 package.

This ASIC has now been through four design/fabrication/testing revision cycles. Prototypes from each cycle have been evaluated and characterized at room (300 K) and liquid nitrogen (77 K) temperatures. During these tests the circuits have been cycled multiple times between the two temperatures and operated without any change in performance. Figure 1.4 shows the measured pulse response, along with details on the adjustability of the gain, peaking time and baseline. These results are in close agreement with the simulations and indicate that both the analog and the digital circuits and interface operate as expected in a cryogenic environment. Also reported in Figure 1.4 are the outputs of the BGR and temperature sensor, which are in close agreement with the simulations as well.

Figure 1.5 shows the measured ENC versus filter-time constant (peaking time). At $1\text{ }\mu\text{s}$ about 650 e^- was measured, to be compared to the simulated value of 500 e^- . The difference is mainly due to the thermal noise from a $\sim 11\text{-ohm}$ parasitic resistance of the input line (shown in the detail of Figure 1.5), which contributes about 350 electrons at 77 K . The width of the line has been increased in a revision in order to make this contribution negligible. A second contribution, on the order of 100 e^- , was due to the dielectric loss from the capacitor (220 pF) used to simulate the wire (the cases of MICA and NPO ceramic were compared). This contribution would not be present with the input connected to a sense wire in the TPC.

Each channel is equipped with an injection capacitor which can be used for test and calibration and can be enabled or disabled through a dedicated register. The injection capacitance has been measured using a calibrated external capacitor. The measurements show that the calibration capacitance is extremely stable, changing

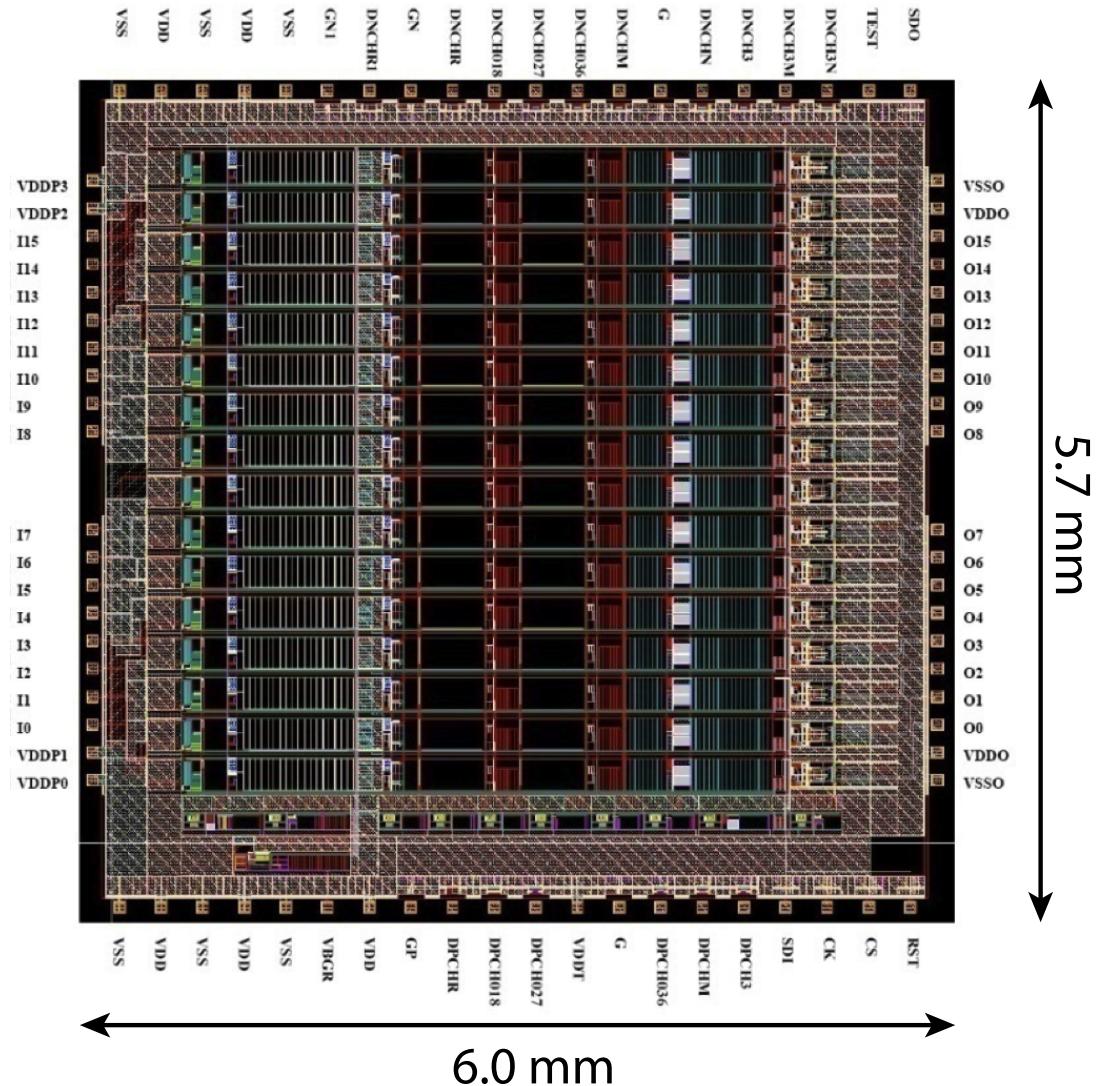


Figure 1.3: The layout of the 16-channel analog FE ASIC

fig:elec_FE_ASIC

Design for a Deep Underground Single-Phase LArTPC

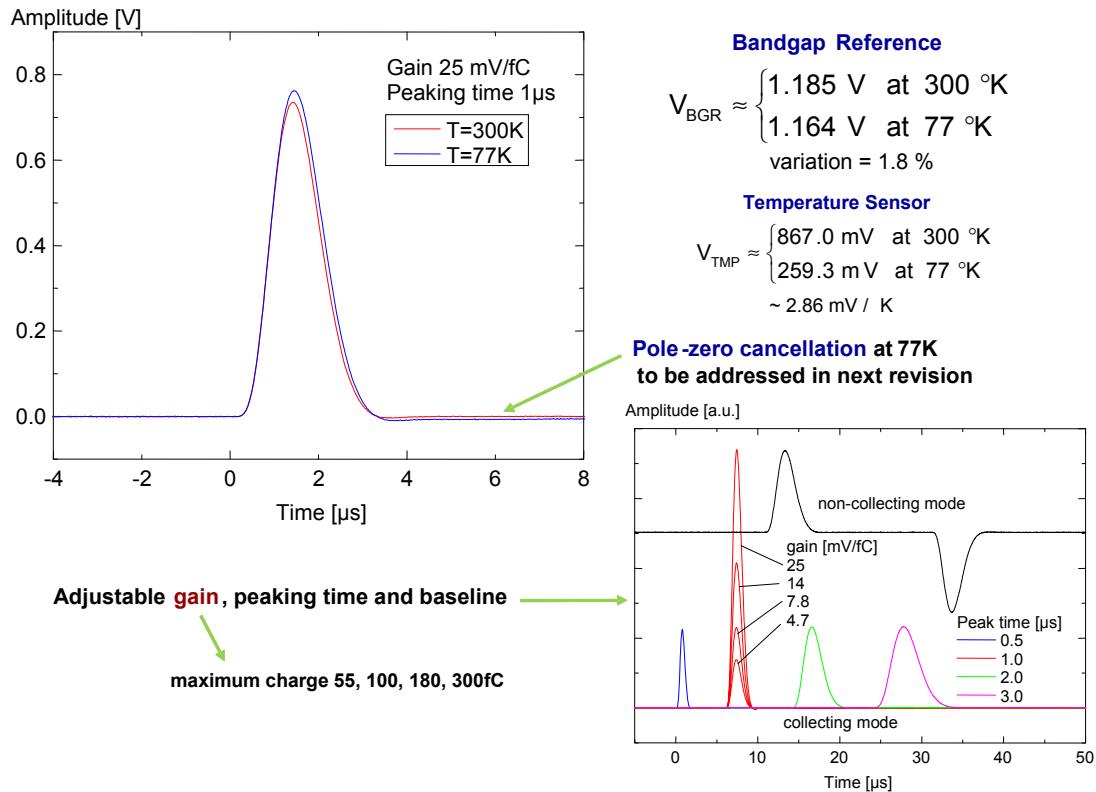


Figure 1.4: Measured pulse response with details on gain, peaking time and baseline adjustments

fig:ce_elec_sh

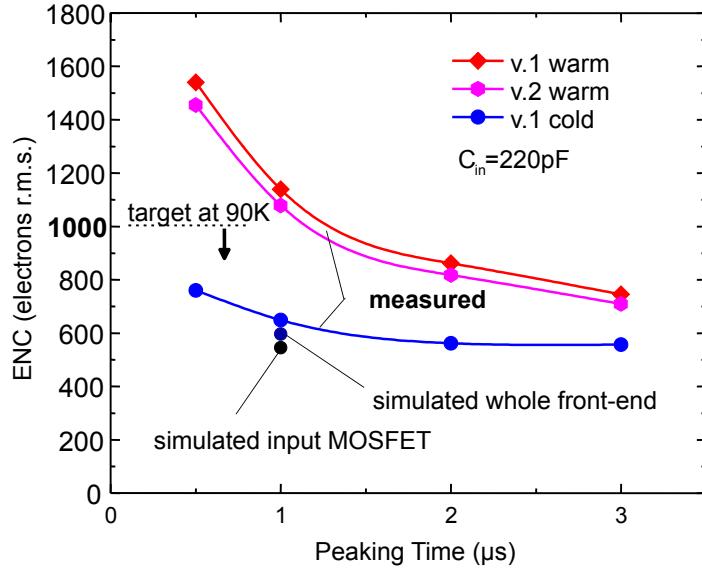


Figure 1.5: Measured ENC vs filter time constant from the first two versions of the analog front end ASICs

fig:ce_elec_en

from 184 fF at room temperature to 183 fF at 77 K. This result and the measured stability of the peaking time demonstrate the high stability of the passive components with the temperature. Channel-to-channel and chip-to-chip variation in the calibration capacitor are typically less than 1%. Measurements are being carried out on the individual test structures fabricated on this ASIC to confirm device models and design guidelines.

The development of the ADC ASIC is also using CMOS process (0.18 μ m and 1.8V). A 16-channel ASIC has been prototyped and tested. The layout of the ADC ASIC is shown in Figure 1.6. The ADC ASIC has 12-bit resolution, 2 MS/s sampling rate, built in FIFO, two 8:1 multiplexing and two pairs of serialized output. The ADC is a complex design, which has more than 300,000 transistors. All of the transistors design has been following the rules of long cryo-lifetime.

The ADC ASIC has input buffer with offset compensation to match the output of FE ASIC. The input buffer first samples the input signal (with a range of 0.2 V to 1.6 V), then provides a current output after compensating for offset voltage error. This current output is then supplied to the ADC which converts the input to digital in two phases. The MSB (Most Significant Bit) 6 bits are first determined followed by the LSB (Least Significant Bit) 6 bits. After the conversion the thermometer code is

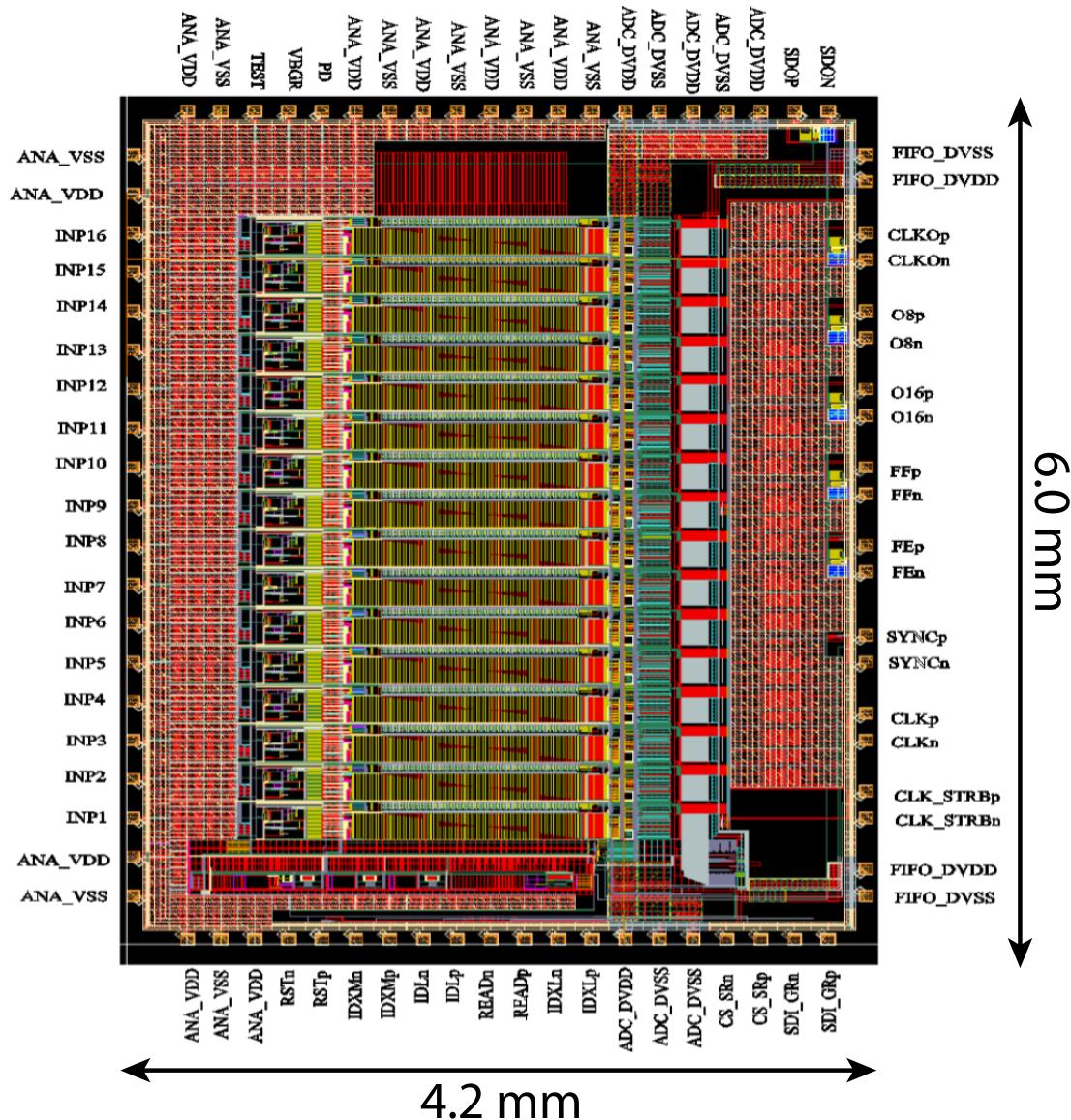


Figure 1.6: The layout of the 16-channel ADC ASIC

fig:elec_ADC_A

33 converted to binary and latched. The output of ADC 16 can be monitored externally.
 34 The data from the 16 ADCs is transferred in parallel to the FIFO block. The built-in
 35 FIFO is 32 bits wide and 192 bits long, it has the full and empty indicator flags to
 36 make it easy to interface to FPGA or digital ASIC. The ADC along with the input
 37 buffers are biased internally using a bias generator and a bandgap voltage reference.
 38 The bandgap voltage (VBGR) can be monitored and/or controlled externally. It can
 1 be put in the low power sleep mode, and waken up in less than 1 *mus*.

2 The ADC ASIC has now been through four design/fabrication/testing revision
 3 cycles. Prototypes from each cycle have been evaluated and characterized at room
 4 (300 K) and liquid nitrogen (77 K) temperatures. During these tests the circuits
 5 have been cycled multiple times. The effective resolution with reference to the input
 6 referred noise is \sim 11.6 bits at both 300 K and 77 K. The differential non-linearity
 7 (DNL) is less than 4 LSBs for 99% of ADC bins at both 300 K and 77 K. The
 8 performance of ADC meets the requirements of far detector.

9 Analog front-end ASIC has been adopted by MicroBooNE experiment in 2010.
 10 A total of 8,256 channels (516 FE ASICs) have been used to instrument the Mi-
 11 croBooNE TPC. The fabrication and installation has been completed in early 2014
 12 successfully. Both FE ASIC and ADC ASIC are being used in the 35 ton LAr TPC
 13 prototype. A total of 2,048 channels (128 FE ASICs and 128 ADC ASICs) are used
 14 to instrument the TPC. The cold front end mother boards have been produced and
 15 tested at 300 K. They are being tested at 77 K before final installation on the TPC.

1.4.2 Cold Digital Data ASICs

16 The development of the COLDATA ASIC will follow the general guidelines developed
 17 for the cold analog ASICs. The COLDATA ASIC design will differ from the analog
 1 design in a couple of aspects. It is anticipated that the digital ASIC will make use
 2 of a 65 nm CMOS technology and require a digital library with accurate cold timing
 3 models allowing for high level language design and automated place and route for
 4 design blocks using extensive digital logic.

5 A block diagram of the COLDATA ASIC is presented in Fig. 1.7. The major
 6 components of the COLDATA ASIC include a downlink which is required to receive
 7 the system clock and the control/download information transmitted from the DAQ.
 8 The download data must be transmitted to the FE and ADC ASICs on the CMB.
 9 The system clock will provide a frequency-reference to a crystal based Phase Lock
 10 Loop (PLL) which will generate a low jitter stable clock to the high speed serializer.

11 A single COLDATA ASIC on each CMB will also be receiving the data from
 12 each of the eight ADCs on board. Each ADC will transmit two streams of data

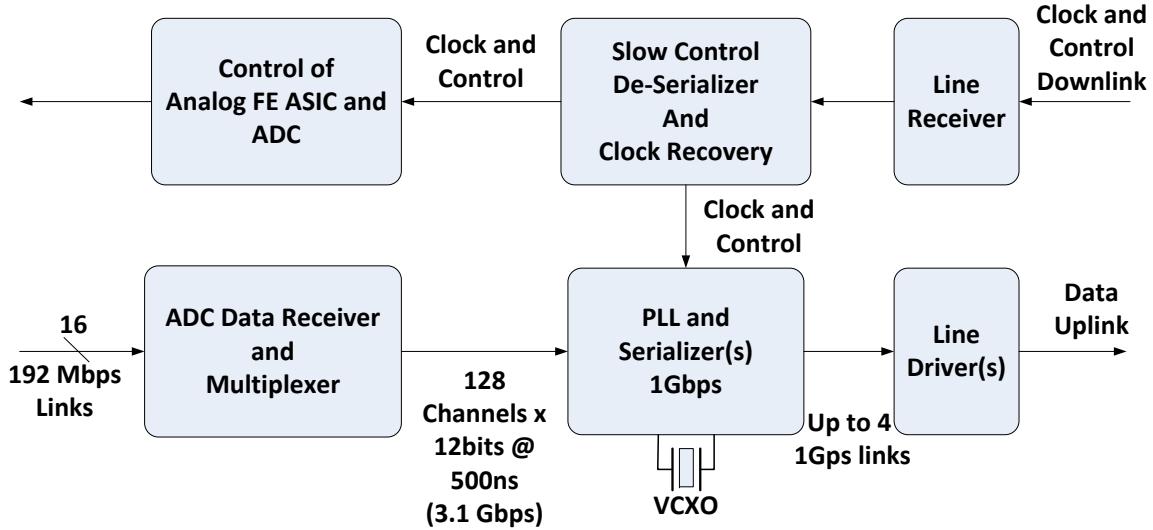


Figure 1.7: Functional Block Diagram of the Cold Digital Data (COLDATA) ASIC

fig:elec_COLDA

- 13 at 192 Mbps for a total data input of 3.072 Gbps. All data will be transmitted off
 14 board. It is anticipated that an encoding scheme, such as 8B10B, will be used and
 15 some frame data will be added to indicate event blocks. Thus, it is planned to drive
 16 four 1 Gbps links from each COLDATA ASIC. A line driver will be designed which
 17 is capable of driving a copper link for the approximate 20 m required to exit the LAr
 18 environment.

1.5 Signal Feedthroughs, Cabling, and Power

- 19 ce_feedthrough
 20 A single type of feedthrough, henceforth “signal feedthrough”, will handle the signals,
 21 supply voltages, and control lines. The TPC data rate per APA, using the full event-
 22 buffer scheme described earlier, is sufficiently low that it is within the capability of
 23 a single LVDS channel on copper, with an overall 32:1 Mux and 80 LVDS channels
 24 per APA. Therefore, all cables inside the cryostat will be copper. In addition to the
 25 high-speed data-output channels, LVDS connections will be made to each APA to
 26 distribute a clock signal and control information. These data can be transmitted at
 27 a lower bit rate. Optical fiber will be employed externally to the cryostat, under
 28 DAQ scope.

29 1.5.1 Signal Feedthroughs

30 No specific design for the Far Detector signal feedthroughs exists at this time. We
 31 are currently exploring the possibility of working in tandem with the Near Detector
 32 group, who have similar feedthrough needs, and are starting with a concept based on
 33 the feedthrough design which has been successfully running in the Atlas experiment
 34 for about 15 years, and has therefore demonstrated both longevity and reliability.
 35 A somewhat different conceptual design of a signal feedthrough flange is shown in
 36 Figure 1.9. Based on a standard 8-in conflat flange with all commercial off-the-shelf
 1 components, each of these feedthroughs would serve the bias/power/digital IO needs
 2 of two APAs.

3 All cables inside the cryostat will be attached to their corresponding feedthroughs
 4 distributed throughout the cryostat roof. The other ends of the cables will be con-
 5 nected to the matching connectors on the APAs in the cryostat. The cables for the
 6 lower APAs must be carefully threaded through the hollow frames of the APA stacks.
 7 The cables will be strain-relieved on the mounting rails above the APAs.

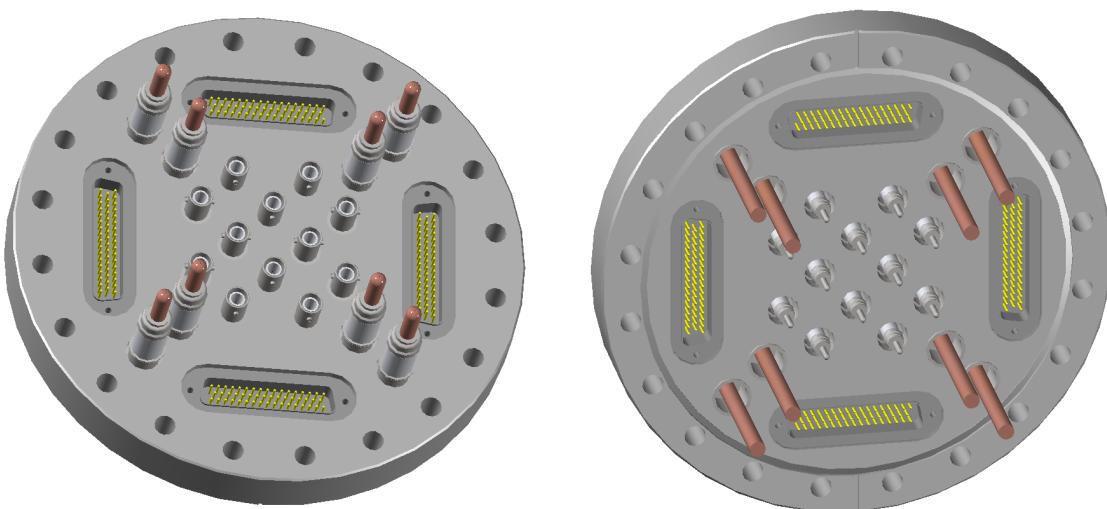


Figure 1.8: A conceptual design of a signal/power feedthrough using all off-the-shelf commercial components

fig:ce_feedthr

8 The 35 Ton prototype detector requires a feedthrough and cable plant similar to
 9 what a single full size APA will require and can serve as a model for at least one
 10 possible solution to the feedthrough problem. In the 35 Ton case, a custom printed
 11 circuit embedded in a single 10" Conflat flange handles all the cabling associated

12 with the TPC and photon detector cabling as well as a small number of cables for a
13 specialized camera system to monitor the Cathode connection. For the 35 Ton APAs
14 there are, in addition to the TPC bias voltages, 16 cold electronics boards with data,
15 power and control wires plus some 74 photon detector signals on individual cables.
16 For a full size Far Detector APA there would be 20 electronics boards with simpler
1 control and power wiring requirements and rather fewer photon detector cables so
2 the 35 Ton feedthrough will serve as a good model for what might be done for the
3 Far Detector. While the electrical connection requirements are straightforward, the
4 reliable gas tightness of the flange with an embedded circuit board needs to be fully
5 verified and the planned method of reducing contamination from the cable plant in
6 the ullage (and the 35 Ton cryostat has a much larger ullage than planned for the far
7 detector) needs to be studied carefully.

8 Measurements in the Materials Test Stand at Fermilab (described in Section ??) sec:mts
9 have shown that impurities (principally O₂ and H₂O) embedded in objects submerged
10 in the liquid argon do not result in a decrease in electron-drift lifetime, whereas
11 impurities in objects located in the warmer gas phase (ullage) do. This indicates
12 the importance of minimizing the amount of material in the gas ullage at the top of
13 the cryostat. Therefore it would be desirable to connect all cables to feedthroughs
14 below the liquid surface, and then pass the cables out of the cryostat, through an
15 evacuated volume that traverses the gas and cryostat insulation, to a matching set
16 of feedthroughs to the outside. In the 35 Ton design, a stainless tube surrounds the
17 cable bundle in the ullage and is partially sealed off below the liquid level to limit
18 contamination. Understanding whether a scheme like this would be sufficient for the
19 longer drift lengths in the far detector is an important question to be addressed.

1.5.2 Cabling for the Cold Electronics

1 There are five basic types of cables which will be required to penetrate the cryostat
2 and service the Cold Electronics. We will require low voltage cables to power the
3 FE boards, wire bias cables to provide the reference voltages for the wire planes,
4 moderate speed cables for a communication downlink to the FE boards, high speed
5 cables to carry the data out of the cryostat and signal cables to carry the photon
6 detection out. All of these cables will pass through the feedthrough port provided
7 for each pair of stacked APAs.

8 The cables will be selected to have a low outgas and provide minimal contam-
9 ination to the LAr environment. The same is true of connectors. Connectors will
10 also need to be tested for usage in LAr to make sure that a low ohmic contact is
11 maintained in the cryogenic environment.

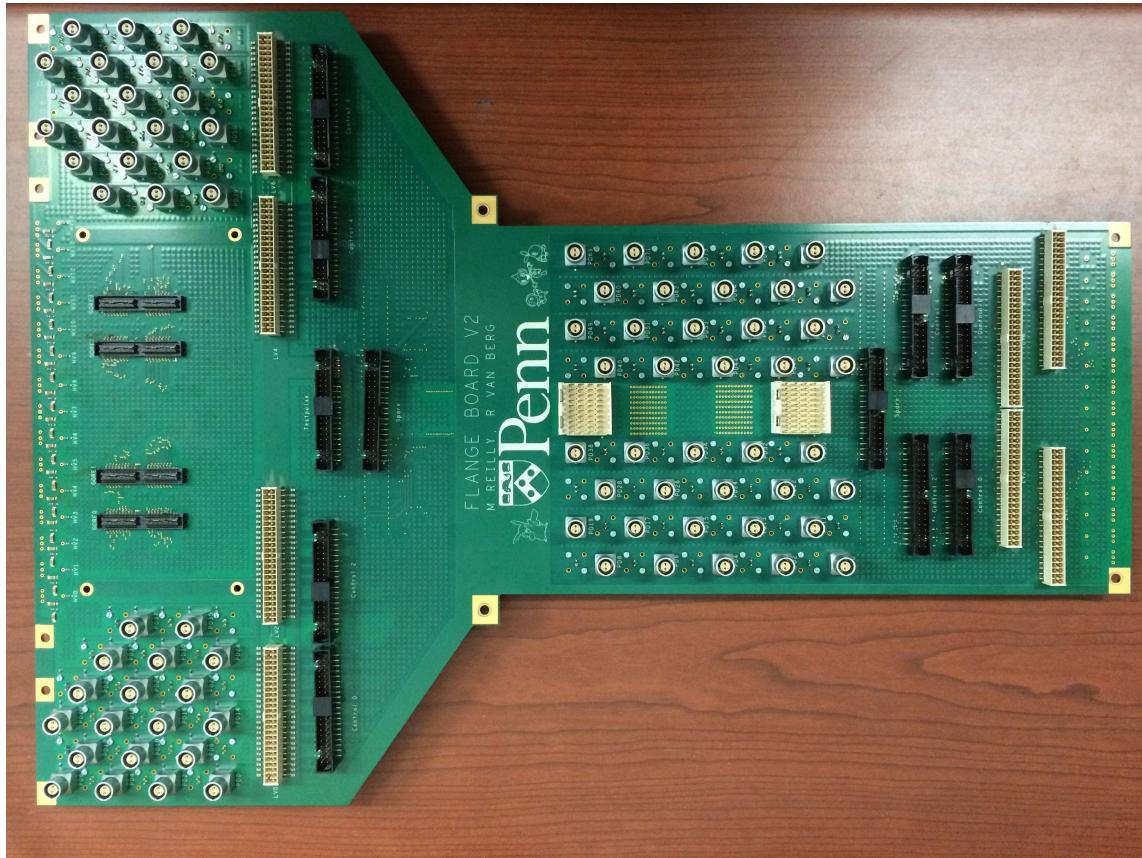


Figure 1.9: Photograph of the 35 Ton “Flange Board”, without the Conflat flange which will be epoxy potted near the center of the printed circuit. This board carries all the electrical connections for the four small APAs in the 35 Ton test cryostat and is similar to the number of connections needed for a Far Detector APA

fig:ce_feedthr

13 Currently, we are looking into several types of cables and connectors. The low
14 voltage cabling will be defined by power needs and whether we decide to go with a
15 higher voltage/lower current feed using DC/DC convertors or a low voltage/higher
16 current feed used by low voltage regulators. Studies will take place to decide the
17 most efficient and practical usage.

18 The wire bias cables must deliver voltages up to a couple thousand volts with
19 less than a couple of millamps. It is anticipated that we use a coaxial cable and
20 connectors which have been tested and found sufficient to provide this load.

21 The cables for the moderate speed downlink could utilize LVDS signaling and
22 low skew pairs. Again, testing will be required to identify and select the final cable
23 and connectors.

24 For the high speed data links, we anticipate using a low skew copper twinax cable.
25 We have prototyped such a cable and found that we can drive data at 2 Gbps for a
26 20 m length.

27 Finally, the photon detector cables currently make use of shielded twisted pair
28 cables which carry both the DC bias voltage as well as the signals. Future work
29 involving these cables is described in the Photon Detector chapter.

30 It will be important that all cables and connectors be somewhat rugged, locking
31 and able to withstand a minimum of several tens of mating cycles. This is in addition
32 to concerns about material compatibility and the fact they must work in the cryogenic
33 environment.

34 **1.5.3 Power for the Cold Electronics**

35 There are two types of power supplies: TPC wire-bias voltages and low-voltage
36 DC power to the readout electronics. The power-per-channel for the FE ASIC is
1 designed to be about 15 mW and the total power requirement for each APA is
2 expected to be about 65 W. Power will be supplied to the electronics on each APA
3 separately by low-noise power supplies outside the cryostat, either directly by low-
4 voltage (1.8 V), high-current (36 A) conductors or by high-voltage (48 V) low-current
5 (2 A) conductors to DC-DC converters placed locally in the LAr. The use of DC-DC
6 converters requires conductors with smaller cross section, minimizing heat input to
7 the cryostat (and ice formation of the feedthroughs). However, the power dissipated
8 by the (somewhat inefficient) converters in the LAr will create boiling which may
9 introduce contamination directly into the high-purity LAr, and if enough LAr is
10 vaporized, may also produce strong mixing of the ullage gas, driving more impurities
11 into the liquid. These effects of boiling LAr, unless they can be demonstrated to
12 be harmless, will drive a preference for eliminating DC-DC converters, and directly

13 powering the front-end readout boards.

14 Heat conduction through the high-current feedthroughs and the self-heating ($I \cdot R$)
15 of the wires are the factors contributing to additional heat load on the cryogenic
16 system. The sum of the these two factors as a function of the wire gauge, however, has
17 a minimum due to the two opposing dependencies on the copper-wire cross section.
18 An optimum wire gauge can be chosen to minimize heat input to the cryostat.

19 **1.5.4 Wire-Bias Voltages**

20 Each anode plane assembly requires three bias voltage connections at +820V, -370V,
21 and -665V. The current on each of these supplies is expected to be zero at normal
22 operation. However the ripple voltage on the supply must be carefully controlled to
23 avoid noise injection into the front-end electronics.

24 The power supplies for the wire bias will be similar to those used for conventional
25 multi-wire proportional chambers. Additional filtering networks will be needed to
26 further reduce voltage ripples. The default feedthroughs are the commercial SHV
27 type. However, other, higher-density multi-channel feedthroughs capable of with-
28 standing the maximum voltage are under investigation.

29 **1.6 CE Installation**

30 Cold electronics will be mounted on the TPC and installed inside the cryostat. Be-
31 cause access to the cold electronics is not possible after the cryostat is sealed, a full
32 complement of tests will be performed during the development stage and before the
33 final installation.

34 **1.6.1 Prototype Testing**

35 Dedicated test boards for the FE ASIC and ADC ASIC, were used to characterize the
36 performance of prototype ASICs at both 300 K and 77 K, and taking them through
1 multiple thermal cycles. An automated test board was built for the FE ASIC to
2 evaluate large numbers of FE ASICs at room temperature, and another such board
3 is currently being designed for the ADC ASIC.

4 The development of the FE and ADC ASICs has proceeded through a series of
5 prototype designs. A 128-ch prototype analog mother board has been developed and
6 tested in the lab. Together with an FPGA mezzanine in place of the digital ASIC
7 mezzanine, they form a front end cold mother board assembly for use in the 35 ton
8 prototype TPC. A test stand has been developed to test the front end mother board

9 assembly using a commercial FPGA evaluation board as a mini-DAQ system. All
10 evaluation test data are stored on a desktop PC and analyzed to determine whether
11 the board is ready to be installed on the detector.

12 During the prototype testing, a procedure has been developed for the production
13 test of the cold electronics boards. This includes key parameters (gain, noise, non-
14 linearity etc.) that should be tested, detailed steps of the test to collect data and
15 extract these parameters, and also the work flows to perform the test at both 300 K
16 and 77K.

17 Prototype cold electronics has been tested with prototype TPC and DAQ system,
18 to evaluate the performance of the APA assembly, and help the development of the
19 DAQ software. A vertical slice test has been used as the test bed for the integration
20 test. It is an important step to identify potential issue, check out system integration
21 and performance before the installation into the cryostat.

22 **1.6.2 Assembly Testing**

23 The front-end readout boards will be thoroughly tested.

- 24 • A small number of the ASICs will undergo a complete suite of tests, including
25 thermal cycling to determine the batch yield.
- 26 • If the yield is high (> 95%), all ASICs will be mounted on the front-end boards.
27 Tests will be performed on each board and bad chips replaced as needed.
- 28 • If the yield is not high, an automated test fixture will be fabricated to validate
29 every ASIC chip before mounting on the readout boards. Board-level tests
30 after mounting the ASICs will be conducted.
- 31 • The fully assembled front-end boards will be thermally cycled multiple times
32 while connected to a simple DAQ system to ensure reliable operation.
- 1 • After the front-end electronics boards have been installed on an APA, an initial
2 calibration of all electronic channels will be performed. The electronic gains
3 and noise levels of all channels will be recorded in a database.
- 4 • Electronic calibration on all channels will be performed while the APA is cold
5 and again after it is warmed up. Significant differences in the cold and warm
6 calibration results will be investigated and remediated.

7 **1.6.3 Commissioning**

8 During installation, the DAQ system will be running continuously. As soon as each
9 stack of APAs is connected to the pre-routed cables, a suite of calibration runs will
10 be performed to validate that all connections have been made properly. Repair or
11 replacement at this stage will still be straightforward.

12 Following the installation of the APAs and the sealing of the cryostat, another
13 complete test will be performed to verify the integrity of cold electronics before the
14 filling with argon. After the cryostat is filled with LAr and the detector cooled down,
15 an electronics calibration test will be performed to evaluate the detector performance
16 prior to data taking.