Low Power NTSC/PAL Video Decoder with Differential CVBS Inputs and MIPI-CSI2 Output Interface

TW9992

The TW9992 is a low power NTSC/PAL analog video decoder that is designed for automotive applications. It supports single-ended, differential and pseudo differential composite video inputs as well as S-Video. Integrated short-to-battery and short-to-ground detection, advanced image enhancement capabilities such as the programmable Automatic Contrast Adjustment (ACA) and the MIPI-CSI2 output interface make the TW9992 an ideal solution for demanding automotive camera applications.

Features

Analog Video Decoder

- Software selectable analog input control allows for combinations of single ended CVBS, and differential CVBS
- Built-in analog antialias filter
- Two 10-bit ADCs and analog clamping circuit
- Fully programmable static gain or automatic gain control for the Y channel
- Programmable white peak control for the Y channel
- 4-H adaptive comb filter Y/C separation
- PAL delay line for color phase error correction
- Digital subcarrier PLL for accurate color decoding
- Digital horizontal PLL for synchronization processing and pixel sampling
- Advanced synchronization processing and sync detection for handling nonstandard and weak signal
- Automatic color control and color killer
- Chroma IF compensation
- VBI slicer supporting industrial standard data services
- VBI data passthrough, raw ADC data output
- Programmable output cropping

Video Processing

- Automatic Contrast Adjustment (ACA)
- RGB565
- Programmable hue, brightness, saturation, contrast and sharpness.
- Image enhancement with peaking and CTI

MIPI Output

- MIPI 1.1 compliant unidirectional output format
- YUV 422 or RGB565 output format

Digital Output

- Output voltage 1.8V to 3.3V with 3.3V tolerance

Miscellaneous

- Low power consumption: 100mW typical
- Power save and Power-down mode
- Short-to-battery detection test
- Short-to-ground detection test
- Two-wire MPU serial bus interface
- Supports real time control interface
- Single 27MHz crystal for all operations
- Supports 24.54MHz and 29.5MHz crystal for high resolution square pixel format decoding
- 3.3V tolerant I/O
- 1.8V/3.3V power supply
- 32 Ld QFN (WQFN with wettable flanks)

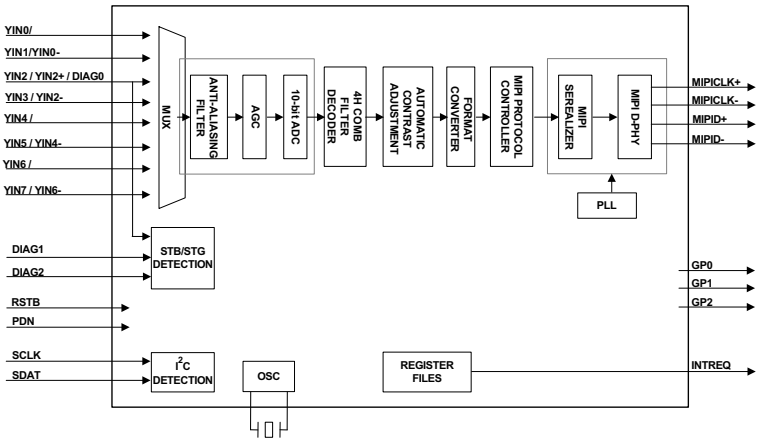
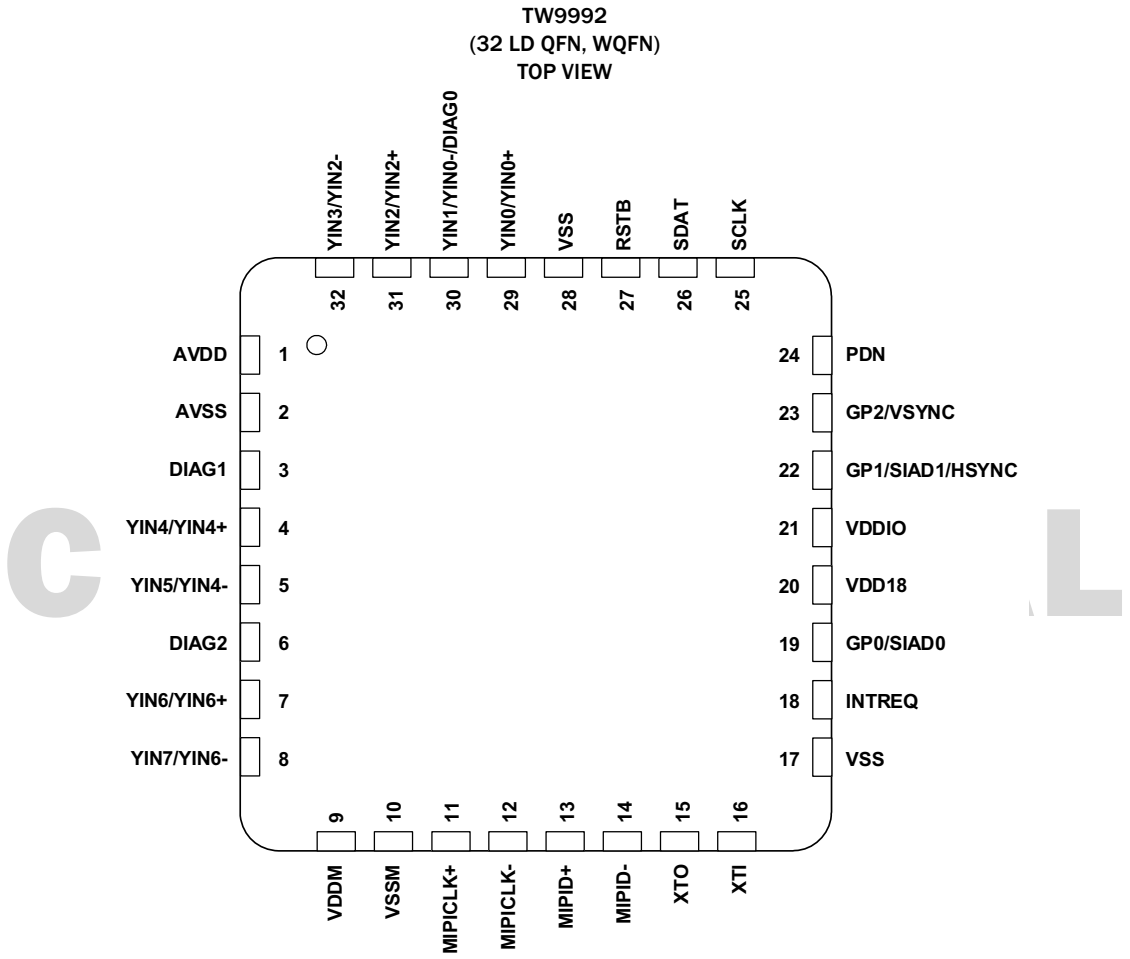


FIGURE 1. TW9992 FUNCTIONAL BLOCK DIAGRAM

Table of Contents

Pin Configuration



Pin Descriptions

PIN#	I/O	PIN NAME	DESCRIPTION
ANALOG VIDEO SIGNALS			
29	I	YIN0/YIN0+	Single-ended analog CVBS or Y input. For differential CVBS connect negative input. Connect unused input to AGND through 0.1µF capacitor.
30	I	YIN1/YIN0-/DIAG0	Single-ended analog CVBS or Y input. For differential CVBS connect positive input. STB/STG detection. Connect unused input to AGND through 0.1µF capacitor.
31	I	YIN2/YIN2+	Single-ended analog CVBS or Y input. For differential CVBS connect positive input. Connect unused input to AGND through 0.1µF capacitor.
32	I	YIN3/YIN2-	Single-ended analog CVBS or Y input. For differential CVBS connect negative input. Connect unused input to AGND through 0.1µF capacitor.
3	I	DIAG1	STB/STG detection. Connect unused input to AGND through 0.1µF capacitor.
4	I	YIN4/YIN4+	Single-ended analog CVBS or Y input. For differential CVBS connect negative input. STB/STG detection mode disables pin as a video input. Connect unused input to AGND through 0.1µF capacitor.
5	I	YIN5/YIN4-	Single-ended analog CVBS or Y input. For differential CVBS connect positive input. Connect unused input to AGND through 0.1µF capacitor.
6	I	DIAG2	STB/STG detection. Connect unused input to AGND through 0.1µF capacitor.
7	I	YIN6/YIN6+	Single-ended Analog CVBS or Y input. For differential CVBS connect positive input. Connect unused input to AGND through 0.1µF capacitor.

Pin Descriptions (Continued)

PIN#	I/O	PIN NAME	DESCRIPTION
8	I	YIN7/YIN6-	Single-ended Analog CVBS or Y input. For differential CVBS connect negative input. Connect unused input to AGND through 0.1µF capacitor.
MIPI SIGNALS			
11	O	MIPICLK+	MIPI Clock
12	O	MIPICLK-	MIPI Clock
13	O	MIPID+	MIPI Data
14	O	MIPID-	MIPI Data
CRYSTAL CLOCK SIGNALS			
15	O	XTO	Clock output. Connected to a crystal.
16	I	XTI	Clock input. A 27MHz fundamental (or 3rd overtone) crystal or a single-ended oscillator can be connected.
GENERAL SIGNALS			
18	O	INTREQ	Interrupt output signal.
19	I/O	GP0/SIAD0	General purpose IO; Power-on serial IO bus address LSB select
22	I/O	GP1/SIAD1/HSYNC	General purpose IO; Power-on serial IO bus address selection: “0” for 88/8A, “1” for 78/7A.
23	I/O	GP2/VSYNC	General purpose IO
24	I	PDN	Power-down control pin. High active Schmitt trigger input
27	I	RSTB	Reset input. Low active Schmitt trigger input
SERIAL IO INTERFACE			
25	I	SCLK	The MPU Serial interface Clock Line. (Schmitt trigger)
26	I/O	SDAT	The MPU Serial interface Data Line. (Schmitt trigger)
POWER AND GROUND PINS			
20	I	VDD18	1.8V digital core power
17, 28	I	VSS	1.8V digital core return
21	I	VDDIO	3.3 /1.8V digital I/O power
1	I	AVDD	1.8V analog ADC supply
2	I	AVSS	1.8V analog ADC return
9	I	VDDM	1.8V MIPI supply
10	I	VSSM	1.8V MIPI return

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
TW9992AT-NA1-GE	TW9992AT NA1-GE	-40 to +105	32 LD WQFN	L32.5x5H
TW9992-NA1-CE	TW9992 NA1-CE	-40 to +85	32 LD QFN	L32.5x5L
TW9992-NA1-EVAL	Evaluation Board			

NOTES:

1. Add “T” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu-Ag plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see product information page for TW9992. For more information on MSL, please see tech brief TB363.

Absolute Maximum Ratings

AVDD to AVSS . . . . . -0.5V to +2.3V
VDDM to VSSM . . . . . -0.5V to +2.3V
VDD18 to VSS . . . . . -0.5V to +2.3V
VDDIO to VSS. . . . . -0.5V to +4.2V
Any Digital Pin to VSS . . . . . -0.5V to +5.5V
Any Analog Pin to AVSS . . . . . -0.5V to +2.3V
ESD Ratings
Human Body Model (Tested per AEC-Q100-002)
TW9992. . . . . 2kV
TW9992AT 2.5kV
Machine Model (Tested per AEC-A100-003). 250V
Charged Device Model (Tested per AEC-Q100-011). 750V
Latch-up (Per JESD-78D; Class 2, Level A; AEC-Q100-004). 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
TW9992, 32 Ld QFN Package (Notes 4, 5)	30	1.8
TW9992AT, 32 Ld QFN Package (Notes 4, 5)	29	1.2

Junction Temperature Range . . . . . -55°C to +125°C
Storage Temperature Range. . . . . -65°C to +150°C
Ambient Temperature Range . . . . . -40°C to +105°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

AVD,VDDM,VDD. . . . . +1.62V to +1.98V
VDD33 . . . . . +2.97V to +3.6V
Ambient Temperature
TW9992. . . . . -40°C to +85°C
TW9992AT. . . . . -40°C to +105°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
5. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Unless otherwise noted, the typical specifications are measured at the following conditions: VDD18 = AVDAD = AVDPLL = 1.8V, VDD33 = VDDO = 3.3V, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +85°C (TW9992), -40°C to +105°C (TW9992AT).**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
INPUT SUPPLY						
IAA18	Analog Supply Current 1.8V		-	16.2	-	mA
IDD33	Digital I/O Supply Current 3.3V		-	2.8	-	mA
IDDO	Digital I/O Supply Current 1.8V		-	1	-	mA
IDDM	Digital MIPI Supply Current 1.8V		-	14.4	-	mA
IDD	Digital Core Supply Current 1.8V		-	27.6	-	mA
DIGITAL INPUTS						
VIH33	Input High Voltage (TTL/CMOS 3.3V Logic)		**2.0**	-	-	V
VIH18	Input High Voltage (TTL/CMOS 1.8V Logic)		**1.17**	-	-	V
VIHS33	Input High Voltage for Schmitt Trigger (TTL/CMOS 3.3V Logic)		**2.0**	-	-	V
VIHS18	Input High Voltage for Schmitt Trigger (TTL/COMS 1.8V Logic)		**1.2**	-	-	V
VIL33	Input Low Voltage (TTL/CMOS 3.3V Logic)		-	-	**0.8**	V
VIL18	Input Low Voltage (TTL/CMOS 1.8V Logic)		-	-	**0.63**	V
VILS33	Input Low Voltage for Schmitt Trigger (TTL/CMOS 3.3V Logic)		-	-	**0.8**	V
VILS18	Input Low Voltage for Schmitt Trigger (TTL/CMOS 1.8V Logic)		-	-	**0.48**	V
IIL, IIH	Input Leakage Current		**-10**	-	**10**	µA
CIN	Input Capacitance	f = 1MHz, VIN = 2.4V	-	5		pF
DIGITAL OUTPUTS						
VOH33	Output High Voltage	IOH = –2mA	**2.4**	-	-	V
VOH18	Output High Voltage	IOH = –2mA	**1.35**	-	-	V
VOL33	Output Low Voltage	IOL = 2mA	-	-	**0.4**	V

Electrical Specifications

Unless otherwise noted, the typical specifications are measured at the following conditions: VDD18 = AVDAD = AVDPLL = 1.8V, VDD33 = VDDO = 3.3V, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +85°C (TW9992), -40°C to +105°C (TW9992AT). (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
VOL18	Output Low Voltage	IOL = 2mA	-	-	**0.45**	V
IOZ	3-State Leakage Current		**-10**	-	**10**	µA
CO	Output Capacitance		**-**	5	**-**	pF
MIPI OUTPUTS LOW POWER						
V_{OL_LP}	Output Low Voltage		**-50**	-	**50**	mV
Z_{O_LP}	Output Impedance		**110**	-	**-**	Ω
$\delta V/\delta t_{SR}$	Slew Rate at C_{LOAD} = 0pF		**-**	-	**500**	mV/ns
$\delta V/\delta t_{SR}$	Slew Rate at C_{LOAD} = 70pF		**-**	-	**150**	mV/ns
MIPI OUTPUTS HIGH SPEED						
V_{CMTX}	Static Common Mode Voltage		**150**	200	**250**	mV
$\lvert\Delta V_{CMTX(1,0)}\rvert$	V_{CMTX} Mismatch Between $V_{OD(0)}$ and $V_{OD(1)}$		**-**	-	**5**	mV
$\Delta V_{CMTX(LF)}$	V_{CMTX} Common level variation		**-**	-	**25**	mV_{PEAK}
$\lvert V_{OD}\rvert$	Differential Voltage		**140**	200	**270**	mV
$\lvert\Delta V_{OD}\rvert$	V_{OD} Mismatch Between $V_{OD(0)}$ and $V_{OD(1)}$		**-**	-	**14**	mV
V_{OHHS}	Output High Voltage		**-**	-	**360**	mV
Z_{OS}	Single-ended Output Impedance		**40**	50	**62.5**	Ω
$\lvert\Delta Z_{OS}\rvert$	Z_{OS} Mismatch		**-**	-	**10**	%
V_{OL_LP}	Output Low Voltage		**-50**	-	**50**	mV
ANALOG INPUTS						
	YIN0~YIN3, CIN0,1, VIN0, 1 Input Range	AC Coupling	**0.5**	1.0	**1.4**	V_{P-P}
	SOG0,1 Input Range		**-**	0.3	**-**	V_{P-P}
C A	Analog Pin Input Capacitance		**-**	7	**-**	pF
HORIZONTAL PLL						
Δf_H	Static Deviation		**-**	-	**6.2**	%
Δf_H	Lock In Range		**±450**	-	**-**	Hz

NOTES:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Crystal Requirement

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
	Nominal Frequency (Fundamental)		27		MHz
	Deviation		-	±50	ppm
RS	Series Resistor		80		Ω

Serial Host Interface Timing

SYMBOL	PARAMETER	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
t_{BF}	Bus Free Time between STOP and START	500			ns
t_{sSDAT}	SDAT Setup Time	50			ns
t_{hSDAT}	SDAT Hold Time	-		0	ns
t_{sSTA}	Setup Time for START Condition	260			ns
t_{sSTOP}	Setup Time for STOP Condition	260			ns
t_{hSTA}	Hold Time for START Condition	260			ns
t_{R_SB}	Rise Time for SCLK and SDAT			120	ns
t_{F_SB}	Fall Time for SCLK and SDAT			120	ns
C_{BUS}	Capacitive Load for Each Bus Line			550	pF
f_{SCLK}	SCLK Clock Frequency			1000	kHz
t_{LOW}	SCLK Low Time	260			ns
t_{HIGH}	SCLK High Time	500			ns

NOTE:

7. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design

Serial Host Interface Timing Diagram

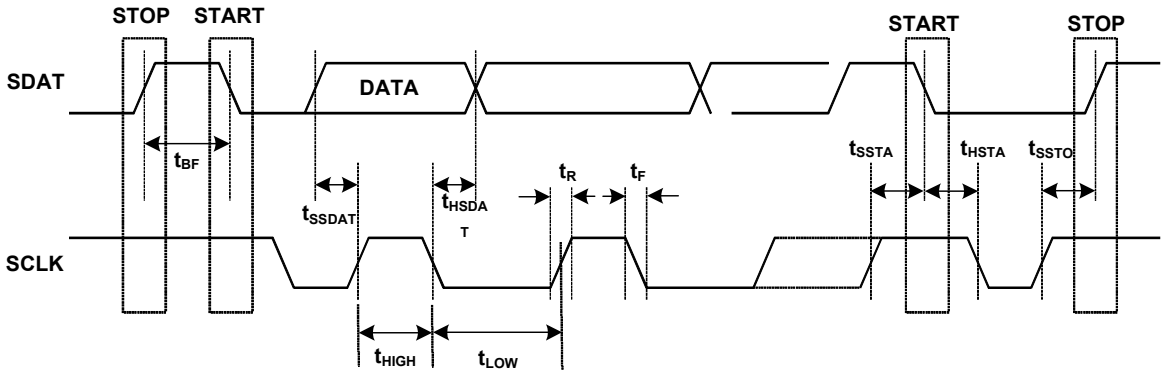


FIGURE 2. SERIAL HOST INTERFACE TIMING DIAGRAM

MIPI Low Power AC Timing

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t_{RLP}/t_{FLP}	Rise/Fall Time 15% to 85% of V_{OH} - V_{OL}	-	16.9/ 14.3	-	ns	At C_{LOAD} = 70pF
t_{REOT}	Rise/Fall Time 30% to 85% from HS EOT Common Level Drops Below 70mV	-	26	-	ns	At C_{LOAD} = 70pF with additional RX side load cap of 60pF
$t_{LP-PULSE-TX}$	Pulse Width of LP XOR Clock	-	74	-	ns	First/last pulse after/before Stop state
$t_{LP-PULSE-TX}$		-	64	-	ns	All other pulses
$t_{LP-PER-TX}$	Period of LP XOR Clock	-	148	-	ns	
t_{LPX}	Transmitted Length (duration) of any Low Power State	-	74	-	ns	This is an internal parameter
$f_{LP(MAX)}$	Maximum Low Power Toggle Frequency	-	6.76	-	MHz	Equivalent to 2*T_{LPX} ns period

MIPI Waveform

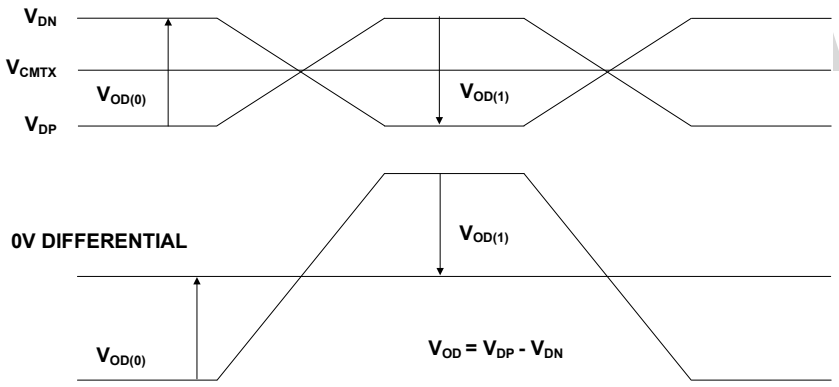


FIGURE 3. MIPI WAVEFORM

MIPI High Speed AC Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Unit Interval Instantaneous	UI_{INST}	-	4.629	-	ns	
UI Variation	ΔUI	-10%	-	10%	UI	Variation within a single burst with UI ≥ 1ns
Clock Lane DDR Clock Frequency (= $1/(2*UI_{INST\ MIN})$	fh_{MAX}	-	108		MHz	At f_{XTAL} = 27MHz with 8b line coding
Rise/Fall Time 20% to 80%	t_R /t_F	-	-	0.3	UI	UI ≥ 1ns
		150	-	-	ps	
Data to Clock Skew	t_{SKEW}	-0.15	-	0.15	UI_{INST}	UI ≥ 1ns

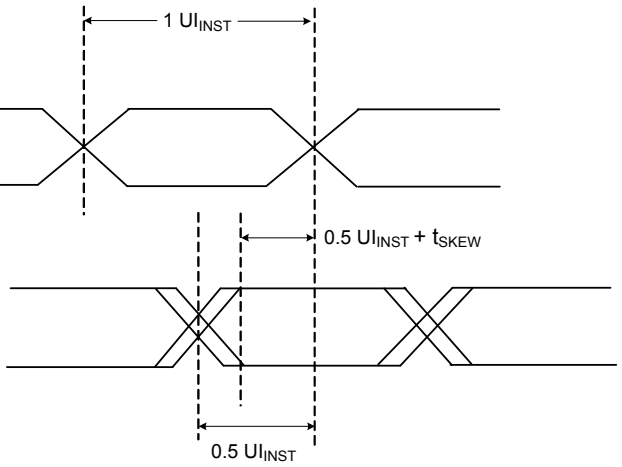


FIGURE 4. MIPI HIGH SPEED AC TIMING DIAGRAM

MIPI Protocol AC Timing

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
$T_{INIT(MASTER)}$	Master/Transmitter Initialization	-	300	-	µs	Stop State is driven; All lanes are initialized simultaneously
T_{WAKEUP}	Wake Up from ULPS	-	1.02	-	ms	Mark-1 State is driven
$T_{CLK-PREPARE}$	Clock Lane in Bridge State (LP - 00)	-	74	-	ns	
$T_{CLK-PREPARE} + T_{CLK-ZERO}$	Clock Lane in “Zero” State (Interval of: LP - 00 + HS - 0)	-	370	-	ns	
$T_{CLK-PRE}$	Clock Lane Pre Drive before Data Lane Exits from Stop State	-	14	-	UI	
$T_{HS-PREPARE}$	Data Lane in Bridge State (LP-00)	-	74	-	ns	
$T_{HS-PREPARE} + T_{HS-ZERO}$	Data Lane in “Zero” State (Interval of: LP-00 + HS-0)	-	370	-	ns	
$T_{HS-TRAIL}$	Interval of Data Lane in Flipped Differential State after Last Payload Data Bit Transmission	-	85	-	ns	
$T_{CLK-POST}$	Interval of Clock Lane Continual Transmission Past $T_{HS-TRAIL}$	-	325	-	ns	
$T_{CLK-TRAIL}$	Interval of Clock Lane in HS-0 State Past $T_{CLK-POST}$	-	105	-	ns	
T_{EOT}	Interval from Start of $T_{CLK-TRAIL}$ ($T_{HS-TRAIL}$) to Start of LP-11 State	-	-	-	ns	$T_{CLK-TRAIL}$ for Clock Lane, and $T_{HS-TRAIL}$ for Data Lane
$T_{HS-EXIT}$	Clock (Data) Lane in LP-11 State Past $T_{CLK-TRAIL}$ ($T_{HS-TRAIL}$)	-	1000	-	ns	

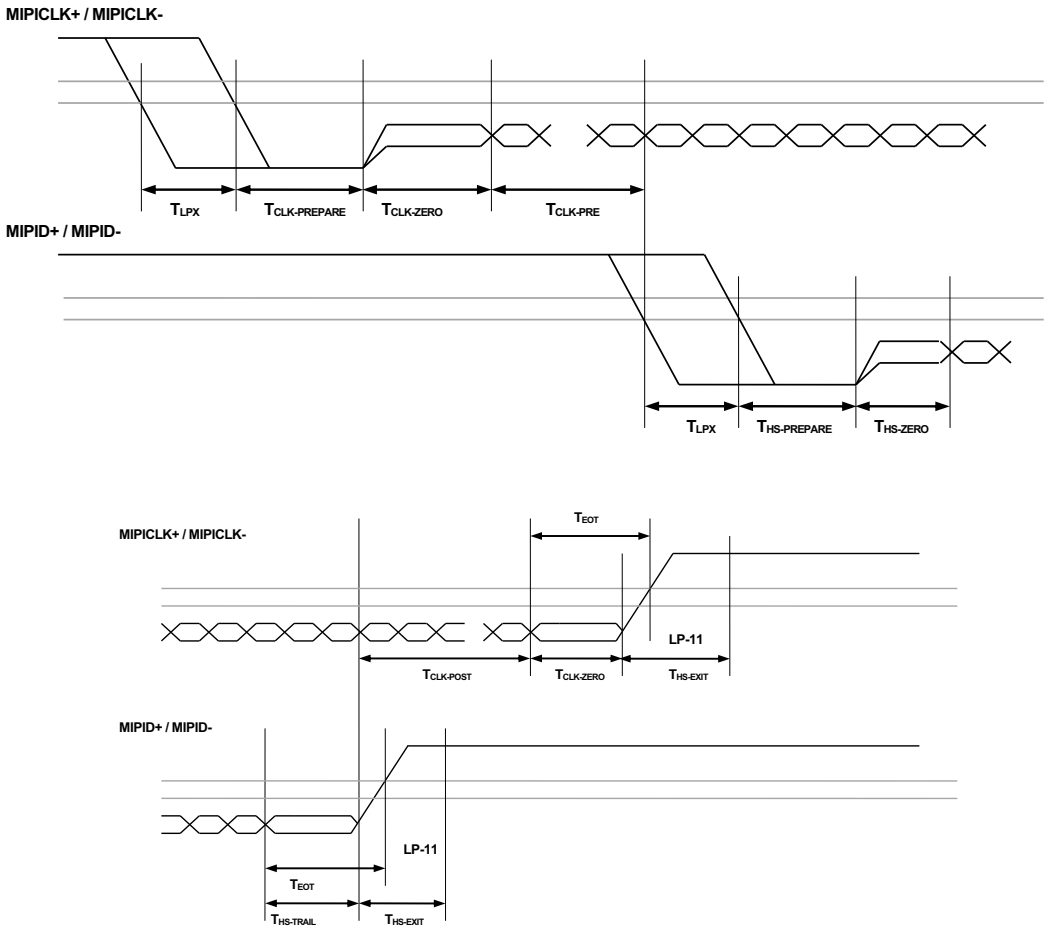


FIGURE 5. MIPI AC TIMING DIAGRAMS

Thermal PAD Considerations

Thermal Pad Land Design Input

The size of the thermal land should at least match the exposed die flag size. But it is necessary to avoid solder bridging between thermal pad and the perimeter pads. We recommend the clearance between thermal pad and perimeter pads is 0.15 mm.

Thermal Via Design

In order to take full advantage of QFN thermal performance, thermal vias are needed to provide a thermal path from top to inner/bottom layers of the motherboard to remove the heat.

- Via size (in diameter): 0.3 ~ 0.33mm
- Via pitch: 1.0 ~ 1.2 mm
- # of thermal vias: depend on the application

STENCIL RECOMMENDATION

- The small multiple openings should be used instead of one big opening.
  - 60 ~ 85% solder paste coverage
  - Rounded corners to minimize clogging
  - Positive taper with bottom opening larger than the top

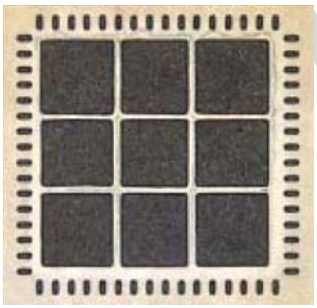


FIGURE 6. NOT RECOMMENDED COVERAGE 91%

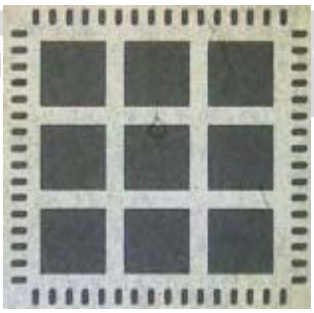


FIGURE 7. RECOMMENDED COVERAGE 77%

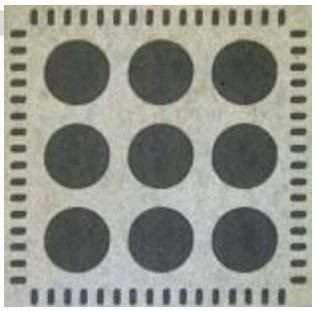


FIGURE 8. RECOMMENDED COVERAGE 65%

Control Registers

TW9992 Register Summary

The registers are organized in functional groups in this Register Summary.

INDEX (HEX)	7	6	5	4	3	2	1	0	RESET (HEX)
00	ID								92
01	Revision				Revision				00
DECODER									
02	-	FC27	IFSEL		YSEL				48
03	VDLOSS	HLOCK	SLOCK	FIELD	VLOCK	-	MONO	DET50	-
04	-	CKHY		-					00
05	Hsp	Vsp	SAVE	-	FBPY	-	-	DEC_SEL	09
06	SRESET	-		AGC_EN	-				00
07	VDELAY_HI		VACTIVE_HI		HDELAY_HI		HACTIVE_HI		02
08	VDELAY_LO								12
09	VACTIVE_LO								F0
0A	HDELAY_LO								0F
0B	HACTIVE_LO								D0
0C	PBW	DEM	PALSW	SET7	COMB	HCOMP	YCOMB	PDLY	CC

Control Registers (Continued)

TW9992 Register Summary

The registers are organized in functional groups in this Register Summary.

INDEX (HEX)	7	6	5	4	3	2	1	0	RESET (HEX)
0D	GenLock Test	Ntsc656	WSSEN	CCODDLINE					00
10	BRIGHTNESS								00
11	CONTRAST								64
12	SCURVE	VSF	CTI		SHARPNESS				11
13	SAT_U								80
14	SAT_V								80
15	HUE								00
17	SHCOR				-	VSHP			80
18	CTCOR		CCOR		VCOR		CIF		44
19	-				RTSEL				06
1A	-	EDS_EN	CC_EN	PARITY	FF_OVF	FF_EMP	CC_EDS	LO_HI	10
1B	CC_DATA								-
1C	DTSTUS	STDNOW			ATREG	STANDARD			0F
1D	START	PAL60	PALCN	PALM	NTSC4	SECAM	PALB	NTSCM	7F
1F	TEST_DEBUG								00
20	CLPEND				CLPST				50
21	NMGAIN				WPGAIN			AGCGAIN8	22
22	AGCGAIN[7:0]								F0
23	PEAKWT								D8
24	CLMPLD	CLMPL							BC
25	SYNCTD	SYNCT							B8
26	MISSCNT				HSWIN				44
27	PCLAMP								38
28	VLCKI		VLCKO		VMODE	DETV	AFLD	VINT	00
29	BSHT			VSHT					00
2A	CKILLMAX		CKILLMIN						78
2B	FCOMB	HTL			VTL1	VTL			44
2C	CKLM	YDLY			HFLT				30
2D	-	EVCNT	-	SDET	TBC_EN	BYPASS	SYOUT	-	14
2E	HPM		ACCT		SPM		CBW		A5
2F	NKILL	PKILL	SKILL	CBAL	FCS	LCS	CCS	BST	E0
30	SID_FAIL	PID_FAIL	FSC_FAIL	SLOCK_FAIL	CSBAD	MVCSN	CSTRIPE	CTYPE	-
31	VCR	WKAIR	WKAIR1	VSTD	NINTL	WSSDET	EDSDET	CCDET	-
32	HFREF/GVAL/PHERRDO/CGAINO/BAMPO/MINAVG/SYTHRD/SYAMP								-
33	FRM		YNR		CLMD		PSP		05
34	INDEX		NSEN/SSEN/PSEN/WKTH						1A
35	CTEST	YCLEN	CCLEN	VCLEN	GTEST	VLPF	CKLY	CKLC	00

Control Registers (Continued)

TW9992 Register Summary

The registers are organized in functional groups in this Register Summary.

INDEX (HEX)	7	6	5	4	3	2	1	0	RESET (HEX)
36	GAIN_SEL		ACLAMP_EN	DCLAMP_EN	CL_MARGIN	TOGGLE_ MODE	CM_CLAMP_MODE		32
37	-		PGA_BIAS[1:0]		HSPGA_EN	-	AAFLPF[1:0]		1A
38	VCMIN_SEL		DCLAMP_ATTEN		ADC_BIAS		IBINBUF_SEL		D9
39	ACLAPM_ATTEN		PASSIVE_ CLAMP	RES_ REFERENCE	-				00
3A	-	SH_THRESH_GND			-	SH_THRESH_BAT			30
3B	-		SH_EN_GND2	SH_EN_BAT2	SH_EN_GND1	SH_EN_BAT1	SH_EN_GND0	SH_EN_BAT0	00
3C	PRECOND	-	AGND_EN	AN_TEST_EN	-		AN_TEST_SEL		80
3D	GAIN_SEL		-		-	PDS2	PDS1	PDS0	00
3F	F1LIEN	F2LIEN	LINENUMBER						1A
VBI									
40	CRCERR	WSSFLD	-		WSS[19:16]				80
41	WSS[15:8]								00
42	WSS[7:0]								00
48	-	LOCK_WTX	LOCK_RDX	AINC	EXTCLK_ENA	OEN	TRI656	DRVSTR	06
49	-					Y16	BT7	RGB565	00
4A	VSP	VSSL			HSP	HSSL			00
4B	CK2S		CK1S		INTOEN	INTPOL	GPSYNCO	DNB_REV	08
4C	-				CLK_PDN	Y_PDN	-		00
4D	-				VSHALF	HSHALF	-	HSYNCODLY [8]	00
4E	HSYNCODLY[7:0]								00
50	GEM1X	GEM2X	VITC	VPS	WST	WSS	EDS	CC	00
51	LINE_INT	-	VDLOSS	DET50	-	SLOCK	HVLOCK	VCR	00
52	-						SHT_GND	SHT_BAT	00
53	GEM1X_STS	GEM2X_STS	VITC_STS	VPS_STS	WST_STS	WSS_STS	EDS_STS	CC_STS	00
54	LINE_INT_STS	MACROV_STS	VDLOSS_ STS	DET50_ STS	-	SLOCK_ STS	HVLOCK_STS	VCR_STS	00
55	-	-	STG_STS2	STB_STS2	STG_STS1	STB_STS1	STG_STS0	STB_STS0	00
56	-	-	-	-	-	IRQ1_ENA			00
57	IRQ2_ENA				-	IRQ2_ENA			00
58	-						IRQ3_ENA		00
60	-				GP3E	GP2E	GP1E	GP0E	00
61	-				GP3OE	GP2OE	GP1OE	GP0OE	00
62	-				GP3OD	GP2OD	GP1OD	GP0OD	00
63	-				GP3I	GP2I	GP1I	GP0I	00

Control Registers (Continued)

TW9992 Register Summary

The registers are organized in functional groups in this Register Summary.

INDEX (HEX)	7	6	5	4	3	2	1	0	RESET (HEX)
MIPI TRANSMITTER REGISTERS									
70	PD_MIPI	TMLS_MIPI	TMHS_MIPI	PAL	PROGRE-SSIVE	LANE_NO			81
71	LNINC1	SWAP_CRC	1FE	PIC_WIDTH[12:8]					85
72	PIC_WIDTH[7:0]								A0
73	SWAP_YC	HS_DPHY_TEST	FS_SP	PIC_HEIGHT[12:8]					01
74	PIC_HEIGHT[7:0]								E0
75	-	FPGA	SDPROG	BLANK_LINE[12:8]					00
76	BLANK_LINE[7:0]								17
77	HSCK_FSFE	HSCK_LSLE	P720	FS_COUNT[12:8]					05
78	FS_COUNT[7:0]								88
79	-	-	LIM656	LS_COUNT[12:8]					06
7A	LS_COUNT[7:0]								28
7B	CHP_ID[1:0]		SM_FRM	ACT_LS_COUNT[12:8]					46
7C	ACT_LS_COUNT[7:0]								B3
7D	INT_PAT	CH_ID		FE_COUNT[12:8]					06
7E	FE_COUNT[7:0]								13
7F	FLDPOL	NOVID	ULPS_FSYNC	NOLN_START	HSCK_ALWAYS_ON	PAL	VC1[1:0]		00
80	WORD_COUNT[15:8]								05
81	WORD_COUNT[7:0]								A0
82	LPX_CNT[3:0]				HS_PREPARE				12
83	HS_ZERO								05
84	HS_TRAIL								02
85	CLK_AHEAD								0E
86	CLK_POST								08
87	MARK_CNT								37
88	-	FORCE_ULPS	ESC_EXIT	LPDT_MODE	RST_MODE	-	ESC_MODE	LINECODE_9B	00
89	WAIT_FRAMES[7:0]								00
8A	EOT_PERIOD[7:0]								02
8B	CLK_PREPARE				CLK_PRE				11
8C	LP11_CNT				CLK_TRAIL				22
8D	CLK_ZERO								03
8E	SHORT_PKT_DELAY				CLK_SOT_CNT				22
8F	ULPS_LP11_CNT								01
90	PRBS_ER_RST	ATG_RESYNC	-	TESTSET0	ATG_INV8	PRBS_SEL	HSTEST_SEL	ATEST_EN	00
91	ESCAPE_DELAY								0C

Control Registers (Continued)

TW9992 Register Summary

The registers are organized in functional groups in this Register Summary.

INDEX (HEX)	7	6	5	4	3	2	1	0	RESET (HEX)
92	PRBS_ERR_DET	-							00
93	FRM_START_LNCNT								0E
94	-	-	-	-	-	INPUT_PIC_HEIGHT[10:8]			00
95	INPUT_PIC_HEIGHT[7:0]								00
96	SP_HSCK_CNT								1A
9B	RESYNC_DELAY_COUNT								02
A0	CTRL_BIT_DATA								00
A1	CTRL_BIT_CLK								00
A2	RON	LOWF	RESETB_PLL	DPHY_RSTB	PWD_BG	PWD_PLL	PWD_DATA	PWD_CLK	0F
A3	PLOCK	FLOCK	VCTL_HIGH	RST_OFF	ITUNE				00
A4	-								00
ACA REGISTERS									
C0	ACA_DBG	HIST_WIN_EN	-	ACA_BYPASS	LPOFF	MLHCOMP	MDLTON	ACA_ON	06
C1	-		ACA_GAIN						20
C2	-		YAVGHLIM						20
C3	-		YAVGLLIM						08
C4	-				YMINMAXR				09
C5	-			BLKLVL					10
C6	-				YCENTER				06
C7	-			WHTLVL					00
C8	-	MOFSLIM							38
C9	-			MOFSSLOPE					10
CA	-		MOFSUPGAIN						1C
CB	-		MOFSDNGAIN						14
CC	-			MDLTCUT					0A
CD	-			MDLTSLOPE					1F
CE	-		YLHAVGDIFF						1A
CF	-			LMAXGRAD					0C
D0	-			HMAXGRAD					0C
D1	-			LGRADUP					0C
D2	-			LGRADDN					08
D3	-			HGRADUP					04
D4	-			HGRADDN					0C
D5	-				LPFCOEFF				04
D6	PDF_INDEX						ACA_MASK	READ_EN	00
D7	HAVST_HIST								00

Control Registers (Continued)

TW9992 Register Summary

The registers are organized in functional groups in this Register Summary.

INDEX (HEX)	7	6	5	4	3	2	1	0	RESET (HEX)
D8	-							HAVSIZE_HIST_HI	01
D9	HAVSIZE_HIST_LO								68
DA	VAVST_HIST								00
DB	-							VAVSIZE_HIST_HI	01
DC	VAVSIZE_HIST_LO								20
E0	YAVG_RAW								76
E1	YAVG_LIM								75
E2	LOW_AVG								4D
E3	HIGH_AVG								AB
E4	Y_MAX								2A
E5	Y_MIN								E0
E6	MOFFSET								07
E7	LGRAD								EB
E8	HGRAD								03
E9	LL_SLOPE								39
EA	LH_SLOPE								4F
EB	HL_SLOPE								3D
EC	HH_SLOPE								3B
ED	X_LOW								42
EE	X_MEAN								75
EF	X_HIGH								B0
F0	Y_LOW								3D
F1	Y_MEAN								7C
F2	Y_HIGH								B4
F3	-						DIS_LINE_EN		02
F4	-							DIS_LINE_SP_HI	00
F5	DIS_LIEN_SP_LO								00

NOTE:

8. "-" for Register means "Reserved", for reset value it means "unknown".

TW9992 Register Descriptions

BIT	FUNCTION	R/W	DESCRIPTION	RESET
0X00 - PRODUCT ID CODE REGISTER (ID)				
7-0	ID	R	Product ID code	92h
0X01 - PRODUCT REVISION CODE REGISTER (ID)				
7-0	REV	R	Revision Number	0
0X02 - INPUT FORMAT (INFORM)				
7	Reserved	R/W	Reserved	-
6	FC27	R/W	1 = Input crystal clock frequency is 27MHz. 0 = Square pixel mode. Must use 24.54MHz for 60Hz field rate source or 29.5MHz for 50Hz field rate source.	1
5-4	IFSEL	R/W	0 = Composite video decoding Others = N/A	0
3-0	YSEL[3:0]	R/W	These three bits control the input video selection. It selects the composite video source For single-ended input: 0 = YIN0 1 = YIN1 2 = YIN2 3 = YIN3 4 = YIN4 5 = YIN5 6 = YIN6 7 = YIN7 For differential input: 8 = YIN0± 9 = YIN2± 10 = YIN4± 11 = YIN6± Codes 12-15 disconnect the input	8
0X03 - DECODER STATUS REGISTER I (STATUS1)				
7	VDLOSS	R	1 = Video not present. (Sync is not detected in number of line periods specified by MISSCNT register) 0 = Video detected.	0
6	HLOCK	R	1 = Horizontal sync PLL is locked to the incoming video source. 0 = Horizontal sync PLL is not locked.	0
5	SLOCK	R	1 = Subcarrier PLL is locked to the incoming video source. 0 = Subcarrier PLL is not locked.	0
4	FIELD	R	1 = Odd field is being decoded. 0 = Even field is being decoded.	0
3	VLOCK	R	1 = Vertical logic is locked to the incoming video source. 0 = Vertical logic is not locked.	0
2	Reserved	R	Reserved	-
1	MONO	R	1 = No color burst signal detected. 0 = Color burst signal detected.	0
0	DET50	R	0 = 60Hz source detected 1 = 50Hz source detected The actual output vertical scanning frequency depends on the current standard invoked.	0
0X04 - HSYNC DELAY CONTROL				
7	Reserved	R/W	Reserved	-
6-5	CKHY	R/W	Color killer time constant 0 = Fastest 3 = Slowest	0
4-0	Reserved	R/W	Reserved	-
0X05 - AFE SELECTION				
7-4	Reserved	R/W	Reserved	0
3	FBPY	R/W	0 = Disable Y channel antialiasing filter (RGB mode) 1 = Enable Y channel antialiasing filter (decoder mode)	1
2-1	Reserved	R/W	Reserved	-
0	DEC_SEL	R/W	AFE control selection 0 = Reserved 1 = Decoder input mode	1

TW9992 Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
0X06 - ANALOG CONTROL REGISTER (ACNTL)				
7	SRESET	W	Soft reset. Write a "1" to reset the device to its default state but all register contents remain unchanged. This bit is self-cleared.	0
6-5	Reserved	R/W	Reserved	-
4	AGC_EN	R/W	0 = AGC loop function enabled. 1 = AGC loop function disabled. Gain is set to by AGCGAIN.	0
3-0	Reserved	R/W	Reserved	-
0X07 - CROPPING REGISTER, HIGH (CROP_HI)				
7-6	VDELAY_HI	R/W	Bit[9:8] of the 10-bit Vertical Delay register.	0
5-4	VACTIVE_HI	R/W	Bit[9:8] of the 10-bit VACTIVE register. Refer to description on Reg0x109 for its shadow register.	0
3-2	HDELAY_HI	R/W	Bit[9:8] of the 10-bit Horizontal Delay register.	0
1-0	HACTIVE_HI	R/W	Bit[9:8] of the 10-bit HACTIVE register.	2
0X08 - VERTICAL DELAY REGISTER, LOW (VDELAY_LO)				
7-0	VDELAY_LO	R/W	Bit[7:0] of the 10-bit Vertical Delay register. The two MSBs are in the CROP_HI register. It defines the number of lines between the leading edge of VSYNC and the start of the active video.	12
0X09 - VERTICAL ACTIVE REGISTER, LOW (VACTIVE_LO)				
7-0	VACTIVE_LO	R/W	Bit[7:0] of the 10-bit Vertical Active register. The two MSBs are in the CROP_HI register. It defines the number of active video lines per frame output. The VACTIVE register has a shadow register for use with 50Hz source when Atreg of Reg0x11C is not set. This register can be accessed through the same index address by first changing the format standard to any 50Hz standard.	F0
0X0A - HORIZONTAL DELAY REGISTER, LOW (HDELAY_LO)				
7-0	HDELAY_LO	R/W	Bit[7:0] of the 10-bit Horizontal Delay register. The two MSBs are in the CROP_HI register. It defines the number of pixels between the leading edge of the HSYNC and the start of the image cropping for active video. The HDELAY_LO register has two shadow registers for use with PAL and SECAM sources respectively. These register can be accessed using the same index address by first changing the decoding format to the corresponding standard.	0F
0X0B - HORIZONTAL ACTIVE REGISTER, LOW (HACTIVE_LO)				
7-0	HACTIVE_LO	R/W	Bit [7:0] of the 10-bit Horizontal Active register. The two MSBs are in the CROP_HI register. It defines the number of active pixels per line output.	D0
0X0C - CONTROL REGISTER I (CNTRL1)				
7	PBW	R/W	Combined with VTL [3], there are four different Chroma bandwidth can be selected. 1 = Wide Chroma BPF BW 0 = Normal Chroma BPF BW	1
6	DEM	R/W	Color killer sensitivity 1 = Low 0 = High	1
5	PALSW	R/W	1 = PAL switch sensitivity low. 0 = PAL switch sensitivity normal.	0
4	SET7	R/W	1 = The black level is 7.5 IRE above the blank level. 0 = The black level is the same as the blank level.	0
3	COMB	R/W	1 = Adaptive comb filter on for NTSC/PAL 0 = Notch filter	1
2	HCOMP	R/W	1 = Operation mode 1. (recommended) 0 = Operation mode 0.	1
1	YCOMB	R/W	This bit controls the comb operation when there is no color burst. 1 = No comb 0 = Comb.	0
0	PDLY	R/W	PAL delay line 1 = Disable 0 = Enable	0

TW9992 Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
0X0D - CC/WSS CONTROL				
7-6	Reserved	R/W	Reserved	-
5	WSSEN	R/W	0 = Disable WSS decoding 1 = Enable	0
4-0	CCODDLINE	R/W	These bits control the Closed Caption decoding line number in case of odd field	00
0X10 - BRIGHTNESS CONTROL REGISTER (BRIGHT)				
7-0	BRIGHTNESS	R/W	These bits control the brightness. They have value of –128 to 127 in 2's complement form. Positive value increases brightness. A value 0 has no effect on the data.	00
0X11 - CONTRAST CONTROL REGISTER (CONTRAST)				
7-0	CONTRAST	R/W	These bits control the contrast. They have value of 0 to 3.98 (FFh). A value of 100 (64h) yields a gain of 100%. The gain ranges from 0 to 255%	64
0X12 - SHARPNESS CONTROL REGISTER I (SHARPNESS)				
7	SCURVE	R/W	This bit controls the center frequency of the peaking filter. The corresponding gain adjustment is HFLT. 0 = Low 1 = Center	0
6	VSF	R/W	This bit is for internal used.	0
5-4	CTI	R/W	Color transient improvement level control. There are 4 enhancement levels with 0 being the lowest and 3 being the highest.	1
3-0	SHARP	R/W	These bits control the amount of sharpness enhancement on the luminance signals. There are 16 levels of control with '0' having no effect on the output image and '15' being the strongest.	1
0X13 - CHROMA (U) GAIN REGISTER (SAT_U)				
7-0	SAT_U	R/W	These bits control the digital gain adjustment to the U (or Cb) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%.	80
0X14 - CHROMA (V) GAIN REGISTER (SAT_V)				
7-0	SAT_V	R/W	These bits control the digital gain adjustment to the V (or Cr) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%.	80
0X15 - HUE CONTROL REGISTER (HUE)				
7-0	HUE	R/W	These bits control the color hue. It is in 2's complement form with 0 being the center value. Positive value results in red hue and negative value gives green hue.	00
0X17 - VERTICAL PEAKING CONTROL I				
7-4	SHCOR	R/W	These bits provide coring function for the sharpness control.	8
3	Reserved	R/W	Reserved	-
2-0	VSHP	R/W	Vertical peaking gain control	0
0X18 - CORING CONTROL REGISTER (CORING)				
7-6	CTCOR	R/W	These bits control the coring function for the CTI. It has internal step size of 2.	1
5-4	CCOR	R/W	These bits control the low level coring function for the Cb/Cr output.	0
3-2	VCOR	R/W	These bits control the coring function of the vertical peaking logic. It has an internal step size of 2.	1
1-0	CIF	R/W	These bits control the IF compensation level. 0 = None 1 = 1.5dB 2 = 3dB 3 = 6dB	0

TW9992 Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
0X19 - TEST MUX SELECTION				
7-4	Reserved	R/W	Reserved	-
3-0	RTSEL	R/W	Misc output signal selection 0: vdloss 1: hlock 2: slock 3: vlock 4: mono 5: det50 6: field 7: rtcout 8: bpg 9: vdet A: cgate B: dqsync C: mcvsn D: act_video E: (reserved) F: sav	6
0X1A - CC/EDS STATUS REGISTER (CC_STATUS)				
7	Reserved	R/W	Reserved	-
6	EDS_EN	R/W	0 = EDS data is not transferred to the CC_DATA FIFO. 1 = EDS data is transferred to the CC_DATA FIFO.	0
5	CC_EN	R/W	0 = CC data is not transferred to the CC_DATA FIFO. 1 = CC data is transferred to the CC_DATA FIFO.	0
4	PARITY	R	0 = Data in CC_DATA has no error. 1 = Data in CC_DATA has odd parity error.	-
3	FF_OVF	R	0 = An overflow has not occurred. 1 = An overflow has occurred in the CC_DATA FIFO.	-
2	FF_EMP	R	0 = CC_DATA FIFO is empty. 1 = CC_DATA FIFO has data available.	-
1	CC_EDS	R	0 = Closed caption (CC) data is in CC_DATA register. 1 = Extended data service (EDS) data is in CC_DATA register.	-
0	LO_HI	R	0 = Low byte of the 16-bit word is in the CC_DATA register. 1 = High byte of the 16-bit word is in the CC_DATA register.	-
0X1B - CC/EDS DATA REGISTER (CC_DATA)				
7-0	CC_DATA	R	These bits store the incoming closed caption or even field closed caption data.	-
0X1C - STANDARD SELECTION (SDT)				
7	DETSTUS	R	0 = Idle1 = Detection in progress	-
6-4	STDNOW	R	Current standard invoked 0 = NTSC(M) 1 = PAL (B,D,G,H,I) 2 = SECAM 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = N/A	-
3	ATREG	R/W	1 = Disable the shadow registers. 0 = Enable VACTIVE and HDELAY shadow registers value depending on standard	0
2-0	STANDARD	R/W	Standard selection 0 = NTSC(M) 1 = PAL (B,D,G,H,I) 2 = SECAM 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = Auto detection	7

TW9992 Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
0X1D - STANDARD RECOGNITION (SDTR)				
7	ATSTART	R/W	Writing 1 to this bit will manually initiate the auto format detection process. This bit is a self-resetting bit.	0
6	PAL6_EN	R/W	1 = Enable recognition of PAL60. 0 = Disable recognition.	1
5	PALN_EN	R/W	1 = Enable recognition of PAL (CN). 0 = Disable recognition.	1
4	PALM_EN	R/W	1 = Enable recognition of PAL (M). 0 = Disable recognition.	1
3	NT44_EN	R/W	1 = Enable recognition of NTSC 4.43. 0 = Disable recognition.	1
2	SEC_EN	R/W	1 = enable recognition of SECAM. 0 = disable recognition.	1
1	PALB_EN	R/W	1 = enable recognition of PAL (B, D, G, H, I). 0 = disable recognition.	1
0	NTSC_EN	R/W	1 = enable recognition of NTSC (M). 0 = disable recognition.	1
0X1F - TEST				
7-0	Test	R/W	Reserved	00
0X20 - CLAMPING GAIN (CLMPG)				
7-4	CLPEND	R/W	These 4 bits set the end time of the clamping pulse in the increment of 8 system clocks. The clamping time is determined by this together with CLPST.	5
3-0	CLPST	R/W	These 4 bits set the start time of the clamping pulse in the increment of 8 system clocks. It is referenced to PCLAMP position.	0
0X21 - INDIVIDUAL AGC GAIN (IAGC)				
7-4	NMGAIN	R/W	These bits control the normal AGC loop maximum correction value.	2
3-1	WPGAIN	R/W	Peak AGC loop gain control.	1
0	AGCGAIN8	R/W	Reserved	0
0X22 - AGC GAIN (AGCGAIN)				
7-0	AGCGAIN	R/W	These bits are the lower 8 bits of the 9-bit register that controls the AGC gain when AGC loop is disabled.	F0h
0X23 - WHITE PEAK THRESHOLD (PEAKWT)				
7-0	PEAKWT	R/W	These bits control the white peak detection threshold.	D8
0X24 - CLAMP LEVEL (CLMPL)				
7	CLMPLD	R/W	0 = Clamping level is set by CLMPL. 1 = Clamping level preset at 60d.	1
6-0	CLMPL	R/W	These bits determine the clamping level of the Y channel.	3C
0X25 - SYNC AMPLITUDE (SYNCT)				
7	SYNCTD	R/W	0 = Reference sync amplitude is set by SYNCT. 1 = Reference sync amplitude is preset to 38h.	1
6-0	SYNCT	R/W	These bits determine the standard sync pulse amplitude for AGC reference.	38
0X26 - SYNC MISS COUNT REGISTER (MISSCNT)				
7-4	MISSCNT	R/W	These bits set the threshold for horizontal sync miss count threshold.	4
3-0	HSWIN	R/W	These bits set the size for the horizontal sync detection window.	4
0X27 - CLAMP POSITION REGISTER (PCLAMP)				
7-0	PCLAMP	R/W	These bits set the clamping position from the PLL sync edge	38

TW9992 Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
0X28 - VERTICAL CONTROL I				
7-6	VLCKI	R/W	Vertical lock in time. 0 = Fastest 3 = Slowest	0
5-4	VLCKO	R/W	Vertical lock out time. 0 = Fastest 3 = Slowest	0
3	VMODE	R/W	Vertical detection window. 0 = Vertical count down mode 1 = Search mode	0
2	DETV	R/W	0 = Normal VSYNC logic 1 = Recommended for special application only	0
1	AFLD	R/W	Auto field generation control 0 = Off 1 = On	0
0	VINT	R/W	Vertical integration time control. 0 = Short 1 = Normal	0
0X29 - VERTICAL CONTROL II				
7-5	BSHT	R/W	Burst PLL center frequency control.	0
4-0	VSHT	R/W	VSYNC output delay control in the increment of half-line length	0
0X2A - COLOR KILLER LEVEL CONTROL				
7-6	CKILMAX	R/W	These bits control the amount of color killer hysteresis. The hysteresis amount is proportional to the value.	1
5-0	CKILMIN	R/W	These bits control the color killer threshold. Larger value gives lower killer level.	38
0X2B - COMB FILTER CONTROL				
7	FCOMB	R/W	1 = Nonadaptive comb 0 = Adaptive comb.	0
6-4	HTL	R/W	Adaptive Comb filter control (factory use only).	4
3	VTL1	R/W	Comb filter bandwidth control	0
2-0	VTL	R/W	Adaptive Comb filter threshold control (factory use only)	4
0X2C - LUMA DELAY AND HFILTER CONTROL				
7	CKLM	R/W	Color Killer mode. 0 = Normal 1 = Fast (for special application)	0
6-4	YDLY	R/W	Luma delay fine adjustment. This 2's complement number provides –4 to +3 unit delay control.	3
3-0	HFLT	R/W	Peaking control 2. The peaking curve is controlled by SCURVE bit.	0
0X2D - MISCELLANEOUS CONTROL REGISTER I (MISC1)				
7	Reserved	R/W	Reserved	-
6	EVCNT	R/W	0 = Normal operation 1 = Even field counter in special mode	0
5	Reserved	R/W	Reserved	-
4	SDET	R/W	ID detection sensitivity. "1" is recommended.	1
3	TBC_EN	R/W	0 = TBC off 1 = Internal TBC enabled. (test purpose only)	0
2	BYPASS	R/W	It controls the standard detection and should be set to '1' in normal use.	1
1	SYOUT	R/W	0 = HSYNC is always generated 1 = HSYNC is disabled when video loss is detected	0
0	Reserved	R/W	Reserved	-

TW9992 Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
0X2E - MISCELLANEOUS CONTROL REGISTER II (MISC2)				
7-6	HPM	R/W	Horizontal PLL acquisition time. 0 = Slow 1 = Medium 2 = Auto 3 = Fast	2
5-4	ACCT	R/W	ACC time constant 0 = No ACC 1 = Slow 2 = Medium 3 = Fast	2
3-2	SPM	R/W	Burst PLL control. 0 = Slowest 1 = Slow 2 = Fast 3 = Fastest	1
1-0	CBW	R/W	Chroma low pass filter bandwidth control. 0 = Low 1 = Medium 2 = High 3 = NA	1
0X2F - MISCELLANEOUS CONTROL III (MISC3)				
7	NKILL	R/W	1 = Enable noisy signal color killer function in NTSC mode. 0 = Disable	1
6	PKILL	R/W	1 = Enable automatic noisy color killer function in PAL mode. 0 = Disable	1
5	SKILL	R/W	1 = Enable automatic noisy color killer function in SECAM mode. 0 = Disable	1
4	CBAL	R/W	0 = Normal output 1 = Special output mode.	0
3	FCS	R/W	1 = Force decoder output value determined by CCS. 0 = Disable	0
2	LCS	R/W	1 = Enable predetermined output value indicated by CCS when video loss is detected. 0 = Disable	0
1	CCS	R/W	When FCS is set high or video loss condition is detected when LCS is set high, one of two colors display can be selected. 1 = Blue color 0 = Black	0
0	BST	R/W	1 = Enable blue stretch. 0 = Disable	0
0X30 - MACROVISION DETECTION (MVSN)				
7	SID_FAIL	R	SECAM ID detection failed	-
6	PID_FAIL	R	PAL ID detection failed	-
5	FSC_FAIL	R	FSC frequency detection failed	-
4	SLOCK_FAIL	R	Subcarrier lock detection failed	-
3	CSBAD	R	Macrovision color stripe detection may be un-reliable	-
2	MCVSN	R	1 = Macrovision AGC pulse detected 0 = Not detected.	-
1	CSTRIPE	R	1 = Macrovision color stripe protection burst detected 0 = Not detected.	-
0	CTYPE	R	This bit is valid only when color stripe protection is detected, i.e., Cstripe = 1. 1 = Type 2 color stripe protection 0 = Type 3 color stripe protection	-

TW9992 Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
0X31 - CHIP STATUS II (CSTATUS2)				
7	VCR	R	VCR signal indicator	-
6	WKAIR	R	Weak signal indicator 2	-
5	WKAIR1	R	Weak signal indicator1	-
4	VSTD	R	Standard line per field indicator	-
3	NINTL	R	Non-interlaced signal indicator	-
2	WSSDET	R	1 = WSS data detected 0 = Not detected	-
1	EDSDET	R	1 = EDS data detected 0 = Not detected	-
0	CCDET	R	1 = CC data detected 0 = Not detected	-
0X32 - H MONITOR (HFREF)				
7-0	HFREF, etc.	R	Horizontal line frequency indicator HREF[9:2] /GVAL[8:1] /PHERRDO /CGAINO /BAMPO /MINAVG /SYTHRD /SYAMP	-
0X33 - CLAMP MODE (CLMD)				
7-6	FRM	R/W	Free run mode. 0 = Auto mode 1 = Auto mode 2 = 60Hz 3 = 50Hz	0
5-4	YNR	R/W	Y HF Noise Reduction. 0 = None 1 = Smallest 2 = Small 3 = Medium	0
3-2	CLMD	R/W	Clamping mode control. 0 = Sync top 1 = Auto 2 = Pedestal 3 = NA	1
1-0	PSP	R/W	Slice level. 0 = Low 1 = Medium 2 = High 3 = NA	1
0X34 - ID DETECTION CONTROL (NSEN/SSEN/PSEN/WKTH)				
7-6	INDEX	R/W	These two bits indicate which of the four lower 6-bit registers is currently being controlled. The write sequence is a two step process unless the same register is written. A write of {ID,000000} selects one of the four registers to be written. A subsequent write will actually write into the register.	0
5-0	NSEN/ SSEN/ PSEN/ WKTH	R/W	IDX = 0 controls the NTSC ID detection sensitivity (NSEN). IDX = 1 controls the SECAM ID detection sensitivity (SSEN). IDX = 2 controls the PAL ID detection sensitivity (PSEN). IDX = 3 controls the weak signal detection sensitivity (WKTH).	1A/ 20/ 1C/ 11
0X35 - CLAMP CONTROL (CLCNTL)				
7	CTEST	R/W	Clamping control for debug use.	0
6	YCLEN	R/W	0 = Enable Y channel clamp 1 = Disable	0
5	CCLEN	R/W	Reserved	0
4	VCLEN	R/W	Reserved	0
3	GTEST	R/W	0 = Normal operation 1 = Test	0
2	VLPF	R/W	Sync filter bandwidth control.	0
1	CKLY	R/W	Clamping current control 1.	0
0	CKLC	R/W	Clamping current control 2.	0

TW9992 Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
0X36 - DIFFERENTIAL CLAMPING CONTROL 1				
7-6	GAIN_SEL	R/W	Analog front end pre-amplifier gain control 0 = 1x 1 = 2x 2 = 4x 3 = 4x	0
5	ACLAMP_EN	R/W	Reserved	1
4	DCLAMP_EN	R/W	Reserved	1
3	CL_MARGIN	R/W	Adjusts the timing spacing between the two nonoverlapping clocks that operate in the toggle-mode. 0 = 3 to 27MHz clock periods 1 = 6 to 27MHz clock periods	0
2	TOGGLE_MODE	R/W	Enables the toggle-mode which eliminates systematic offsets between the two output phases of the Common Mode Restore Amp by swapping them from line to line. 0 = Disable toggle mode 1 = Enable	0
1-0	CM_CLAMP_MODE	R/W	Selects between 4 modes of operation for the Common-Mode-Restore: table needed derived from Verilog module. 00 = Clamp counter 01 = Blanking period 10 = Burst period 11 = Back-porch counter	2
0X37 - DIFFERENTIAL CLAMPING CONTROL 2				
7-6	Reserved	R/W	Reserved	0
5-4	PGA_BIAS	R/W	Controls PGA bias current 0 = 20µA 1 = 40µA 2 = 60µA 3 = 80µA	1
3	PGA_EN	R/W	PGA enable 0 = PGA disabled 1 = PGA enabled	1
2	Reserved	R/W	Reserved	0
1-0	AAFLPF	R/W	Antialiasing filter control 00 = 9MHz, 0dB in pass band 01 = 10MHz, -3dB in pass band 10 = 7MHz, 0dB in pass band 11 = 8MHz, -3dB in pass band	2
0X38 - DIFFERENTIAL CLAMPING CONTROL 3				
7-6	VCMIN_SEL	R/W	Input common mode voltage control from 400mV to 1.02V in 20mV increment 00 = 700mV 01 = 800mV 10 = 900mV (Decoder) 11 = 1000mV	3
5-4	DCLAMP_ATTEN	R/W	DC restore clamp current control 00 = 30µA 01 = 25µA 10 = 10µA 11 = 5µA	1
3-2	ADC_BIAS	R/W	ADC bias current selection 00 = 10µA (Decoder) 01 = 15µA 10 = 20µA 11 = 25µA	2
1-0	IBINBUF_SEL	R/W	Bias current control for AFE preamplifier 00 = 20µA (Decoder) 01 = 40µA 10 = 60µA 11 = 80µA	1

TW9992 Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
0X39 - DIFFERENTIAL CLAMPING CONTROL 4				
7-6	ACLAMP_ATTEN	R/W	Reduces the strength of the common-mode restore clamp	0
5	PASSIVE_CLAMP	R/W	Selects between current mode (active amplifier) and voltage mode (passive resistor network) for the common-mode-restore function. 0 = Passive resistor network for the common-mode-restore function 1 = Active amplifier for common mode restore	0
4	RES_REFERENCE	R/W	Selects alternate common-mode reference. Normal operation mode is 0.	0
3-0	Reserved	R/W	Reserved	-
0X3A - SHORT DETECTION CONTROL				
7	RESERVED	R/W	Reserved	0
6-4	SH_THRESH_GND	R/W	Selects threshold for Short-to-Ground-Detection for DIAG0, DIAG1, and DIAG2	3
3	RESERVED	R/W	Reserved	0
2-0	SH_THRESH_BAT	R/W	Selects threshold for Short-to-Battery-Detection for DIAG0, DIAG1, and DIAG2	0
0X3B - SHORT DETECTION CONTROL 1				
7-6	Reserved	R/W	Reserved	0
5	SH_EN_GND2	R/W	Enables Short-to-Ground-Detection for DIAG2 0 = Disable 1 = Enable	0
4	SH_EN_BAT2	R/W	Enables Short-to-Battery-Detection for DIAG2 (Battery or High-side Supply) 0 = Disable 1 = Enable	0
3	SH_EN_GND1	R/W	Enables Short-to-Ground-Detection for DIAG1 0 = Disable 1 = Enable	0
2	SH_EN_BAT1	R/W	Enables Short-to-Battery-Detection for DIAG1 (Battery or High-side Supply) 0 = Disable 1 = Enable	0
1	SH_EN_GND0	R/W	Enables Short-to-Ground-Detection for DIAG0 0 = Disable 1 = Enable	0
0	SH_EN_BAT0	R/W	Enables Short-to-Battery-Detection for DIAG0 (Battery or High-side Supply) 0 = Disable 1 = Enable	0
0X3C - DIFFERENTIAL CLAMPING CONTROL 5				
7	Reserved	R/W	Enables Common-Mode-Input-Preconditioning. Forces unused (unselected) inputs to ½ supply 0 = Disable 1 = Enable	1
6	Reserved	R/W	Reserved	0
5	AGND_EN	R/W	AGND selection	0
4	AN_TEST_EN	R/W	Enables the analog test mux 0 = Disable muxes 1 = Enable muxes	0
3-2	Reserved	R/W	Reserved	-
1-0	AN_TEST_SEL	R/W	Selects analog signals from the AFE for the test mux 00 = Input mux output 01 = PREAMP/PGA/AAF output 10 = VREFP, VREFN 11 = VCMref, VCOM_ADC	0

TW9992 Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
0X3D - DIFFERENTIAL CLAMPING CONTROL 6				
7-3	Reserved	R/W	Reserved	0
2	PDS2	R/W	Power-down diagnostic circuit #2. 0 = Normal operation 1 = Power down	0
1	PDS1	R/W	Power-down diagnostic circuit #1. 0 = Normal operation 1 = Power down	0
0	PDS0	R/W	Power-down diagnostic circuit #0. 0 = Normal operation 1 = Power-down	0
0X3F - LINENUMBER INT				
7	F1LIEN	R/W	0 = Disable LINE_INT during field 1 1 = Enable LINE_INT during field 1	0
6	F2LIEN	R/W	0 = Disable LINE_INT during field 2 1 = Enable LINE_INT during field 2	0
5-0	LINENUMBER	R/W	LINE_INT (Line Interrupt Status) register bit is set when the video line number is equal or greater than this number.	1A
0X40 - WSS1				
7	CRCERR	R	This bit is only valid in 525 line video system. 1: CGMS (WSS525) CRC error detected in current field. 0: No CRC error	1
6	WSSFLD	R	0: Current WSS data is received in Odd field 1: Current WSS data is received in Even field	0
5-4	Reserved	R	Reserved	-
3-0	WSS[19:16]	R	CGMS (WSS525) Bit19-16 in 525 line video system. Wide Screen Signaling Bit19-16 in 625 line video system.	0
0X41 - WSS2				
7-0	WSS[15:8]	R	CGMS (WSS525) Bit15-8 in 525 line video system. These bits show CRC 6 bits in CGMS (WSS525). These bits are only valid in 525 line video system.	0
0X42 - WSS3				
7-0	WSS[7:0]	R	CGMS (WSS525) Bit7-0 in 525 line video system. Wide Screen Signaling Bit7-0 in 625 line video system.	0
0X48 - IO BUFFER CONTROL				
7	Reserved	R/W	Reserved	-
6	LOCK_WTX	R/W	Serial interface multibyte write lock function 1 = Disable (no lock, each byte take effect after written) 0 = Enable	0
5	LOCK_RDX	R/W	Serial interface multibyte read lock function 1 = Disable 0 = Enable	0
4	AINC	R/W	Serial interface auto-indexing control 1 = Non-auto 0 = Auto-increment	0
3	EXTCLK_ENA	R/W	Enable external clock input	0
2	OEN	R/W	Tri-state all digital signal outputs 1: Tri-state 0: Release overall tri-state, output enable depends on each signal pin's tristate control	1
1	TRI656	R/W	Tri-State the VD bus and VDCLK in 48 Pin package	1
0	DRVSTR	R/W	Digital output buffer driver strength selection 0: 4mA 1: 8mA	0

TW9992 Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
0X49 - DATA CONVERSION				
7-3	Reserved	R/W	Reserved	0
6	Y16	R/W	Y pedestal level selection of YUV to RGB conversion. 1: Decimal 16 level become black level 0: No offset adjustment	0
1	BT7	R/W	Conversion matrix selection of YUV to RGB conversion. 1: Matrix for HDTV standard 0: Matrix for SDTV standard	0
0	RGB565	R/W	Output data is RGB565 1 = RGB565 0 = YUV422	0
0X4A - SYNC CONTROL				
7	VSP	R/W	0 = VSYNC pin output polarity is active high 1 = VSYNC pin output polarity is active low	0
6-4	VSSL	R/W	VSYNC pin output control 0 = VSYNC 1 = VACT 2 = FIELD 3 - 5 = Reserved 6 = Factory test only 7 = 0	0
3	HSP	R/W	0 = HSYNC pin output polarity is active high 1 = HSYNC pin output polarity is active low	0
2-0	HSSL	R/W	HSYNC pin output control 0 = HACT 1 = HSYNC 2 = HLOCK 3 = ASYNCW 4 - 5 = Reserved 6 = Factory test only 7 = 0	0
0X4B - OUTPUT CONTROL				
7-6	CK2S	R/W	VDCLK pin output selection. 00 = SYSCLK 01 = CLK27/2 10 = CLK27/4 11 = BYTE_CLK	0
5-4	CK1S	R/W	VDCLK polarity control. 00: Normal 01: Invert 1X: Reserved	0
3	INTOEN	R/W	0 = Enable INTREQ output 1 = Disable INTREQ output	1
2	INTPOL	R/W	0 = Negative polarity 1 = Positive polarity	0
1	GPSYNCO	R/W	Enable GPIO to output sync signals. The corresponding GPIO enable bit (0x60) has to be disabled. Applicable to GP2 ~ GP0. GP2: VSYNC (source selected by VSSL in 0x4A) GP1: HSYNC (source selected by HSSL in 0x4A) GP0: Field (source selected by RTSEL in 0x19)	0
0	Reserved	R/W	Reserved	-

TW9992 Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
0X4C - POWER-DOWN REGISTER				
7-4	Reserved	R/W	Reserved	-
3	CLK_PDN	R/W	0 = Normal clock operation. 1 = 27MHz clock in power down mode.	0
2	Y_PDN	R/W	0 = Luma ADC in normal operation. 1 = Luma ADC in power down mode.	0
1-0	Reserved	R/W	Reserved	-
0X4D - HSYNC OUTPUT ADJUSTMENT				
7-4	Reserved	R/W	Reserved	-
3	VSHALF	R/W	VSYNC transitions at falling edge of clock	0
2	HSHALF	R/W	HSYNC transitions at falling edge of clock	0
1	Reserved	R/W	Reserved	-
0	HSYNCODLY	R/W	MSB of HSYNC output position delay adjustment	0
0X4E - HSYNC OUTPUT ADJUSTMENT				
7-0	HSYNCODLY	R/W	LSB of HSYNC output position delay adjustment	0
0X50 - IRQ1 REGISTER				
7-3	Reserved	R/W	Reserved	0
2	WSS	R/W	WSS status change interrupt. Write “1” to clear the active status.	0
1	EDS	R/W	EDS status change interrupt. Write “1” to clear the active status.	0
0	CC	R/W	CC status change interrupt. Write “1” to clear the active status.	0
0X51 - IRQ2 REGISTER				
7	LINE_INT	R/W	LINE_INT status change interrupt. Write “1” to clear the active status.	0
6	Reserved	R/W	Reserved	-
5	VDLOSS	R/W	VDLOSS status change interrupt. Write “1” to clear the active status.	0
4	DET50	R/W	DET50 detection status change interrupt. Write “1” to clear the active status.	0
3	Reserved	R/W	Reserved	-
2	SLOCK	R/W	SLOCK status change interrupt. Write “1” to clear the active status.	0
1	HVLOCK	R/W	HLOCK/VLOCK status change interrupt. Write “1” to clear the active status.	0
0	VCR	R/W	VCR detection status change interrupt. Write “1” to clear the active status.	0
0X52 - IRQ3 REGISTER				
7-2	Reserved	R/W	Reserved	-
1	SHT_GND	R/W	Short-to-ground interrupt Write “1” to clear the active status.	0
0	SHT_BAT	R/W	Short-to-battery interrupt Write “1” to clear the active status.	0

TW9992 Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
0X53 - INTERRUPT SOURCE STATUS 1				
7-3	Reserved	R	Reserved	-
2	WSS_STS	R	WSS data is detected	-
1	EDS_STS	R	EDS (Extended Data Service) data is detected	-
0	CC_STS	R	CC (Closed Caption) data is detected	-
0X54 - INTERRUPT SOURCE STATUS 2				
7	LINE_INT_STS	R	Current Video line number is larger than the number specified in the LINENUMBER register 0x3F [5:0].	-
6	MACROV_STS	R	Macrovision status change in current field	-
5	VDLOSS_STS	R	1: Video is not preset 0: Video detected	-
4	DET50_STS	R	1: Video source is 50Hz 0: Video source is 60Hz	-
3	Reserved	R	Reserved	-
2	SLOCK_STS	R	Subcarrier PLL is locked to the incoming video source	-
1	HVLOCK_STS	R	HLOCK/VLOCK status: 0: Both HLOCK and VLOCK are “0” 1: At least one of HLOCK and VLOCK is “1”	-
0	VCR_STS	R	VCR detection status	-
0X55 - INTERRUPT SOURCE STATUS 3				
7-6	Reserved	R	Reserved	-
5	STG_STS2	R	Short-to-ground status for DIAG2	-
4	STB_STS2	R	Short-to-battery status for DIGA2	-
3	STG_STS1	R	Short-to-ground status for DIAG1	-
2	STB_STS1	R	Short-to-battery status for DIGA1	-
1	STG_STS0	R	Short-to-ground status for DIAG0	-
0	STB_STS0	R	Short-to-battery status for DIAG0	-
0X56 - IRQ1 ENABLE				
7-3	Reserved	R/W	Reserved	-
2-0	IRQ1_ENA	R/W	IRQ enable for IRQ 1 REGISTER. A “0” for any bit disables the interrupt for that specific bit.	00
0X57 - IRQ2 ENABLE				
7-4	IRQ2_ENA	R/W	IRQ enable for IRQ 2 REGISTER. A “0” for any bit disables the interrupt for that specific bit.	00
3	Reserved	R/W	Reserved	-
2-0	IRQ2_ENA	R/W	IRQ enable for IRQ 2 REGISTER. A “0” for any bit disables the interrupt for that specific bit.	00
0X58 - IRQ3 ENABLE				
7-2	Reserved	R/W	Reserved	-
1-0	IRQ3_ENA	R/W	IRQ enable for IRQ 3 REGISTER. A “0” for any bit disables the interrupt for that specific bit.	0
0X60 - GPIO ENABLE				
7-4	Reserved	R/W	Reserved	0
3	GP3E	R/W	GPIO #3 enable	0
2	GP2E	R/W	GPIO #2 enable	0
1	GP1E	R/W	GPIO #1 enable	0
0	GP0E	R/W	GPIO #0 enable	0

TW9992 Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
0X61 - GPIO OE				
7-4	Reserved	R/W	Reserved	0
3	GP3OE	R/W	GPIO #3 output enable	0
2	GP2OE	R/W	GPIO #2 output enable	0
1	GP1OE	R/W	GPIO #1 output enable	0
0	GP0OE	R/W	GPIO #0 output enable	0
0X62 - GPIO OD				
7-4	Reserved	R/W	Reserved	0
3	GP3OD	R/W	GPIO #3 output data	0
2	GP2OD	R/W	GPIO #2 output data	0
1	GP1OD	R/W	GPIO #1 output data	0
0	GP0OD	R/W	GPIO #0 output data	0
0X63 - GPIO ID				
7-4	Reserved	R	Reserved	-
3	GP3ID	R	GPIO #3 input data	-
2	GP2ID	R	GPIO #2 input data	-
1	GP1ID	R	GPIO #1 input data	-
0	GP0ID	R	GPIO #0 input data	-
MIPI Transmitter Registers				
0X70 - MIPI CONTROL, VIDEO INPUT FORMAT AND NUMBER OF DATA CHANNELS				
7	PD_MIPI	R/W	1 = Power-down-MIPI-module, 0 = Normal-MIPI-operation	1
6	TMLS_MIPI	R/W	Reserved	0
5	TMHS_MIPI	R/W	Reserved	0
4	PAL	R/W	1 = PAL-25 FRAMES/SEC; 0 = NTSC-30 FRAMES/SEC	0
3	PROGRESSIVE	R/W	1 = PROGRESSIVE; 0 = INTERLACED INPUT FORMAT	0
2-0	LANE_NO	R/W	Reserved	1
0X71 - PICTURE WIDTH				
7	LINE_INC1	R/W	Reserved	1
6	SWAP_CRC	R/W	SWAP THE MSB-BYTE AND LSB-BYTE OF CRC[15:0]	0
5	ONE_FE	R/W	1 = One-FE-packet per-frame, 0 = Two-FE packets per frame	0
4-0	PIC_WIDTH	R/W	ACTIVE AREA PIC_WIDTH[12:8] OF INPUT VIDEO	5
0X72 - PICTURE WIDTH				
7-0	PIC_WIDTH	R/W	ACTIVE AREA PIC_WIDTH[7:0] OF INPUT VIDEO	A0
0X73 - PICTURE HEIGHT				
7	SWAP_YC	R/W	Reserved	0
6	HS_DPHY_TEST	R/W	Reserved	0
5	FS_SPECIAL	R/W	1 = Frame-start-packet at special 1st line-start location 0 = Normal FS location	0
4-0	PIC_HEIGHT	R/W	Reserved	1
0X74 - PICTURE HEIGHT				
7-0	PIC_HEIGHT	R/W	Reserved	E0

TW9992 Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
0X75 - BLANK LINE NUMBER				
7	Reserved		Reserved	0
6	FPGA_RUN	R/W	Reserved	0
5	SD_PROG	R/W	Reserved	0
4-0	RESERVED	R/W	Reserved	0
0X76 - BLANK LINE NUMBER				
7-0	BLANK_LINE	R/W	Reserved	17h
0X77 - FRAME-START COUNT (FOR FS PACKET INSERTION)				
7	HSCKON_FSFE	R/W	1 = HSCK - always on between frame-start and frame-end	0
6	HSCKON_LSLE	R/W	1 = HSCK - always on between line-start and line-end	0
5	P720	R/W	Reserved	0
4-0	FS_COUNT	R/W	Reserved	5
0X78 - FRAME-START COUNT (FOR FS PACKET INSERTION)				
7-0	FS_COUNT	R/W	Reserved	88h
0X79 - LINE START COUNT (FOR LS PACKET INSERTION)				
7	Reserved		Reserved	-
6	Reserved		Reserved	-
5	LIM_656	R/W	Reserved	0
4-0	LS_COUNT	R/W	Reserved	6
0X7A - LINE START COUNT (FOR LS PACKET INSERTION)				
7-0	LS_COUNT	R/W	Reserved	28h
0X7B - ACTIVE LINE START COUNT (FOR ACT-LS PACKET INSERTION)				
7-6	CHP_ID[1:0]	R/W	Reserved	1
5	SMALL_FRAME	R/W	Reserved	0
4-0	ACT_LS_COUNT	R/W	Reserved	6
0X7C - ACTIVE LINE START COUNT (FOR ACT-LS PACKET INSERTION)				
7-0	ACT_LS_COUNT	R/W	Reserved	B3h
0X7D - FRAME-END COUNT (FOR FE PACKET INSERTION)				
7	INT_PAT	R/W	1 = Use internal pattern generator, 0 = Use AFE output from external analog video input	0
6-5	CH_ID	R/W	Reserved	0
4-0	FE_COUNT	R/W	Reserved	6
0X7E - FRAME-END COUNT (FOR FE PACKET INSERTION)				
7-0	FE_COUNT	R/W	Reserved	13h
0X7F - VIRTUAL CHANNEL NUMBERS				
7	INV_FLD_POL	R/W	Reserved	0
6	NOVID	R/W	Reserved	0
5	ULPS_FSYNC	R/W	1 = ULPS-mode starts and ends in SYNC with Frame Reader SYNC	0
4	NO_LINE_START	R/W	1 = No line start packet between lines; 0 = One line start packet between lines	0
3	HSCK_ALWAYS_ON	R/W	1 = High-speed-clock-always-on mode, for test usage 0 = Normal operation with low-speed and high-speed transitions	0
2	GEN_PAL	R/W	1 = PAL format for internal pattern generator output	0
1-0	VC1[1:0]	R/W	Reserved	0

TW9992 Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
0X80 - WORD_COUNT IN LONG PACKET				
7-0	WORD_COUNT [15:8]	R/W	Upper 8-bit of word_count inside HS long packet	05
0X81 - WORD_COUNT IN LONG PACKET				
7-0	WORD_COUNT [7:0]	R/W	Lower 8-bit of word_count inside HS long packet	A0
0X82 - D_PHY TIMING				
7-4	LPX_CNT[3:0]	R/W	SOT initial wait time	1
3-0	HSPREP_CNT	R/W	HS-prepare time, between [40ns + 4*UI] and [85ns + 6*UI]	2
0X83 - D-PHY TIMING				
7-0	HS_ZERO	R/W	Long packets' HS_ZERO timing between [60ns + 4*UI] and [105ns + 6*UI]. Note: Short packets' HS_ZERO is controlled by Reg. 0x8E [7:4].	05h
0X84 - D_PHY TIMING				
7-0	HS_TRAIL	R/W	HS_TRAIL timing max (8*UI, 60ns + 4*UI)	02h
0X85 - CLI-2 HS_CLK TIMING				
7-0	CLK_AHEAD	R/W	Number of cycles HS_CLK is asserted ahead of HS_DATA, 0x0E for SD-27MHz, 0x3C for HD-125MHz	0Eh
0X86 - D_PHY TIMING				
7-0	CLK_POST	R/W	CLK_POST timing, greater than [60ns + 52*UI]	08h
0X87 - D_PHY TIMING				
7-0	MARK_WAIT	R/W	ULPS mode exit wait time/512; 0x37 for 27MHz, 0xF5 for 125MHz	37h
0X88 - MIPI D-PHY PARAMETERS				
7	RESERVED	R/W	Reserved	-
6	FORCE_ULPS	R/W	Force D-PHY to enter ULPS mode	0
5	ESC_EXIT	R/W	Force ESC-mode to exit ULPS or trigger or LPDT mode	0
4	LPDT	R/W	Include MIPI-LPDT mode to D-PHY output	0
3	RST_MODE	R/W	Include MIPI-reset mode to D-PHY output	0
2	RESERVED	R/W	Reserved	-
1	ESCAPE	R/W	Include MIPI-escape mode to D-PHY output	0
0	LINECODE_9B	R/W	1 = Use 9-bit line code; 0 = Use 8-bit line code in D-PHY	0
0X89 - SOT_PERIOD IN D-PHY				
7-0	WAIT_FRAMES	R/W	Reserved	00
0X8A - EOT_PERIOD IN D-PHY				
7-0	EOT_PERIOD	R/W	End_of_transmission_period in "UI" unit for D-PHY	02
0X8B - D-PHY TIMING				
7-4	CLK_PREP	R/W	CLK_PREPARE; between 38ns to 95ns	1
3-0	CLK_PRE	R/W	Reserved	1
0X8C - D-PHY TIMING				
7-4	LP_11	R/W	SOT LP11 state wait time	2
3-0	CLK_TRAIL	R/W	CLK_TRAIL 60ns	2
0X8D - D-PHY TIMING				
7-0	CLK_ZERO	R/W	CLK_ZERO, greater than 240ns	03h

TW9992 Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
0X8E - D-PHY TIMING				
7-4	SHORT_PKT_DLY	R/W	SHORT-PACKET-DELAY is used to control short-packets' HS_ZERO timing period.	2
3-0	CLK_SOT	R/W	CLK_SOT wait time	2
0X8F - D-PHY TIMING				
7-0	ULPS_11_CNT	R/W	ULPS LP11 wait time	01h
0X90 - TEST PATTERN GENERATOR				
7	PRBS_ERR_RSTB	R/W	Reserved	0
6	ATG_RESYNC	R/W	Reserved	0
5	RESERVED		Reserved	
4	TESTSET0	R/W	Reserved	0
3	ATG_INV_8B	R/W	Reserved	0
2	ATG_PRBS_SEL	R/W	Reserved	0
1	HS_TEST_SEL	R/W	Reserved	0
0	MIPIAFE_TEST_EN	R/W	Reserved	0
0X91 - ESCAPE_MODE TIMING				
7-0	ESC_DELAY	R/W	Data lane delay from clock lane in escape mode	0Ch
0X92 - AUTOMATIC TEST ERROR DETECTION				
7	PRBS_ERR_DET	R	Reserved	0
6-0	Reserved	R/W	Reserved	0
0X93 - FRAME-START LINE COUNT				
7-0	FRM_START_ LNCNT	R/W	Reserved	0Eh
0X94 - PICTURE_HEIGHT HIGH BITS				
7-3	Reserved	R/W	Reserved	00
2-0	PIC_HEIGHT[10:8]	R	Reserved	-
0X95 - PICTURE_HEIGHT LOW BYTE				
7-0	PIC_HEIGHT[7:0]	R	Reserved	-
0X96 - SPECIAL HSCK COUNT				
7-0	SP_HSCK_CNT	R/W	Reserved	1Ah
0X9B - RESYNC-DELAY COUNT				
7-0	RESYNC_DLY	R/W	RESYNC_DELAY is used to control the phase of divide-by-2 bit-clock, whose phase is crucial in the 8-bit to 9-bit line code encoding. The unit is the byte_clk period; *Use for 9-bit data*	02h
0XA0 - MIPI ANALOG CTRL DATA				
7:0	CTRL_BIT_DATA	R/W	Reserved	0
0XA1 - MIPI ANALOG CTRL CLOCK				
7:0	CTRL_BIT_CLK	R/W	Reserved	0

TW9992 Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
0XA2 - MIPI ANALOG CTRL MISC				
7	RON	R/W	Reserved	0
6	LOWF	R/W	Reserved	0
5	RESETB_PLL	R/W	Reset D-Phy PLL. Active Low	0
4	DPHY_RSTB	R/W	Reset D-Phy. Active Low	0
3	PWD_BG	R/W	Power-down band gap 1: Power down 0: Normal operation	1
2	PWD_PLL	R/W	Power-down D-Phy PLL 1: Power-down 0: normal operation	1
1	PWD_DATA	R/W	Power-down data lane driver 1: Power-down 0: Normal operation	1
0	PWD_CLK	R/W	Power-down clock 1: Power-down 0: Normal operation	1
0XA3 - MIPI ANALOG STATUS				
7	PLOCK	R	Reserved	-
6	FLOCK	R	Reserved	-
5	VCTLHIGH	R	Reserved	-
4	RST_OFF	R/W	Reserved	0
3:0	ITUNE	R/W	Reserved	0
0XA4 - MIPI ANALOG REGISTER				
7:0	Reserved	R/W	Reserved	0
ACA Registers				
0XC0 - ACA CONTROL				
7	ACA_DBG	R/W	ACA debug function 1: Enable 0: Disable	0
6	HIST_WIN_EN	R/W	Histogram measure window enable 1: Enable 0: Disable	0
5	Reserved	R/W	Reserved	0
4	ACA_BYPASS	R/W	ACA function bypass 1: Enable 0: Disable	0
3	LPOFF	R/W	Low pass filter disable 1: Disable 0: Enable	0
2	MLHCOMP	R/W	Low/High offset compensation enable 1: Enable 0: Disable	1
1	MDLTON	R/W	Y Delta compensation enable 1: Enable 0: Disable	1
0	ACA_ON	R/W	ACA function enable 1: Enable 0: Disable	0
0XC1 - ACA GAIN CONTROL				
7-6	Reserved	R/W	Reserved	0
5-0	ACA_GAIN	R/W	ACA gain control 00: ACA off 20: Max	20h
0XC2 - Y AVERAGE HIGH LIMIT CONTROL				
7-6	Reserved	R/W	Reserved	0
5-0	YAVGHLIM	R/W	Reserved	20h

TW9992 Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
0XC3 - Y AVERAGE LOW LIMIT CONTROL				
7-6	Reserved	R/W	Reserved	0
5-0	YAVGLLIM	R/W	Reserved	08h
0XC4 - Y DETECTION THRESHOLD				
7-4	Reserved	R/W	Reserved	0
3-0	YMINMAXR	R/W	Reserved	9h
0XC5 - BLACK LEVEL				
7-5	Reserved	R/W	Reserved	0
4-0	BLKLVL	R/W	Y black level control (max: 10h)	10h
0XC6 - CENTER LEVEL				
7-4	Reserved	R/W	Reserved	0
3-0	YCENTER	R/W	Y center level control	6h
0XC7 - WHITE LEVEL				
7-5	Reserved	R/W	Reserved	0
4-0	WHTLVL	R/W	Y white level control	00h
0XC8 - MEAN OFFSET LIMIT				
7	Reserved	R/W	Reserved	0
6-0	MOFSLIM	R/W	Reserved	38h
0XC9 - MEAN OFFSET SLOPE				
7-5	Reserved	R/W	Reserved	0
4-0	MOFSSLOPE	R/W	Reserved	10h
0XCA - MEAN OFFSET UP GAIN				
7-6	Reserved	R/W	Reserved	0
5-0	MOFSUPGAIN	R/W	Reserved	1Ch
0XCB - MEAN OFFSET DOWN GAIN				
7-6	Reserved	R/W	Reserved	0
5-0	MOFSDNGAIN	R/W	Reserved	14h
0XCC - DELTA CUTOFF THRESHOLD				
7-5	Reserved	R/W	Reserved	0
4-0	MDLTCUT	R/W	Reserved	0Ah
0XCD - DELTA SLOPE				
7-5	Reserved	R/W	Reserved	0
4-0	MDLTSLOPE	R/W	Reserved	1Fh
0XCE - LOW/HIGH AVERAGE THRESHOLD				
7-6	Reserved	R/W	Reserved	0
5-0	YLHAVGDIFF	R/W	Reserved	1Ah
0XCF - LOW MAX LEVEL CONTROL				
7-5	Reserved	R/W	Reserved	0
4-0	LMAXGRAD	R/W	Low max level control (max: 10h)	0Ch
0XD0 - HIGH MAX LEVEL CONTROL				
7-5	Reserved	R/W	Reserved	0
4-0	HMAXGRAD	R/W	Reserved	0Ch

TW9992 Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
0XD1 - LOW UP GAIN CONTROL				
7-5	Reserved	R/W	Reserved	0
4-0	LGRADUP	R/W	Reserved	0Ch
0XD2 - LOW DOWN GAIN CONTROL				
7-5	Reserved	R/W	Reserved	0
4-0	LGRADDN	R/W	Reserved	08h
0XD3 - HIGH UP GAIN CONTROL				
7-5	Reserved	R/W	Reserved	0
4-0	HGRADUP	R/W	Reserved	04h
0XD4 - HIGH DOWN GAIN CONTROL				
7-5	Reserved	R/W	Reserved	0
4-0	HGRADDN	R/W	Reserved	0Ch
0XD5 - LOW PASS FILTER COEFFICIENT				
7-4	Reserved	R/W	Reserved	0
3-0	LPFCOEF	R/W	Low pass filter coefficient control	4h
0XD6 - PDF INDEX				
7-2	PDF_INDEX	R/W	Reserved	0
1	ACA_MASK	R/W	Reserved	0
0	READ_EN	R/W	Reserved	0
0XD7 - HISTOGRAM WINDOW H START				
7-0	HAVST_HIST	R/W	Histogram measure window horizontal start from H active	0
0XD8 - HISTOGRAM WINDOW H SIZE				
7-1	Reserved	R/W	Reserved	0
0	HAVSIZE_HIST_HI	R/W	MSB of histogram measure window horizontal size, total 9 bits	1
0XD9 - HISTOGRAM WINDOW H SIZE				
7-0	HAVSIZE_HIST_LO	R/W	LSB of histogram measure window horizontal size, total 9 bits	68h
0XDA - HISTOGRAM WINDOW V START				
7-0	VAVST_HIST	R/W	Histogram measure window Vertical start from V active	0
0XDB - HISTOGRAM WINDOW V SIZE				
7-1	Reserved	R/W	Reserved	0
0	VAVSIZE_HIST_HI	R/W	MSB of histogram measure window vertical size, total 9 bits	1
0XDC - HISTOGRAM WINDOW V SIZE				
7-0	VAVSIZE_HIST_LO	R/W	LSB of histogram measure window vertical size, total 9 bits	20h
0XE0 - Y AVERAGE				
7-0	YAVG_RAW	R/W	Reserved	76h
0XE1 - Y AVERAGE LIMIT				
7-0	YAVG_LIM	R/W	Reserved	75h
0XE2 - LOW AVERAGE				
7-0	LOW_AVG	R/W	Reserved	4Dh
0XE3 - HIGH AVERAGE				
7-0	HIGH_AVG	R/W	Reserved	ABh
0XE4 – Y MAX				
7-0	Y_MAX	R/W	Reserved	2Ah

TW9992 Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
0XE5 - Y MIN				
7-0	Y_MIN	R/W	Reserved	E0h
0XE6 - MOFFSET				
7-0	MOFFSET	R/W	Reserved	07h
0XE7 - LOW GAIN				
7-0	LGRAD	R/W	Reserved	EBh
0XE8 - HIGH GAIN				
7-0	HGRAD	R/W	Reserved	03h
0XE9 - LL SLOPE				
7-0	LL_SLOPE	R/W	Reserved	39h
0XEA - LH SLOPE				
7-0	LH_SLOPE	R/W	Reserved	4Fh
0XEB - HL SLOPE				
7-0	HL_SLOPE	R/W	Reserved	3Dh
0XEC - HH SLOPE				
7-0	HH_SLOPE	R/W	Reserved	3Bh
0XED - X LOW				
7-0	X_LOW	R/W	Reserved	42h
0XEE - X MEAN				
7-0	X_MEAN	R/W	Reserved	75h
0XEF - X HIGH				
7-0	X_HIGH	R/W	Reserved	B0h
0XF0 - Y LOW				
7-0	Y_LOW	R/W	Reserved	3Dh
0XF1 - Y MEAN				
7-0	Y_MEAN	R/W	Reserved	7Ch
0XF2 - Y HIGH				
7-0	Y_HIGH	R/W	Reserved	B4h
0XF3 - ACA CONTROL				
7-2	Reserved	R/W	Reserved	-
1-0	DIS_LINE_EN	R/W	Reserved	2
0XF4 - ACA CONTROL				
7-1	Reserved	R/W	Reserved	-
0	DIS_LINE_SP_HI	R/W	Reserved	0
0XF5 - ACA CONTROL				
7-0	DIS_LINE_SP_LO	R/W	Reserved	0

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
March 23, 2015	FN8722.0	Initial Release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

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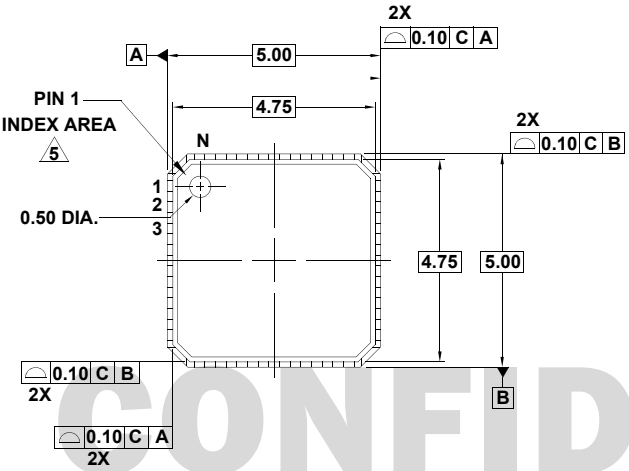
Package Outline Drawing

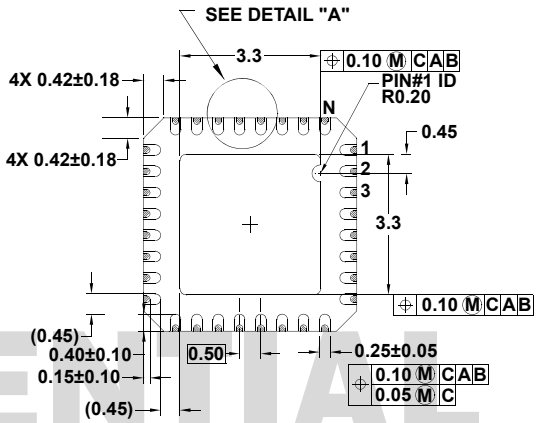
L32.5x5H

32 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (PUNCH QFN WITH WETABLE FLANK)

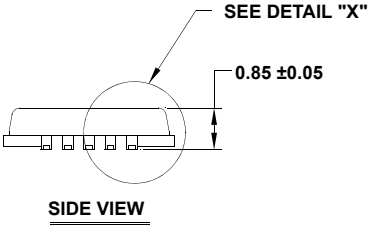
Rev 1, 9/14



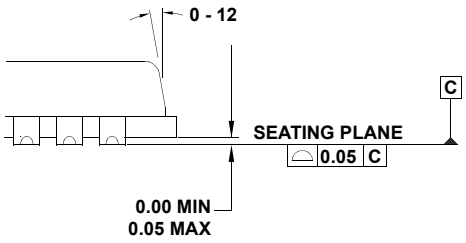
TOP VIEW



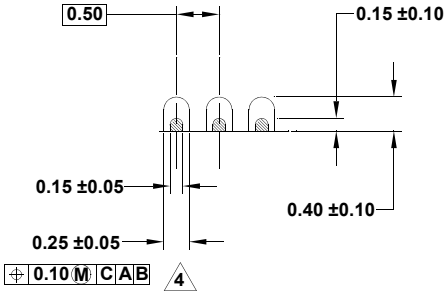
BOTTOM VIEW



SIDE VIEW



DETAIL "X"



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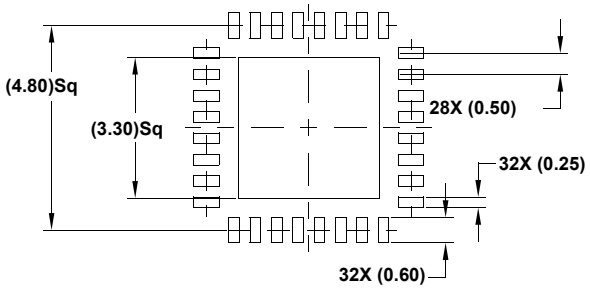


TYPICAL RECOMMENDED LAND PATTERN

NOTES:

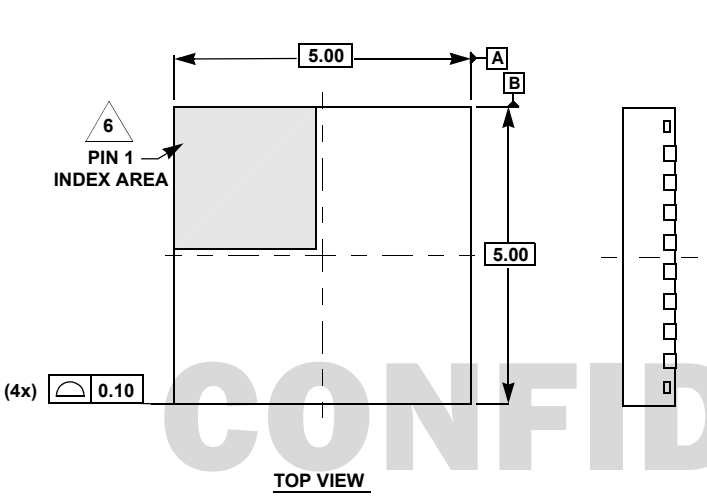
1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the plated terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
6. Reference document: JEDEC MO220

Package Outline Drawing

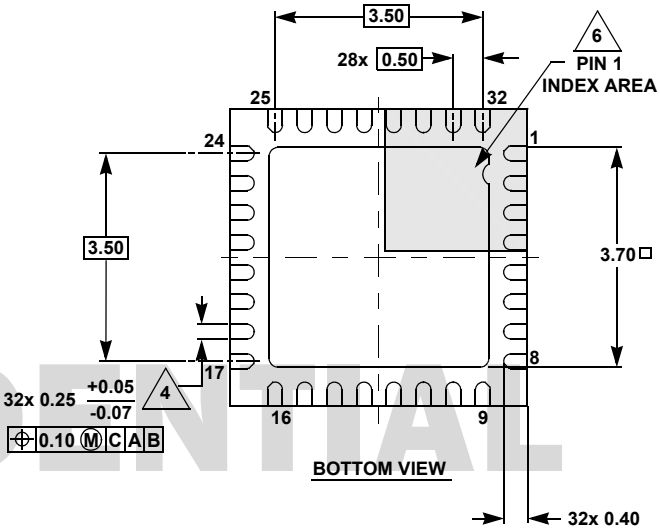
L32.5x5L

32 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

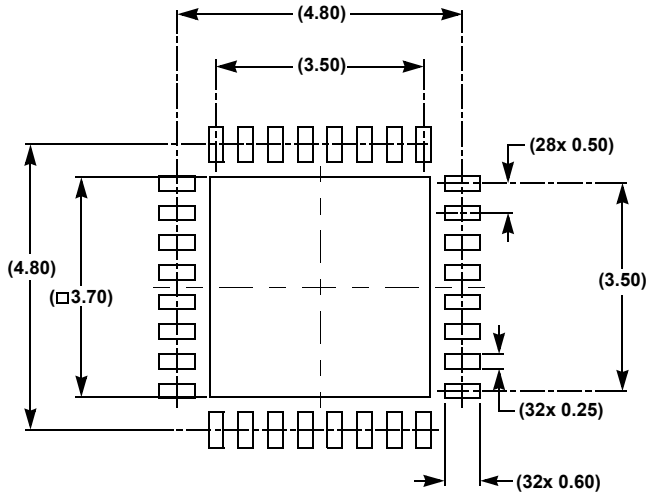
Rev 0, 10/14



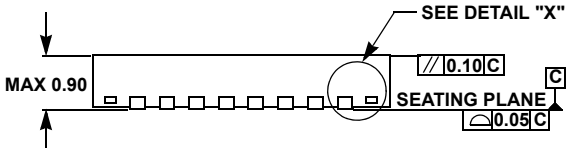
TOP VIEW



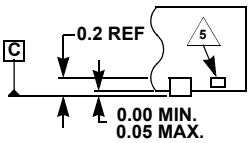
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDEVIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.