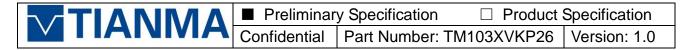
Specification

RFQ Number: <u>YX-TFTRFQ-ZX-20181221001</u>
Customer Part Number: <u>10.95.241032_008</u>
Tianma Part Number: <u>TM103XVKP26</u>
Description: <u>10.25" 1920x720</u>

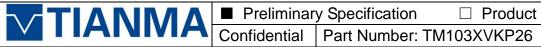
	Department	Name	Signature
Tianma	Integrate Project Manager	Cross Liu	
	Project Management	Xiaohong Qin	



Revision History

Version	Name	Date		
1.0	Section All	Revision Items First release	Xiaohong Qin	2019/2/11

RoHS





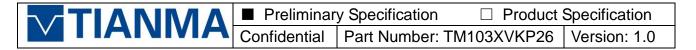
☐ Product Specification

Version: 1.0

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1. Features

This is 10.25 inch Amorphous-TFT-LCD (Thin Film Transistor Liquid Crystal Display) module. It is composed of a 10.25 inch TFT-LCD panel, LCD Driver IC with T-con integrated, FPC, a backlight unit and a CTP.

This is 10.25 inch TFT-LCD Normally Black SFT technology module which is designed for Automotive and other high reliability electronic products required high performance flat panel displays.

Requirements on Environmental Protection of this 10.25 inch module are Following RoHS.

2. General Specification

3. Feature	Specification	Remark
Diagonal Size	10.25 inch	
Resolution	1920(RGB) x 720	
Active Area(mm)	243.65 x 91.37	
CTP View Area(mm)	244.45x92.37	
Pixel Pitch (mm)	0.1269 x 0.1269	
Pixel Configuration	R.G.B. Vertical Stripe	
Technology Type	a-Si	
Display Mode	Normally Black	
Landscape or Portrait	Landscape	
Surface Treatment (Top Polarizer)/CTP Surface Treatment	HC/AG	
Gray Scale Inversion Direction	NA	
Optimal Viewing Direction	NA	
Interface	2 Port LVDS, VESA mode	
Color Depth	16.7 M	
Dimension (H x V x D) (mm)	259.84 x 109.30 x 8.5 module	Note 1
Dimension (H x V x D) (mm)	284.4 x 121.47 x10.6 with CTP	Note 2:
Weight (g)	456 (TYP)	Note 3:

Table 2.1 General TFT Specifications

Note 1: Requirements on Environmental Protection: RoHS

Note 2: The height dimension does not include the length of FPC

Note 3: LCM weight tolerance: ± 10%

CTP Feature	Specification	Remark
Surface Treatment	AGAF	
Top glass/layer hardness	3H(500g)	
Number of Simultaneous Touches	5Point	Note 3



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Accuracy central area	±2 mm	Note 1
Accuracy whole area (use 8mm copper column)	±2 mm	Note 1
Linearity central area	± 2 mm	Note 1
Linearity whole panel (use 8mm copper column)	±2 mm	Note 1
Report rate	120HZ	Note 2
1st touch latency	≤50ms	

Table 2.2 CTP Specifications

Note 1: Use 8mm copper column

Note 2: Max report rate for one finger on panel, only for reference

Note 3: Suggest no more than 5 points

3. Input/ Output Terminals

3.1 CN1 Pin assignment (TFT Interface)

Mating connector type (recommended): CN1 Connector: Iriso 11501S-50A-GFN1.

No	Symbol	I/O	Description	Remark
1	GND	Р	Ground	Note1
2	GND	Р	Ground	
3	GND	Р	Ground	
4	VDD	Р	3.3+/-0.3V	
5	VDD	Р	3.3+/-0.3V	
6	VDD	Р	3.3+/-0.3V	
7	VDD	Р	3.3+/-0.3V	
8	GND	Р	Ground	
9	SDA	I/O	Serial Interface address and data input/output keep floating.(TM Use For OTP Operation)	Note2
10	SCL	_	Serial Interface Clock input keep floating. (TM Use For OTP Operation)	
11	CSB	I	Serial Interface chip enable signal keep floating. (TM Use For OTP Operation)	
12	GND	Р	Ground	
13	OLV0N		Odd LVDS data input 0-	
14	OLV0P	ı	Odd LVDS data input 0+	
15	GND	Р	Ground	





16	OLV1N		Odd LVDS data input 1-	
17	OLV1N	- <u>'</u> 	'	
	GND	 Р	Odd LVDS data input 1+	
18			Ground	
19	OLV2N	<u> </u>	Odd LVDS data input 2-	
20	OLV2P	l	Odd LVDS data input 2+	
21	GND	Р	Ground	
22	OLVCKN		Odd LVDS Clock input -	
23	OLVCKP		Odd LVDS Clock input +	
24	GND	Р	Ground	
25	OLV3N		Odd LVDS data input 3-	
26	OLV3P	I	Odd LVDS data input 3+	
27	GND	Р	Ground	
28	ELV0N		Even LVDS data input 0-	
29	ELV0P		Even LVDS data input 0+	
30	GND	Р	Ground	
31	ELV1N		Even LVDS data input 1-	
32	ELV1P		Even LVDS data input 1+	
33	GND	Р	Ground	
34	ELV2N		Even LVDS data input 2-	
35	ELV2P		Even LVDS data input 2+	
36	GND	Р	Ground	
37	ELVCKN		Even LVDS Clock input -	
38	ELVCKP		Even LVDS Clock input +	
39	GND	Р	Ground	
40	ELV3N		Even LVDS data input 3-	
41	ELV3P	I	Even LVDS data input 3+	
42	GND	Р	Ground	
43	RESET	I	Global reset pin, active low.	
44	STBYB	I	Standby mode setting pin, active low.	
45	SHLR	I	Horizontal shift direction (source output) selection	Mario
46	UPDN	l	Vertical shift direction (gate output) selection	Note3
47	Fail_T	0	Output for fail detection	Note4
				•

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48	GND	Р	Ground, normally pull low	
49	NC	N	no connect	
50	NC	N	no connect(Reserve for VDD_OTP)	

Table 3.1.1 Pin assignment for TFT interface

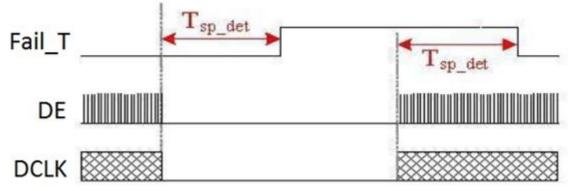
Note1: All of GND pins should be connected to system ground.

Note2: I/O definition.

I---Input, O---Output, P--- Power/Ground, N--- No connection

Note3: SHLR and UPDN pull "H" by customer

Note4:Fail_T—: normally pull L in IC, active "H".(when Hsync or Vsync or Clk miss, this pin will pull "H")



When CLK lost, Tsp det is 4000 DCLK (about 89us).

When DE lost, Tsp det is 1050000dclk (about 24ms).(assume DCLK = 45MHz)

Don't connect this pin to an output pin in customer system, it must be connected to Input pin or NC. Please keep no any pull up or pull low resister connect this pin on your system when this pin is used for fail detection.

Note5.Scan Direction Control Description

The level of TB and RL signal control vertical shift direction and horizontal shift direction.

Relationship between source output and RL.

SHLR	Source output sequence and data order	Remark
Н	Left→Right	Default
L	Right→Left	-

Relationship between vertical shift direction and TB.

UPDN	Function	Remark
Н	Top→Bottom	Default
L	Bottom→Top	-

Table 3.1.2 Scan direction Description

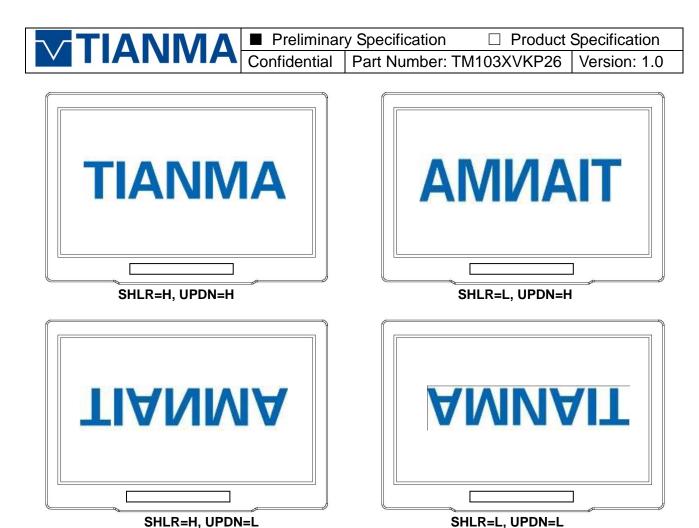


Figure 3.1.1 Description of Scan Direction

3.2 Pin assignment for backlight interface

Mating connector type: Iriso 12001S-12A-GEN1

No	Symbol	I/O	Description Re	emark				
1	A1	Р	VLED+ Anode1					
2	A2	Р	VLED+ Anode2					
3	A3	Р	VLED+ Anode3					
4	A4	Р	VLED+ Anode4					
5	NC	N	No Connection					
6	THER+	I/O	Thermistor +					
7	THER-	I/O	Thermistor -					
8	NC	N	No Connection					
9	C4	Р	VLED- Cathode4					
10	C3	Р	VLED- Cathode3					

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\	TIANINA		TIANMA ■ Preliminary Specification Confidential Part Number: TM10				☐ Product	Specification
		IIVI	Confidential	Part Number: T	M103XVKP26	Version: 1.0		
11	C2	Р		VLED- Cathode	2			
12	C1	Р		VLED- Cathode	1			

Table3.2.1 Pin assignment for backlight interface

3.3 Pin assignment for CTP interface

Mating connector type: Iriso 12001S-12A-GFN1

No	Symbol	I/O	Description	Comment
1	GND	Р	Ground	
			Serial Interface for programming.TM use it to	
2	SWDIO	I/O	upgrade CTP's firmware. If not use, please keep	
			floating.	
3	SCL	I	CTP I ² C Clock	
4	SDA	ı	CTP I ² C data	
5	INT	ı	CTP interrupt	
6	GND	Р	Ground	
7	GND	Р	Ground	
8	AVDD	Р	CTP power supply	
9	DVDD	Р	CTP power supply	
10	GND	Р	Ground	
11	REST	I	CTP reset input	
12	GND	Р	Ground	

Table3.1.3 Pin assignment for CTP interface

Note1: All of GND pins should be connected to system ground.

Note2: I/O definition: P--- Power/Ground, N--- No connection, I/O---Input/Output.

4. Absolute Maximum Ratings

GND=0V. Ta = 25° C

				5.12 	14 - 20 C
ltem	Symbol	Min	Max	Unit	Remark
Logic supply voltage	VDD	-0.3	3.96	V	
VDD Current(DC)	IVDD		600	mA	Note1
CTP power supply	AVDD	VSS-0.5	3.6	V	
CTP power supply	DVDD	VSS-0.5	3.6	V	
Operating Temperature	Тор	-30	85	$^{\circ}$ C	Note1
Storage Temperature	Tst	-40	90	$^{\circ}$	Note2,3

Table 4.1.1 Absolute Maximum Rating

Note1:test conditions: (1):VDD=3.3V,





(2):frame rate=60Hz,

(3)test temperature=25°C,

(4)test pattern: white pattern(max loading)

Note2:During -40~-30C(ambient),the operating performance is not guaranteed except functional failure occurs

Note3: Only for TFT module. For optical bonding, it is suggested shall not exceed 90 ℃.

Note4: If the voltage exceeds its absolute maximum ratings, the LCM may be damaged. If the LCM is operated with the absolute maximum ratings for a long time, performance will decreased

Note5: Functional operation should be restricted under normal ambient temperature.

5. Electrical Characteristics

5.1 DC Characteristics for Panel Driving

GND=0V, Ta = 25° C

Item	Symbol	MIN	TYP	MAX	Unit	Remark	
Supply voltage	VDD	3.0	3.3	3.6	V		
Permissible Ripple Voltage of VDD	Vr			100	mV	Note 1	
Input High Voltage	VIH	0.7*VDD		VDD+0.3	V	Note 2	
Input Low Voltage	VIL	GND-0.3		0.3*VDD	V	Note 2	
Output High Voltage	VOH	VDD-0.4		-	V	Note 3	
Output Low Voltage	VOL	GND		GND+0.4	V	inote 3	
Pull High/Low Resistor	RI		80		$K\Omega$	Note 4	

Table 5.1.1 Operating Voltages

Note1: Condition VDD=3.3V, white pattern, Typical input timing

Note2: SCL, CSB, SDA (SPI write), RESET, STBYB, SHLR, UPDN

Note3: SDA (SPI read), Fail_T

Note4: SCL, CSB, SDA, RESET, STBYB, SHLR, UPDN

Parameter	Symbol	mbol Condition		Spec				
Farameter	Parameter Symbol Condition		Min	Тур.	Max	Unit		
Differential input high threshold voltage	Vth	VCM=1.2V	+0.2	-	-	V		
Differential input low threshold voltage	Vtl	V CIVI= 1.2 V	-	-	-0.2	V		
Differential input common mode voltage	VCM	-	1	1.2	1.7- Vid /2	V		
LVDS input voltage	VINLV	-	0.7	-	1.7	V		
△LVDS common mode voltage	ΔVCM	1V <v 1.6v<="" <="" cm="" td=""><td>No limit</td><td>-</td><td>-</td><td>-</td></v>	No limit	-	-	-		
△LVDS common mode voltage	ΔVCM	1V <v 1.6v<="" <="" cm="" td=""><td>-</td><td>-</td><td>250</td><td>mV</td></v>	-	-	250	mV		

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	Confide	ntial	Part Number: TM103		3XVKP2	6 Version:	1.0	
Differential input voltage	Vid		-	0.2	_	0.6	V	
LVDS terminal match resistor	RLVDS				100		Ω	

Table 5.1.2 LVDS mode DC electrical characteristics

Note1: Above of all these items spec is the precondition that panel can operate normally.

Note 2: This is preliminary SPEC, some of these items may be updated according to panel actually display quality and actually electrical characteristics.

Note3: Description of |Vid| is as below

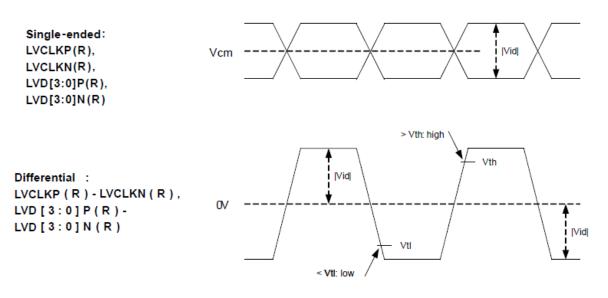


Table 5.1.3 Operating voltage

Table 5.1.2 Current consumption

5.2 DC Characteristics for CTP

GND=0V, Ta = 25° C

Item	Symbol	Min	Тур.	Max	Unit	Remark
Digital power supply for CTP controller	DVDD	3.0	3.3	3.6	V	
Analog power supply for CTP controller	AVDD	3.0	3.3	3.6	V	
Input signal high level	VIH	0.7 × VDD	ı	VDD	V	Note1
Input signal low level	VIL	0	-	0.3× VDD	V	
Output signal high level	VOH	VDD-0.6	-	VDD	V	

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TIANIM	▲ Prelimination	■ Preliminary Specification			☐ Product Specification TM103XVKP26 Version: 1.0				
V IIAIVIA	Confidenti	ial Part N	lumber: ⁻	TM103XVKI	P26 V	ersion: 1.0			
·									
Output signal low level	VOL	0	-	0.4	V				

Table 5.2.1 Operating Voltages

Note1: DVDD=AVDD

5.3 DC Characteristics for Backlight Driving

Item	Symbol	Min	Тур.	Max	Unit	Remark	
Forward Current	I _F	-	70	90	mA	Note1	
Forward Voltage	V_{BL}	23.76	26.46	28.26	V	I 70m Λ	
Backlight Power Consumption	W _{BL}	6.65	7.41	7.91	W	I _F =70mA	
Lifetime	-	10000	-	-	Hrs	Note2	

Table 5.3.1 LED backlight characteristics

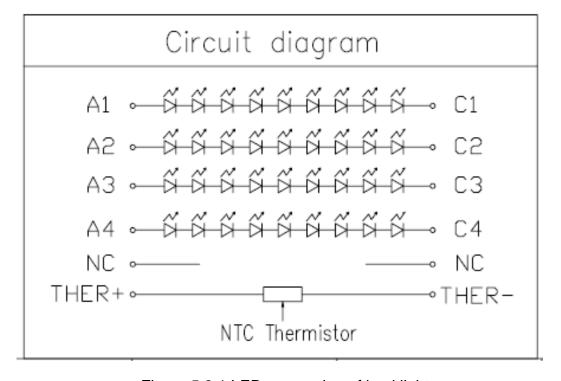


Figure 5.3.1 LED connection of backlight

Item	Value	Remarks
Part Number	NCP15XH103F0SRC	Murata
Resistance Tolerance	10k Ω ±1%	Ta=25℃
Permissive Operating Current	0.31mA	Ta=25℃





Table 5.3.2 Thermistor Description

Note 1: I_F =70mA is defined for one channel LED, There are total 4 LED channels in back light unit Under LCM operating, the stable forward current should be inputted.

Note 2: Optical performance should be evaluated at Ta=25°C only. If LED is driven by high current, high ambient temperature & humidity condition, the life time of LED will be reduced. Operating life means brightness goes down to 80% of original brightness.it is suggested Customer to make sure the LCM module in the system is well heat dissipation.

Note3: An NTC thermistor is included in the LED circuit. Part number: NCP15XH103F0SRC. It is used for the measuring LED temperature and is located in the LED circuit on the backlight FPC.

Note4: To reduce the influence of NTC self-heating and improve the measurement accuracy, suggest the operating current of NTC is 0.031mA.

Note5: When operating at high temperature, NTC resistance should not be below TBD

5.4 Recommended Power ON/OFF Sequence

Power on Sequence

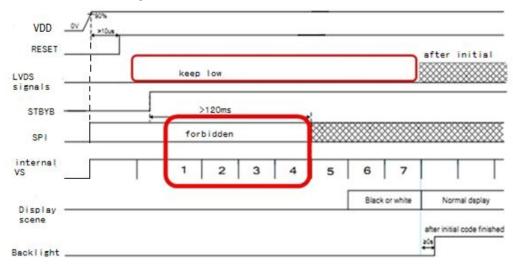


Figure 5.4.1 Power on Sequence

Note:

- (1) The system must start to continuously apply external display data before STBYB rising.
- (2) The SPI signals should start 120ms after STBYB rising.

Power off Sequence

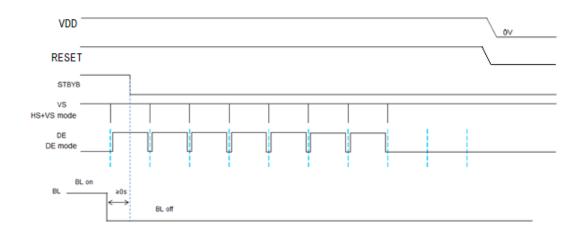


Figure 5.4.2 Power off Sequence

Note1: The low level of these signals and analog powers are GND level.

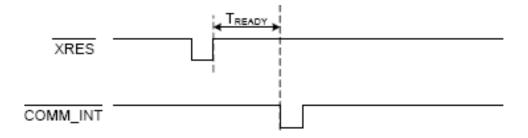
Note2: All of the power and signals should be kept at GND level before power on. If there are residual voltages on them, the LCD might not work properly.

Note3: VLED is the voltage applied to backlight. Keep it turned off until the display stabilizes.

5.5 Recommended Power ON Sequence for CTP

5.5.1 Chip-Level AC Specifications

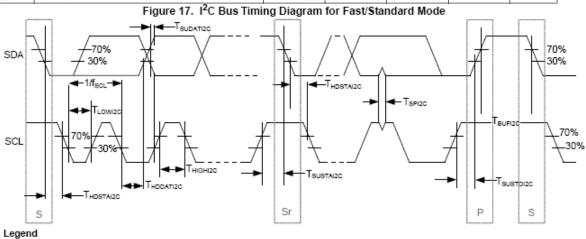
Symbol	description	condition	MIN	TYP	MAX	Unit
TXRST	External reset (XRES) pulse width	After VDDD is valid	10	ı	-	μ s
TREADY	Time from deassertion of XRES to COMM_INT(CTP_INT)	-	-	1	16	ms
TCAL	Calibration routine execution time	-	-	1	2500	ms
FIMOTO L1	Frequency variation at 37 MHz and 48 MHz	-	-	-	±2	%





5.5.2 AC Characteristics of the I2C SDA and SCL Pins(CTP_VDD=3.3V)

O la l	B	Standa	rd Mode	Fast		
Symbol	Description	Min	Max	Min	Max	Units
f _{SCLI2C}	SCL clock frequency	0	100	0	400	kHz
T _{HDSTAI2C}	Hold time (repeated) start condition. After this period, the first clock pulse is generated.	4	_	0.6	-	μs
T _{LOWI2C}	LOW period of SCL clock	4.7	-	1.3	-	μs
T _{HIGHI2C}	HIGH period of SCL clock	4	-	0.6	-	μs
T _{SUSTAI2C}	Setup time for repeated start condition	4.7	-	0.6	-	μs
T _{HDDATI2C}	Data hold time	0	-	0	-	μs
T _{SUDATI2C}	Data setup time	250	-	100	-	ns
T _{VDDATI2C}	Data valid time	_	3.45	_	0.9	μs
T _{VDACKI2C}	Data acknowledge time	_	3.45	-	0.9	μs
T _{SUSTOI2C}	Setup time for stop condition	4	-	0.6	-	μs
V_{HH}	Input hysteresis high voltage, $1.71V \le V_{DDD} \le 1.95V$ or $3.0V \le V_{DDD} \le 5.5V$	0.1 × V _{DDD}	_	0.1 × V _{DDD}	-	V
T _{BUFI2C}	Bus free time between a stop and start condition	4.7	_	1.3	_	μs
T _{SPI2C}	Pulse width of spikes that are suppressed by input filter	-	-	50	-	ns
C _{BUS}	Capacitance load for SDA or SCL	-	400	-	400	pF
V _{IL_I2C}	Input low voltage	-0.5	0.3 × V _{DDD}	-0.5	0.3 × V _{DDD}	V
V _{IH_I2C}	Input high voltage	0.7 × V _{DDD}	-	0.7 × V _{DDD}	-	V
V _{OL_I2C_L}	Output low voltage (V _{DDD} ≤ 2V, 3 mA sink)	0.2 × V _{DDD}	-	0.2 × V _{DDD}	-	V
V _{OL_I2C_H}	Output low voltage (V _{DDD} > 3V, 3 mA sink)	0.4	-	0.4	-	V
	Output low current	-	3	-	3	mA
OL_I2C	Output low current V _{OL} = 0.6V	_	-	-	6	mA
V _{H I2C}	Input hysteresis	0.1 × V _{DDD}	_	0.1 × V _{DDD}	-	m∨



S: I²C Start Condition Sr: I²C Repeat Start Condition

P: I2C Stop Condition

Note1 more information please refer to the CTP driver SPEC.

5.6 LCD Module Block Diagram



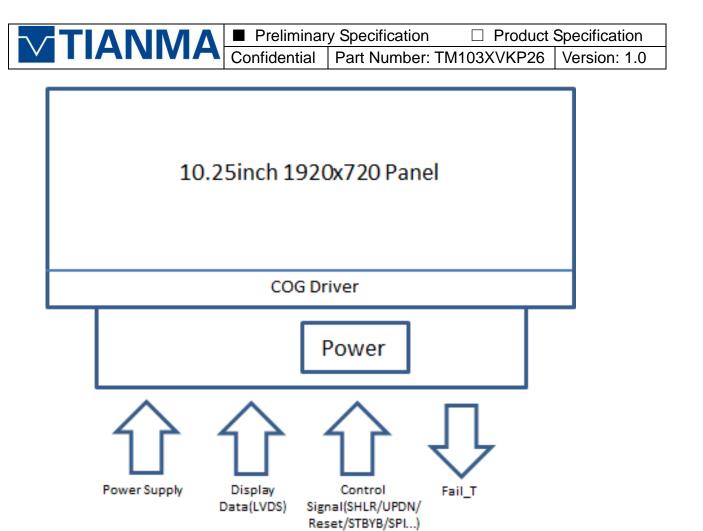


Figure 5.6.1 LCD Module Block Diagram

6. Timing Characteristics

6.1 Input Timing Characteristics

(GND=0V)

Parameter	Symbol	Unit	Min.	Тур.	Max.	REMARKS
Clock Frequency	f _{dck}	MHz	44.6	44.7	50.2	
H Total Time	T _{hp}	clocks	1020	1024	1150	
H Active Time	HA	clocks		960		
V Total Time	T _{vp}	lines	726	728	849	
V Active Time	VA	lines		720		
V Frequency	f _v	Hz	-	60Hz	-	

Table 6.1.1 Input timing



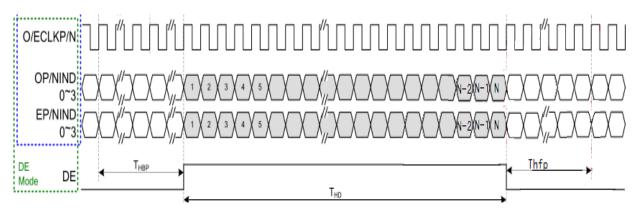


Figure 6.1.1 Horizontal input timing

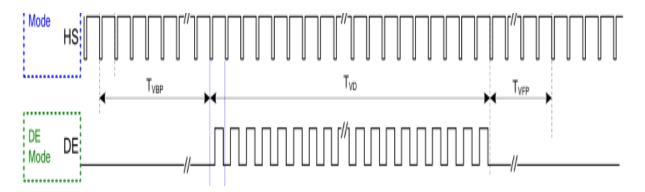
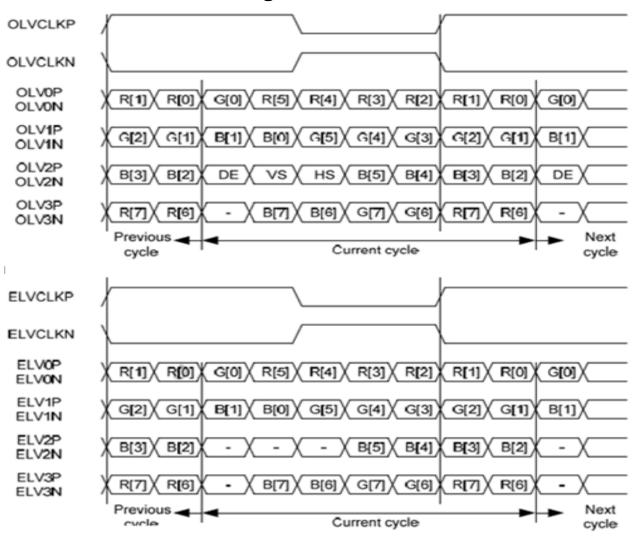


Figure 6.1.2 Vertical input timing



6.2 LVDS Interface Timing Characteristics



2-port LVDS signals, VESA format (8-bit) Figure 6.2.1 LVDS data mapping

Parameter	Symbol	Min	Тур.	Max	Unit	Condition
Clock frequency	FLVCLK	25	-	85	MHz	Refer to input
						timing table
Clock Period	TLVCLK	40	-	11.7	ns	
				6		
Clock high time	TLVCH	-	4/(7*	-	ns	
			RXFCLK)			
Clock low time	TLVCL	-	3/(7*	-	ns	
			RXFCLK)			
Input data skew	TRSKM	-	-	0.25	UI	VCC_IF=1.8V
margin						w/o SSC
Strobe width	TSW	0.5	-	-	UI	

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_	ı		1	1	1	1
1 data bit time	UI	-	1/7	-	TLVC	
					LK	
Position 1	TPOS1	-0.25	0	0.25	UI	
Position 0	TPOS0	0.75	1	1.25	UI	
Position 6	TPOS6	1.75	2	2.25	UI	
Position 5	TPOS5	2.75	3	3.25	UI	
Position 4	TPOS4	3.75	4	4.25	UI	
Position 3	TPOS3	4.75	5	5.25	UI	
Position 2	TPOS2	5.75	6	6.25	UI	
PLL wake-up	TenPLL	-	-	150	us	
time						
Modulation	SSCMF	23	-	93	KHz	
Frequency						
Modulation Rate	SSCMR	-3	-	3	%	LVDS clock =
						81MHz, center
						spread

Figure 6.2.2 LVDS mode AC electrical characteristics

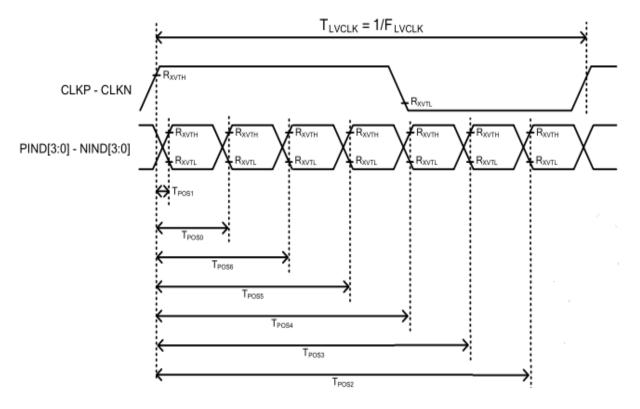


Figure 6.2.3 LVDS input timing



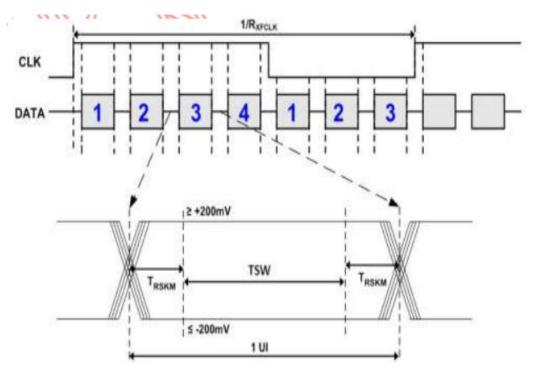


Figure 6.2.4 LVDS input eye diagram

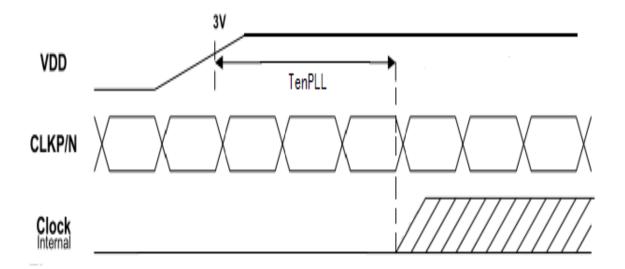


Figure 6.2.5 LVDS wake up time

RoHS



7. Optical Characteristics

Iten	n	Symbol	Condition	Min	Тур.	Max	Unit	Remark	
		θU		80	88				
\ <i>r</i>		θD	CD > 10	80	88		D	N 1	
Viewing A	ngie	θL	CR≧10	80	88		Degree	Note1	
		θR		80	88				
Contrast F	Ratio	CR	Vertical,25℃	700	1000			Note2 Note3	
		T _{ON} / T _{OFF}	25℃			30			
Response	Time	T _{ON} / T _{OFF}	0℃				ms		
ТСОРОПОС	TIITIC	T _{ON} / T _{OFF}	-20℃			250	1113	Note4	
		T _{ON} / T _{OFF}	-30℃			600			
	White	Х	CIE1931-XY Z	0.267	0.307	0.347			
	VVIIILE	у		0.294	0.334	0.374		Note5 Note2	
	Red	Х		0.606	0.636	0.666			
Chromoticity		у		0.304	0.334	0.364			
Chromaticity	Green	Х		0.290	0.320	0.350			
	Green	у		0.602	0.632	0.662			
	Blue	х		0.117	0.147	0.177			
	Dide	у		0.028	0.058	0.088			
NTSC			CIE1931-XY Z	65	70		%	Note5	
Uniformity W		U	25℃	80			%	Note2 Note6	
Luminance		L	25℃	800			cd/m ²	Note2 Note7	
Flicker						-20		Note9	
Reflectivity	(SCI)					7%		Note8	
Gamm	a	Υ	VESA	2.2	2.5	2.8			

Test Conditions:

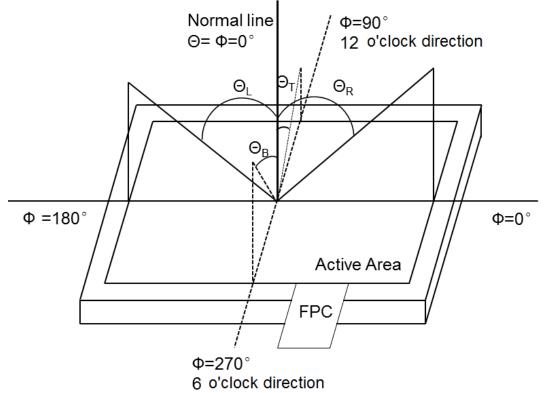
- 1. I_F = 70 mA(one channel), there are total 4 LED channels in back light unit Under LCM operating , the stable forward current should be inputted, the ambient temperature is 25 $^{\circ}$ C.
- 2. The test systems refer to Note 1 and Note 2.

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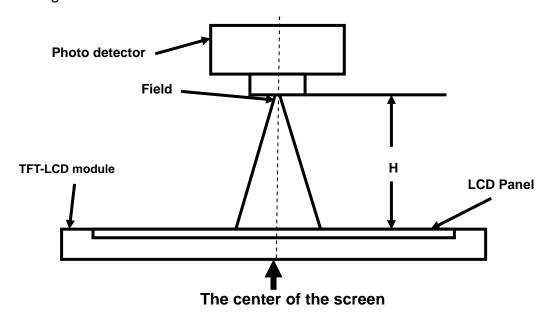


Note1: Definition of viewing angle range and measurement system



Note2: Definition of optical measurement system Measured at the center of the panel by SR-3. Measuring condition:

- Measuring surroundings: Dark room.
- Measuring temperature: Ta=+25°C.
- Adjust operating voltage to get optimum contrast at the center of the display.
- Measured value at the center point of LCD panel after more than 10 minutes while backlight is turned on.



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Item	Photo detector	Field	High	
Contrast Ratio				
Luminance	SR-3/ CS2000	1°	H=500mm	
Chromaticity	3R-3/ C32000	l l	H=300HIII	
Lum Uniformity				
Contrast Plot	EZ-Contrast/ DMS	6mm/3mm	H=1mm/H≈80mm	
Response Time	LCD5200	3mm	H=200mm	
Reflectivity	CM3600A/CM2600	8mm/25.4mm	H=0mm	

Note3: Definition of contrast ratio:

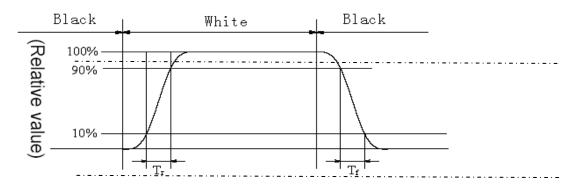
Contrast Ratio(CR)= Luminance When LCD is White Luminance When LCD is Black

Contrast Ratio is measured in optimum common electrode voltage

Note4: Definition of Response time:

Top is the temperature of panel surface.

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (T_{ON}) is the time between photo detector output intensity changed from 10% to 90%. And fall time (T_{OFF}) is the time between photo detector output intensity changed from 90% to 10%. Refer to the figure below:

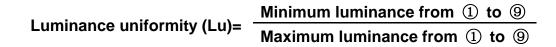


Note5: Definition of color chromaticity (CIE1931)

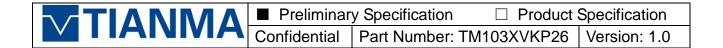
Color coordinates measured at the center point of the LCD.

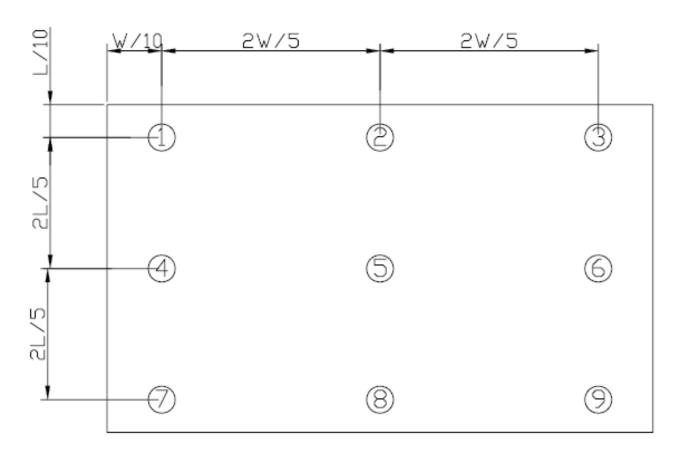
Note6: Definition of Luminance Uniformity

The luminance uniformity is calculated by using following formula.



Luminance is measured at the 9 points shown below.





Note7: Definition of Luminance

Measure the luminance at white state at the center point.

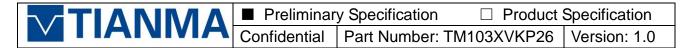
Note8: SCI reflective ratio measure method.

Measurement system: CM 3600A fully integral sphere

Light source: D65 d/8° (ASTM E 1164-09) Observing angle: 10° State: LCD powered off

Standard d/8° Integration Sphere Spectroscopic – Reflectometer

Note9: The value % base on CR measurement method, dB base on JEITA method



8. CTP Characteristics

No.	Parameters	Unit	Requirement
1	Structure	-	OGS
2	Sensor structure	-	SITO SENSOR GLASS
3	Type of touch	-	Projected capacitive type
4	ITO pattern type	-	ITO bridge
5	Multi-touch	points	5points
6	Outline Size	mm	284.40(H)x121.47(V)x1.96(T)
7	Active Area	mm	244.45(H) x 92.37(V)
8	Finger Size	mm	8
9	Finger Separation	mm	≤ 15
10	Reflectance(λ =550nm)	%	Optical bonding type, reflector 7%(max) with TFT
11	Transmittance (λ =550nm)	%	≥ 90(with OCR)
12	Surface Treatment(Haze)	%	≤ 7.5%
13	Operating Temp.	\mathbb{C}	-30~85
14	Operating Humidity.	%	≤ 90
15	Storage Temp.	$^{\circ}$	-40~90
16	Response Time	ms	≤ 30
17	Surface hardness	-	≥3H(500gf)

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9. Reliability Test

9.1 Content of Reliability Test

No.	Test Item	Test condition	Criterion
1	High Temperature Storage	90°C 500H RH<=45% Restore 2H at 25°C Power off	Note 1, Note 2 IEC 60 068 - 2 - 2Bb
2	Low Temperature Storage	-40°C 500H Restore 2H at 25°C Power off	Note 1, Note 2 IEC 60 068 - 2 - 1Ab
3	High Temperature Operation	+85°C 500H RH<=45% Restore 2H at 25°C Power on	Note 1 , Note 2,Note 3 IEC 60 068 - 2 - 2Bb
4	Low Temperature Operation	-30°C 500H Restore 2H at 25°C Power on	Note 1, Note 2 IEC 60 068 - 2 - 1Ab
5	High Temperature & Humidity Operation	60°C, 90%RH 500H Power on	Note 1 IEC 60 068 - 2 - 3Ca
6	Thermal Shock	-40° C→ change→+85° C 30min 5min 30min 100cycle non-operation	Note 1 , Note 2 IEC 60 068 - 2 - 14Nb
7	Vibration Test	Frequency: 8 - 33.3 Hz, Total amplitude: 1.3mm Frequency: 33.3 - 400 Hz, Acceleration: 29.4 m/s² sweep time: 15 minutes 2 hours each for X and Z directions, 4 hours for Y direction (total 8 hours) Non-operation	Note 2 IEC 60 068 - 2 - 6Fc
8	Shock Test	100 x 9.8m/s2, t=6ms, XYZ directions, Half sin curve, [non-operating],each directions 2 times	Note 2 IEC 60 068 - 2 - 27Ea
9	ESD	Air discharge: $C=150pF\pm10\%, R=330~\Omega\pm10\%, 5$ point/panel Air: +/-15KV, 5times Contact discharge: $C=150pF\pm10\%, R=330~\Omega\pm10\%, 5$ point/panel Contact: +/-8KV,5times	GB/T17626 (IEC61000) / ISO10605 Class C GB/T17626 (IEC61000) / ISO10605 Class C

Notes:

The test result shall be evaluated after the sample has been left at room temperature and TIANMA MICROELECTRONICS CO., LTD 26 / 36





humidity for 2 hours without load. No condensation shall be accepted. The sample shall be free from defects:

- 1). Air bubble in the LCD;
- 2).Sealleak
- 3).Non-display
- 4).missing segments
- 5).Glass crack

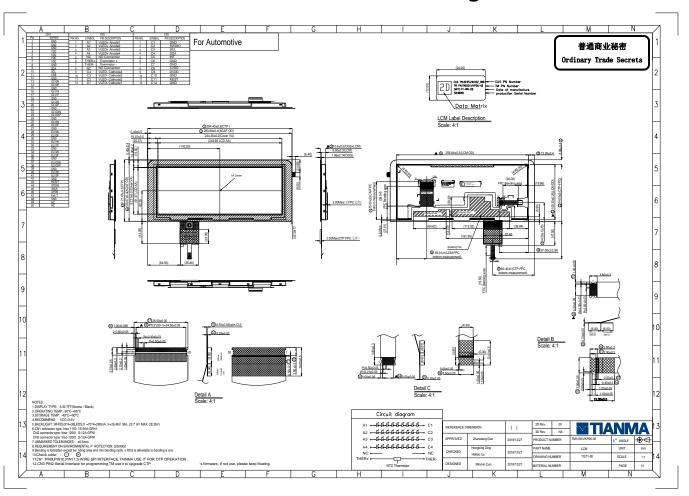
Note 2: Each test item applies for a test sample only once, the test sample can't be used again in any other test item. The samples of these tests will not be accepted if appear these defects as Note1

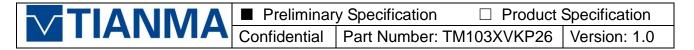
Note 3: LED forward current should follow the De-rating curve and the NTC resistance should not be below TBD

Note 4: After item 1 to 6 tests, the Mura, BLU peeling ,bubbles and PC delamination caused by CTP warpage are not controlled, and the client agrees to accept them.

10.

Mechanical Drawing





11. Product Inspection Criteria

11.1 Inspection Conditions

The customer shall inspect the modules within twenty calendar days of the delivery date (the inspection period) at its own cost. The result of the inspection (acceptance or rejection) shall be recorded in writing, and a copy of this writing will be promptly sent to the seller, If the results of the inspecting from buyer does not send to the seller within twenty calendar days of the delivery date. The modules shall be regards as acceptance.

Should the customer fail to notify the seller within the inspection period, the buyers right to reject the modules. Shall be lapsed and the modules shall be deemed to have been accepted by the buyer.

11.2 Inspection Conditions

11.2.1 Ambient conditions:

a. Temperature: Room temperature 25±5°C

b. Humidity: (60±10) %RH

c. Illumination:

Visual test: Max 300Lux Appearance test: Min 700Lux

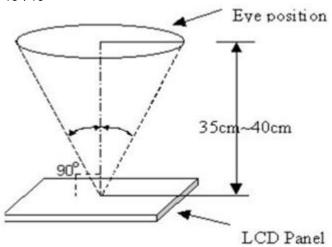
11.2.2 Viewing distance

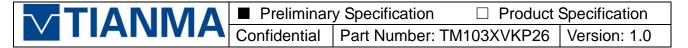
The distance between the LCD and the inspector's eyes shall be $35 \sim 40$ cm.

The distance between LCD and ND filter is 3~5cm.

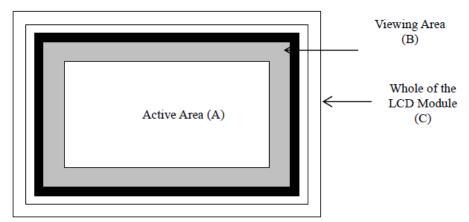
11.2.3 Viewing Angle

U/D: 30°/25°, L/R: 40°/40°





11.2.4 Definition of LCD zone



A-zone: The inside of the Active Area(as defined on the product drawing)

B-zone: The inside of the Viewing Area which is between A-zone and the metal

frame.(Including CTP Black painting area)

C-zone: Whole of the LCD Module except the zone A and B. (Including FPC& Metal

Frame & backside of the LCD Module)

11.3 Dot and Line defect Criteria

Defects are classified as major defects and minor defects according to the definition hereunder:

11.3.1 Major defect

No	Inspection Items	Inspection Standard
1	All functional defects	1) No display 2) Abnormal display 3) Short circuit 4) Line defect
2	Missing	Missing function component.
3	Crack	Glass crack

11.3.2 Minor defect

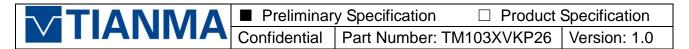
Item No	Items to be inspected	Inspection standard
1	Spot Defect Including Black spot White spot	For dark/white spot is defined φ = (x+y) /2 → X ← ↓ y

	B/L particle Cell particle	Size φ (mm)	Acceptable Quantity
	Polarizer particle	φ ≰0.2	Ignore
		0.2 < <i>φ</i> ≤0.40	3 (distance ≱0mm)
		0.40 < φ	Not allowed
		Define:	h .
2	Line Defect Including Black line	Width(mm) Length(mm)	Acceptable Quantity
	White line Scratch	W≤0.03 and L≤5	Ignore
		0.03< W≤0.05 and L≤5	4 (distance≥15mm)
		0.05< W or L>5	Not allowed
		Size φ (mm)	Acceptable Quantity
	5.1.	<i>φ</i> € 0.25	Ignore
3	Polarizer Dent/Bubble	0.25 < ⊕ €0.4	3 (distance≥10mm)
		0.4 < φ	0
		Bright and Black dot def	ine:
	Electrical Dot Defect	克 點	and
4		Inspection pattern: Full vand blue screens	white、Full black、Red、green
		Item	Acceptable Quantity
		Black dot defect	€3
		Bright dot defect	0

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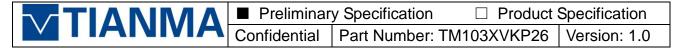
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	1	T		
5	Display non-uniformity	3% ND filter is used when display black pattern	There should not be visible non-uniformity	
6	Other cosmetic defect	Crack、split、 deformation、shock trace	Not allowed	
7	CTP glass	Y≤0.05mm	Ignore	
	Protrusion	X≤1mm, and 0.05mm <y≤0.1mm< td=""><td colspan="2">每边≤2 个,总数≤5 个,间距大于 15mm</td></y≤0.1mm<>	每边≤2 个,总数≤5 个,间距大于 15mm	
		<i>φ</i> ≤ 0.10mm	Ignore	
8	BM Dot pervious to light	0.10 < <i>φ</i> ≤ 0.20	≤4 (distance≥15mm)	
		$\varphi>$ 0.20	None	
9		W≤0.02	Ignore	
	BM Strip pervious to light	0.02 <w≤0.03,l ≤<br="">3mm</w≤0.03,l>	N≤3 (distance≥10mm)	
		W>0.03mm	None	
10	Printing edge sawtooth / light	W ≦ 0.1 mm	Ignore	
	leakage	W > 0.1mm	None	
11	IR/Key/Logo issue(light leakage/ Color difference / sawtooth,etc)	φ \leqslant 0.03	None	
		0.03< <i>φ</i> ≤0.05	One side allows one	
		0.05mm <w⊴0.10mm</w	One side allows one One side N≤3	



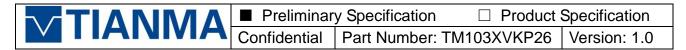


12	CTD shipping	Corner Fragment: X≤0.3mm Y≤0.3mm Z≤1/2T	Ignore T: Glass thickness	
	CTP chipping	Side Fragment: X≤3mm Y≤0.3mm Z≤1/2T	Ignore T: Glass thickness	
13		D≤0.20mm	3	
	Bad camera hole	0.2≰ 0 ≰0.30mm	1	
		D>0.3	None	
1.4	BM \ ink fall off	W⊴0.1mm	Ignore	
14		W>0.1mm	None	
15	AG/ASF	By product edge inward 1mm range no controlled	1	
16	Dirty/Dust	Those wiped out easily are acceptable	1	

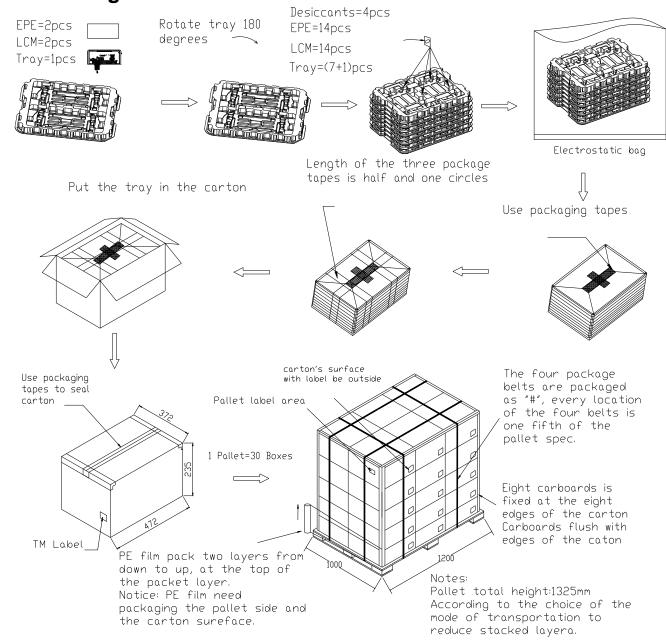
Remarks: Cosmetic criterion or RA criterion which not specified in CTP specification are not managed and controlled by Tianma.

Note:

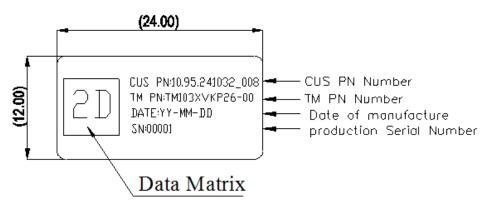
- 1. Dot defect is defined as the defective area is larger than 50% of the dot area. Continuous dot defect is not allowed. And the bright dot defect must be visible through 3% ND filter.
- 2. Polarizer bubble is defined as the bubble appears on active display area. The defect of polarizer bubble shall be ignored if the polarizer bubble appears on the outside of active display area.



12.Packing Instruction

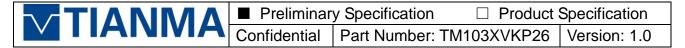


Module label information



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13. Appendix

13.1 The relationship of temperature and resistance for NTC:

TEMP	Resistance	TEMP	Resistance	TEMP	Resistance	TEMP	Resistanc
(deg.C)	(kohm)	(deg.C)	(kohm)	(deg.C)	(kohm)	(deg.C)	е
			, ,		, ,		(kohm)
-40.000	195.652	2.000	24.988	44.000	5.086	86.000	1.413
-39.000	184.917	3.000	23.951	45.000	4.917	87.000	1.375
-38.000	174.845	4.000	22.963	46.000	4.754	88.000	1.338
-37.000	165.391	5.000	22.021	47.000	4.597	89.000	1.303
-36.000	156.513	6.000	21.123	48.000	4.446	90.000	1.268
-35.000	148.171	7.000	20.267	49.000	4.301	91.000	1.234
-34.000	140.330	8.000	19.450	50.000	4.161	92.000	1.202
-33.000	132.958	9.000	18.670	51.000	4.026	93.000	1.170
-32.000	126.022	10.000	17.926	52.000	3.896	94.000	1.139
-31.000	119.494	11.000	17.214	53.000	3.771	95.000	1.110
-30.000	113.347	12.000	16.534	54.000	3.651	96.000	1.081
-29.000	107.565	13.000	15.886	55.000	3.535	97.000	1.053
-28.000	102.116	14.000	15.266	56.000	3.423	98.000	1.026
-27.000	96.978	15.000	14.674	57.000	3.315	99.000	0.999
-26.000	92.132	16.000	14.108	58.000	3.211	100.000	0.974
-25.000	87.559	17.000	13.566	59.000	3.111	101.000	0.949
-24.000	83.242	18.000	13.049	60.000	3.014	102.000	0.925
-23.000	79.166	19.000	12.554	61.000	2.922	103.000	0.902
-22.000	75.316	20.000	12.081	62.000	2.834	104.000	0.880
-21.000	71.677	21.000	11.628	63.000	2.748	105.000	0.858
-20.000	68.237	22.000	11.195	64.000	2.666	106.000	0.837
-19.000	64.991	23.000	10.780	65.000	2.586	107.000	0.816
-18.000	61.919	24.000	10.382	66.000	2.509	108.000	0.796
-17.000	59.011	25.000	10.000	67.000	2.435	109.000	0.777
-16.000	56.258	26.000	9.634	68.000	2.364	110.000	0.758
-15.000	53.650	27.000	9.284	69.000	2.294	111.000	0.740
-14.000	51.178	28.000	8.947	70.000	2.228	112.000	0.722
-13.000	48.835	29.000	8.624	71.000	2.163	113.000	0.705
-12.000	46.613	30.000	8.315	72.000	2.100	114.000	0.688
-11.000	44.506	31.000	8.018	73.000	2.040	115.000	0.672
-10.000	42.506	32.000	7.734	74.000	1.981	116.000	0.656
-9.000	40.600	33.000	7.461	75.000	1.925	117.000	0.640
-8.000	38.791	34.000	7.199	76.000	1.870	118.000	0.625
-7.000	37.073	35.000	6.948	77.000	1.817	119.000	0.611
-6.000	35.442	36.000	6.707	78.000	1.766	120.000	0.596
-5.000	33.892	37.000	6.475	79.000	1.716	121.000	0.583
-4.000	32.420	38.000	6.253	80.000	1.669	122.000	0.569
-3.000	31.020	39.000	6.039	81.000	1.622	123.000	0.556
-2.000	29.689	40.000	5.834	82.000	1.578	124.000	0.544

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TIANMA		// -	■ Preliminary Specification		n 🗆 P	□ Product Specification			
		Co	nfidential	Part Number	Part Number: TM103XVk		ersion: 1.0		
-1.000	28.423	41.000	5.636	83.000	1.535	125.000	0.531		
0.000	27.219	42.000	5.445	84.000	1.493				
1.000	26.076	43.000	5.262	85.000	1.452				

14. Precautions for Use of LCD Module

14.1Handling Precautions

- 13.1.1The display panel is made of glass. Do not subject it to mechanical shock by dropping it, etc.
- 13.1.2If the display panel is damaged and the liquid crystal fluid inside it leaks out be sure not to get any in your mouth. If the fluid comes into contact with your skin or clothes promptly wash it off using soap and water.
- 13.1.3 Do not apply excessive force to the display surface or the bezel since this may cause the color tone to vary.
- 13.1.4 The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle the polarizer carefully.
- 13.1.5 If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If it is still not completely clear use a moist cloth with one of the following solvents:
 - Isopropyl alcohol
 - Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Specifically, do not use the following:

- Water
- Ketone
- Aromatic solvents
- 13.1.6 Do not attempt to disassemble the LCD Module.
- 13.1.7 If the logic circuitry is powered off, do not apply the input signals.
- 13.1.8 To prevent destruction of the module by static electricity, be careful to maintain an optimum work environment.
 - 13.1.8.1Be sure to ground your body when handling the LCD Modules.
 - 13.1.8.2Tools used for assembly, such as soldering irons, must be properly grounded.
 - 13.1.8.3 To reduce the amount of static electricity generated, do not conduct assembly or other work under very low humidity conditions.
 - 13.1.8.4 The LCD Module is covered with a film to protect the display surface. Be careful when peeling off this protective film since static electricity may be generated.

14.2 Storage precautions

- 13.1.9When storing the LCD modules avoid exposure to direct sunlight or to the light of fluorescent lamps.
- 13.1.10 The LCD modules should be stored within the rated storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature: 15 ~ 35 degree C (or at least Temp. 10 ~ 40 degree C / Humidity



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25% ~ 75%), for National Std. recommendation

13.1.11 The LCD modules should be stored in a room without acid, alkali or other harmful gases.

14.3 Transportation Precautions

The LCD modules should not be dropped or subject to violent mechanical shock during transportation. Also they should avoid excessive pressure, water, high humidity and direct sunlight.