i.MX 6 Development Deep Dive: Image and Display Application

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External Use

IPU Overview

Video & Graphics System in i.MX6 D/Q

Full HW Support –> Multiple Advantages

- The CPU does not have to touch pixels –> available to run application
- Optimized data path –> reduced DDR load –> complex use cases
- Lower power consumption (because of both aspects above)

Video Sources

Displays

Interface Bridges
LVDS, HDMI, MIPI

DCICs
Display Content Integrity Check

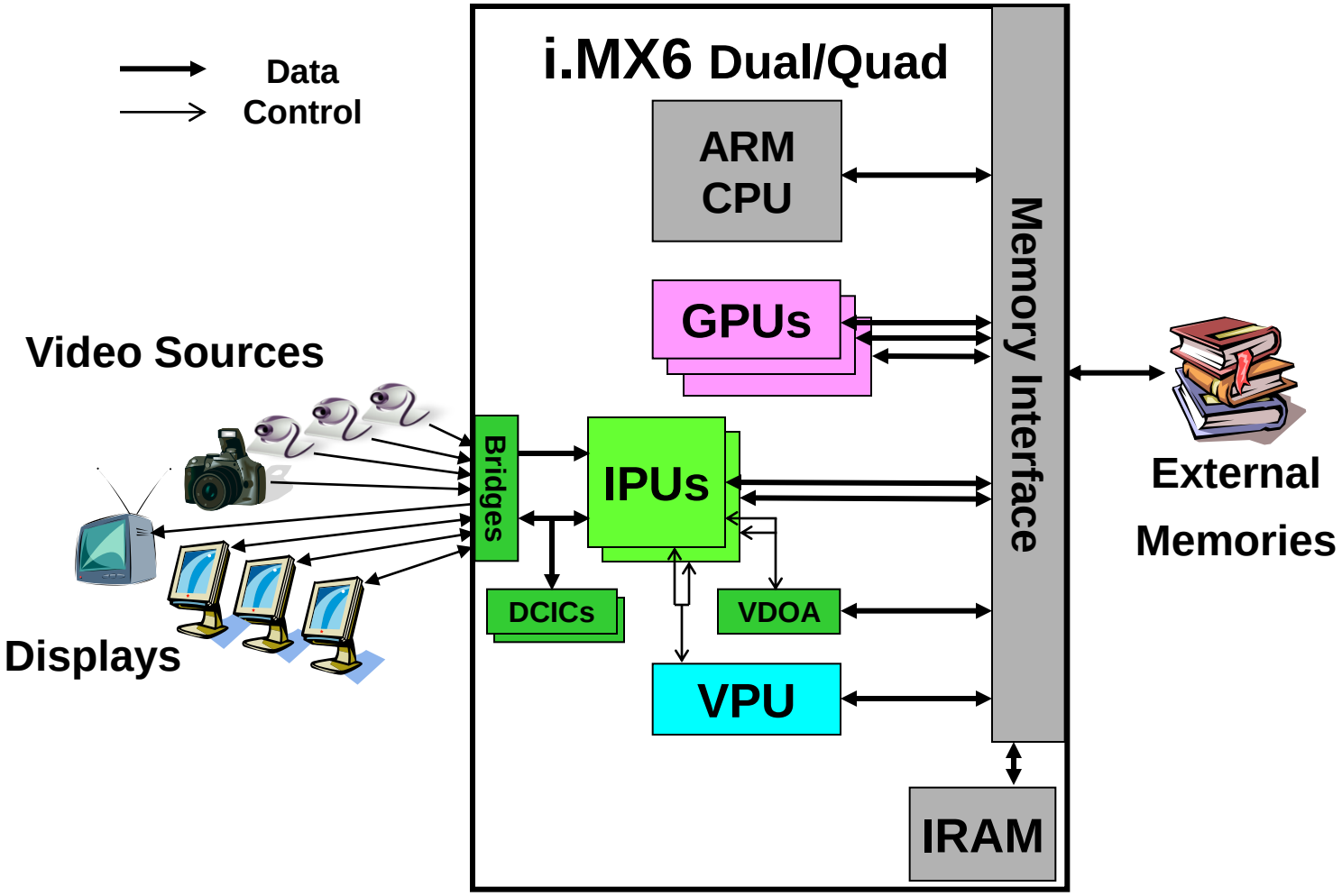
IPUs
(Image Processing Unit)

- Connectivity to relevant devices
- Image processing: conversions, enhancement…
- Synchronization and control

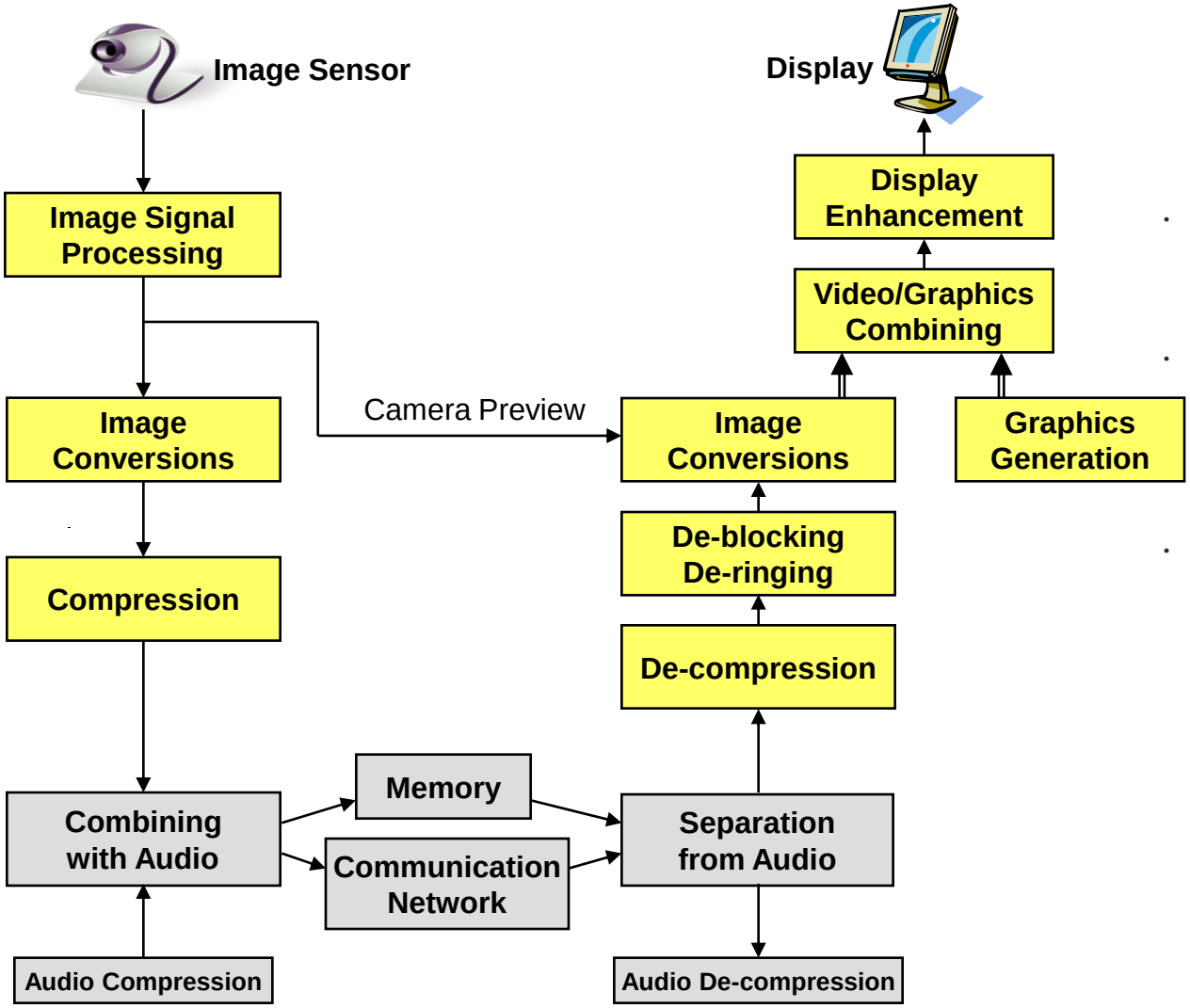
VPU
(Video Processing Unit)
Video encoding and decoding

GPUs
(Graphics Processing Units)
Graphics generation

Video/Graphics Subsystem in i.MX6 D/Q

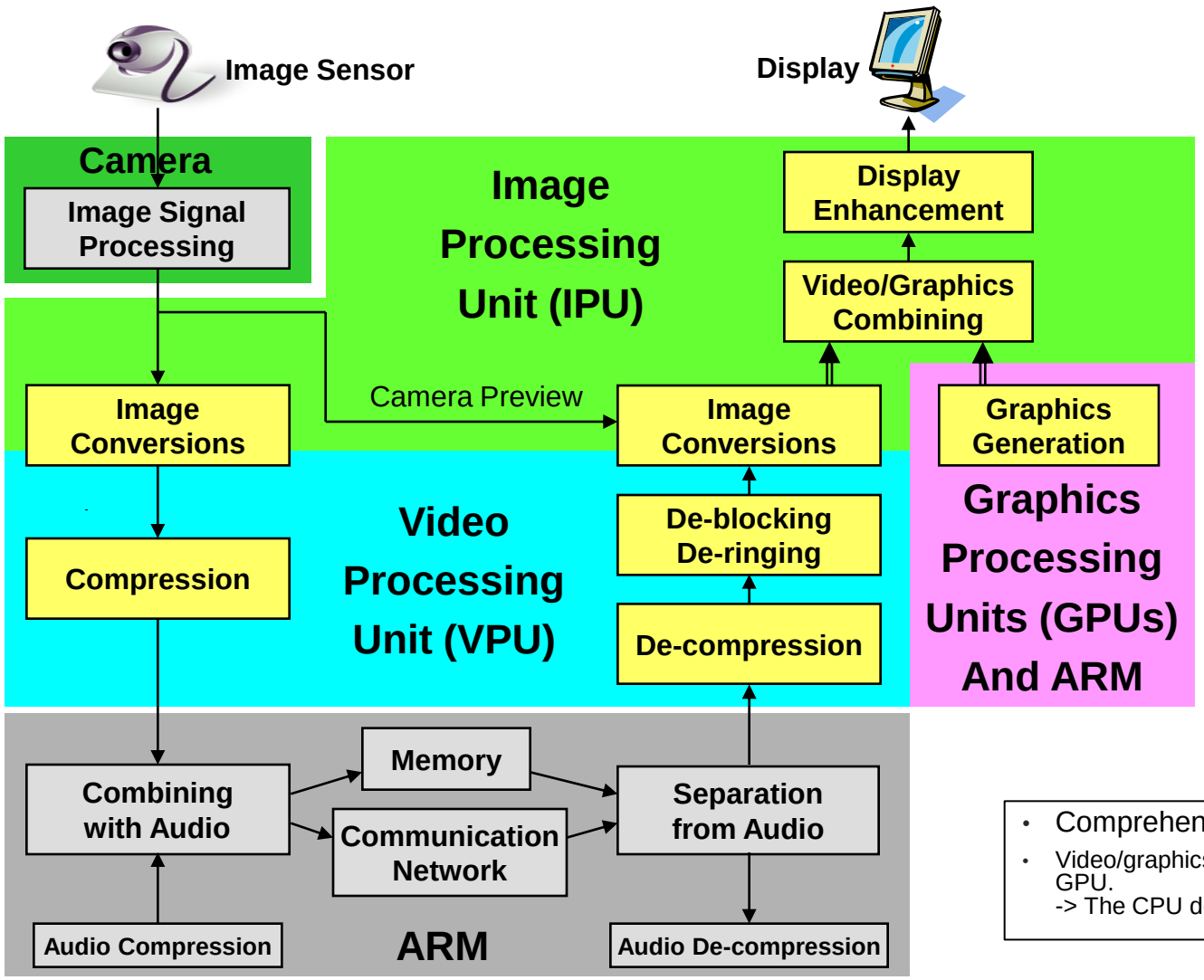


Multimedia Processing Chain



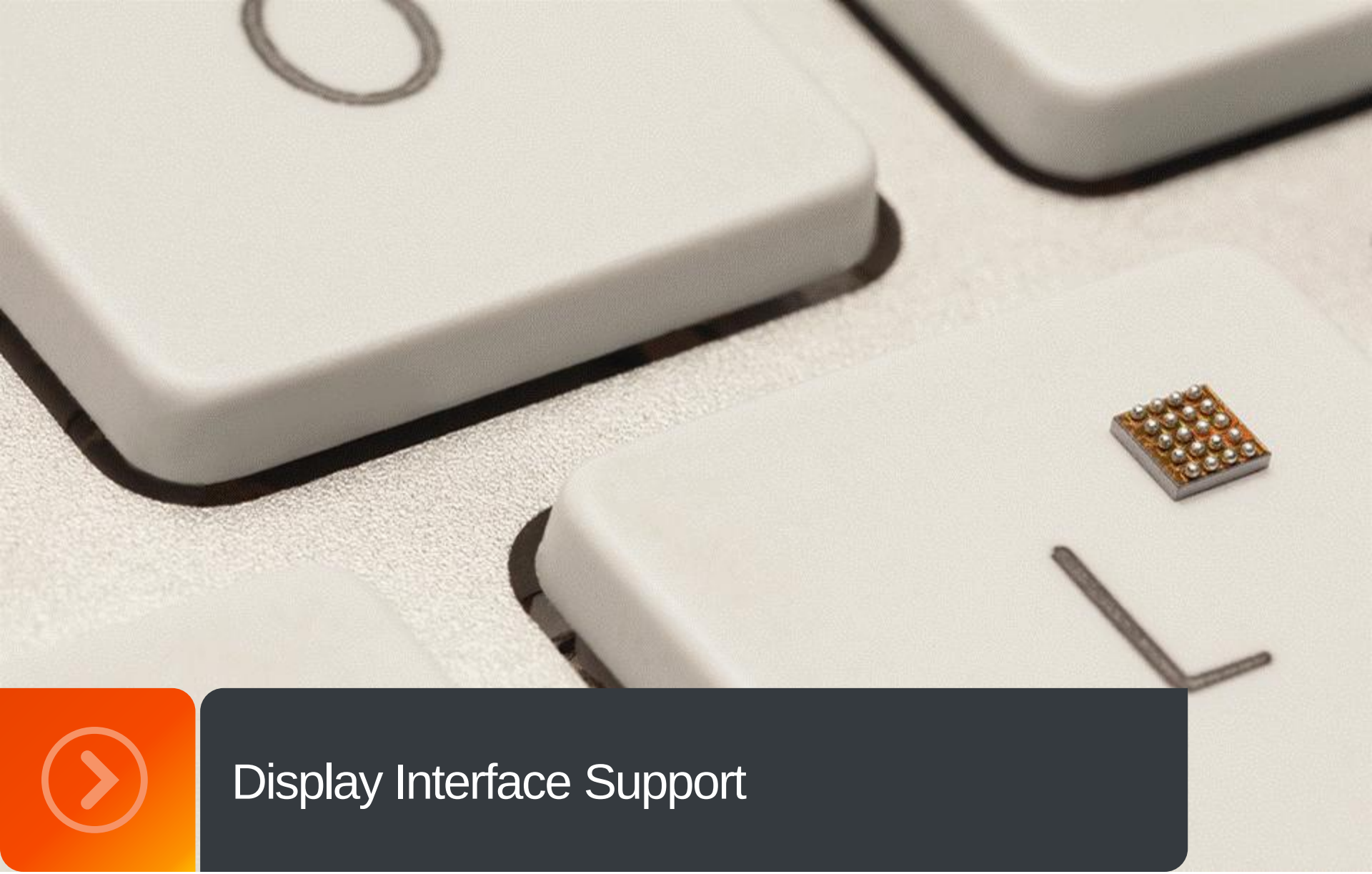
- Image Signal Processing
  - Bayer -> YUV conversion
  - Image quality enhancement
  - Camera corrections
- Image Conversions
  - De-interlacing
  - Resizing (resolution adjustment)
  - Rotation & Inversion
  - Color Space Conversion
  - Pixel Format Conversion (packing…)
- Display Enhancement:
  - Color adjustments and gamut mapping
  - Gamma correction and contrast stretching
  - Compensation for low-light conditions and backlight reduction

Multimedia Processing Chain - Implementation



HW Accelerated

- Comprehensive HW support:
- Video/graphics fully handled by IPU, VPU and GPU.
  -> The CPU does not have to touch pixels



Display Interface Support

i.MX37, i.MX51, i.MX53, i.MX6 D/Q – Display Support

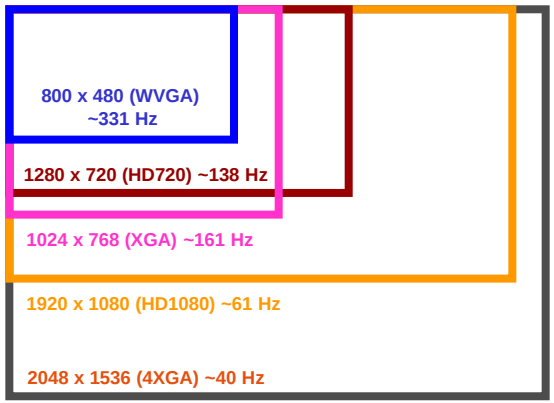
Feature		i.MX51 (IPUv3EX) i.MX37 (IPUv3D)	i.MX53 (IPUv3M)	i.MX6 D/Q (2 x IPUv3H)
Throughput	# of outputs	2		4
	Pixel clock rate	Up to 133 MHz	Up to 200 MHz	Up to 266 MHz per IPU
	Resolution (@ 60 Hz)	WXGA+ (1600x900) 720p (1280x720) + SVGA (800x600)	WUXGA (1920x1200) 1080p (1920x1080) + WVGA (800x480)	2 x 4XGA (2048x1536) 2 x [1080p + WXGA (1280x720)]
Interfaces	Parallel	Two ports 24 bits + 18 bits	Two ports 24 bits + 24 bits	
		Synchronous (for display refresh) and asynchronous (to memory) Very flexible - glue-less connection to RAM-less displays, display controllers, and TV encoders.		
	LVDS	No	Two channels; consumer version (multiple pairs); 2x 85 MHz or 170MHz	
	HDMI	No		One port
	MIPI/DSI	No		One port, 2 lanes x 1 Gbps (non-Automotive)
	Analog	One port; TV-out i.MX37: SDTV i.MX51: also 720p60 or 1080i/p30	Also VGA Rate increased to 1080p60	None (phased out)
Display Content Authentication (CRC)		No		Yes, for 2 displays
Processing	On-the-fly combining (for high resolution displays)	2 planes (up to 3 more planes for lower resolutions)		For 2 displays, 2 planes for each (6 more planes for lower resolutions)
	Off-line combining	Up to 20 MP/sec	Up to 200+ MP/sec	Up to 500+ MP/sec
	Display enhancement	Color adjustment and smart gamut mapping; gamma correction and contrast enhancement Supporting effective proprietary algorithms		
	Backlight power optimization	Yes; Supporting efficient proprietary algorithms		

IPU in i.MX6 D/Q (IPUv3H) – Maximal Resolution & Refresh Rate

- Capabilities
  - Maximal display resolution: 4096x4096 pixels
  - Maximal pixel rate: 266 MP/sec

- Display refresh rate
  - The maximal refresh rate is: 266M / (W * H * B)
    - W*H is the display resolution
    - B is a factor >1 reflecting blanking overhead, e.g. as specified by VESA, CEA-861-D, etc.
  - The table provides the maximal refresh rates for some typical resolutions
  - Usually, the refresh rate is required to be at least 60 Hz, to prevent blinking.
  - The blanking overhead factor assumed for the calculation is 1.3.
    - The actual factor depends on the display and is often closer to 1, allowing higher resolutions @ 60 Hz (e.g. HD1440).
    - For example, for HD1080, the standard specifies B~1.2
  - This is the capability of each of the two IPUs, so the total capability of the processor is doubled.
  - Note: these rates refer only to screen refresh, gated by the capabilities of the display port. A full use case typically includes additional activities and to confirm its support with a given refresh rate, additional aspects – video processing capabilities, capacity of the memory system, etc. – should be also analyzed carefully.

Name	Resolution				Maximal Refresh Rate [Hz]
	Width	x	Height	Total [MP]	
VGA	640	x	480	0.31	666
PAL	720	x	480	0.35	592
WVGA	800	x	480	0.38	533
NTSC	720	x	576	0.41	493
SVGA	800	x	600	0.48	426
WSVGA	1024	x	600	0.61	333
XGA	1024	x	768	0.79	260
HD720	1280	x	720	0.92	222
WXGA	1366	x	768	1.05	195
WXGA+	1440	x	900	1.30	158
SXGA	1280	x	1024	1.31	156
SXGA+	1400	x	1050	1.47	139
WSXGA+	1680	x	1050	1.76	116
UXGA	1600	x	1200	1.92	107
HD1080	1920	x	1080	2.07	99
WUXGA	1920	x	1200	2.30	89
9VGA	1920	x	1440	2.76	74
4XGA	2048	x	1536	3.15	65
HD1440	2560	x	1440	3.69	56
4WXGA	2560	x	1600	4.10	50
4K x 2K	4096	x	2048	8.39	25

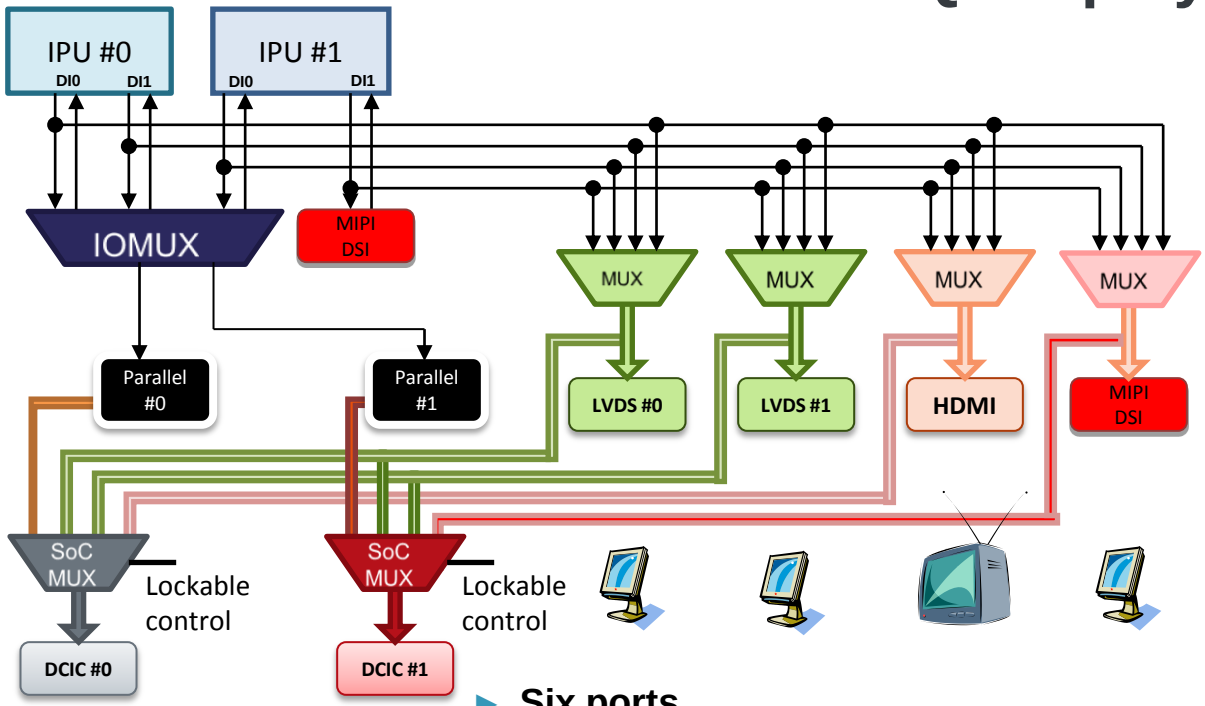


IPU in i.MX6 D/Q (IPUv3H) – Dual-Display Capabilities

First Display \ Second Display	SDTV 480i30/576i25 (27 MHz)	WSVGA (1024x600) (44-49 MHz)	HDTV 720p60/1080i30 (74.25 MHz)	WXGA (1366x768) (72-85 MHz)	WSXGA+ (1680x1050) (119-146 MHz)	HDTV 1080p60 (148.5 MHz)
WXGA (1366x768 ~ 1.0 MP; 72-85 MHz)	**Full**	**Full**	**Full**	**Full**	**Full**	**Full**
SXGA (1280x1024 ~ 1.3 MP; 91-109 MHz)	**Full**	**Full**	**Full**	**Full**	**Partial**	**Partial**
SXGA+ (1400x1050 ~ 1.5 MP; 101-122 MHz)	**Full**	**Full**	**Full**	**Full**	**Partial**	
WSXGA+ (1680x1050 ~ 1.8 MP; 119-146 MHz)	**Full**	**Full**	**Full**	**Full**	**Partial**	
UXGA (1600x1200 ~ 1.9 MP; 130-161 MHz)	**Full**	**Full**	**Full**	**Partial**		
WUXGA (1920x1200 ~ 2.3 MP; 154-193 MHz)	**Full**	**Partial**	**Partial**			
9VGA (1920x1440 ~ 2.8 MP; 185-234 MHz)	**Partial**	**Partial**				
4XGA (2048x1536 ~ 3.2 MP; 209-267 MHz)	**Partial**					

- Notes
  - ***This is the capability of each of the two IPUs, so the total capability of the processor is doubled.***
  - The maximal pixel clock rate supported by the display ports
    - Each display: 220 MHz
    - Total: 240 MHz
  - For a TV, the clock rate is fixed by the corresponding standards
  - For other displays
    - The assumed screen refresh rate is 60 Hz
    - The blanking overhead – impacting the pixel clock rate – may vary between displays.
      The table refers – for concreteness – to the VESA CVT (Coordinated Video Timing) specification
      - "**Full support**": allowing full blanking (which is typically required for CRTs)
      - "**Partial support**": allowing only reduced blanking (which is still typically sufficient for digital displays, e.g. LCDs)
  - The above table describes only the capabilities of the display ports to perform screen refresh. A full use case typically includes additional activities and to confirm its support with a given display configuration, additional aspects – video processing capabilities, capacity of the memory system, etc. – should be also analyzed carefully.

i.MX6 D/Q Display Ports Muxing



- **Six ports**
  - Two parallel - driven directly by the IPU
  - Two LVDS channels - driven by the LVDS bridge
  - One HDMI – driven by the HDMI transmitter
  - One MIPI-DSI – driven by the MIPI-DSI transmitter
- **Four simultaneous outputs**
  - Each IPU has two display ports (DI0 and DI1)
  - Therefore, up to four external ports can be active at any given time.
  - Additional asynchronous data flows can be sent through the parallel ports and the MIPI-DSI port
- **Display Content Integrity Check (DCIC)**
  - For parallel interfaces: probes the I/O loopback (essentially equivalent to probing the external wires)
  - For other integrated interfaces (e.g. LVDS): probes the IPU output (essentially equivalent to the inputs to the serializers)

Max Display Port Resolutions

- MIPI DSI, 2 lanes
  - WXGA (1366 x 768) or 720p (1280 x 720)
- RGB
  - Port 1 – 4XGA (2048 x 1536)
  - Port 2 – 4XGA (2048 x 1536)
- LVDS
  - Single channel – WXGA (1366 x 768) or 720p (1280 x 720)
  - Dual channel – UXGA (1600 x 1200) or 1080p (1920 x 1080)
- HDMI
  - 1080p (1920 x 1080) or 4XGA (2048 x 1536)

Note: Assuming 30% blanking intervals overhead, 24bpp, 60fps

Video Support

i.MX51, i.MX53, i.MX6 D/Q – Video Support

Feature		i.MX51 (IPUv3EX)	i.MX53 (IPUv3M)	i.MX6 D/Q (2 x IPUv3H)
Video Input Interfaces	Parallel	Two ports, 20 bits + 8 bits		
		120 MHz; e.g. 6 MP @ 15 fps	180 MHz; e.g. 9 MP @ 15 fps	200 MHz; e.g. 10 MP @ 15 fps
	MIPI/CSI-2	No		One port, 4 lanes x 1 Gbps
Video Rate	Playback	720p30 (1280x720) @ 30 fps	1080i/p (1920x1080) @ 30 fps	1080i/p + D1 @ 30 fps
	Record	D1 (720x480@30 fps or 720x576@25 fps)	720p30 (1280x720) @ 30 fps	1080p @ 30 fps
	2-way		720p @ 20 fps	720p @ 30 fps
Video Processing	De-interlacing	High-quality motion adaptive algorithm		
	Resizing	Yes – fully flexible		
	Rotation/inversion	Yes		
	Color conversion	Yes – fully flexible		
Memory Interface	Protocol	AXI – Including split transaction		
	Throughput	64-bit, 133 MHz	64-bit, 200 MHz	64-bit, 266 MHz
Efficient memory bus utilization		Selective read for combining		
Control capabilities		Display controller, DMA controller, Internal synchronization Autonomous operations: display refresh/update, view-finder		
Synchronization (to prevent tearing)		Double/triple buffering Frame-by-frame or tight – sub-frame (utilizing internal memory)		

Video Input Ports In i.MX6 D/Q

- Three ports; up to six input channels
  - Two parallel – connected directly to the IPUs; independent clock and format setting
  - One MIPI/CSI-2 – can transfer up to four concurrent channels
  - Each port: up to 150Mpxl/s @200MHz, e.g. 10Mpxl @ 15fps

- Four concurrent channels
  - Each IPU has two input ports (CSI0 and CSI1), each can process an input channel from one of the external ports.
  - The MIPI/CSI-2 bridge sends all its channels to all the IPU input ports and each port can select for processing a different channel, identified by its DI (Data Identifier).
  - Additional channels can be transferred through a CSI transparently – as generic data – directly to the system memory.

- Formats supported:
  - BT.656
  - BT.1120
  - BT 1358 (not validated)
  - YUV422, RGB888, YUV444 = over an 8 bit bus
  - RAW format up to 16bpp which will be translated to 8 bit using companding
  - Generic data up to 20bit

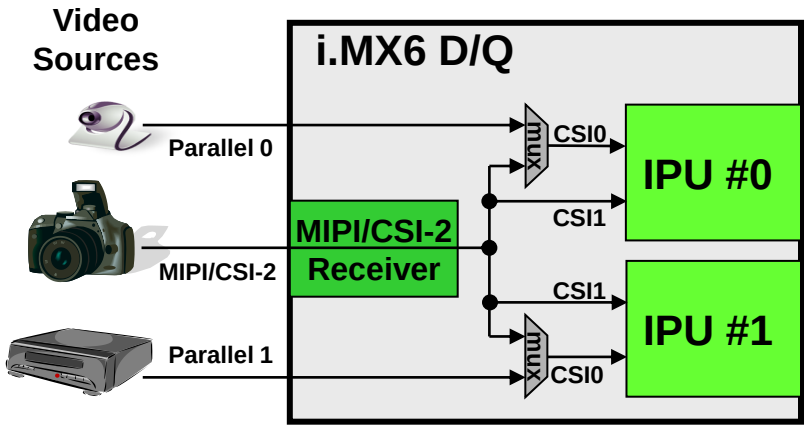
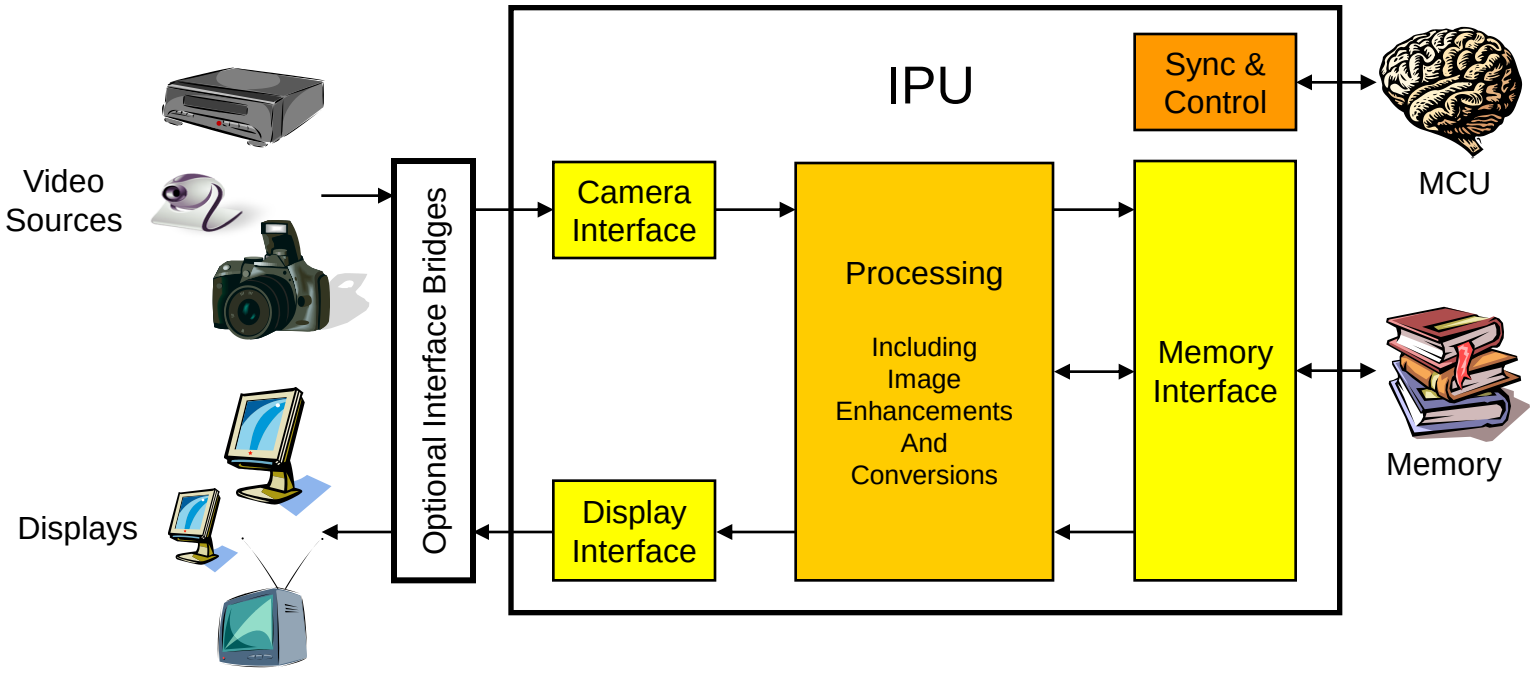


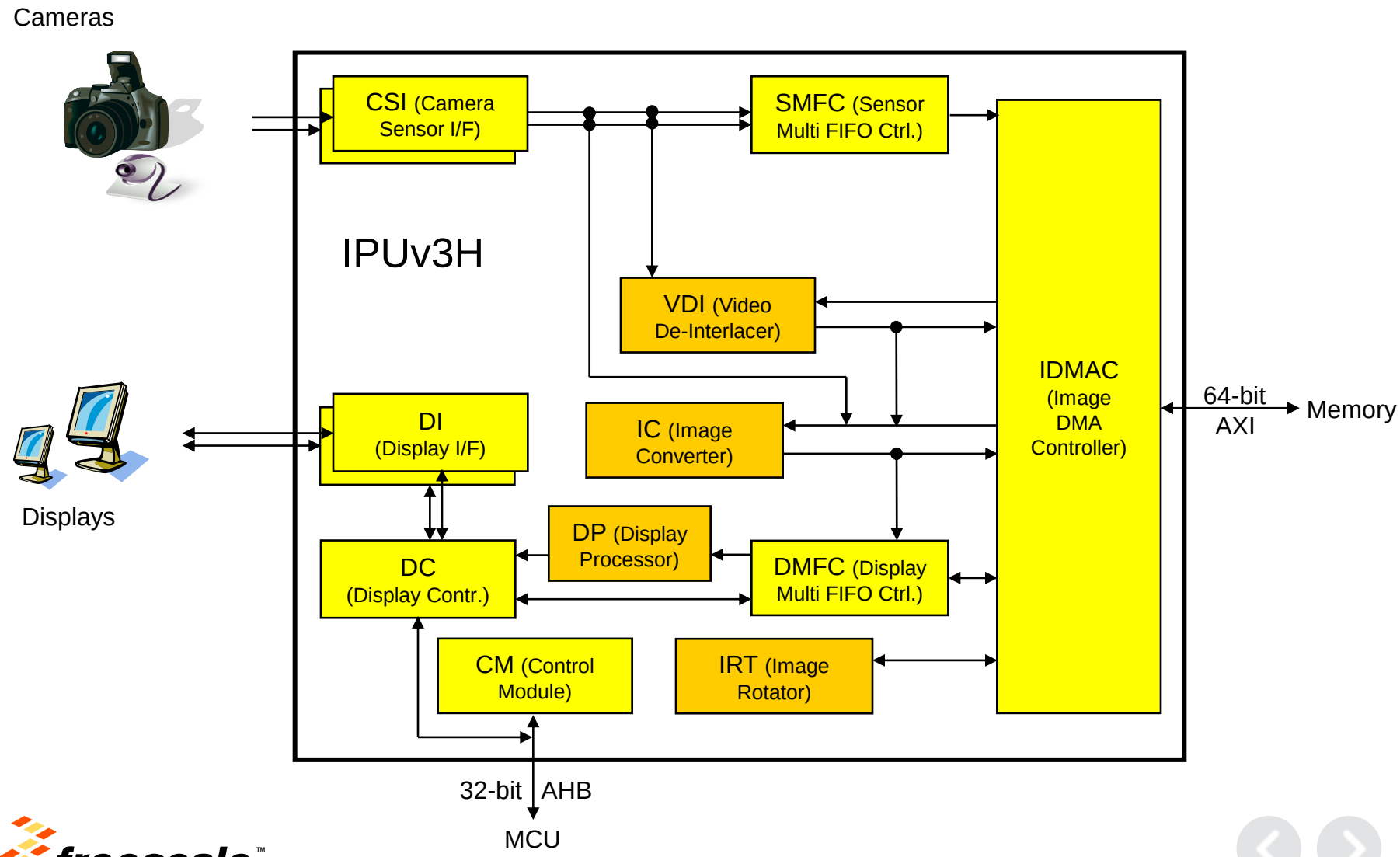
Image Processor Fundamentals

The Image Processing Unit



- Functions: comprehensive support for the flow of data from an image sensor and/or to a display device.
  - Connectivity to relevant devices
  - Related image processing and manipulation
  - Synchronization and control capabilities

IPUv3H – Internal Structure



IPU Fundamentals - DI

- The DI is responsible for the timing waveforms of each signal in the display's interface.

- The DI is composed of
  - 8 sets of waveform generators controlling signals associated with the DI's clock; These signals drive PIN1-PIN8. These pins can be used for signals like VSYNC,HSYNC
  - 12 sets of waveform generators controlling signals associated with the data; These signals drive PIN11-PIN17 + 2 CS signals.
    These pins can be used for signals like DRDY,CS,RS
  - The DI generates the clock to the display
    - The DI clock can be derived from the IPUv3 hsp_clk
    - The DI clock can be derived from an external to the IPU clock (PLL or pin)

The Image DMA Controller – IDMAC

- Role: control the memory ports; transfer data to/from system memory

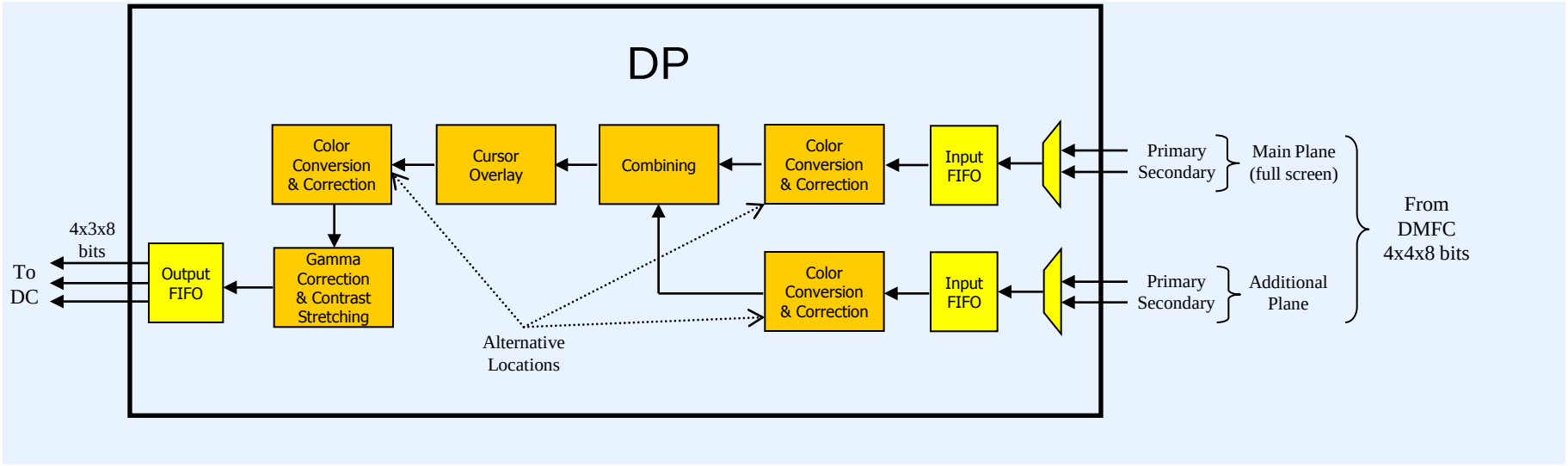
- Memory ports - AXI
  - IMDAC: 1 read, 1 write

- Throughput:
  - External: 64 bits @ 264 MHz
  - Internal: up to 2 pixels/cycle @ 264 MHz (through each port)
  - Shared by all DMA channels: input from sensor, output to display and off-line processing -> efficient utilization of the bandwidth in different use cases
  - Efficient pipelining: 4 AXI ID's; multiple outstanding transactions: read – 8; write – 6

- Data arrangement in memory
  - Row-after-row, with flexible line-stride – as needed for a window in a video/graphics buffer

- Access order
  - Block-by-block – for rotation
  - Row-by-row – used for all other channels
    - Needed for output to display or input from sensor
    - Decreases the memory bus load by increasing its utilization efficiency

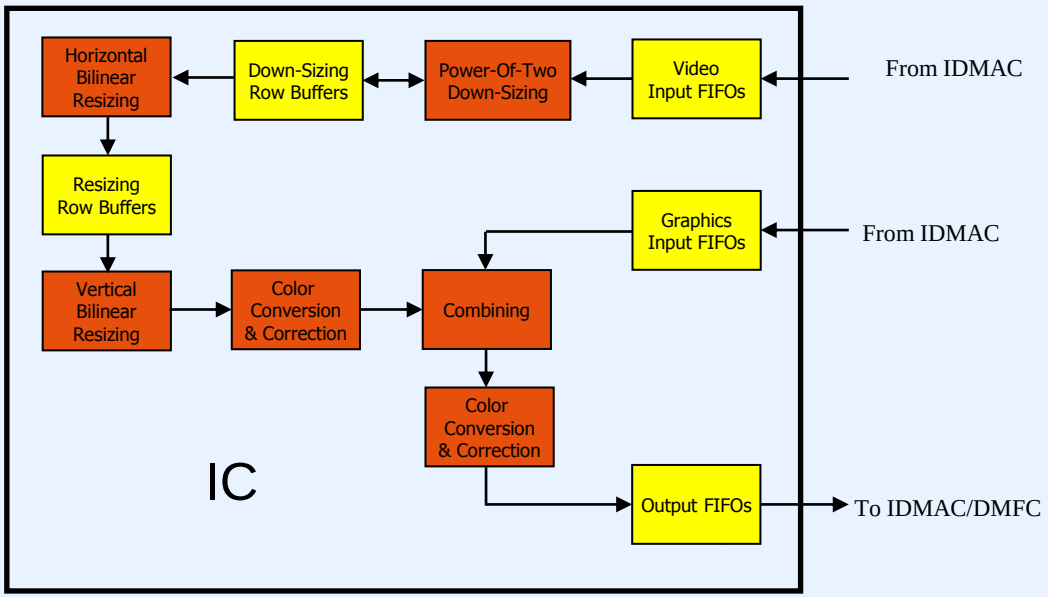
DP (Display Processor)



DP has following features;

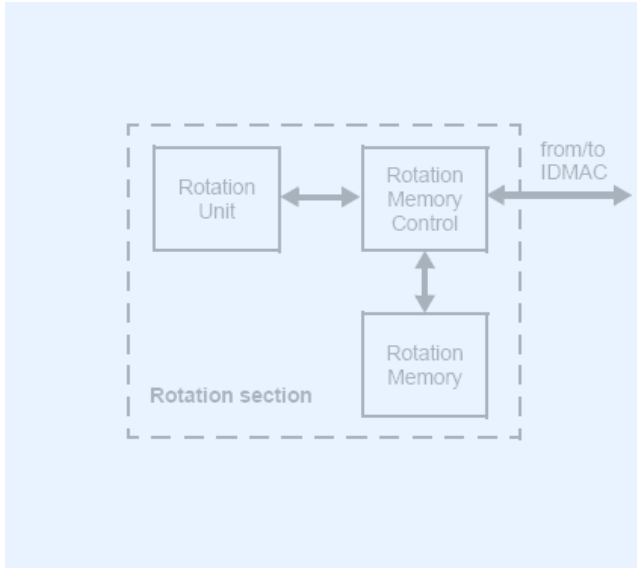
- Support input format YUVA/RGBA
- Combining 2 video/graphics planes
- Color conversion (YUV <-> RGB, YUV<->YUV) & Correction (gamut-mapping)
- Gamma correction and Contrast stretching
- Support output format YUV/RGB
- Dynamic task switching between async and sync flows

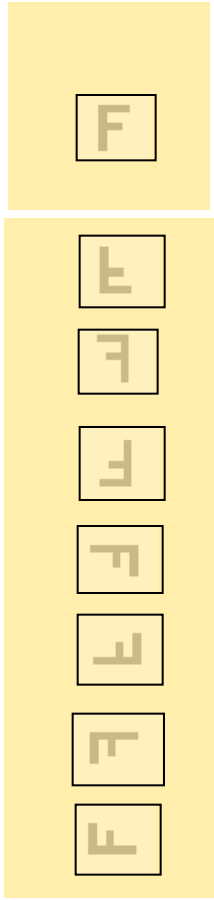
IC (Image Converter)



- Resizing
  - -Fully flexible resizing ratio
    Maximal downsizing ratio: 8:1
    Maximal upsizing ratio: 1:8192
  - - Independent horizontal and vertical resizing ratios
- Color conversion/correction
  - -YUV <-> RGB, YUV <-> YUV conversion
- Combining with a graphic plane

The Image Rotator - IRT





- Role: performs rotation and inversion
  - Rotation: 90, 180, 270 degrees
  - Inversion: horizontal and vertical
- Rate: up to 100M pixels/sec
- Additional features
  - Acts on 8x8 blocks
  - Multi-tasking: up to three tightly time-shared tasks – block-by-block
  - Pixel format: 24-bit

The Video De-Interlacer or combiner - VDIC

- Role 1: performs de-interlacing – converting interlaced video to progressive
  - Method: a high-quality motion adaptive filter
    - For slow motion – retains the full resolution (of both top and bottom fields), by using temporal interpolation
    - For fast motion – prevents motion artifacts, by using vertical interpolation
  - Resolution: up to 720x1024 pixels
  - Output rate: up to 120M pixels/sec

The Video De-Interlacer or combiner - VDIC

- Role 2 : performs combining – overlaying of 2 frames at the same color space

- As an alternative to the de interlacing function the VDIC HW can perform combining

  - Combining of 2 planes
  - Doesn’t have to be of the same size
  - Must be of the same color space (no CSC)
  - Perform 1 pixel per cycle
  - Color keying, alpha blending

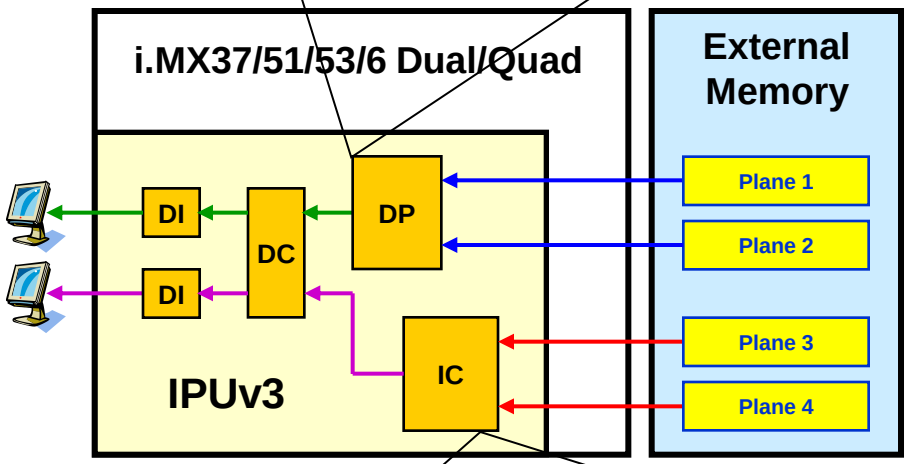
Combining

IPUv3 – Basic Combining Capabilities

Combining in the Display Processor (DP)
Two planes
- One plane may have any size and location
- The other one must be “full-screen” (cover the full output area)

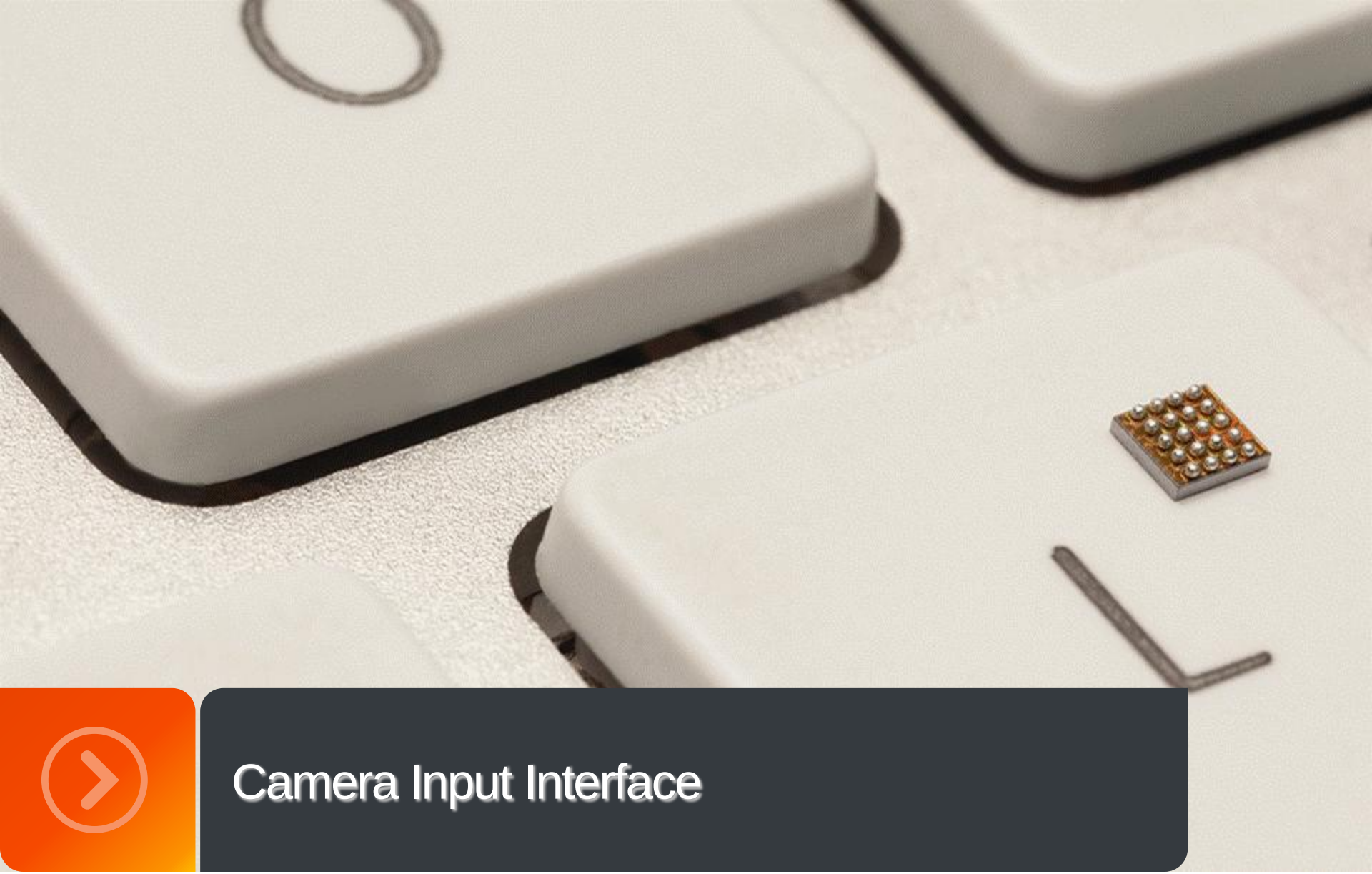
Maximal rate: i.MX37/51 – 133 MP/sec, i.MX53 – 200 MP/sec, i.MX6 Dual/Quad – 264 MP/sec

- Combining methods (in both cases)
  - Color keying and/or alpha blending
  - Alpha: global or per-pixel; interleaved with the pixels (upper plane) or as a separate input



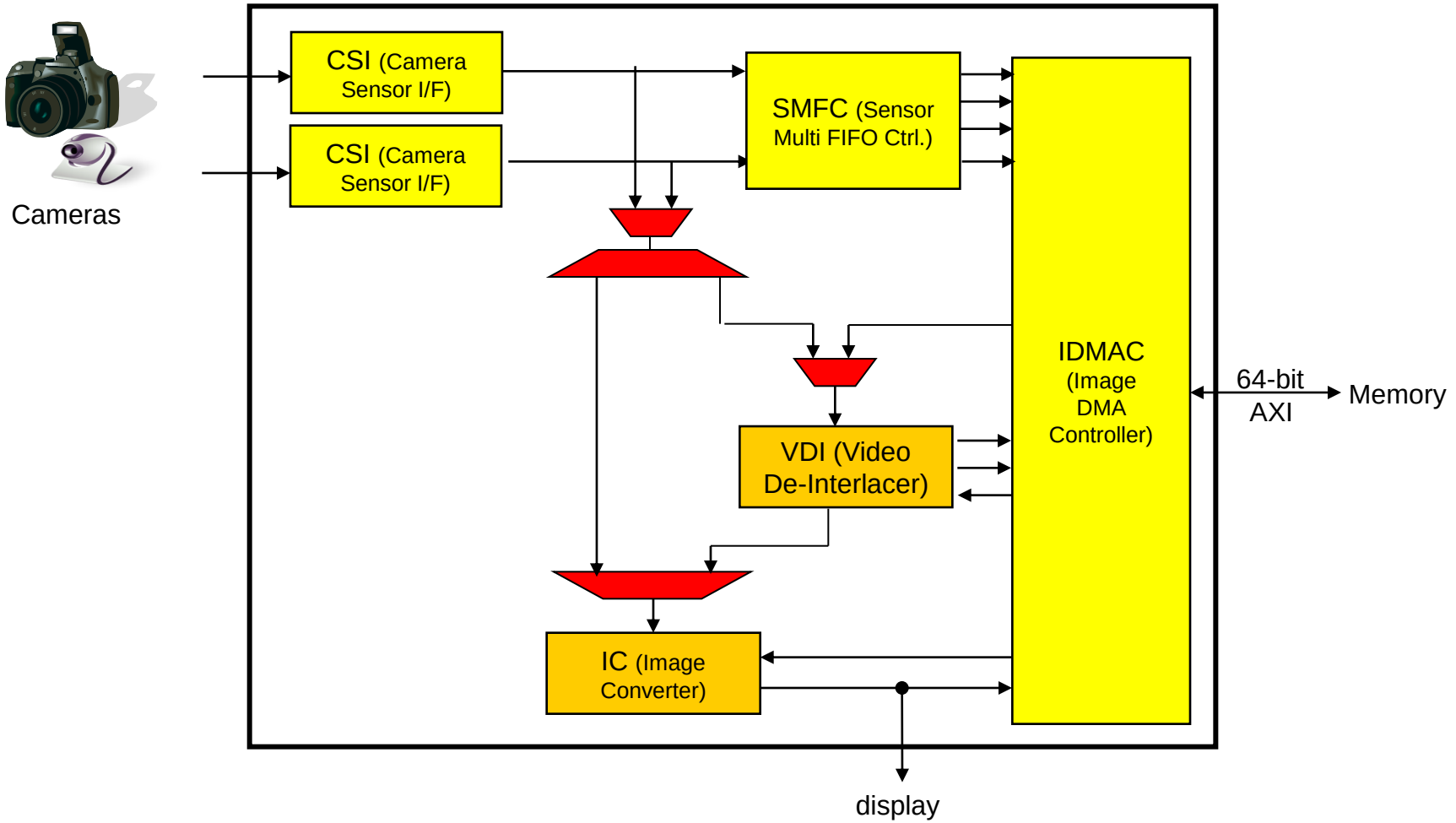
***Note**: This is the capability of each of the two IPUs, so the total capability of the processor is doubled.*

Combining in the Image Converter (IC)
Two planes; both “full-screen” (cover the full output area)
Maximal rate: i.MX37/51 – 20 MP/sec , i.MX53 – 30 MP/sec, i.MX6 Dual/Quad – 40 MP/sec



Camera Input Interface

IPUv3H – The camera port



The Camera Sensor Interface - CSI

- Role: controls the camera port

  Provides direct connectivity to relevant image sensors and connectivity bridges: CSI-2, HDMI receiver, TV decoder…

- Data bus – up to 20 bits
  - Single value – up to 16 bits
  - Two values – up to 10 bits each; e.g. HDTV YUV 4:2:2 input

- Variety of data formats
  - Main (with on-the-fly processing): YUV 4:2:2/4:4:4, RGB 16/24 bpp
  - Other: as generic data, including compressed streams
  - All mandatory CSI-2 formats

- Frame resolution:

  Essentially unlimited (up to 8192 x 4096 pixels)

- Input rate:
  - 240M values/sec peak (@ 264 MHz internal clock)

- Additional features:
  - Frame rate reduction – by skipping (reduction ratio: m:n, m<=n<=12)
  - Window-of-interest selection – by cropping

16 bit camera support

- **16 bit YUV422**
  - CSI receives 2 components per cycle.
  - CSI [16 bit generic data.] => SMFC => MEM [16bit generic data] => IPU[YUV422]

- **16 bit RGB as generic data**
  - CSI receives 3 components per cycle.
  - Use a 16 bit sample of it (such as RGB565)
  - CSI [16 bit generic data.] => SMFC => MEM [16bit generic data] => IPU [16 bit RGB] => IPU [map to 24bpp RGB]

- **16 bit RGB565**
  - On the fly processing of 16 bit data.
  - CSI is programmed to receive 16 bit generic data.
  - The interface is restricted to be in "non-gated mode" and the CSI#_DATA_SOURCE bit has to be set
  - If the external device is 24bit - the user can connect a 16 bit sample of it (RGB565 format).
  - The IPU has to be configured in the same way as the case of CSI#_SENS_DATA_FORMAT=RGB565

Use case Examples & tips

Boot cmdline for multiple display

imx6q: LVDS0 + HDMI

---

setenv display_mode 'video=mxcfb0:dev=ldb,LDB-XGA,if=RGB565,bpp=16 ldb=sep0 video=mxcfb1:dev=hdmi,1920x1080M@60,if=RGB24' (lvds0+hdmi)

imx6q: LVDS1 + HDMI

---

setenv display_mode 'video=mxcfb0:dev=ldb,LDB-XGA,if=RGB565,bpp=16 ldb=sep1 video=mxcfb1:dev=hdmi,1920x1080M@60,if=RGB24' (lvds1+hdmi)

imx6q: LCD + HDMI

---

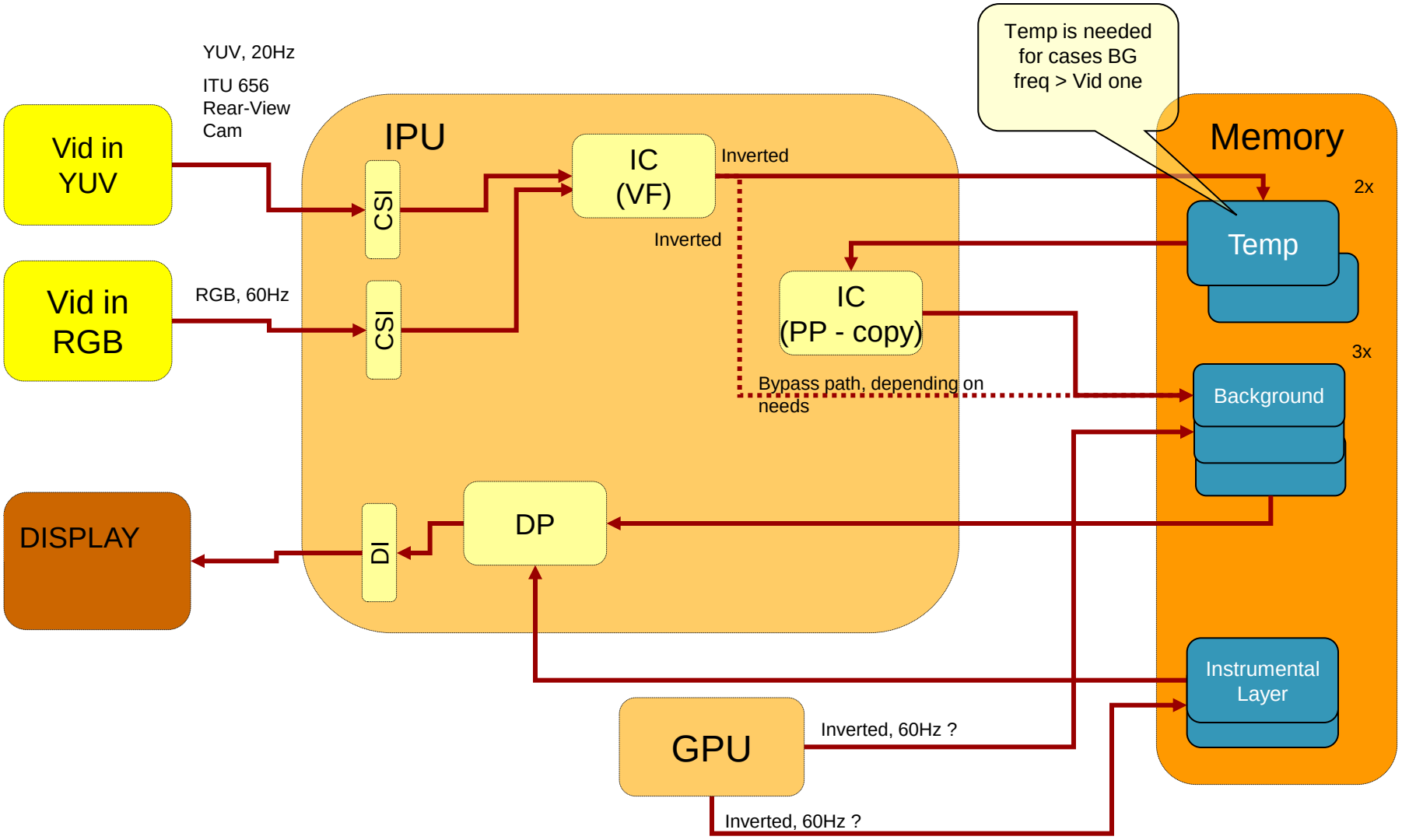
setenv lcd_mode 'video=mxcfb0:dev=lcd,CLAA-WVGA,if=RGB565,int_clk video=mxcfb1:dev=hdmi,1920x1080M@60,if=RGB24'

imx6q: LVDS0 + LVDS1 + HDMI

---

setenv display_mode 'video=mxcfb0:dev=ldb,LDB-XGA,if=RGB565,bpp=16 ldb=sep0 video=mxcfb1:dev=hdmi,1920x1080M@60,if=RGB24, video=mxcfb2:dev=ldb,LDB-XGA,if=RGB565,bpp=16'

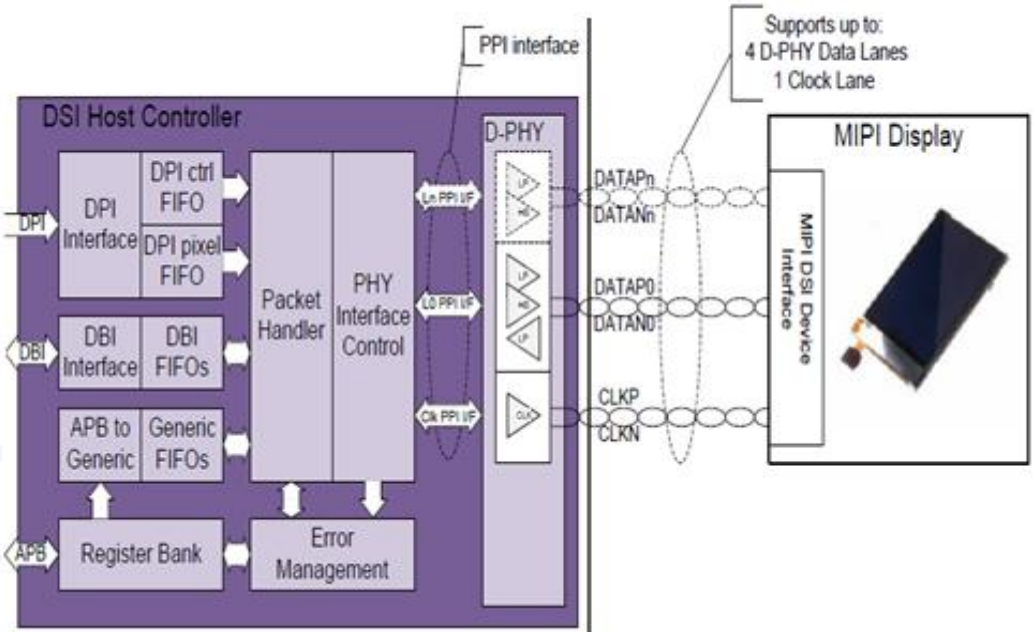
Dual video-in use case example



Back up

MIPI DSI

The DSI MIPI Interface is a digital core accompanied with a multi-lane D-PHY that implements all protocol functions defined in the MIPI DSI Specification, providing an interface between the System and MIPI DSI compliant Display



Features of the MIPI DSI complex:

Supported standard version:

- MIPI DSI Compliant
- DSI Version 1.01
- DPI Version 2.0
- DBI Version 2.0
- DSC Version 1.02
- PPI for D-PHY
- MIPI D-PHY Version 1.0

Configuration: one clock lane, two data lanes
Speed: Up to 1Gb/s per lane (fast speed). Low speed/low power signaling supported

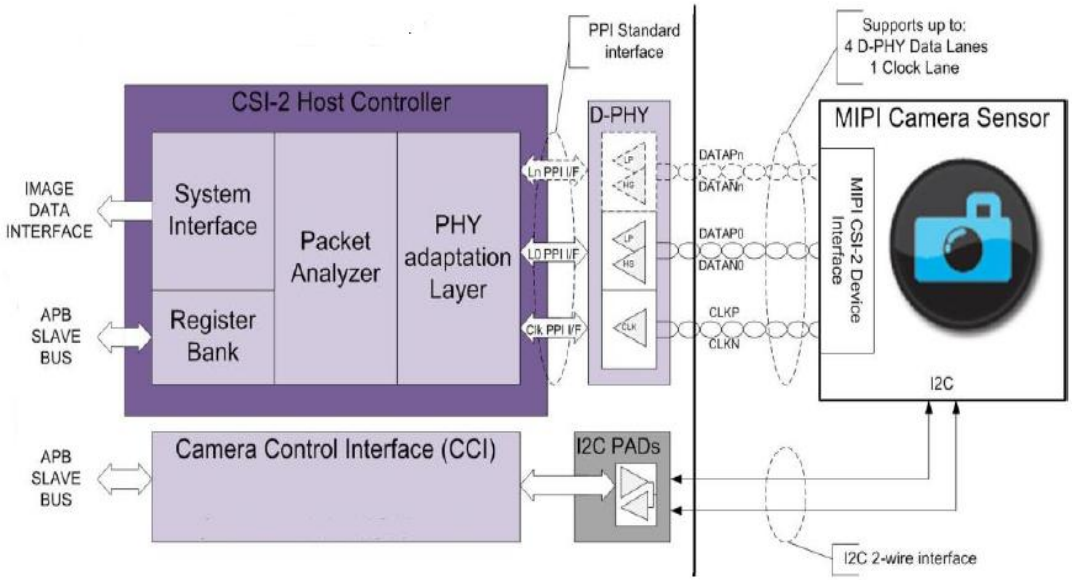
DSI can support both command and video modes and up to four virtual channels to accommodate multiple displays.

- Command and video mode support (type 1, 2, 3, and 4 display architecture)
- Mode switching: low power and ultra low power
- Burst mode: dual video channel
- Non-burst mode: single video channel
- Bus turnaround
- Fault error recovery scheme

Both DPI and DBI coexist in the system but only one of them could be active in a certain time moment

MIPI CSI-2

The CSI-2 MIPI Interface is a digital core accompanied with multi-lane D-PHY that implements all protocol functions defined in the MIPI CSI-2 Specification, providing an interface between the System and MIPI CSI-2 compliant Camera Sensor



The features of the MIPI CSI-2 complex:

Supported standard version: MIPI CSI-2 Version 1.0
Configuration: one clock lane, four data lanes
Speed: Up to 1Gb/s per lane
Throughput: 250MB/sec

•Timing accurate signaling of Frame and Line synchronization packets;
•Support for several frame formats such as:
- •General Frame or Digital Interlaced Video with or without accurate sync timing
- •Data type (Packet or Frame level) and Virtual Channel interleaving

•32-bit Image Data Interface delivering data formatted as recommended in CSI-2 Specification;
- •Directly supports all primary data formats conversion to IPU input. Some secondary formats are treated as “generic” data
- •RGB, YUV and RAW color space definitions;
- •From 24-bit down to 6-bit per pixel;
- •Generic or user-defined byte-based data types

LDB Features

- **LDB Structure**:
  - 2 Channels , same/independent data
  - Each channel contains 4 data pairs + 1 clock pair
- **Resolutions/Rates**:
  - Single Channel (up to WXGA): Up to 85 MHz, 3 or 4 data pairs
  - Dual Channel (up to UXGA): Up to 170 MHz, 6 or 8 data pairs
  - For example: can support 1080p60 or UXGA @60fps
- **Pixel Depths**:
  - 18 bpp – 3 LVDS data pairs
  - 24 bpp – 4 LVDS data pairs
- **Control signals:**
  - Supports HSYNC, VSYNC, DE

HDMI General Features

- **Description:** High-Definition Multimedia Interface (HDMI) Transmitter including both HDMI TX Controller and PHY
- **Standard Compliance:** HDMI 1.4a, DVI 1.0, HDCP 1.4 (with keys stored in embedded eFuses)
  - Supporting majority of primary 3D Video formats
- **TMDS Core Frequency:** From 25 MHz to 340 MHz
- **Consumer Electronic Control:** Supported
- **Monitor Detection:** Hot plug/unplug detection and link status monitor support
- **Testing Capabilities:** Integrated test module
- **Maximal Power Consumption:** 70mW
- **Temperature Range:** -40C to +125C (Tj)

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