飞思卡尔 i.MX6 平台 DRAM 接口高阶应用指导-DDR3 篇

本文意于介绍基于i.MX6平台如何使用官方工具调试DDR3.

以下内容会在本文中涉及：原理图及 PCB 版图设计规则，DDR3 初始化代码生成工具，DDR3 自校准和压力测试工具。

Contents

1 设计 DRAM 的注意事项

飞思卡尔的硬件应用团队总结了一个名为 “HW Design Checking List for i.Mx6” 的文档来分享 i.MX6 硬件设计经验。 请通过以下链接来获得该文档: https://community.freescale.com/docs/DOC-93819

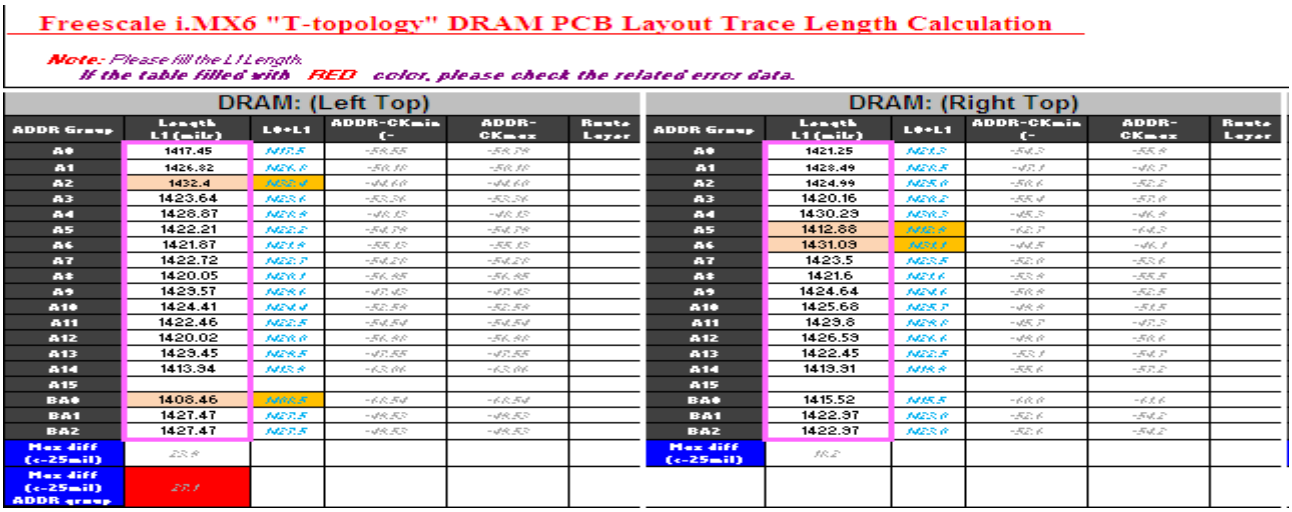
1.1 原理图和布线设计规则

下表中的内容摘自“HW Design Checking List for i.Mx6”。使用i.MX6平台进行设计时务必遵循里面的规则。设计者应当逐条予以确认。如有任何疑问或不确定之处，请寻求飞思卡尔的技术支持本们的帮助。

原理图检查清单	
1	i.Mx6 和 DDR 芯片的 ZQ 管脚需要分别外加一个 1%精度的 240 欧姆电阻到地
2	提供一路低噪声并且等于 50%NVCC_DRAM 电压值的电源给 DRAM_VREF 管脚（更多细节请参考原文档）
3	DRAM_RESET 管脚需要外接一个 10 K 欧姆的电阻到地（更多细节请参考原文档）
4	差分时钟端接设计规则（更多细节请参考原文档）
5	如果 DDR3 颗粒的数量少于等于四颗-PCB 顶面两颗底面两颗，建议使用 T 拓扑结构。如果 PCB 单面需要部多于两颗 DDR3 颗粒，建议使用 Fly-by 拓扑结构。

布线检查清单	
1	DQS 和 CLK 信号线需要差分 100 欧姆阻抗控制，数据,地址和控制信号线需要阻抗控制为单端 50 欧姆
2	差分信号线长度差小于 5 mils
3	所有信号线要保证有至少一个连续的地作层为参考平面（更多细节请参考原文档）
4	DQS 和 CLK 走线与其他信号线之间至少保持 3 倍线宽间距（边到边）
5	信号线走线长度规则（更多细节请参考原文档）

如下图所示，文档 “HW Design Checking List for i.Mx6”中的“MX6 DRAM Bus Length Check”页提供给设计者一个自行检查的工具。输入当前设计的线长参数到粉色框内的格中后，如果违反规则同一列内最底下的格子会变成红色。



Freescale i.MX6 "T-topology" DRAM PCB Layout Trace Length Calculation

Note: Please fill the L1 Length
If the table filled with RED color, please check the related error data.

DRAM: (Left Top)

ADDR Group	Length L1 (mils)	L0-L1	ADDR-CKmin (-	ADDR-CKmax	Route Layer
A0	1417.45				
A1	1426.82				
A2	1432.4				
A3	1423.64				
A4	1428.87				
A5	1422.21				
A6	1421.87				
A7	1422.72				
A8	1420.05				
A9	1423.57				
A10	1424.41				
A11	1422.46				
A12	1420.02				
A13	1423.45				
A14	1413.94				
A15					
BA0	1408.46				
BA1	1427.47				
BA2	1427.47				
Max diff (<-25mil)					
Max diff (<-25mil) ADDR group					

DRAM: (Right Top)

ADDR Group	Length L1 (mils)	L0-L1	ADDR-CKmin (-	ADDR-CKmax	Route Layer
A0	1421.25				
A1	1428.49				
A2	1424.99				
A3	1420.16				
A4	1430.29				
A5	1412.88				
A6	1431.09				
A7	1423.5				
A8	1421.6				
A9	1424.64				
A10	1425.68				
A11	1429.8				
A12	1426.59				
A13	1422.45				
A14	1419.91				
A15					
BA0	1415.52				
BA1	1422.37				
BA2	1422.37				
Max diff (<-25mil)					

2 DDR3 初始化脚本生成工具

In this chapter we will show how to generate DDR3 initialization script for a specific design.

Since DDR3 initialization script has many registers; JESD79-3 and board design knowledge are required for configuration. It is very time consuming to generate it for dedicated design.

Freescale AE team created “i.Mx6DQSDL DDR3 Script Aid” for making this work easier. The latest Excel aid can be found through following link: https://community.freescale.com/docs/DOC-94917

2.1 How to use the Aid?

Both schematic and DDR3 chip Datasheet which used in the schematic should be ready for reference.

All “Orange” and “Blue” cells should be input properly.

Device Information	
Manufacturer:	Micron
Memory part number:	MT41K128M16JT-125
Memory type:	DDR3-1600
DRAM density (Gb)	2
DRAM Bus Width	16
Number of Banks	8
Number of ROW Addresses	14
Number of COLUMN Addresses	10
Page Size (K)	2
Self-Refresh Temperature (SRT)	Normal
tRCD=tRP=CL (ns)	13.75
tRC Min (ns)	48.75
tRAS Min (ns)	35
System Information	
i.Mx Part	i.Mx6Q
Bus Width	64
Density per chip select (Gb)	8
Number of Chip Selects used	1
Total DRAM Density (Gb)	8
DRAM Clock Freq (MHz)	528
DRAM Clock Cycle Time (ns)	1.894
Address Mirror (for CS1)	Disable
SI Configuration	
DRAM DSE Setting - DQ/DQM (ohm)	48
DRAM DSE Setting - ADDR/CMD/CTL (ohm)	48
DRAM DSE Setting - CK (ohm)	48
DRAM DSE Setting - DQS (ohm)	48
System ODT Setting (ohm)	60

2.1.1 Device information

All the inputs below can be obtained from chip Datasheet

Manufacturer: Type chip vendor name in the row

We use Micron as an example in this section.

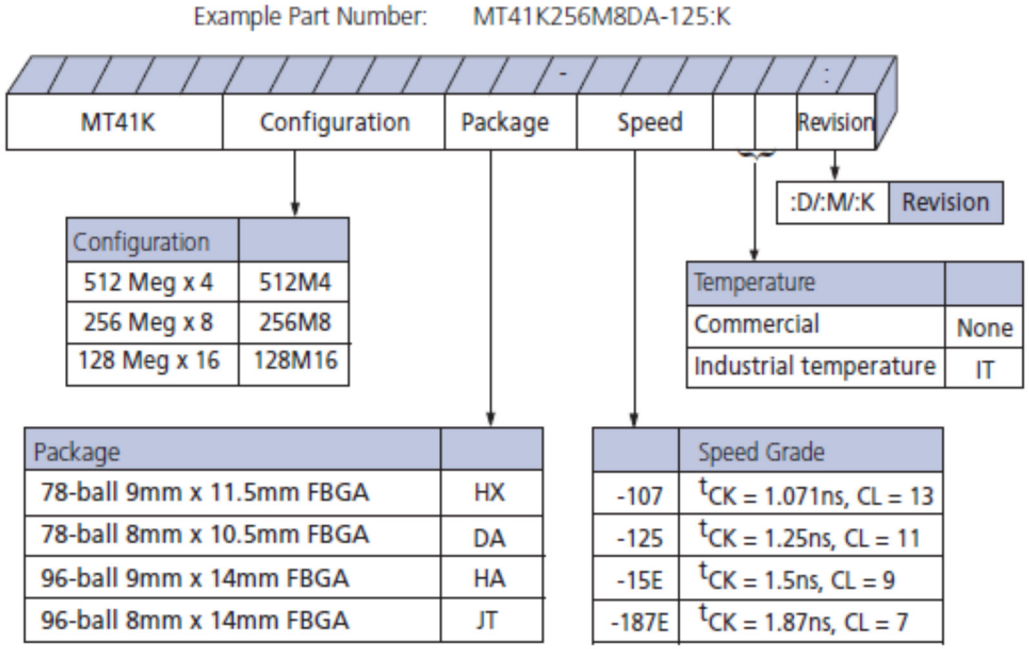
Memory part number: Type full part/order number of chip in this row

We use MT41K128M16JT-125 as an example in this section. Chip Datasheet can be found through below link.

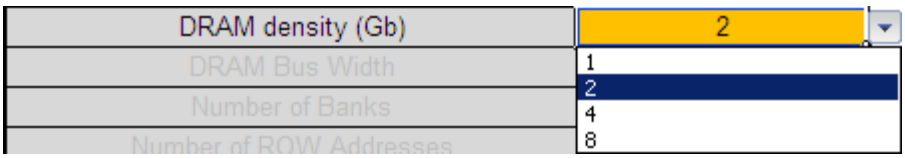
http://www.micron.com/~/media/Documents/Products/Data%20Sheet/DRAM/DDR3/2Gb_1_35V_DDR3L.pdf

Memory Type: Select chip type in the list of this row

MT41K128M16JT-125 Datasheet shows below info.



DRAM density (Gb): Select density of each chip in the list of this row



DRAM Bus Width: Select bus width of each chip in the list of this row

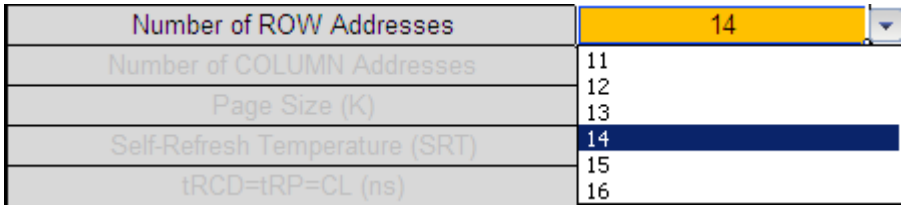
Number of Banks: Type band numbers of chip in this row

MT41K128M16JT-125 Datasheet shows below info.

DDR3L SDRAM

MT41K512M4 – 64 Meg x 4 x 8 banks
MT41K256M8 – 32 Meg x 8 x 8 banks
MT41K128M16 – 16 Meg x 16 x 8 banks

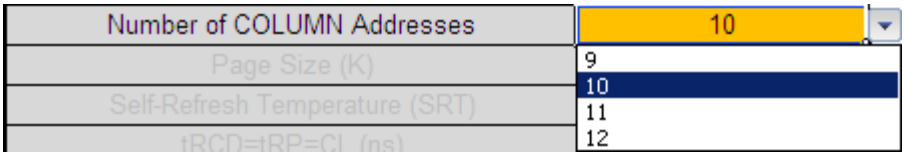
Number of ROW Addresses: Select Row Address numbers of chip in the list of this row



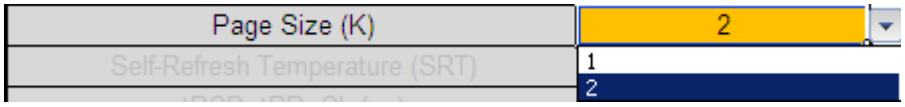
MT41K128M16JT-125 Datasheet shows below info.

Parameter	128 Meg x 16
Configuration	16 Meg x 16 x 8 banks
Refresh count	8K
Row address	16K A[13:0]
Bank address	8 BA[2:0]
Column address	1K A[9:0]

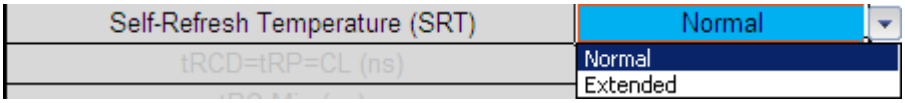
Number of COLUMN Addresses: Select Column Address numbers of chip in the list of this row



Page Size (K): Select page size of chip in the list of this row



Self-Refresh Temperature (SRT): Select SRT type of chip in the list of this row



tRCD=tRP=CL (ns): Type tRCD/tRP/CL parameter of chip in this row

MT41K128M16JT-125 Datasheet shows below info.

Speed Grade	Data Rate (MT/s)	Target tRCD-tRP-CL	tRCD (ns)	tRP (ns)	CL (ns)
-125[1, 2]	1600	11-11-11	13.75	13.75	13.75

tRC Min (ns): Type tRC parameter of chip in this row

tRAS Min (ns): Type tRAS parameter of chip in this row

MT41K128M16JT-125 Datasheet shows below info.

DDR3L-1600 Speed Bin		-125[1]		
CL-tRCD-tRP		11-11-11		
Parameter	Symbol	Min	Max	Unit
ACTIVATE-to-ACTIVATE or REFRESH command period	tRC	48.75	–	ns
ACTIVATE-to-PRECHARGE command period	tRAS	35	9 x tREFI	ns

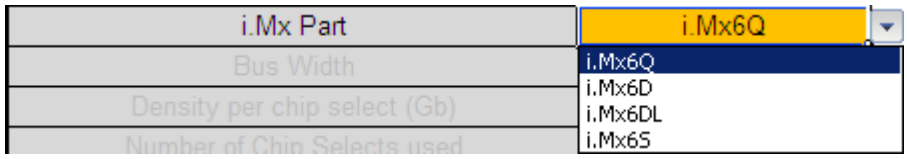
2.1.2 System information

All below input can be gotten from schematic.

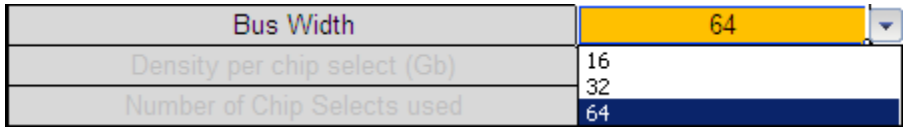
We use SABRE Board for Smart Devices as an example in this section. The design file can be found through below link.

https://www.freescale.com/webapp/sps/download/license.jsp?colCode=iMX6_SABRE_SDB_DESIGNFILES&appType=file2&location=null&DOWNLOAD_ID=null

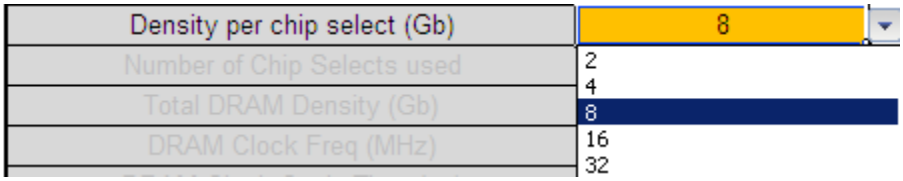
i.Mx Part: Select i.Mx type in the list of this row



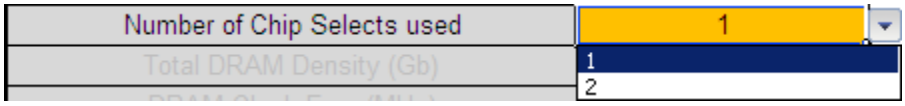
Bus Width: Select used i.Mx DRAM bus width in the list of this row



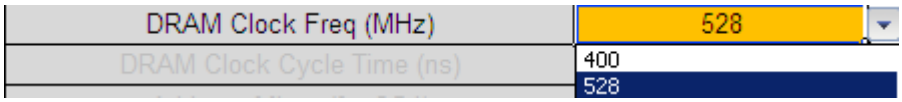
Density per chip selects (Gb): Select total density of each CS in the list of this row



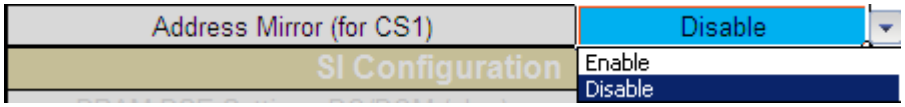
Number of Chip Selects used: Select numbers of CS are used in the list of this row



DRAM Clock Freq (MHz): Select target DRAM working frequency in the list of this row



Address Mirror (for CS1): Select address mirror function in the list of this row



2.1.3 SI (Signal Integrity) Consideration

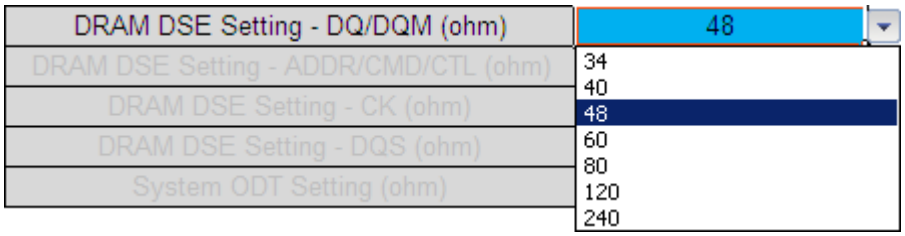
The inputs below can be based on SI design experience or simulation result.

General speaking drive strength (DSE) and ODT should match the characteristic impedance of transmission line. Actual test report of trace impedance should be delivered by PCB vendor.

For example, for 45 ohm single end trace DSE can select 40ohm or 48ohm; for 100ohm differential trace DSE of one pin of pair can select 48ohm etc.

About ODT selection, it isn't sensitive like DSE and can work well with a larger margin. For above example both single and differential case, 60 ohm should be fine.

DRAM DSE Setting - DQ/DQM (ohm): Select DQ/DQM pads driver strength value in the list of this row

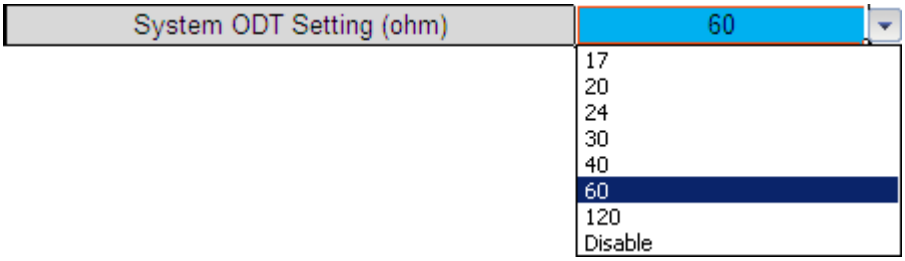


DRAM DSE Setting - ADDR/CMD/CTL (ohm): Select ADDR/CMD/CTL pads driver strength value in the list of this row

DRAM DSE Setting - CK (ohm): Select CK pads driver strength value in the list of this row

DRAM DSE Setting - DQS (ohm): Select DQS pads driver strength value in the list of this row

System ODT Setting (ohm): Select ODT value for both DDR3 and i.Mx in the list of this row



2.2 Delay lines - which should according real board

Except parameters in section 2.1, designer also need fill four delay lines (Write Leveling delay, Read DQS Gating Delay, Read Delay, Write Delay) in script.

2.2.1 What are delay lines working for?

MMDC PHY Write Leveling Delay Control Register:
The write leveling calibration can generate a delay between the clock and the write DQS for each byte
MMDC PHY Read DQS Gating Control Register:
The read DQS gating calibration is used to adjust the read DQS gating with the middle of the read DQS preamble.
MMDC PHY Read delay-lines Configuration Register:
This register controls read delay-lines functionality; it determines DQS delay relative to the associated DQ read access. The delay-line compensates for process variations and produces a constant delay regardless of the process, temperature and voltage.

MMDC PHY Write delay-lines Configuration Register:

This register controls write delay-lines functionality, it determines DQ/DM delay relative to the associated DQS in write access. The delay-line compensates for process variations, and produces a constant delay regardless of the process, temperature and voltage.

Detailed configuration descriptions about above registers can be found in i.Mx6 Reference Manual.

There are red marked registers in page “RealView.inc” of “i.Mx6DQSDL DDR3 Script Aid”

```
// For target board, may need to run write leveling calibration to fine tune these settings.
setmem /32      0x021b080c  =   0x00000000
setmem /32      0x021b0810 =    0x00000000
setmem /32      0x021b480c  =   0x00000000
setmem /32      0x021b4810 =    0x00000000
////Read DQS Gating calibration
setmem /32      0x021b083c =    0x00000000  // MPDGCTRL0 PHY0
setmem /32      0x021b0840 =    0x00000000  // MPDGCTRL1 PHY0
setmem /32      0x021b483c =    0x00000000  // MPDGCTRL0 PHY1
setmem /32      0x021b4840 =    0x00000000  // MPDGCTRL1 PHY1
//Read calibration
setmem /32      0x021b0848 =    0x40404040  // MPRDDLCTL PHY0
setmem /32      0x021b4848 =    0x40404040  // MPRDDLCTL PHY1
//Write calibration
setmem /32      0x021b0850 =    0x40404040  // MPWRDLCTL PHY0
setmem /32      0x021b4850 =    0x40404040  // MPWRDLCTL PHY1
```

2.2.2 How to achieve them?

Freescale AE team had build a tool named “i.MX6 DDR Stress Test Tool” which can be run on and achieve all delay lines parameters of target board. Please download latest version through following link: https://community.freescale.com/docs/DOC-96412

Next chapter will introduce how to use the tool.

3 DDR Stress Test Tool

The DDR stress test tool serves two purposes.

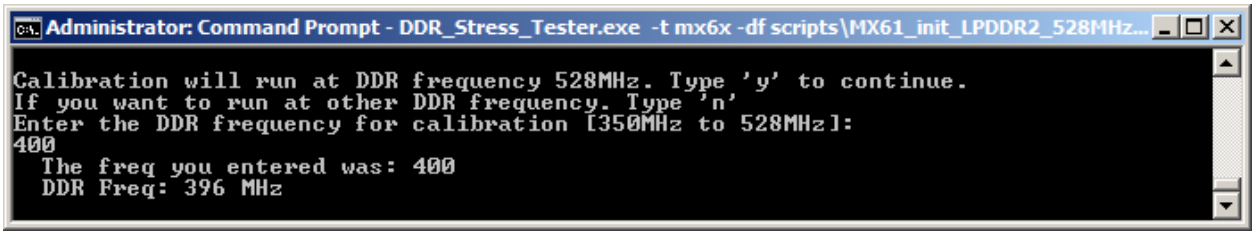
First, it can perform calibrations for DDR3 to match the MMDC PHY delay settings with PCB for optimal DRAM performance. The process is fully automatic, and therefore the customers can get there DDR3 working in much shorter time.

In addition, the tool can run a memory stress test to verify the DDR3 functionality as well as the reliability. The stress test can help verifying the hardware connections, MMDC registers parameters, and DDR3 mode registers setting. The most important purpose of the test is that it allows the customers to verify that the DDR3 operations are stable on their board.

3.1 Calibration

There are four calibration processes required for DDR3 on i.MX6 processors. These calibration processes fine tune the delay registers on the MMDC PHY to compensate the skew between signals due the pads output delay variance and traces length difference to obtain the best DRAM performance.

The calibration will start on the DDR Stress Test Tool after entering the DDR3 configuration. First, the test will prompt for the DRAM frequency on calibration. The default value for i.MX6Q and i.MX6D is 528MHz. For i.MX6DL, i.MX6S, and i.MX6SL, the default value is 400MHz. These are the DRAM frequencies used by BSP. Press ‘y’ to proceed with the calibration process. There is an option to select a specific frequency by press ‘n’. It should be only be used for debugging only.



After ending the DRAM frequency, then the tool will start the calibrations.

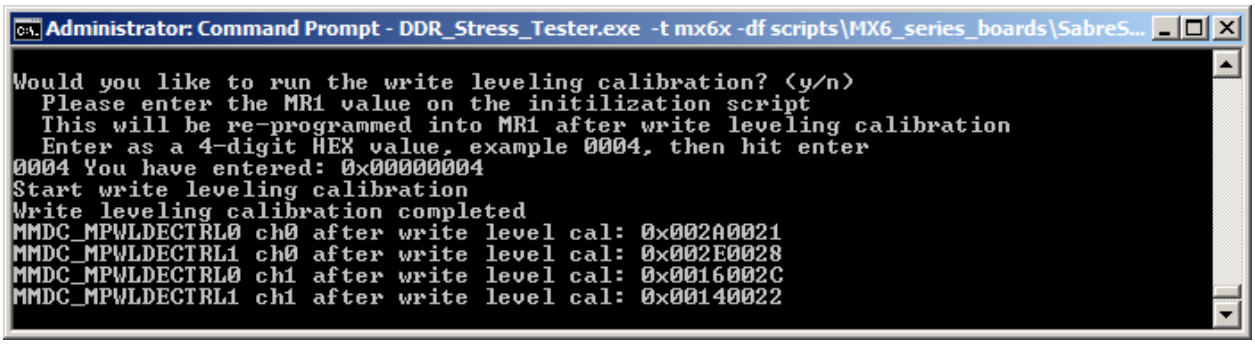
3.1.1 Write Leveling Calibration

This is the first calibration for fine tuning the delay between DRAM clock and write DQS output from i.MX6 processor. Press ‘y’ to continue with the calibration. If the board has been calibrated and calibration result had been integrated into script, press ‘n’ to skip the calibration.

After pressing ‘y’ to start the calibration, you need to enter the value of Mode Register MR1 for the DDR3. The MR1 value can be located on the following line on the initialization script. The value is the two most significant bytes after the ‘=’ sign, i.e. 0x0004 on this example.

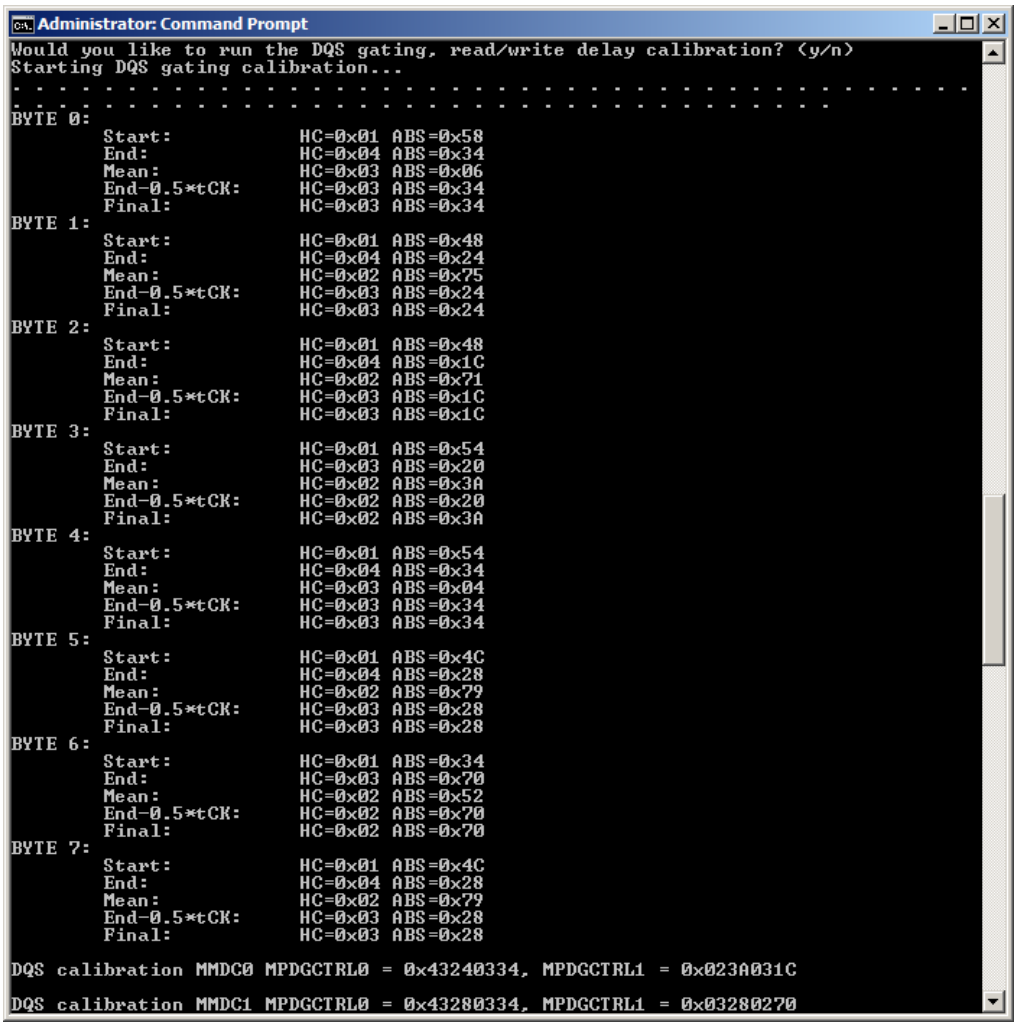
```
setmem /32      0x021b001c =    0x00048031      // MMDC0_MDSCR, MR1 write, CS0
```

This value must be the same as the one used on the DDR initialization script. Otherwise, the results in the following parts of the test are invalid as this value is used for recovering the MR1 value on the DDR3 when leaving the write leveling mode.



3.1.2 Read DQS Gating Calibration

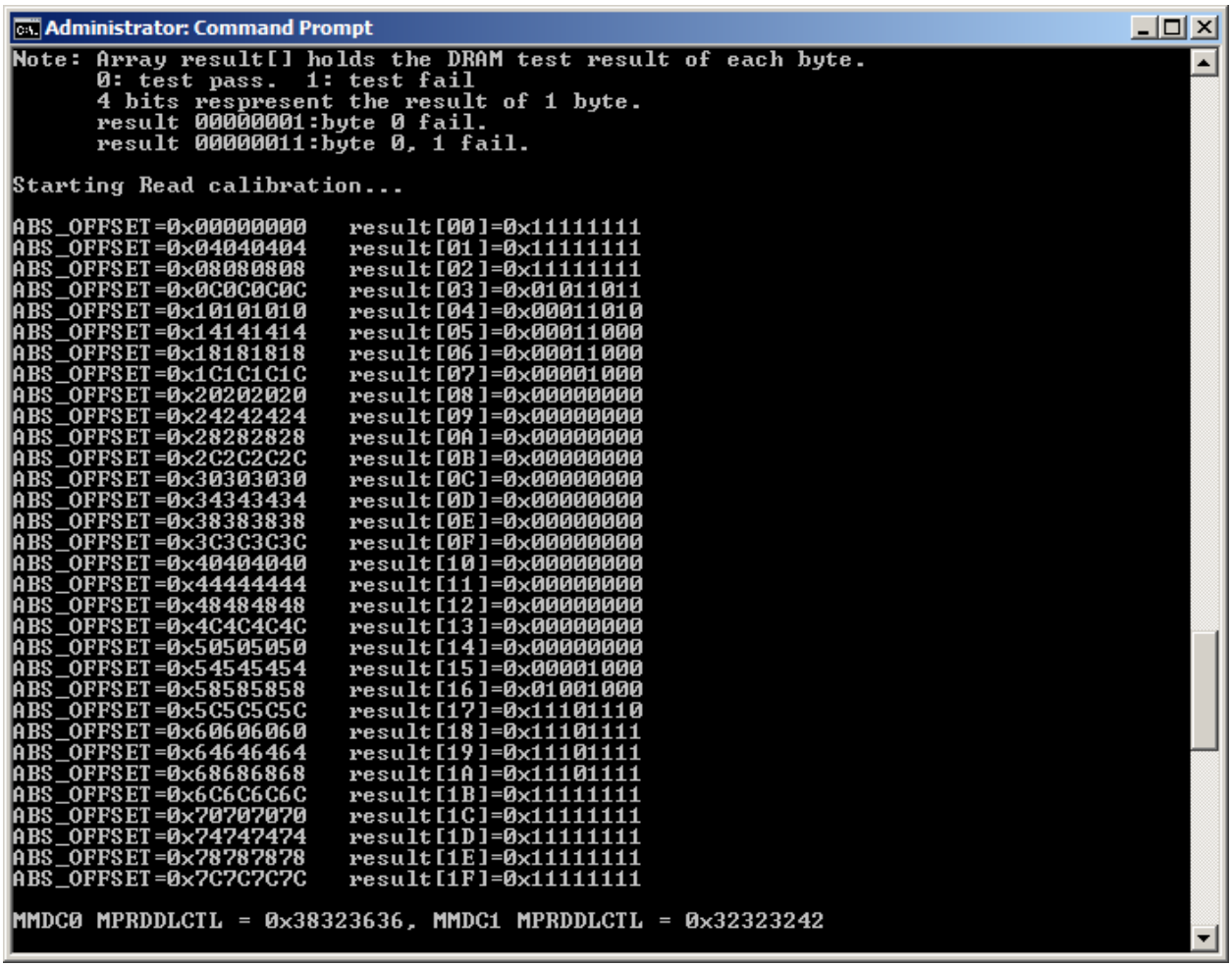
The second calibration process is DQS gating calibration. It is used to fine tune the read DQS gating so that it could capture the read DQS signal reliably. The calibration adjusts the DQS gating delay in 4/256 clock cycle steps to locate the valid DQS delay window. Press ‘y’ to start the calibration. It will continue with the read and write delay calibration also. If the board has been calibrated and calibration result had been integrated into script, press ‘n’ to skip the calibration.



The start and end of the valid DQS gating delay window for each byte will be shown after the calibration. The wider the valid window, i.e. the difference between start and end of the window is larger, implies more timing margin on the DQS gating delay. The mean of start and end of the window and end of the window minus half clock will also be shown as a reference. The suggested DQS delay will be shown as last and it is calculated by the formula max [mean (start, end), end-0.5tCK].

3.1.3 Read and Write Delay Calibrations

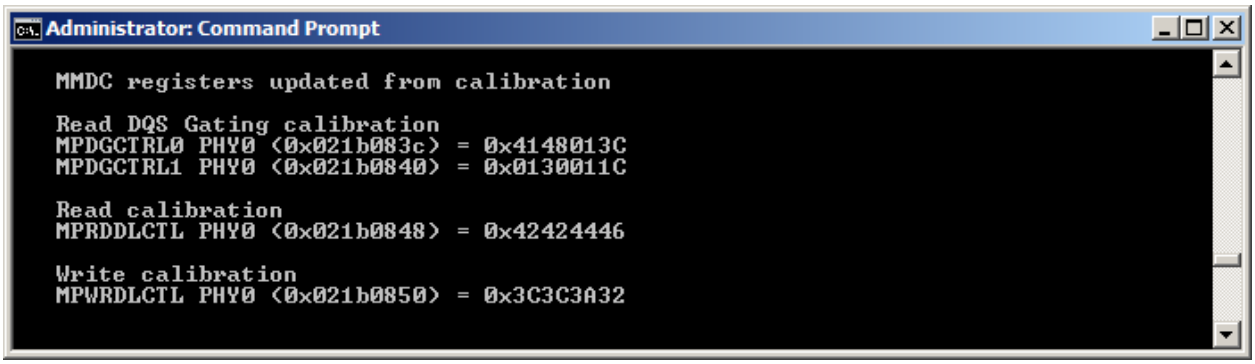
The last calibration processes are read and write delay calibrations. This is for fine tuning the delay between DQS and data on reading and writing DDR3 respectively. It helps to obtain the best timing between DQS and DQ signals. It will start after the DQS delay calibration is finish.



The format for read and write delay calibrations result are the same. The results are shown in increasing delay between DQS and DQ in 4/256 clock cycle steps. The results for each byte are shown with first byte on the first bit on the right, second byte on the second bit from the right and so on. For each byte, a “0” indicates a pass which mean the byte can perform a read/write reliably with that delay setting. A “1” indicates that the byte cannot pass the read/write test. The valid delay windows can be visualized by counting the number of 0 vertically. The wider the window implies the more margins for that byte.

3.1.4 Calibration Results

After finishing all the calibration process, the calibration results are summarized and as shown below.



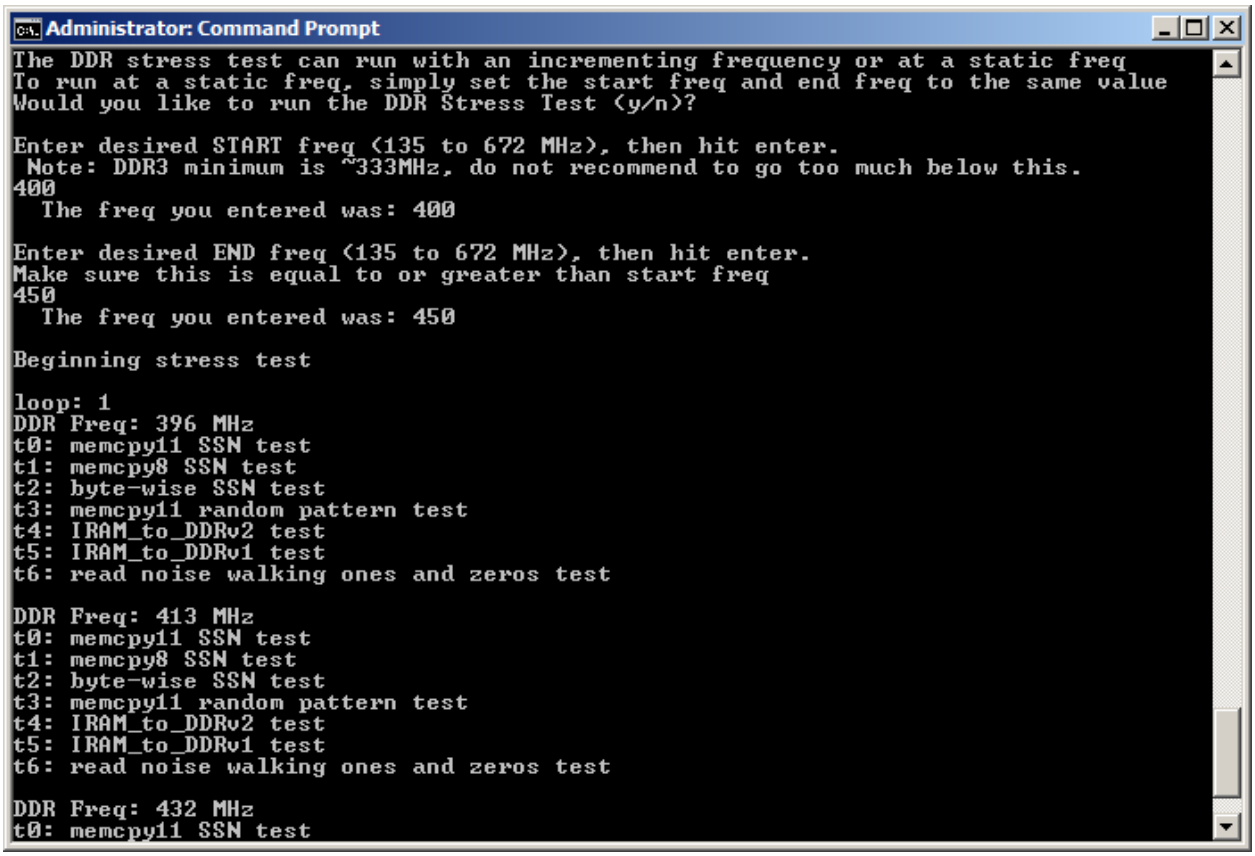
The tool will proceed to run the DRAM stress test with the delay registers updated with these calibration results.

However, it is very important that these results should be recorded down and the DRAM initialization script should be updated accordingly. When porting the MMDC parameters to the firmware, the delay registers must be programmed according to the updated script. Otherwise, the DDR3 may not be able to run stably on the firmware.

3.2 Stress Test

After finishing all the calibration processes, it tool will start the DRAM stress test. The stress test will perform read/write tests on the DDR3 with different patterns to ensure the DDR3 connections are correct, the MMDC parameters have been properly configured, and the PCB layout (and thus the signal integrity) is good for the DDR3 running reliably at the target operation frequency.

The stress test can run repeatedly on a single frequency or with incrementing frequencies. When the test starts, it will prompt for the start and end frequencies. For incrementing frequencies test, enter the start and end frequencies accordingly. The frequency has to be in the range of 135 MHz to 672 MHz Since tCK(AVG).MIN=3ns limits when DLL enable and script from “Aid” only support DLL enable, so please set DDR3 working point higher than 333MHz. If it is desired to test a single frequency, simply enter the same number for both start and end frequencies.



The test will stop if any error occurs, the failure pattern will also be shown.

It is suggested to run the stress test at the target DDR3 operating frequency (528 MHz for i.MX6Q and i.MX6D; 400 MHz for i.MX6DL, i.MX6S, and i.MX6SL) for an extended period of time to verify the DDR3 performance on the target board. Running the stress test higher than the target operating frequency is not meaningful. The DDR3 waveform is not simple square wave in 400 – 500 MHz range that the DDR3 is operating. The signal waveform may change a lot as the frequency increases. Therefore, passing the stress test at a frequency higher than the target operating frequency does not necessarily mean that there is more timing margin.

BTW, we strongly suggest customer applying real high loading SW application case under corner environment condition to verify stability both SW and HW.

3.3 Using the DDR Stress Test Tool for Troubleshooting DDR3 Issue

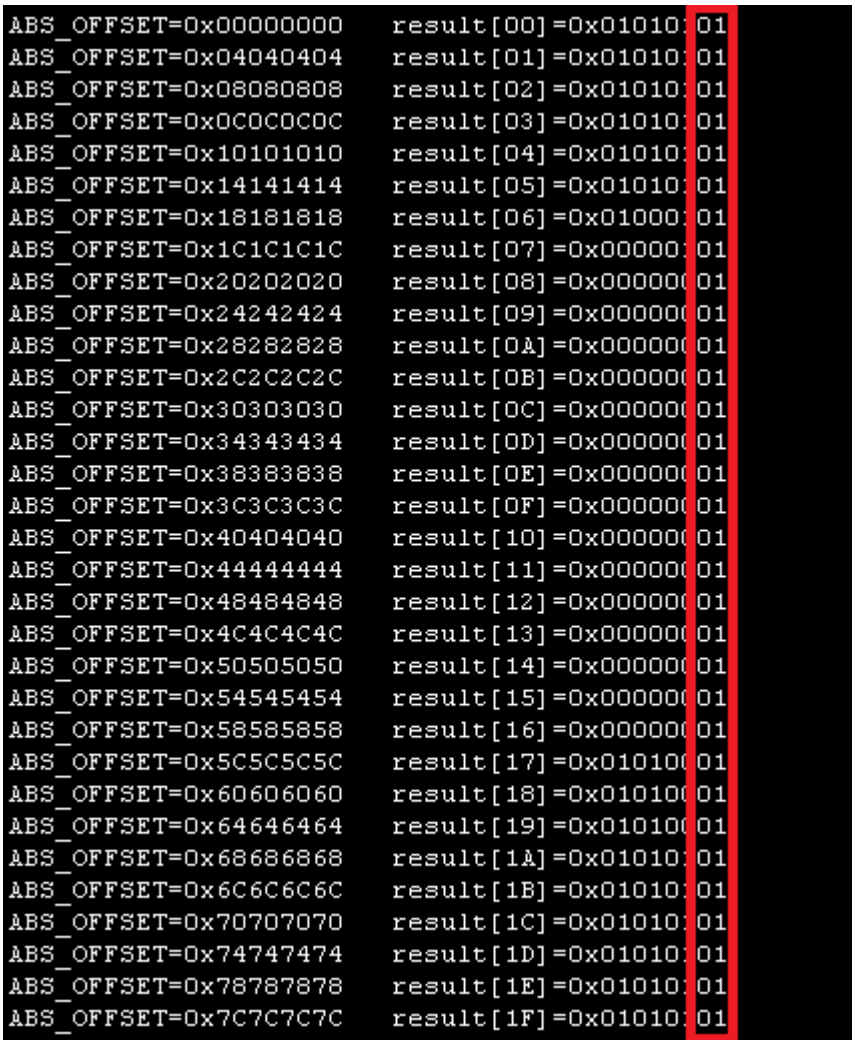
When first bringing up a new PCB, it must run the calibrations to obtain the optimal delay registers setting for the board. It is an important step; the setting on default initialization script fine tuned the delay registers on Freescale Evaluation Board only. Without the calibration, the DDR3 might be affected even if all the AC timing related MMDC registers have been configured properly.

3.3.1 Identifying Issue on Calibrations

During the calibration processes, the valid delay window is shown for each calibration (except Write Leveling Calibration). The delay windows us a rough idea how much timing margin on read DQS, and data setup and hold time for DDR3 read and write operations. In general, the wider the window, the board has more time margin. The delay windows on Freescale Evaluation boards can be used as reference. The DQS gating delay window on Freescale board is around 1.1 to 1.2 tCK. For read and write delay, the window is around 0.3 to 0.4 tCK.

There is a chance that there is an error during the calibration, it may fail to find a valid delay window for some particular bytes. In such a case, DO NOT use the calibration result and proceed with the rest of the tests even the tool may show a result after the calibration finish!

If the tool fails to find a valid window for a byte, it would be a good idea to fine tune the drive strength of both DQS and DQ of that byte. The AC timing parameters should be configured properly as valid windows could be found on other bytes. The example below shows that byte 0 always fails on read calibration, meaning that the byte fail to read no matter which delay value is used. Ideally, the drive strength should match the trace impedance. If the information is not available, you could increase or decrease the drive strength and see if there is any improvement. If there is still no improvement after changing the drive strength, it should be the time to check the PCB layout. Design rules can be found in “HW Design Checking List for i.Mx6”.



3.3.2 Identifying Issue on Stress Test

The stress test will stop when an error is found. The address for the memory location that the error occurs and the error pattern will be printed out as in the examples below.

In this example, an error is found when reading back the data on address pattern test. The report reports an error as the memory content should be the same as the address, i.e. 0x10000000. The stress test reports an error because the data read from the address is 0xfd0000ff instead.

```
DDR Freq: 396 MHz
t0.1: data is addr test
Address of failure: 0x10000000
Data was: 0xfd0000ff
But pattern  should match address
```

In this second example, an error is found when reading back the data that is written with a specific pattern. In this case, DATA[2] is supposed to be 0 but it is found to be run. Therefore, we could focus on check hardware and drive strength for byte 0 in this case.

```
Address of failure:       0x12000040
Data was:                 0x04000400
But pattern was:          0x04040404
```

In case the board fails the stress test at target frequency, we can run the test with incrementing frequencies to check what is the highest frequency that the DDR3 can run properly. This test could give us an idea the problem is due to an error on the DDR3 connections, improper MMDC settings or poor PCB layout.

If the DDR3 cannot even pass the stress test at a low frequency, say 200 MHz, it is more likely to be a hardware problem. Then, it would be a good starting point to check the DDR3 connections. In addition, you should check the power supply for the DDR3, i.MX6 MMDC and DDR3 I/O to see if voltage is valid and ripple is not too large.

If case the board cannot pass the stress test at the target frequency but it can pass the stress test at a slightly lower frequency, you could try fine tuning the drive strength of the DDR3 I/O. It is also a good idea to re-visit the MMDC parameters and see if all of the AC timing can be met at the target frequency.

4 Further Reading

In order to make user better understanding DDR3 script, some configuration examples will be showed in this Chapter.

Due to limitation knowledge of author, some errors are unavoidable.

I will appreciate if someone can enter comments into following link:
https://community.freescale.com/docs/DOC-94917

The DDR3/DDR3L interface mode of i.Mx6 fully complies with JESD79-3D DDR3 JEDEC standard release.
Latest JESD79-3 standard document can be downloaded through below link.
http://www.jedec.org/standards-documents/results/taxonomy%3A3193

4.1 DDR3 Device Related Configurations

In i.Mx6DQ Reference Manual, we use 44.12.5 MMDC Core Timing Configuration Register 0 (MMDC*x*_MDCFG0) as an example.
The register MMDC*x*_MDCFG0 is corresponding below row in page "RealView.inc" of "i.Mx6DQSDL DDR3 Script Aid".

setmem /32 0x021b000c = 0x54597955 // MMDC0_MDCFG0

Field info of MMDC*x*_MDCFG0 is showed.

Address: Base address + Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	tRFC								tXS								tXP			tXPDLL				tFAW						tCL			
Reset	0	0	1	1	0	0	1	0	0	0	1	1	0	1	1	0	0	0	1	0	0	0	1	0	1	1	0	1	0	0	1	1

tXPDLL field detailed info can be found in following table.

12–9 tXPDLL	Exit precharge power down with DLL frozen to commands requiring DLL. This field is not relevant in LPDDR2 mode. See DDR3 SDRAM Specification JESD79-3E (July 2010) and LPDDR2 SDRAM Specification JESD209-2B (February 2010) for a detailed description of this parameter. 0x0 1 clock 0x1 2 clocks 0x2 3 clocks 0xE 15 clocks 0xF 16 clocks

Below table is extracted from "Table 68 — Timing Parameters by Speed Bin" in JESD79-3.

		DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600	
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	max(10nCK, 24ns)	-	max(10nCK, 24ns)	-	max(10nCK, 24ns)	-	max(10nCK, 24ns)	-

Target speed is 528MHz in the design. We can get tCK approximate 1.894ns.

Using column DDR3-1600 parameter, max (10nCK, 24ns)/1.894ns=24ns/1.894ns=12.67

Then tXPDLL should be 13 clocks and register value should be 0x0C according tXPDLL field in RM.

tFAW field detailed info can be found in following table.

8–4 tFAW	Four Active Window (all banks). See DDR3 SDRAM Specification JESD79-3E (July 2010) and LPDDR2 SDRAM Specification JESD209-2B (February 2010) for a detailed description of this parameter. 0x0 1 clock 0x1 2 clocks 0x2 3 clocks 0x1E 31 clocks 0x1F 32 clocks

Related define is extracted from “Table 68 — Timing Parameters by Speed Bin” in JESD79-3 as below.

		DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Units
Four activate window for 1KB page size	tFAW	40	-	37.5	-	30	-	30	-	ns
Four activate window for 2KB page size	tFAW	50	-	50	-	45	-	40	-	ns

2Gb =128Mx16 (2K page size) is used

Following second row of column DDR3-1600, 40ns/1.894ns = 21.12

Then tFAW should be 22 clocks and register value should be 0x15 according tFAW field in RM.

4.2 System Design Related Configurations

tRFC field detailed info can be found in following table.

31–24 tRFC	Refresh command to Active or Refresh command time. See DDR3 SDRAM Specification JESD79-3E (July 2010) and LPDDR2 SDRAM Specification JESD209-2B (February 2010) for a detailed description of this parameter. 0x0 1 clock 0x1 2 clocks 0x2 3 clocks 0xFE 255 clocks 0xFF 256 clocks

Related define is extracted from “Table 61 — Refresh parameters by device density” in JESD79-3 as below.

Parameter	Symbol	512Mb	1Gb	2Gb	4Gb	8Gb	Units
REF command to ACT or REF command time	tRFC	90	110	160	260	350	ns

Based on known info, tRFC = 160ns/1.894ns=84.5.

Then tRFC should be 85 clocks and register value should be 0x54 according tRFC field in RM.

4.3 SI Related Configurations

In i.Mx6DQ Reference Manual, we use 36.4.350 Pad Control Register (IOMUXC_SW_PAD_CTL_PAD_DRAM_SDCLK0_P) as an example.

The register IOMUXC_SW_PAD_CTL_PAD_DRAM_SDCLK0_P is corresponding below row in page "RealView.inc" of "i.Mx6DQSDL DDR3 Script Aid".

setmem /32 0x020e0588 = 0x00000028 // IOMUXC_SW_PAD_CTL_PAD_DRAM_SDCLK_0

Field info of IOMUXC_SW_PAD_CTL_PAD_DRAM_SDCLK0_P is showed.

Address: 20E_0000h base + 588h offset = 20E_0588h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0												DDR_SEL		DDR_INPUT	HYS
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	PUS		PUE	PKE	0	ODT			0		DSE		0			
W																
Reset	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

DSE field detailed info can be found in following table.

5–3 DSE	Drive Strength Field Select one of next values for pad: DRAM_SDCLK_0. 000 **HIZ** — HI-Z 001 **240_OHM** — 240 Ohm 010 **120_OHM** — 120 Ohm 011 **80_OHM** — 80 Ohm 100 **60_OHM** — 60 Ohm 101 **48_OHM** — 48 Ohm 110 **40_OHM** — 40 Ohm 111 **34_OHM** — 34 Ohm

As mentioned in section 2.1.3, the register can be configured by default based on SI design experience or simulation result.