maxim integrated

MAX9283/MAX9285 (Pass-1)

GMSL1 Serializer with 4-Lane MIPI DSI Input Port

General Description

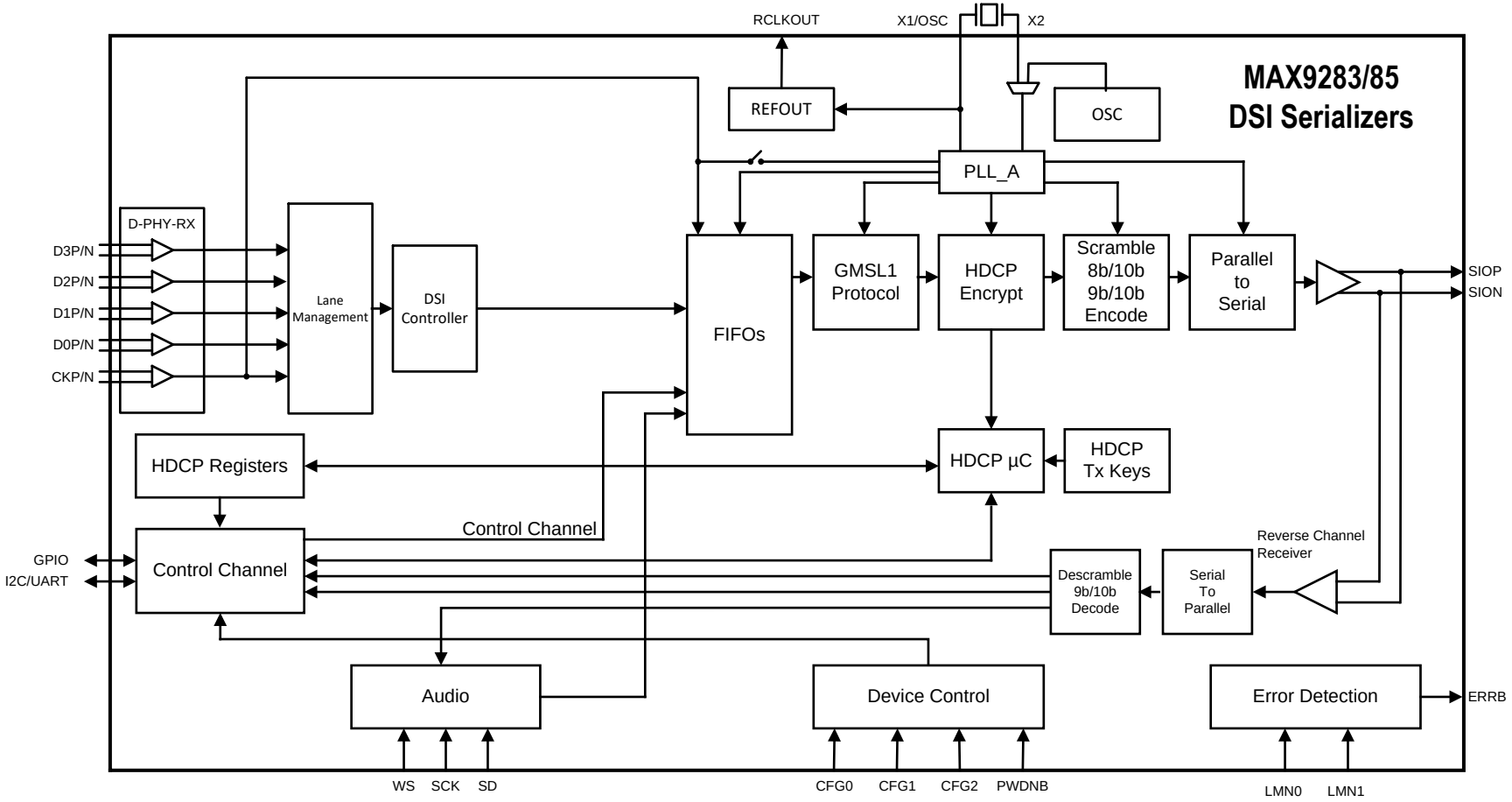
The MAX9283 and MAX9285 convert MIPI DSI v1.3 input to GMSL1 serial output. A MIPI D-PHY v1.2 4-lane input port is provided supporting data rates from 80Mbps to 2.5Gbps per lane. The MAX9283 and MAX9285 send and receive control channel data, enabling bi-directional transmission of video and data over cables up to 15m in length. Works with low-cost 50Ω coax or 100Ω STP cables that meet the GMSL channel specification. The GMSL link operates at rates from 500Mbps to 4.5Gbps in the forward direction and 1Mbps in reverse. The MAX9285 adds the High-bandwidth Digital Encryption Protection (HDCP) engine. Operation is specified over the automotive temperature range of -40°C to +105°C and the device is AEC-Q100 qualified.

Features

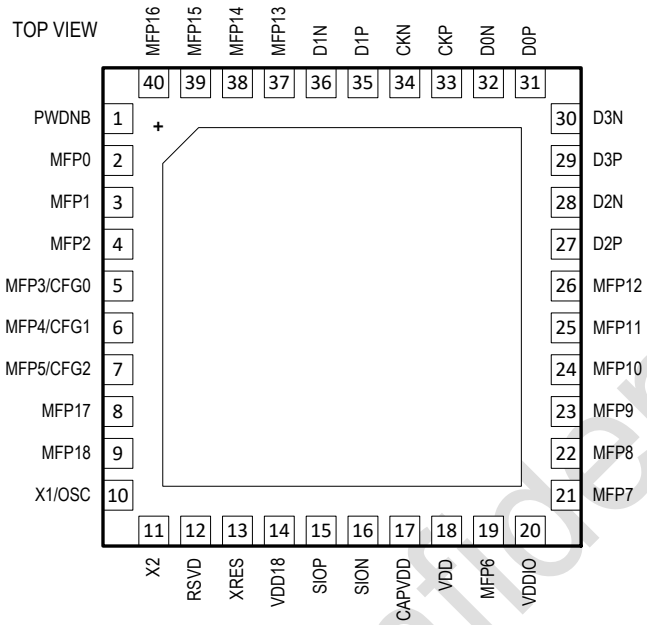
- MIPI D-PHY v1.2 4-lane input port
- MIPI DSI v1.3 peripheral controller
- DSI ECC and Checksum error detection and flagging
- DSI lane polarity flip
- DSI lane reassignment
- HDCP v2.2 content protection with keys stored securely on-chip (MAX9285 only)
- Up to 19 sampled or register-programmable GPIO
- Works with low-cost 50Ω coax or 100Ω STP cables that meet the GMSL channel specification
- 9.6kbps to 1Mbps Control Channel in UART or I2C Mode with Clock-Stretch Capability
- High Immunity Mode (HIM) for robust control channel EMC tolerance
- I^2S or 7.1 TDM audio in forward direction
- Programmable spread spectrum on serial I/O for EMI reduction
- Cross point switch maps video pixel data to any desired deserializer output order
- Line-fault monitor detects serial I/O shorted together, to ground, to battery or open
- Built-in PRBS generator for BER testing of the serial link
- Eight hardware programmable device addresses*
- 6x6mm Side Wettable TQFN package with 40 leads and 0.5mm lead pitch
- +1.7V to +1.9V analog supply
- Flexible core supply accepts a ±5% tolerance supply with nominal value of 1.0V, 1.1V, 1.2V or 1.8V
- +1.7 to +3.6V I/O supply
- ±8kV Contact and ±15kV air ISO10605 and IEC61000-4-2 ESD tolerance on GMSL2 links
- -40°C to +105°C operating temperature
- Meets AEC-Q100 specification

*Pass-2 and production devices will have only 8 hardware programmable device addresses

MAX9283 and MAX9285 Block Diagram



MAX9283 and MAX9285 Package Pinout PRELIMINARY - MAY CHANGE WITHOUT NOTICE



6x6mm TQFN package with 40 leads and 0.5mm lead pitch:
Package Outline Document Control Number: 21-0141
Package Land Pattern Document Control Number: 90-0055

6x6mm Side Wettable TQFN package with 40 leads and 0.5mm lead pitch:
Package Outline Document Control Number: 21-100157
Package Land Pattern Document Control Number: 90-0055

Pin Description

Pin	Pin Name	Default Function	Alternate Functions		Description
1	PWDNB	PWDNB			PWDNB: Active-low power-down input.
2	MFP0	CNTL0	GPIO00		CNTL0: Auxiliary Control-Signal Input. Used only in high-bandwidth mode (BWS = Z). GPIO00: General Purpose Input or Output.
3	MFP1	CNTL1	GPIO01		CNTL1: Auxiliary Control-Signal Input. Used only in high-bandwidth mode (BWS = Z or 1). GPIO01: General Purpose Input or Output.
4	MFP2	RCLKOUT	GPIO02		RCLKOUT: 25MHz frequency reference output. GPIO02: General Purpose Input or Output.
5	MFP3/CFGO	GPO3	GPO3		CFG0: A resistive divider (+/-1% tolerance) is required on each CFG pin between VDDIO and EP. The resistor values determine the device configuration at power-up. See table TBD for details. GPO3: General-purpose output. **Note: this pin requires >1MΩ load impedance at power-up**
6	MFP4/CFG1	GPO4	GPO4		CFG1: A resistive divider (+/-1% tolerance) is required on each CFG pin between VDDIO and EP. The resistor values determine the device configuration at power-up. See table TBD for details. GPO4: General-purpose output. **Note: this pin requires >1MΩ load impedance at power-up**
7	MFP5/CFG2	GPO5	GPO5		CFG2 A resistive divider (+/-1% tolerance) is required on each CFG pin between VDDIO and EP. The resistor values determine the device configuration at power-up. See table TBD for details. GPO5: General-purpose output. **Note: this pin requires >1MΩ load impedance at power-up**
8	MFP17	SDA_RX	ODO17	GPIO17	SDA_RX: I2C data input/output or UART input. ODO17: General Purpose Open-Drain Output. GPIO17: General Purpose Input or Output.
9	MFP18	SCL_TX	ODO18	GPIO18	SCL_TX: I2C clock input/output or UART output. ODO18: General Purpose Open-Drain Output. GPIO18: General Purpose Input or Output.
10	X1/OSC	X1/OSC			Crystal/Oscillator Input. If crystal used, connect to one terminal of a 25MHz crystal. If oscillator used, supply a 25MHz ±200ppm signal.
11	X2	X2			Crystal Input. Connect to one terminal of a 25MHz ±200ppm crystal.
12	RSVD	RSVD			Reserved. Not internally connected. Leave open.
13	XRES	XRES			Connect a 400Ω ±1% resistor between XRES and ground.
14	VDD18	VDD18			1.7V to 1.9V analog supply
15	SIOP	SIOP			Non-inverted Coax/Twisted-Pair Serial-Data output.
16	SION	SION			Inverted Twisted-Pair Serial-Data output
17	CAPVDD	CAPVDD			Connect a 0.1uF capacitor from VDDCAP to EP.
18	VDD	VDD			+/-5% tolerance core supply accepts nominal 1.8V, 1.2V, 1.1V or 1.0V
19	MFP6	GPO	GPIO06		GPO: General Purpose Output. Tracks GPI of GMSL1 deserializer. GPIO06: General Purpose Input or Output.
20	VDDIO	VDDIO			1.7V to 3.6V I/O supply
21	MFP7	MS	GPIO07		MS: Mode Select with Internal 1MΩ Pulldown to VSS. Set MS = low to select base mode. Set MS = high to select bypass mode. The state of MS latches at power-up. GPIO07: General purpose Open Drain Output. General Purpose Input or Output.
22	MFP8	GPIO08	WS		GPIO08: General Purpose Input or Output. WS: I2S/TDM Serial-Word Input with Internal 1MΩ Pulldown to VSS.
23	MFP9	GPIO09	SCK		GPIO09: General Purpose Input or Output. SCK: I2S/TDM Serial-Clock Input with Internal 1MΩ Pulldown to VSS.
24	MFP10	GPIO10	SD		General Purpose Input or Output. SD: I2S/TDM Serial-Data Select Input with Internal 1MΩ Pulldown to VSS. GPIO10:
25	MFP11	LMN0	GPIO11		LMN0: line fault monitor input GPIO11: General Purpose Input or Output.
26	MFP12	LMN1	GPIO12		LMN1: line fault monitor input GPIO12: General Purpose Input or Output.
27	D2P	D2P			D2P: DSI data lane 2 non-inverted input.
28	D2N	D2N			D2N: DSI data lane 2 inverted input.
29	D3P	D3P			D3P: DSI data lane 3 non-inverted data input.
30	D3N	D3N			D3N: DSI data lane 3 inverted data input.
31	D0P	D0P			D0P: DSI data lane 0 non-inverted data input.
32	D0N	D0N			D0N: DSI data lane 0 inverted data input.
33	CKP	CKP			CKP: DSI clock lane non-inverted input.
34	CKN	CKN			CKN: DSI clock lane inverted input.
35	D1P	D1P			D1P: DSI data lane 1 non-inverted data input.
36	D1N	D1N			D1N: DSI data lane 1 inverted data input.

37	MFP13	LFLTB/ERRB	GPIO13		LFLTB_ERRB: Line fault or Error output. Goes low when a line fault on LMN0 or LMN1 is detected or a DSI ECC or Checksum error is detected.
38	MFP14	GPIO14			GPIO14: General Purpose Input or Output.
39	MFP15	CNTL2	GPIO15		CNTL2: Auxiliary Control-Signal Input. CNTL2: Used only in high-bandwidth mode (BWS = Z or 1). GPIO15: General Purpose Input or Output.
40	MFP16	CNTL3	GPIO16		CNTL3: Auxiliary Control-Signal Input. CNTL3: Used only in high-bandwidth mode (BWS = Z). GPIO16: General Purpose Input or Output.

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 0.9V to 1.1V, V_{DD18} = 1.7V to 1.9V, V_{VDDIO} = 1.7V to 3.6V, R_L= 100Ω ±1% (differential), R_L = 50Ω ± 1% (single-ended), EP connected to PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DD} = 1.0V, $V_{DD!8}$ = 1.8V, V_{DDIO} = 1.8V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	TYPE	GL
I/O PINS (MFP_)								
High-Level Input Voltage	V_{IH}		V_{DDIO} * 0.7			V	Normal	II
Low-Level Input Voltage	V_{IL}				V_{DDIO} * 0.3	V	Normal	II
High-Level Output Voltage	V_{OH}	I_{OH} = -2mA I_{OH} = -8mA	V_{DDIO} - 0.2 V_{DDIO} - 0.4			V	Normal	II
Low-Level Output Voltage	V_{OL}	I_{OL} = 2mA I_{OL} = 8mA			0.2 0.4	V	Normal	II
Input Current	I_{IN}	V_{IN} = 0 to V_{DDIO}. All pull-up/pull-down devices disabled.			1	µA	Normal	II
Input Capacitance	C_{IN}	Each pin.		5		pF	Normal	II
OPEN DRAIN PINS (SDA/RX, SCL/TX, LOCK, LFLTB/ERRB)								
High-Level Input Voltage	V_{IH2}		V_{DDIO} * 0.7			V	Normal	II
Low-Level Input Voltage	V_{IL2}				V_{DDIO} * 0.3	V	Normal	II
Low-Level Open-Drain Output Voltage	V_{OL}	I_{OL} = 2mA I_{OL} = 8mA			0.2 0.4	V	Normal	II
Input Current	I_{IN}	V_{IN} = 0 to $V_{DDIO.}$ R_{PU} disabled.			1	µA	Normal	II
Input Capacitance	C_{IN}	Each pin.		5		pF	Normal	II
Internal Pull-up Resistor	R_{PU}			40		kΩ	Normal	II
INPUT ONLY PIN (PWDNB)								
High-Level Input Voltage	V_{IH}		VDDIO x 0.7			V		
Low-Level Input Voltage	V_{IL}				VDDIO x 0.3	V		
Input Current	I_{IN}	VIN = 0 to VDDIO			5	µA		
Input Capacitance	C_{IN}	Each pin.		5		pF		
Internal Pull-down Resistor	R_{PD}			1		MΩ		
GMSL DIFFERENTIAL OUTPUTS (SIOP/N)								
Differential Output Voltage	V_{OD}	Pre/deemphasis off	300	400	500	mV		
		3.3dB preemphasis (Note 5)	350		610			
		3.3dB deemphasis	240		425			
Change in V_{OD} Between Complimentary Output States	ΔV_{OD}	Preemphasis off and deemphasis only			25	mV		
Output Offset Voltage	V_{OS}	$(V_{SIOP} + V_{SION})/2 = V_{OS}$ Preemphasis off	1.1	1.4	1.56	V		
Change in VOS Between Complimentary Output States	ΔVOS				25	mV		

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 0.9V to 1.1V, V_{DD18} = 1.7V to 1.9V, V_{VDDIO} = 1.7V to 3.6V, R_L= 100Ω ±1% (differential), R_L = 50Ω ± 1% (single-ended), EP connected to PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DD} = 1.0V, $V_{DD!8}$ = 1.8V, V_{DDIO} = 1.8V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	TYPE	GL
Output Short-Circuit Current	I_{OS}	V_{SIOP} or V_{SION} = 0V	-62			mA		
		V_{SIOP+} or V_{SION} = 1.9V			25			
Magnitude of Differential Output Short-Circuit Current	I_{OSD}	V_{OD} = 0V			25	mA		
Output Termination Resistance (Internal)	R_O	From SIOP or SION to V_{DDD}	45	54	63	Ω		
REVERSE CONTROL-CHANNEL RECEIVER (SIOP/N)								
High Switching Threshold	V_{CHR}	Legacy			27	mV		
		High-immunity			40			
Low Switching Threshold	V_{CLR}	Legacy	-27			mV		
GMSL SINGLE-ENDED OUTPUTS (SIOP and SION)								
Single-Ended Output Voltage	V_{OUT}	Pre/deemphasis off	375	500	625	mV		
		3.3dB preemphasis (Note 5)	435		765			
		3.3dB deemphasis	300		535			
Output Short-Circuit Current	I_{OS}	V_{SIOP} or V_{SION} = 0V	-69			mA		
		V_{SIOP} or V_{SION} = 1.9V			32			
Output Termination Resistance (Internal)	R_O	From OUT+ or OUT- to V_{AVDD}	45	54	63	Ω		
LINE-FAULT DETECTION INPUTS (LMN0, LMN1)								
Short-to-GND Threshold	V_{TG}				0.3	V		
Normal Thresholds	V_{TN}		0.57		1.07	V		
Open Thresholds	V_{TO}		1.45		V_{DDIO} + 0.06	V		
Open Input Voltage	V_{IO}		1.47		1.75	V		
Short-to-Battery Threshold	V_{TE}		2.47			V		

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 0.9V to 1.1V, V_{DD18} = 1.7V to 1.9V, V_{VDDIO} = 1.7V to 3.6V, R_L= 100Ω ±1% (differential), R_L = 50Ω ± 1% (single-ended), EP connected to PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DD} = 1.0V, $V_{DD!8}$ = 1.8V, V_{DDIO} = 1.8V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	TYPE	GL
D-PHY PIN CHARACTERISTICS (D[3:0]P/N, CKP/N)								
Signal Voltage Range	V_{PIN}		-50		1350	mV		
Leakage Current	I_{LEAK}	Note 1	-10		+10	µA		
Ground Shift	V_{GNDSH}					mV		
Transient Voltage Level	$V_{PIN(absmax)}$	Note 3				mV		
Maximum Transient Time	$T_{VPIN(absmax)}$	Above (VPIN(MAX) or Below VPIN(MIN), Note 2				mV		
Note: 1. *When the pad voltage is in the signal voltage range from $V_{GNDSH,MIN}$ to V_{OH} + $V_{GNDSH,MAX}$ and the Lane Module is in LP receive mode.* 2. *The voltage overshoot and undershoot beyond the VPIN is only allowed during a single 20ns window after any LP-0 to LP-1 transition or vice versa. For all other situations, it must stay within the VPIN range.* 3. *3. This value includes ground shift.*								
D-PHY HS RECEIVER (D[3:0]P/N, CKP/N)								
Common-mode voltage HS receive mode	$V_{CMRX(DC)}$	Note 1, 2	70		330	mV		
Differential input high threshold	V_{IDTH}	Note 3			7	mV		
		Note4			4	mV		
Differential input low threshold	V_{IDTL}	Note 3	-70			mV		
		Note4	-40			mV		
Single-ended input high voltage	V_{IHHS}	Note 1			460	mV		
Single-ended input low voltage	V_{ILHS}	Note 1	-40			mV		
Single-ended threshold for HS termination enable	$V_{TERM-EN}$				450	mV		
Differential input impedance	Z_{ID}		80	100	125	Ω		

Note:
1. *Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.*
2. *This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz*
3. *For devices supporting data rates <= 1.5 Gbps.*
4. *For devices supporting data rates > 1.5 Gbps.*

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 0.9V to 1.1V, V_{DD18} = 1.7V to 1.9V, V_{VDDIO} = 1.7V to 3.6V, R_L= 100Ω ±1% (differential), R_L = 50Ω ± 1% (single-ended), EP connected to PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DD} = 1.0V, $V_{DD!8}$ = 1.8V, V_{DDIO} = 1.8V, T_A = +25°C.)

D-PHY LP RECEIVER (D[3:0]P/N, CKP/N)								
Logic 1 input voltage	V_{IH}	Note 1	880			mV		
		Note 2	740			mV		
Logic 0 input voltage, not in ULP State	V_{IL}				550	mV		
Logic 0 input voltage, ULP State	$V_{IL-ULPS}$				300	mV		
Input hysteresis	V_{HYST}		25			mV		
Note: ***1.*** *Applicable when the supported data rate <= 1.5 Gbps.* ***2.*** *Applicable when the supported data rate > 1.5 Gbps.*								
D-PHY CLOCK (CKP/N)								
UI Instantaneous	UI_{INST}	Note 1, 2			12.5	ns		
UI Variation	ΔUI	Note 3	-10%		10%	UI		
		Note 4	-5%		5%	UI		
Note: 1. This value corresponds to a minimum 80 Mbps data rate. 2. The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst. The allowed instantaneous UI variation can cause instantaneous data rate variations. Therefore, devices should either accommodate these instantaneous variations with appropriate FIFO logic outside of the PHY or provide an accurate clock source to the Lane Module to eliminate these instantaneous variations. 3. When UI ≥ 1ns, within a single burst. 4. When 0.667ns < UI < 1ns, within a single burst.								
CRYSTAL OSCILLATOR (X1, X2)								
Frequency		Fundamental mode only; includes crystal tolerance		27		MHz		
Input Capacitance	C_{X1}, C_{X2}	Each pin		4		pF		
Load Capacitance	C_{L1}, C_{L2}	XTAL property		1		pF		
OSCILLATOR INPUT (X1/OSC)								
High-Level Input Voltage	V_{IHX}	X1 as frequency Input	0.70 x V_{VDDIO}			V		
Low-Level Input Voltage	V_{ILX}	X1 as frequency Input			0.30 x V_{VDDIO}	V		
Input Current	I_{INX}	V_{IN} = 0 to V_{XVDD}	-5		+5	µA		
Input Frequency Range		X1 as frequency Input (Note 5)	26		28.5	MHz		

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 0.9V to 1.1V, V_{DD18} = 1.7V to 1.9V, V_{VDDIO} = 1.7V to 3.6V, R_L= 100Ω ±1% (differential), R_L = 50Ω ± 1% (single-ended), EP connected to PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DD} = 1.0V, $V_{DD!8}$ = 1.8V, V_{DDIO} = 1.8V, T_A = +25°C.)

POWER SUPPLY									
Worst-Case Pattern Supply Current	I_{WCS2}	$f_{RXC\_}$ = tbd	VDD18		TBD	TBD	mA		
			VDD		TBD	TBD			
			VDD+VDD18		TBD	TBD			
			VDDIO (3.0V to 3.6V)		TBD	TBD			
			VDDIO (1.7V to 1.9)		TBD	TBD			
		$f_{RXC\_}$ = tbd	VDD18		TBD	TBD			
			VDD		TBD	TBD			
			VDD+VDD18		TBD	TBD			
			VDDIO (3.0V to 3.6V)		TBD	TBD			
			VDDIO (1.7V to 1.9)		TBD	TBD			
		$f_{RXC\_}$ = tbd	VDD18		TBD	TBD			
			VDD		TBD	TBD			
			VDD+VDD18		TBD	TBD			
			VDDIO (3.0V to 3.6V)		TBD	TBD			
			VDDIO (1.7V to 1.9)		TBD	TBD			
		$f_{RXC\_}$ = tbd	VDD18		TBD	TBD			
			VDD		TBD	TBD			
			VDD+VDD18		TBD	TBD			
			VDDIO (3.0V to 3.6V)		TBD	TBD			
			VDDIO (1.7V to 1.9)		TBD	TBD			
Sleep-Mode Supply Current	I_{CCS}	Single wake-up receiver enabled				2	mA		
Power-Down Supply Current	I_{CCZ}	**PWDN** = EP				2	mA		
ESD PROTECTION									
SIOA±, SIOB±	V_{ESD}	Human Body Model, R_D = 1.5kΩ, C_S = 100pF			±8		kV	Normal	VI
SIOA±, SIOB±	V_{ESD}	IEC61000-4-2, R_D = 330Ω, C_S = 150pF, Contact discharge			±8		kV	Normal	VI
SIOA±, SIOB±	V_{ESD}	IEC61000-4-2, R_D = 330Ω, C_S = 150pF, Air discharge			±15		kV	Normal	VI
SIOA±, SIOB±	V_{ESD}	ISO10605, R_D = 2kΩ, C_S = 330pF, Contact discharge			±8		kV	Normal	VI
SIOA±, SIOB±	V_{ESD}	ISO10605, R_D = 2kΩ, C_S = 330pF, Air discharge			±15		kV	Normal	VI
All Other Pins	V_{ESD}	Human Body Model, R_D = 1.5kΩ, C_S = 100pF			±4		kV	Normal	VI

AC ELECTRICAL CHARACTERISTICS

(V_{DD} = 0.9V to 1.1V, V_{DD18} = 1.7V to 1.9V, V_{VDDIO} = 1.7V to 3.6V, R_L= 100Ω ±1% (differential), R_L = 50Ω ± 1% (single-ended), EP connected to PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DD} = 1.0V, $V_{DD!8}$ = 1.8V, V_{DDIO} = 1.8V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS	TYPE	GL
I2C/UART PORT TIMING (SDA_RX/SCL_TX)									
I2C/UART Bit Rate				9.6		1000	kbps	Normal	V
Output Rise Time	t_R	30% to 70%, C_L = 10pF to 100pF, 1kΩ pullup to VDDIO		20		150	ns		
Output Fall Time	t_F	70% to 30%, C_L = 10pF to 100pF, 1kΩ pullup to VDDIO		20		150	ns		
I²C TIMING (SDA_RX/SCL_TX)									
SCL Clock Frequency	f_{SCL}		Low range	9.6		100	kHz		
			Mid range	> 100		400			
			High range	> 400		1000			
START Condition Hold Time	$t_{HD:STA}$	f_{SCL} range	Low	4.0			µs		
			Mid	0.6					
			High	0.26					
Low Period of SCL Clock	t_{LOW}	f_{SCL} range	Low	4.7			µs		
			Mid	1.3					
			High	0.5					
High Period of SCL Clock	t_{HIGH}	f_{SCL} range	Low	4.0			µs		
			Mid	0.6					
			High	0.26					
Repeated START Condition Setup Time	$t_{SU:STA}$	f_{SCL} range	Low	4.7			µs		
			Mid	0.6					
			High	0.26					
Data Hold Time	$t_{HD:DAT}$	f_{SCL} range	Low	0			µs		
			Mid	0					
			High	0					
Data Setup Time	$t_{SU:DAT}$	f_{SCL} range	Low	250			ns		
			Mid	100					
			High	50					
Setup Time for STOP Condition	$t_{SU:STO}$	f_{SCL} range	Low	4.0			µs		
			Mid	0.6					
			High	0.26					
Bus Free Time	t_{BUF}	f_{SCL} range	Low	4.7			µs		
			Mid	1.3					
			High	0.5					
Data Valid Time	$t_{VD:DAT}$	f_{SCL} range	Low			3.45	µs		
			Mid			0.9			
			High			0.45			

AC ELECTRICAL CHARACTERISTICS

(V_{DD} = 0.9V to 1.1V, V_{DD18} = 1.7V to 1.9V, V_{VDDIO} = 1.7V to 3.6V, R_L= 100Ω ±1% (differential), R_L = 50Ω ± 1% (single-ended), EP connected to PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DD} = 1.0V, $V_{DD!8}$ = 1.8V, V_{DDIO} = 1.8V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS	TYPE	GL
Data Valid Acknowledge Time	$t_{VD:ACK}$	f_{SCL} range	Low			3.45	µs		
			Mid			0.9			
			High			0.45			
Pulse Width of Spikes Suppressed	t_{SP}	f_{SCL} range	Low			50	ns		
			Mid			50			
			High			50			
Capacitive Load Each Bus Line	C_B					100	pF		
GPIO PINS (MFP_)									
Rise-and-Fall Time	t_R, t_F	20% to 80%, C_L = 10pF (Note 5)	V_{IOVDD} = 1.7V to	0.5		3.6	ns		
			V_{IOVDD} = 3.0 to	0.3		2.2			
GMSL DIFFERENTIAL OUTPUTS (SIOP/N)									
Rise-and-Fall Time	t_R, t_F	20% to 80%, V_{OD} ≥ 400mV, R_L = 100Ω, serial bit rate = 3.12Gbps (Note 5)			90	160	ps		
Total Serial Output Jitter	t_{TSOJ1}	3.12Gbps PRBS, measured at V_{OD} = 0V, pre/deemphasis disabled			0.25		UI		
Deterministic Serial Output Jitter	t_{DSOJ2}	3.12Gbps PRBS, measured at V_{OD} = 0V, pre/deemphasis disabled			0.15		UI		
GMSL SINGLE-ENDED OUTPUT (SIOP, SION)									
Rise-and-Fall Time	t_R, t_F	20% to 80%, V_O ≥ 500mV, R_L = 50Ω, serial bit rate = 3.12Gbps (Note 5)			90	160	ps		
Total Serial Output Jitter	t_{TSOJ1}	3.12Gbps PRBS, measured at V_O/2, pre/deemphasis disabled			0.25		UI		
Deterministic Serial Output Jitter	t_{DSOJ2}	3.12Gbps PRBS, measured at V_O/2, pre/deemphasis disabled			0.15		UI		
D-PHY HS RECEIVER (D[3:0]P/N, CKP/N)									
Common-mode interference beyond 450 MHz	ΔVCMRX(HF)	Note 2, 5				100	mV	Normal	
		Note 2, 6				50	mV	Normal	
Common-mode interference 50MHz – 450MHz	ΔVCMRX(LF)	Note 1, 4, 5		-50		50	mV	Normal	
		Note 1, 4, 6		-25		25	mV	Normal	

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 0.9V to 1.1V, V_{DD18} = 1.7V to 1.9V, V_{VDDIO} = 1.7V to 3.6V, R_L= 100Ω ±1% (differential), R_L = 50Ω ± 1% (single-ended), EP connected to PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DD} = 1.0V, $V_{DD!8}$ = 1.8V, V_{DDIO} = 1.8V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	TYPE	GL
Common-mode termination	CCM	Note 3			60	pF	Normal	

Note:

1. *Excluding 'static' ground shift of 50mV*
2. *ΔVCMRX(HF) is the peak amplitude of a sine wave superimposed on the receiver inputs.*
3. *For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.*
4. *Voltage difference compared to the DC average common-mode potential.*
5. *For devices supporting data rates <= 1.5 Gbps.*
6. *For devices supporting data rates > 1.5 Gbps.*

D-PHY LP RECEIVER (D[3:0]P/N, CKP/N)								
Input pulse rejection	e_{SPIKE}	Notes 1, 2, 3			300	V·ps	Normal	
Minimum pulse width response	T_{MIN-RX}	Note 4	20			ns	Normal	
Peak interference amplitude	V_{INT}				200	mV	Normal	
Interference frequency	f_{INT}		450			MHz	Normal	

Note:

1. *Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1 state. eSpike generation will ensure the spike is crossing both VIL,max and VIH,min levels.*
2. *An impulse less than this will not change the receiver state.*
3. *In addition to the required glitch rejection, implementers shall ensure rejection of known RF- interferers.*
4. *An input pulse greater than this shall toggle the output.*

D-PHY DATA-CLOCK TIMING								
Data to Clock Skew	$T_{SKEW[TX]}$	0.08Gbps ≤ Freq. ≤1.0Gbps	-0.15		0.15	ULinst		
		1.0Gbps < Freq. ≤1.5Gbps	-0.2		0.20	ULinst		
	$T_{SKEW[TLIS]}$	0.08Gbps ≤ Freq. ≤1.0Gbps	-0.20		0.20	ULinst		
		1.0Gbps < Freq. ≤1.5Gbps	-0.10		0.10	ULinst		
Data to Clock Setup Time	$T_{SETUPO[RX]}$	0.08Gbps ≤ Freq. ≤1.0Gbps	0.15			ULinst		
		1.0Gbps < Freq. ≤1.5Gbps	0.20			ULinst		
Data to Clock Hold Time	$T_{HOLD[RX]}$	0.08Gbps ≤ Freq. ≤1.0Gbps	0.15			ULinst		
		1.0Gbps < Freq. ≤1.5Gbps	0.20			ULinst		
Static Data to Clock Skew (TX)	$T_{SKEW[TX]}$ static	>1.5Gsps	-0.20		0.20	ULinst		
Static Data to Clock Skew (channel)	TSKEW[TLIS] static	>1.5Gsps	-0.10		0.10	ULinst		
Static Data to Clock Skew (RX)	TSKEW[RX] static	>1.5Gsps	-0.20		0.20	ULinst		
Dynamic Data to Clock Skew (TX)	TSKEW[TX] dynamic	>1.5Gsps	-0.15		0.15	ULinst		

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 0.9V to 1.1V, V_{DD18} = 1.7V to 1.9V, V_{VDDIO} = 1.7V to 3.6V, R_L= 100Ω ±1% (differential), R_L = 50Ω ± 1% (single-ended), EP connected to PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DD} = 1.0V, $V_{DD!8}$ = 1.8V, V_{DDIO} = 1.8V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	TYPE	GL
Channel ISI	ISI	>1.5Gsps			0.20	ULinst		
Dynamic Data to Clock Skew Window RX Tolerance	$T_{SETUP[RX]}$ + $T_{HOLD[RX]}$ dynamic	> 1.5Gsps	0.50			ULinst		
I2S/TDM Timing								
WS Frequency	f_{WS}		8		192	kHz	Normal	IV
Sample Word Length	n_{WS}		8		32	Bits	Normal	IV
SCK Frequency	f_{SCK}	$f_{SCK} = f_{WS} \times n_{WS} \times$ (2 or 8)	(8 x 8) x 2		(192 x 32) x 8	kHz	Normal	IV
SCK Clock High Time	t_{HC}	$V_{SCK} \geq V_{IH}$, $t_{SCK} = 1/f_{SCK}$	0.35 x t_{SCK}			ns	Normal	IV
SCK Clock Low Time	t_{LC}	$V_{SCK} \leq V_{IL}$, $t_{SCK} = 1/f_{SCK}$	0.35 x t_{SCK}			ns	Normal	IV
SD, WS Setup Time	t_{SET}		2			ns	Normal	IV
SD, WS Hold Time	t_{HOLD}		2			ns	Normal	IV
SWITCHING CHARACTERISTICS (SIOP and SION)								
Serial Output Rise/Fall time	t_R, t_F	20% to 80%, V_{OD} ; 400mV differential R_L = 100Ω, 500mV single-ended R_L = 50Ω			250	ps	Normal	V
Deterministic Serial Output Jitter (Differential output)	tDSOJ2	PRBS, measured at VOD = 0V differential		0.15		UI	Normal	V
Total Serial Output Jitter (Single-ended output)	tTSOJ1	PRBS, measured at VO/2,		0.25		UI	Normal	V
Deterministic Serial Output Jitter (Single-ended output)	tDSOJ2	1.74Gbps PRBS, measured at VO/2		0.15		UI	Normal	V
Serializer Delay	tSD	Spread spectrum enabled			TBD	TPCLK	Normal	IV
Serializer Delay	tSD	Spread spectrum disabled			TBD	TPCLK	Normal	IV
Link Start Time	tLOCK				2	ms	Normal	IV
Power-up Time	tPU				7	ms	Normal	IV
GENERAL TIMING								
GPI-to-GPO Delay	t_{GPIO}	Deserializer GPI to MAX9291/ MAX9293 GPO			350	µs		
Device Delay	t_{SD}	(Notes 5, 10) Spread spectrum	83		174	Bits		
		(Notes 5, 10) Spread spectrum	99		126			
Link Start Time	t_{LOCK}	PLLs locked			3.5	ms		
Power-Up Time	t_{PU}				8	ms		

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 0.9V to 1.1V, V_{DD18} = 1.7V to 1.9V, V_{VDDIO} = 1.7V to 3.6V, R_L= 100Ω ±1% (differential), R_L = 50Ω ± 1% (single-ended), EP connected to PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DD} = 1.0V, $V_{DD!8}$ = 1.8V, V_{DDIO} = 1.8V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	TYPE	GL
I²S/TDM								
WS Frequency	f_{WS}		8		192	kHz		
Sample Word Length	n_{WS}		8		32	Bits		
SCK Frequency	f_{SCK}	$f_{SCK} = f_{WS} \times n_{WS} \times$ (2 or 8)	(8 x 8) 2		(192 x x 32) x 8	kHz		
SCK Clock High Time	t_{HC}	$V_{SCK} \geq V_{IH}$, $t_{SCK} = 1/f_{SCK}$	0.35 x t_{SCK}			ns		
SCK Clock Low Time	t_{LC}	$V_{SCK} \leq V_{IL}$, $t_{SCK} = 1/f_{SCK}$	0.35 x t_{SCK}			ns		
SD, WS Setup Time	t_{SET}		2			ns		
SD, WS Hold Time	t_{HOLD}		2			ns		
REFERENCE CLOCK OUTPUT (RCLKOUT)								
Clock Frequency	$f_{PCLKOUT}$	BWS = 0, DRS = 1	6.25	27	74.25	MHz		
Clock Duty Cycle	DC	t_{HIGH}/t_T or t_{LOW}/t_T (Figure 6, Note 7)	40	50	60	%		
Clock Jitter	t_J	Period jitter, peak to peak,		0.05		UI		

CFG Latch at Power-up Pins (Pass-1)

The CFG control functions will change from 16 levels to 8 levels in Pass-2 and production devices.

At power-up or after reset, the voltage level at the CFG pins (set by the voltage divider) is sampled. The sampled level sets the initial value of certain registers.

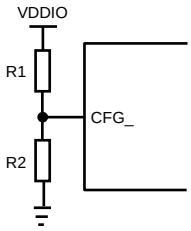


Figure TBD. Configuration Pin Circuit

I/O Matrix

Config		CFG0	CFG1	CFG2
(LSB)	0	I2CSEL	GMSL2	RCLKEN
	1	ADD0		DRS
	2	ADD1	HIM	BWS
(MSB)	3	ADD2	CXTP	HIBW

Table 1 - CFG0 Input Map

CFG1 INPUT VOLTAGE (note a, b) (percent of VDDIO)			**MAPPED CONFIGURATION** (note c)		
MIN	**TYP**	**MAX**	**ADDR[2:0]**	**I2CSEL**	**DEVICE ADDRESS**
0.0%	11.02%	13.37% - 17mV	000	UART (0)	0x80
13.37% + 17mV	15.72%	18.21% - 17mV	000	I2C (1)	0x80
18.21% + 17mV	20.70%	23.23% - 17mV	001	UART (0)	0x84
23.23% + 17mV	25.76%	27.97% - 17mV	001	I2C (1)	0x84
27.97% + 17mV	30.17%	32.79% - 17mV	010	UART (0)	0x88 (splitter)
32.79% + 17mV	35.40%	38.00% - 17mV	010	I2C (1)	0x88 (splitter)
38.00% + 17mV	40.60%	42.88% - 17mV	011	UART (0)	0xC0
42.88% + 17mV	45.16%	47.58% - 17mV	011	I2C (1)	0xC0
47.58% + 17mV	50.00%	52.42% - 17mV	100	UART (0)	0xC4
52.42% + 17mV	54.84%	57.12% - 17mV	100	I2C (1)	0xC4
57.12% + 17mV	59.40%	62.00% - 17mV	101	UART (0)	0xC8 (splitter)

62.00% + 17mV	64.60%	67.21% - 17mV	101	I2C (1)	0xC8 (splitter)
67.21% + 17mV	69.83%	72.03% - 17mV	110	UART (0)	0x40
72.03% + 17mV	74.24%	76.77% - 17mV	110	I2C (1)	0x40
76.77% + 17mV	79.30%	81.79% - 17mV	111	UART (0)	0x44
81.79% + 17mV	84.28%	86.63% - 17mV	111	I2C (1)	0x44

Notes:

a) Resistor divider tolerance, VDDIO supply ripple and external loading must not cause the CFG0 input voltage to exceed the maximum or minimum limits.
b) Other than the CFG0 input resistor divider, any load on CFG0 must be ≥ 25 x (R1 + R2).
c) I2CSEL: I2C or UART interface for SDA_RX and SCL_TX
ADDR[2:0]: device address register bits
DEVICE ADDRESS: device address

Table 2 – CFG1 Input Map

CFG1 INPUT VOLTAGE (note a, b) (percent of VDDIO)			**MAPPED CONFIGURATION** (note c)	
MIN	**TYP**	**MAX**	**CXTP**	**HIM**
0.0%	11.02%	13.37% - 17mV	STP (0)	HIM Disabled (0)
Reserved				
18.21% + 17mV	20.70%	23.23% - 17mV	STP (0)	HIM Disabled (0)
Reserved				
27.97% + 17mV	30.17%	32.79% - 17mV	STP (0)	HIM Enabled (1)
Reserved				
38.00% + 17mV	40.60%	42.88% - 17mV	STP (0)	HIM Enabled (1)
Reserved				
47.58% + 17mV	50.00%	52.42% - 17mV	COAX (1)	HIM Disabled (0)
Reserved				
57.12% + 17mV	59.40%	62.00% - 17mV	COAX (1)	HIM Disabled (0)
Reserved				
67.21% + 17mV	69.83%	72.03% - 17mV	COAX (1)	HIM Enabled (1)
Reserved				
76.77% + 17mV	79.30%	81.79% - 17mV	COAX (1)	HIM Enabled (1)
Reserved				

Notes:

a) Resistor divider tolerance, VDDIO supply ripple and external loading must not cause the CFG1 input voltage to exceed the maximum or minimum limit.
b) Other than the CFG1 input resistor divider, any load on CFG1 must be ≥ 25 x (R1 + R2).
c) CXTP: coax (SIOP) or shielded-twisted-pair (SIOP, SION) serial link.
HIM: High Immunity Mode for reverse control channel.

Table 3 – CFG2 Input Map

CFG2 INPUT VOLTAGE (note a, b) (percent of VDDIO)			**MAPPED CONFIGURATION** (note c)			
MIN	**TYP**	**MAX**	**HIBW**	**BWS**	**DRS**	**RCLKEN**
0.0%	11.02%	13.37% - 17mV	HIBW (0)	24-Bit Mode (0)	NO REPETITION (0)	RCLKOUT DISABLED (0)
13.37% + 17mV	15.72%	18.21% - 17mV	HIBW (0)	24-Bit Mode (0)	NO REPETITION (0)	RCLKOUT ENABLED (1)
18.21% + 17mV	20.70%	23.23% - 17mV	HIBW (0)	24-Bit Mode (0)	PIXEL REPETITION (1)	RCLKOUT DISABLED (0)
23.23% + 17mV	25.76%	27.97% - 17mV	HIBW (0)	24-Bit Mode (0)	PIXEL REPETITION (1)	RCLKOUT ENABLED (1)
27.97% + 17mV	30.17%	32.79% - 17mV	HIBW (0)	32-Bit Mode (1)	NO REPETITION (0)	RCLKOUT DISABLED (0)
32.79% + 17mV	35.40%	38.00% - 17mV	HIBW (0)	32-Bit Mode (1)	NO REPETITION (0)	RCLKOUT ENABLED (1)
38.00% + 17mV	40.60%	42.88% - 17mV	HIBW (0)	32-Bit Mode (1)	PIXEL REPETITION (1)	RCLKOUT DISABLED (0)
42.88% + 17mV	45.16%	47.58% - 17mV	HIBW (0)	32-Bit Mode (1)	PIXEL REPETITION (1)	RCLKOUT ENABLED (1)
47.58% + 17mV	50.00%	52.42% - 17mV	27-Bit Mode (1)	Don't Care (x)	NO REPETITION (0)	RCLKOUT DISABLED (0)
52.42% + 17mV	54.84%	57.12% - 17mV	27-Bit Mode (1)	Don't Care (x)	NO REPETITION (0)	RCLKOUT ENABLED (1)
57.12% + 17mV	59.40%	62.00% - 17mV	27-Bit Mode (1)	Don't Care (x)	PIXEL REPETITION (1)	RCLKOUT DISABLED (0)
62.00% + 17mV	64.60%	67.21% - 17mV	27-Bit Mode (1)	Don't Care (x)	PIXEL REPETITION (1)	RCLKOUT ENABLED (1)
67.21% + 17mV	69.83%	72.03% - 17mV	27-Bit Mode (1)	Don't Care (x)	NO REPETITION (0)	RCLKOUT DISABLED (0)
72.03% + 17mV	74.24%	76.77% - 17mV	27-Bit Mode (1)	Don't Care (x)	NO REPETITION (0)	RCLKOUT ENABLED (1)
76.77% + 17mV	79.30%	81.79% - 17mV	27-Bit Mode (1)	Don't Care (x)	PIXEL REPETITION	RCLKOUT DISABLED

					(1)	(0)
81.79% + 17mV	84.28%	86.63% - 17mV	27-Bit Mode (1)	Don't Care (x)	PIXEL REPETITION (1)	RCLKOUT ENABLED (1)

Notes:

a) Resistor divider tolerance, VDDIO supply ripple and external loading must not cause the CFG1 input voltage to exceed the maximum or minimum limit.

b) Other than the CFG1 input resistor divider, any load on CFG1 must be ≥ 25 x (R1 + R2).

c) HIBW: Selects 27-bit mode
BWS: Selects 32 Bit or 27 Bit mode when HIWB = 0, Don't Care when HIBW = 1
DRS: Low (pixel repetition) or High Data Rate (no pixel repetition)
RCLKEN: RCLOCK out enable or disable

Table 4. GMSL1 Effective PCLK Selection Table

GMSL1 or GMSL2 Mode	DRS BIT SETTING	BWS PIN SETTING	SOURCE PCLK FREQUENCY RANGE* (MHZ)
GMSL1	0 (high data rate)	Low (high bandwidth mode)	16.66 to 150
		High (32-bit mode)	12.5 to 112.5
GMSL1	1 (low data rate)	Low (high bandwidth mode)	8.33 to 16.66
		High (32-bit mode)	6.25 to 12.5