Qualcomm Technologies, Inc.

DragonBoard™ 410c based on Qualcomm® Snapdragon™ 410E processor

Android Display Overview

September 2016

Questions or comments: https://www.96boards.org/DragonBoard410c/forum

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LM80-P0436-10 Rev D

Revision history

Revision	Date	Description
D	September 2016	Update to ‘E’ part.
C	June 12, 2015	Miscellaneous updates
B	May 22, 2015	Updated Revision history and © date for Rev B.
A	May 6, 2015	Initial release

Contents

Figures

Tables

1 Introduction

1.1 Purpose

This document will familiarize you with the Qualcomm® Snapdragon™ 410E (APQ8016E) Linux Android™ display, including:

- Distinction between display-related hardware and software components.
- Display capabilities and performance benefits of the Multimedia Display Sub-System (MDSS).
- Control flow and data flow.
- Basic information on source code layout, build, and debugging.

1.2 Scope

This document provides an introduction to the Android display driver on the Qualcomm Technologies, Inc. APQ ASICs. This document is applicable to:

- Chipset – Snapdragon 410E (APQ8016E) processor
- Platform – Linux/Android

1.3 Display hardware in APQ8016E Android

- Provides hardware-accelerated image processing using MDSS architecture.
  - Up to four parallel processing pipes, two RGB pipes, one YUV pipe, and one DMA pipe.
  - Supports various image processing for each video and graphics surface.
- Kicks off image data to display interface.
  - MIPI DSI (in default use case Bridge chip ADV7533BCBZ converts DSI to HDMI).
  - Multiple mixers allows simultaneous update to primary and WFD.
- Enhances the image quality on the screen.
  - Post processing and color correction.
  - Panel calibration.

1.4 Display driver in APQ8016E Android

- Provides the optimized interface to access the hardware.
  - SurfaceFlinger, Hardware Composer (HWC), and overlay
  - Framebuffer driver
  - MIPI DSI interface

1.5 Acronyms, abbreviations, and terms

Table 1-1 provides definitions for the acronyms, abbreviations, and terms used in this document.

Table 1-1 Acronyms, abbreviations, and terms

Term	Definition
ABGR	Alpha Blue Green Red
API	Application Programming Interface
APQ	Application Processor Qualcomm
ARGB	Alpha Red Green Blue
BG	Blue Green
BGR	Blue Green Red
BGRA	Blue Green Red Alpha
CABL	Content Adaptive Backlight
CAF	C++ Actor Framework
DMA	Direct Memory Access
DSI	Display Serial Interface
DSP	Destination Surface Processor
DSPP	Destination Surface Processor Pipes
HAL	Hardware Abstraction Layer
HDMI	High Definition Multimedia Interface
HWC	Hardware Composer
IOCTL	Input/Output Control
LM	Layer Mixer
LUT	Look-Up Table
MDP	Mobile Development Platforms
MDSS	Multimedia Display Sub-System
MIPI	Mobile Industry Processor Interface
MSM	Mobile Station Modem
PCMN	Phase control M/N
RGB	Red Green Blue
RGBA	Red Green Blue Alpha
SMP	Simple Management Protocol
SSPP	Source Surface Processor Pipes

Term	Definition
SVI	Sunlight Visibility Improvement
WB	Wide Band
WFD	Wi-Fi Display

1.6 Additional information

For additional information, go to http://www.96boards.org/db410c-getting-started/.

2 System Architecture

2.1 MDSS 1.0 multimedia display subsystem overview

- Source Surface Processor (ViG, RGB, DMA - SSPP)
  - Format conversion and quality improvement for source surfaces (video, graphics, etc.)
- Layer Mixer (LM)
  - Blend and mix source surface together
- Destination Surface Processor (DSPP)
  - Conversion, correction, and adjustment based on panel characteristics
- Write-Back/Rotation (WB)
  - Write back to memory
  - Perform rotation if required
- Display interface
  - Timing generator and interface connecting the display peripheral

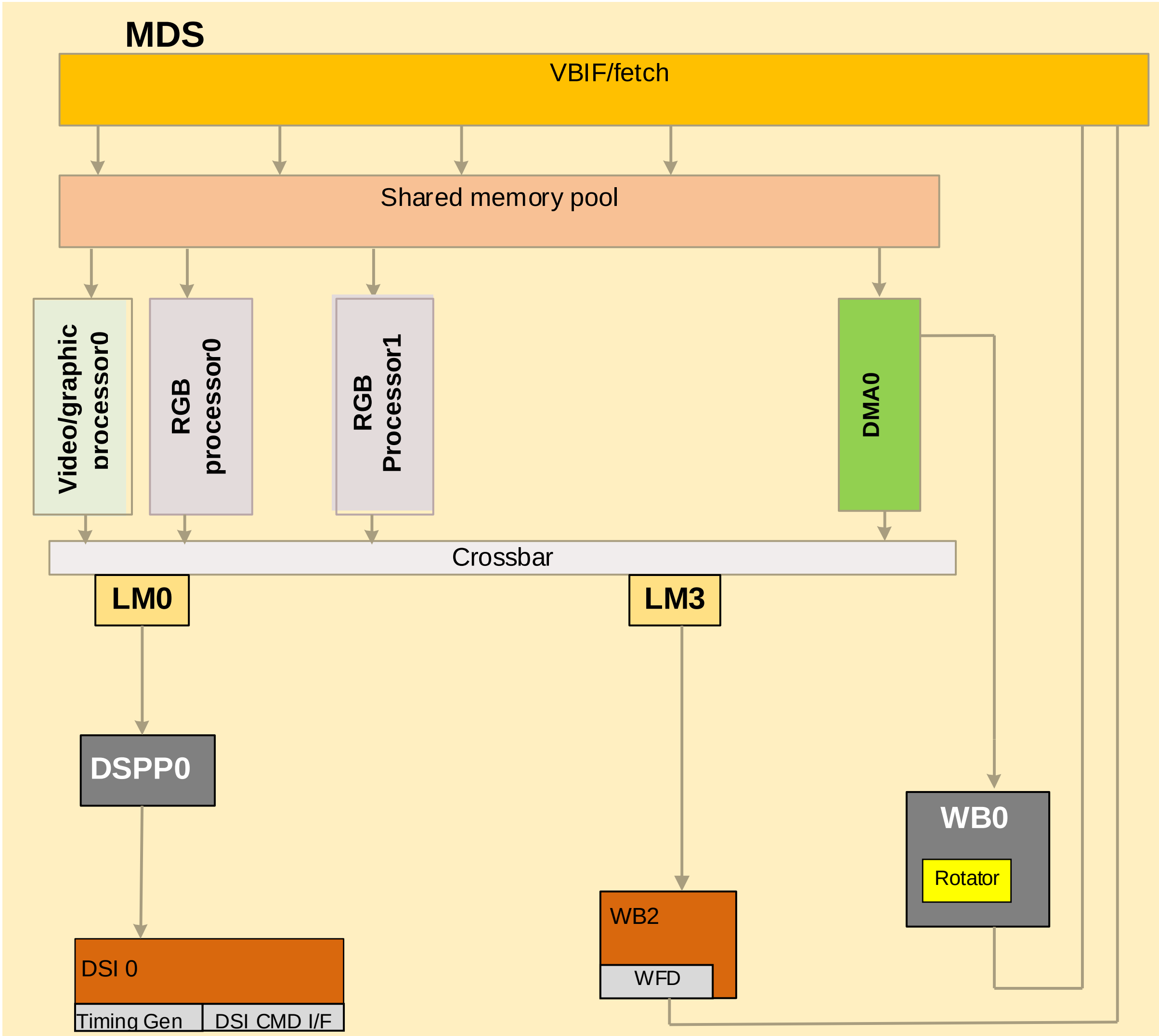
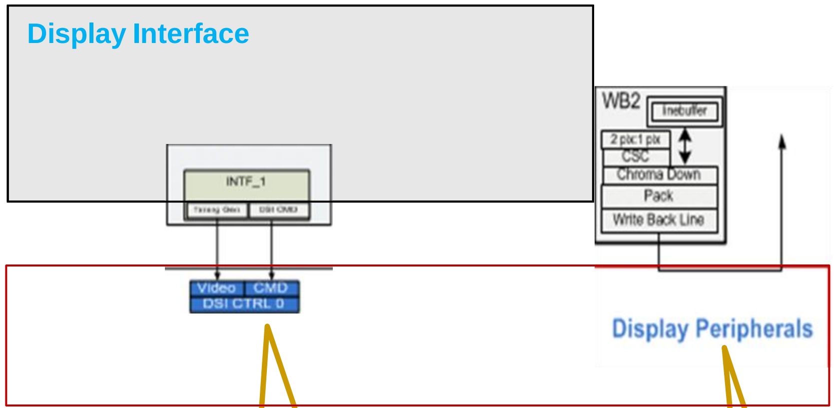


Figure 2-1 Display peripheral



MIPI DSI

- One MIPI DSI
- Supports both Video and Command modes
- Up to 1.5 Gbps per lane with 24 BPP support DATA+/-, CLK+/- (for 1-lane)
- Supports up to 1280 x 800 resolution with 60 fps

WFD

- 1280 x 720 @ 30 fps

Figure 2-2 MIPI DSI

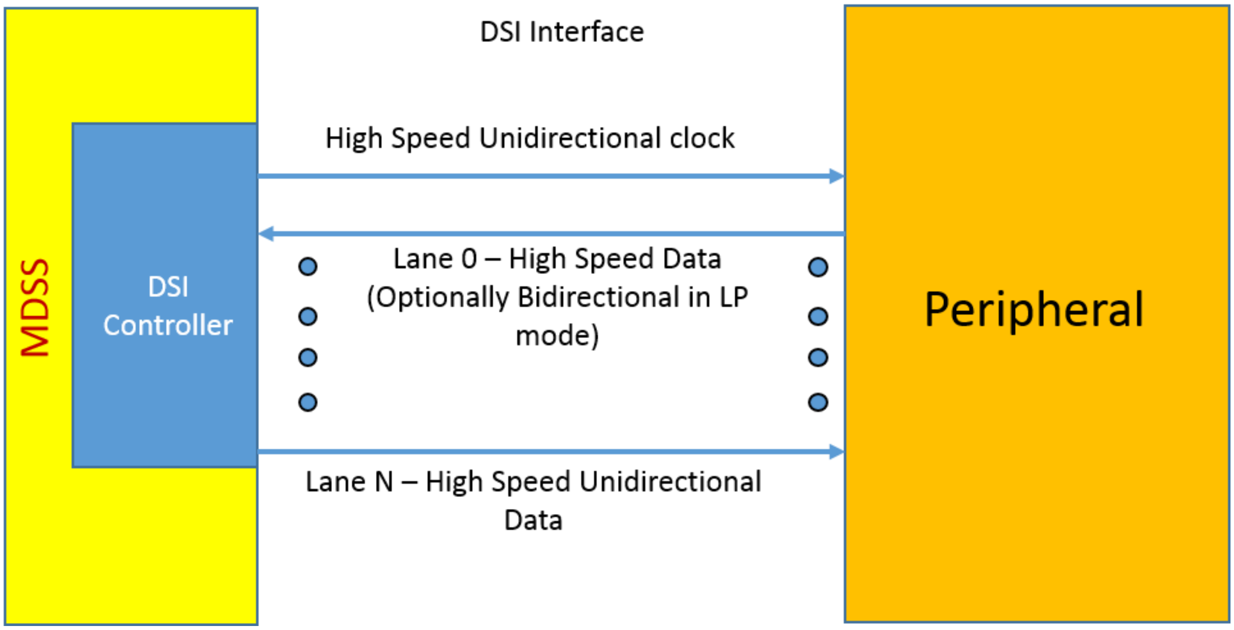


Figure 2-3 DSI interface

- The DSI controller is implemented to support the MIPI Alliance Standard for Display Serial Interface (DSI).
- The DSI controller includes one high-speed clock lane and one or more data lanes. Each lane is carried on two wires and uses low-voltage differential signaling.
- There are two modes of operations for DSI-compliant peripherals: Command mode and Video mode

3 Feature Overview

3.1 Supported interfaces

APQ8016E supports up to two concurrent displays:

- DSI up to 1200 x 800 @ 60 fps (in default use case Bridge chip ADV7533BCBZ converts DSI to HDMI)
- Wi-Fi display 1280 x 720 @ 30 fps

Table 3-1 Source Surface Processor Pipes (SSPP)

Feature	ViG	RGB	DMA
Number of pipes	1	2	1
	▪ 2s4-bit RGB (888) ▪ 16-bit RGB (565) ▪ 16-bit x/ARGB (4444,1555) ▪ 32-bit x/ARGB (8888) (with ARGB/RGBA/ABGR/BGRA and RGB/BGR permutation) ▪ YCbCr422 interleaved (YCrYCb, YCbYCr, CbYCrY, and CrYCbY) ▪ AYCrCb444 interleaved ▪ YCbCr420 pseudo planar (NV12 and NV21) ▪ YCbCr422 pseudo planar (H1V2 and H2V1) ▪ NV12/NV21 + alpha ▪ YCbCr422 pseudo planar + alpha ▪ YCbCr420 planar ▪ YCbCr422 planar	▪ 24-bit RGB (888) ▪ 16-bit RGB (565) ▪ 16-bit x/ARGB (4444 and 1555) ▪ 32-bit x/ARGB (8888) (with ARGB/RGBA/ABGR/BGR A, and RGB/BGR permutation)	▪ 24-bit RGB (888) ▪ 16-bit RGB (565) ▪ 16-bit x/ARGB (4444,1555) ▪ 32-bit x/ARGB (8888) (with ARGB/RGBA/ABGR/BGR A, and RGB/BGR permutation) ▪ YCbCr422 interleaved (YCrYCb, YCbYCr, CbYCrY, and CrYCbY) ▪ AYCrCb444 interleaved ▪ YCbCr420 pseudo planar (NV12 and NV21) ▪ YCbCr422 pseudo planar (H1V2 and H2V1) ▪ NV12/NV21 + alpha ▪ YCbCr422 pseudo planar + alpha ▪ YCbCr420 planar ▪ YCbCr422 planar
CSC	Yes	No	No
Content adaptive contrast enhancement	256-bin histogram 256-entry LUT	No	No
Flip	Vertical and horizontal flip		

Table 3-2 Layer mixer, BG color, and hardware cursor

Feature	DragonBoard 410C support
Number of layer mixers	2
Maximum number of surfaces blended	4 + BG color + hardware cursor
Total number of pipes for blending	4 (1ViG + 2 RGB + 1 DMA)
Alpha blending	Constant alpha, per pixel alpha, pre-multiplied alpha, modulation alpha. Reverse alpha for all the above.
Alpha blending for BG color	Yes
BG color generation	Yes (no data fetch for BG color)
Transparency color key	Source color key, destination color key, simultaneous source and destination color key, and color key range
Arbitrary blending order	Yes
Blending in linear space	Yes
Blending color depth	12-bits/component
Hardware cursor size	64 x 64

Table 3-3 Destination Surface Processor Pipes (DSPP)

Feature	DragonBoard 410C support
Sunlight Visibility Improvement (SVI)	Global tone mapping
Content Adaptive Backlight (CABL) scaling	256-bin histogram and 256-entry LUT
Panel color correction	3 x 11 polynomial
Bit-depth for color correction	12-bits/component
Gamma correction	3-channel LUT
Picture adjustment	Smooth curve, soft clip, memory, and 6-zone color adjustment
Dither	4 x 4 ordered dithering performed without panel depth reduction

Table 3-4 Rotator and WB

Feature	DragonBoard 410C support
Rotator	
Input format support	Same as ViG
Rotation modes	90, 180, 270°
WB	
Number of WBs	2 – WB0 and WB2
WB performance	WB0 – 1280 x 800 @ 60 fps and WB2 – 1280 x 720 @ 30 fps

Feature	DragonBoard 410C support
WB format	▪ 24-bit RGB (888) ▪ 16-bit RGB (565) ▪ 16-bit x/ARGB (4444 and 1555) ▪ 32-bit x/ARGB (8888) – With ARGB/RGBA/ABGR/BGRA and RGB/BGR permutation ▪ YCbCr420 pseudo planar (NV12 and NV21) ▪ YCbCr422 pseudo planar (H1V2 and H2V1) ▪ NV12 + alpha ▪ YCbCr422 pseudo planar + alpha ▪ YCbCr420 planar ▪ YCbCr422 planar

Table 3-5 Wireless display

Feature	DragonBoard 410C support
Number of WBs used	1 (WB2 with display processing)
WFD	WB2 – 720p at 30 fps
WFD possible formats	▪ 24-bit RGB (888) ▪ 16-bit RGB (565) ▪ 32-bit x/ARGB or BGRx/A(8888) ▪ YCbCr420 pseudo planar (NV12)
Composition	WB for the final composition surface and WB2 with hardware cursor

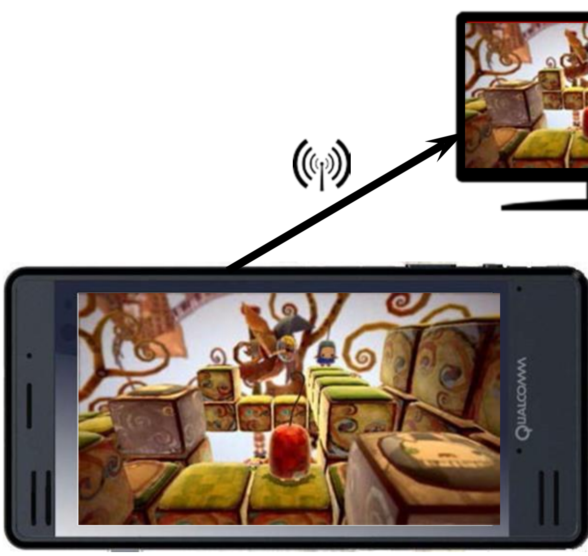


Figure 3-1 Display over WiFi

4 Display and Video Processing Features

Table 4-1 Scaling

Feature		ViG pipe	RGB pipe
Scaling	Scaling ratio	1/64-20x (decimation for <1/4)	No
	Upscaling filter	▪ 4-tap CAF (32 phases) ▪ 2-tap bilinear (32 phases) ▪ Nearest neighbor (32 phases)	No
	Downscaling filter	PCMN (8 phases)	No
Content Adaptive Filter (CAF) – Adjust filter coefficients based on content Phase control M/N (PCMN) – Phase control M/N. Fractional averaging filter for downscaling.			

5 APQ8016E Display Features

Table 5-1 Performance

Features	APQ8016E
Panel resolution	1200 x 800 @ 60 fps
Number of displays	2
External resolution	WFD – 1280 x 720 @ 30 fps
Maximum concurrency	1200 x 800 @ 60 primary + 1280 x 720 @ 30 WFD

Table 5-2 Image processing

Item	APQ8016E
Scaling	1/64 to 20x (Only VG pipe)
Composition layers	4 (1 ViG + 2 RGB + 1 DMA) + BG color + hardware cursor
SMP blocks	8 blocks of 8 KB
MDP clock	320 MHz

6 Software Architecture

6.1 Android display subsystem

- Android frameworks – Surface texture and SurfaceFlinger
- HALs – Overlay, graphics allocation, and hardware composer
- Primary panel interfaces – MIPI DSI
- External display – WFD
- MDP core – MDP drivers, overlay pipe management, clocks/power/performance
- Post processing and color management – CABL, color conversion, etc.

6.2 Composition

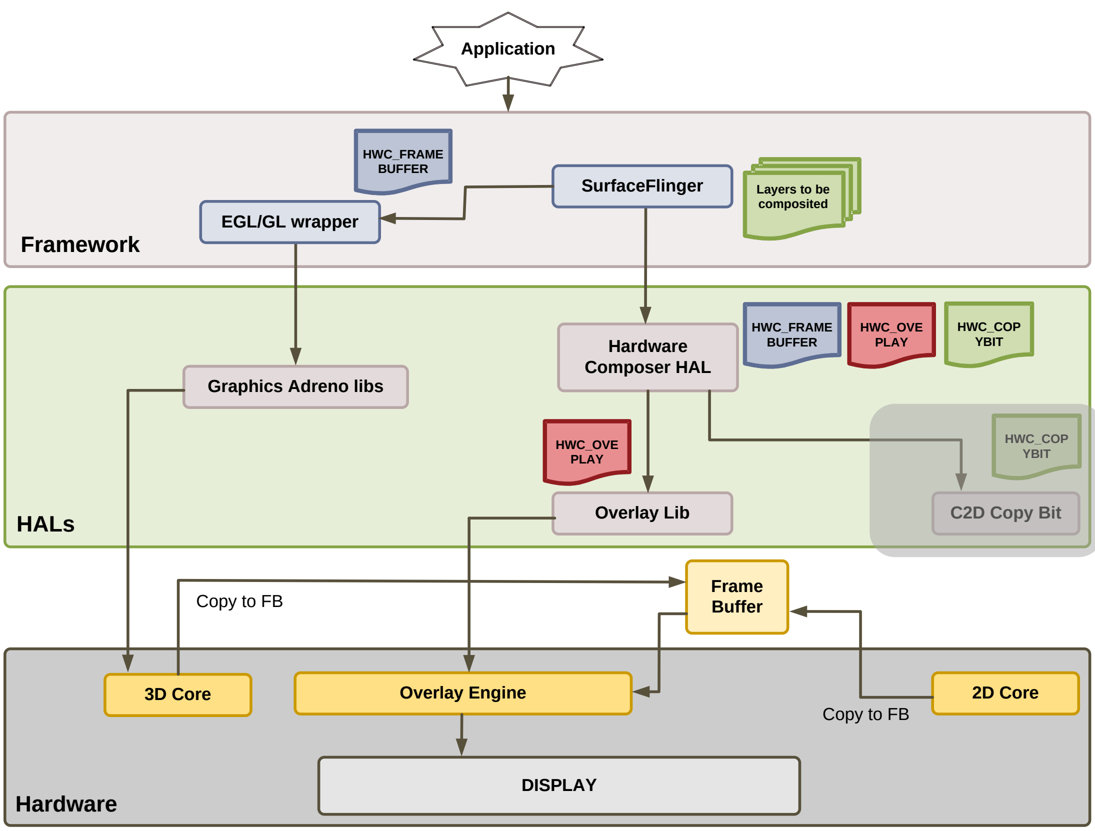


Figure 6-1 3D core overlay engine 2D core

6.3 MDSS driver software block diagram

- mdss_fb → Top-level IOCTL/native framebuffer interface
- mdss_mdp.c → MDP resources (clocks/irq/bus-bw/power)
- mdss_mdp_overlay → Overlay/DMA top-level API
- mdss_mdp_ctl → Controls the hardware abstraction to club the (LM + DSPP + Ping-pong + interface)
- mdss_mdp_pipe → SRC pipe related handling
- mdss_mdp_intf_cmd/mdss_mdp_intf_video/mdss_mdp_intf_writeback → MDP panel interface related handling
- mdss_mdp_pp → Postprocessing related implementation
- mdss_mdp_rotator → Rotator APIs (overlay_set/overlay_play interface)
- mdss_mdp_pp.c → Postprocessing related material

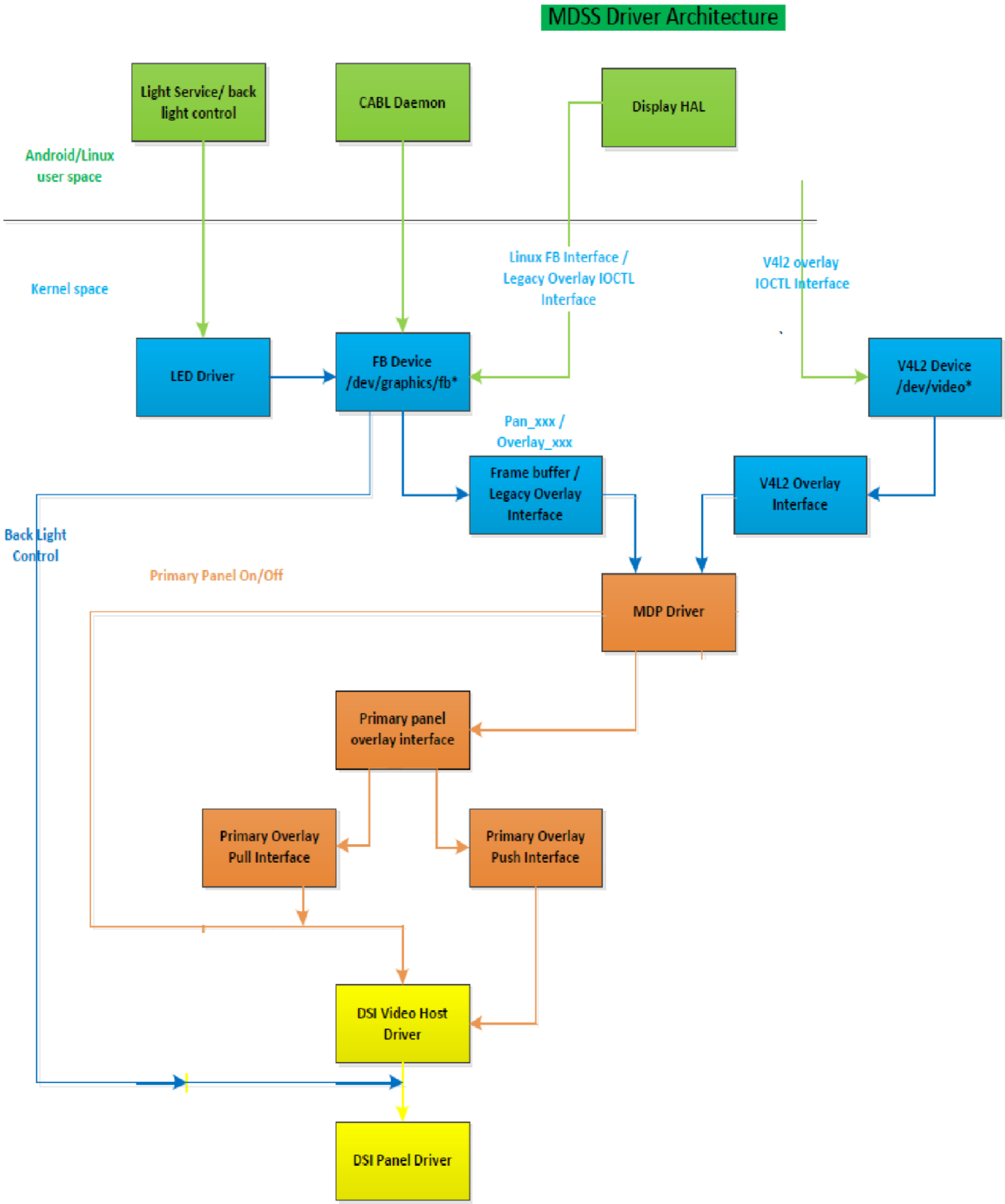


Figure 6-2 MDSS driver architecture

7 Source Code Layout

7.1 Software directory structure (userspace)

- SurfaceTexture – frameworks\native\libs\gui
- SurfaceFlinger – frameworks\native\services\surfaceflinger
- Overlay HAL – hardware\qcom\display\liboverlay
- Graphics alloc – hardware\qcom\display\libgralloc
- Hardware composer – hardware\qcom\display\libhwcomposer

7.2 Software directory structure (driver)

- MDSS driver – kernel\drivers\video\msm\mdss
    - Source surface process
        - mdss_mdp_overlay.c
        - mdss_mdp_pipe.c
- Layer Mixer
    - mdss_mdp_ctl.c
- Destination Surface Processor (DSP)
    - mdss_mdp_intf_cmd.c
    - mdss_mdp_intf_video.c
    - mdss_mdp_intf_writeback.c
    - mdss_mdp_rotator
- Display peripheral interface
    - mdss_dsi.c
    - mdss_dsi_host.c

8 Software Interface Structure (Userspace and Driver)

8.1 Support for standard IOCTLs of Android

- FBIOGET_VSCREENINFO – Gets variable information of framebuffer device
- FBIOPUT_VSCREENINFO – Put variable information of framebuffer device
- FBIOBLANK – Turns on/off framebuffer device (display on/off)
- FBIOPAN_DISPLAY – Updates display/framebuffer device with new image

8.2 Qualcomm added IOCTLs

- MSMFB_OVERLAY_GET – Gets overlay pipe/rotator information
- MSMFB_OVERLAY_SET – Sets parameters/allocating overlaypipe/rotator
- MSMFB_OVERLAY_UNSET – Closes pipe/rotator
- MSMFB_OVERLAY_PLAY_ENABLE – Controls overlay update
- MSMFB_OVERLAY_PLAY – Queues buffer to pipe
- MSMFB_OVERLAY_PLAY_WAIT – Waits for vsync
- MSMFB_CURSOR – Hardware cursor support
- MSMFB_SET_LUT – Gamma look up table setup for CABL
- MSMFB_HISTOGRAM – Reading histogram
- MSMFB_HISTOGRAM_START – Starting Histogram
- MSMFB_HISTOGRAM_STOP – Stopping Histogram

EXHIBIT 1

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