



512Mb, 1.8V Xccela Flash Memory Features

Micron Xccela™ Flash Memory

1.8V, Octal I/O, 4KB, 32KB, 128KB, Sector Erase

MT35XU512ABA

Features

- SPI-compatible Xccela™ bus interface
 - Octal DDR protocol
 - Extended-SPI protocol with octal commands
- Single and double transfer rate (SDR/DDR)
- Clock frequency
 - 166 MHz (MAX) in SDR (166 MB/s)
 - 200 MHz (MAX) in DDR (400 MB/s) with DQS
- Execute-in-place (XIP)
- PROGRAM/ERASE SUSPEND operations
- Volatile and nonvolatile configuration settings
- Software reset
- Reset pin available
- 3-byte and 4-byte address modes – enable memory access beyond 128Mb
- Dedicated 64-byte OTP area outside main memory
 - Readable and user-lockable
 - Permanent lock with PROGRAM OTP command
- Erase capability
 - Bulk erase
 - Sector erase 128KB uniform granularity
 - Subsector erase 4KB, 32KB granularity
- Security and write protection
 - Volatile and nonvolatile locking and software write protection for each 128KB sector
 - Nonvolatile configuration locking
 - Password protection
 - Protection Management Register offering enhanced security features
 - Hardware write protection: nonvolatile bits (BP[3:0] and TB) define protected area size
 - Program/erase protection during power-up
 - CRC detects accidental changes to raw data
- Electronic signature
 - JEDEC-standard 3-byte signature
 - Extended device ID: two additional bytes identify device factory options
- JESD47I-compliant
 - Minimum 100,000 ERASE cycles per sector
 - Data retention: 20 years (TYP)

Options

- Voltage
 - 1.7–2.0V
- Density
 - 512Mb
- Device stacking
 - Monolithic
- Device Generation
 - B
- Die revision
 - A
- Configuration
 - Boot in SDR ×1
 - Boot in DDR ×8
- Sector Size
 - 128KB
- Packages – JEDEC-standard, RoHS-compliant
 - 24-ball T-PBGA 05/6mm × 8mm (5 × 5 array)
- Security features
 - Standard security
- Special options
 - Standard
 - Automotive
- Operating temperature range
 - From –40°C to +85°C
 - From –40°C to +105°C

Marking

U

512

A

B

A

1

2

G

12

0

S

A

IT

AT

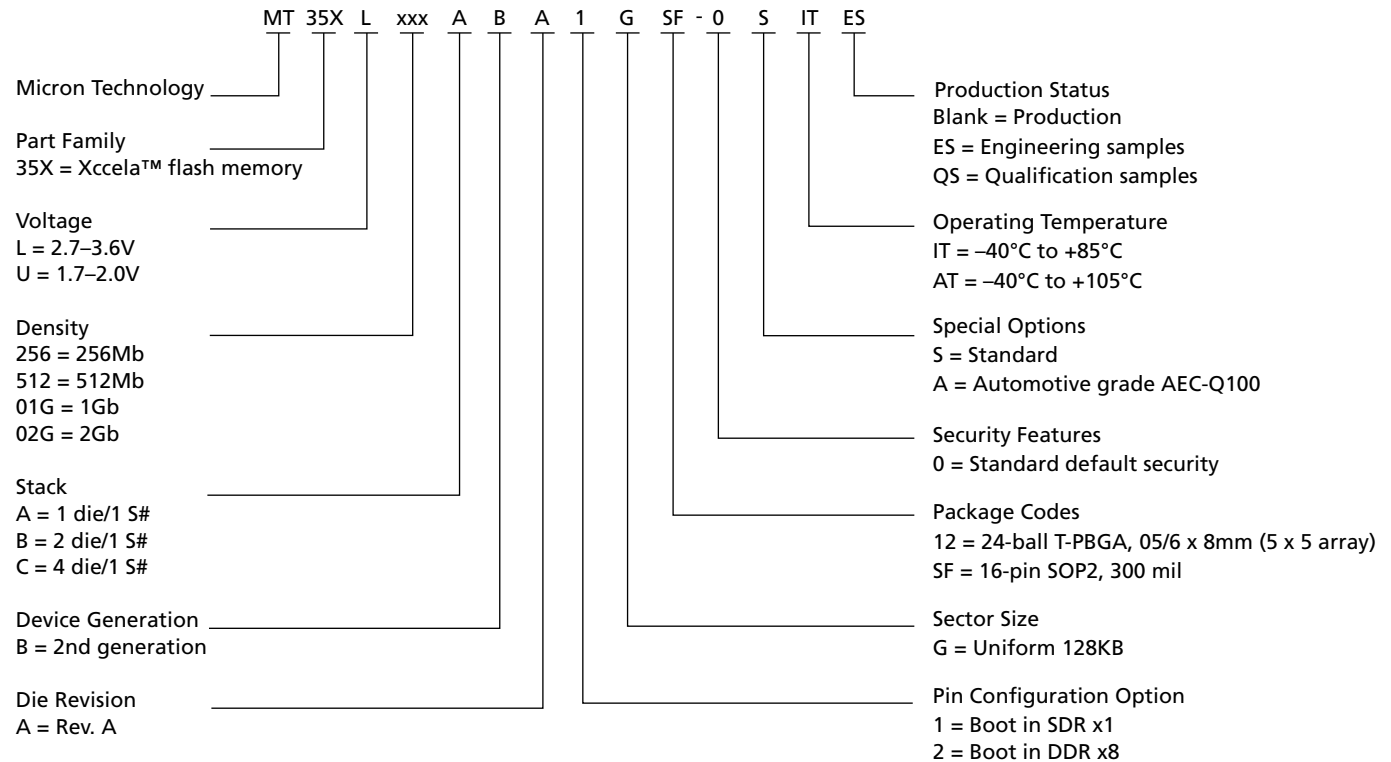


512Mb, 1.8V Xcela Flash Memory Features

Part Number Ordering

Micron Xcela flash devices are available in different configurations and densities. Verify valid part numbers by using Micron's part catalog search at www.micron.com. To compare features and specifications by device type, visit www.micron.com/products. Contact the factory for devices not found.

Figure 1: Part Number Ordering Information





512Mb, 1.8V Xccela Flash Memory Features

Contents

Device Description	7
Block Diagram	8
Device Logic Diagram	9
Advanced Security Protection	9
Signal Assignments	10
Signal Descriptions	11
Package Dimensions – Package Code: 12	12
Memory Map – 512Mb Density	13
Status Register	14
Block Protection Settings	15
Flag Status Register	16
Internal Configuration Register	17
Nonvolatile Configuration Register	18
Volatile Configuration Register	20
Supported Clock Frequencies	21
Data Sequence Wraps by Density	22
Security Registers	23
Sector Protection Security Register	24
Nonvolatile and Volatile Sector Lock Bits Security	25
Nonvolatile Lock Bit Security Register	26
Volatile Lock Bit Security Register	26
Protection Management Register	27
Protection Management Register Operations	28
Device ID Data	29
Serial Flash Discovery Parameter Data	30
Command Definitions	31
Software RESET Operations	34
RESET ENABLE and RESET MEMORY Commands	34
READ ID Operation	35
READ ID Command	35
READ SERIAL FLASH DISCOVERY PARAMETER Operation	36
READ SERIAL FLASH DISCOVERY PARAMETER Command	36
READ MEMORY Operations	37
4-BYTE READ MEMORY Operations	37
READ MEMORY Operations Timings	38
WRITE ENABLE/DISABLE Operations	41
READ REGISTER Operations	42
WRITE REGISTER Operations	43
CLEAR FLAG STATUS REGISTER Operation	44
PROGRAM Operations	45
4-BYTE PROGRAM Operations	46
PROGRAM Operations Timings	47
ERASE Operations	48
SUSPEND/RESUME Operations	50
PROGRAM/ERASE SUSPEND Operations	50
PROGRAM/ERASE RESUME Operations	50
ONE-TIME PROGRAMMABLE Operations	52
READ OTP ARRAY Command	52
PROGRAM OTP ARRAY Command	52
ADDRESS MODE Operations	54



512Mb, 1.8V Xccela Flash Memory Features

ENTER and EXIT 4-BYTE ADDRESS MODE Command	54
CYCLIC REDUNDANCY CHECK Operations	55
State Table	57
XIP Mode	58
Activate or Terminate XIP Using Volatile Configuration Register	58
Activate or Terminate XIP Using Nonvolatile Configuration Register	58
Confirmation Bit Settings Required to Activate or Terminate XIP	59
Terminating XIP After a Controller and Memory Reset	60
Power-Up and Power-Down	60
Power-Up and Power-Down Requirements	60
Power Loss and Interface Rescue	62
First Step – Power Loss Recovery and Interface Rescue	62
Second Step – Power Loss Recovery	62
Second Step – Interface Rescue	62
Initial Delivery Status	63
Absolute Ratings and Operating Conditions	64
DC Characteristics and Operating Conditions	66
AC Characteristics and Operating Conditions	68
AC Reset Specifications	70
Program/Erase Specifications	74
Revision History	75
Rev. F – 06/17	75
Rev. E – 12/16	75
Rev. D – 08/16	75
Rev. C – 01/16	75
Rev. B – 10/15	75
Rev. A – 04/15	75



512Mb, 1.8V Xcelera Flash Memory Features

List of Figures

Figure 1: Part Number Ordering Information	2
Figure 2: Block Diagram – Components and Signals	8
Figure 3: Logic Diagram	9
Figure 4: 24-Ball TBGA, 5 × 5 (Balls Down)	10
Figure 5: 24-Ball T-PBGA (5 × 5 ball grid array) – 6mm × 8mm	12
Figure 6: Internal Configuration Register	17
Figure 7: Sector and Password Protection	23
Figure 8: RESET ENABLE and RESET MEMORY – 66h and 99h	34
Figure 9: READ ID Command	35
Figure 10: READ SERIAL FLASH DISCOVERY PARAMETER Command – 5Ah	36
Figure 11: READ – 03h/13h ²	38
Figure 12: FAST READ – 0Bh/0Ch ³	38
Figure 13: OCTAL OUTPUT FAST READ – 8Bh/7Ch ³	39
Figure 14: OCTAL I/O FAST READ – CBh/CCh ³	39
Figure 15: OCTAL OUTPUT FAST READ with DDR ADDRESS and DATA – 9Dh	40
Figure 16: OCTAL I/O FAST READ with DDR ADDRESS and DATA – FDh	40
Figure 17: WRITE ENABLE and WRITE DISABLE Timing	41
Figure 18: READ STATUS REGISTER – 05h	42
Figure 19: READ CONFIGURATION REGISTER – B5h/85h	43
Figure 20: WRITE STATUS REGISTER – 01h	44
Figure 21: WRITE CONFIGURATION REGISTER – B1h/81h	44
Figure 22: CLEAR FLAG STATUS REGISTER Timing	45
Figure 23: PAGE PROGRAM – 02h/12h	47
Figure 24: OCTAL INPUT FAST PROGRAM – 82h/84h	47
Figure 25: EXTENDED OCTAL INPUT FAST PROGRAM – C2h/8Eh	47
Figure 26: SUBSECTOR and SECTOR ERASE Timing	49
Figure 27: BULK ERASE Timing	49
Figure 28: PROGRAM/ERASE SUSPEND or RESUME Timing	51
Figure 29: READ OTP Command	52
Figure 30: PROGRAM OTP Command	53
Figure 31: XIP Mode Entered at Power-On	58
Figure 32: XIP Mode Entry by Volatile Configuration Register	59
Figure 33: Power-Up Timing	61
Figure 34: AC Timing I/O Reference Levels	65
Figure 35: Reset AC Timing During PROGRAM or ERASE Cycle	71
Figure 36: Serial Input Timing	71
Figure 37: Serial Input Timing – DDR	71
Figure 38: Write Protect Setup and Hold During WRITE STATUS REGISTER Operation (SRWD = 1)	72
Figure 39: Output Timing – SDR	72
Figure 40: Output Timing – DDR	72
Figure 41: Output Timing – DDR with DQS	73
Figure 42: V _{PPH} Timing	73



512Mb, 1.8V Xccela Flash Memory Features

List of Tables

Table 1: Signal Descriptions	11
Table 2: Sectors[511:0]	13
Table 3: Status Register	14
Table 4: Protected Area – 128KB Sectors	15
Table 5: Flag Status Register	16
Table 6: Nonvolatile Configuration Register	18
Table 7: Volatile Configuration Register	20
Table 8: Clock Frequencies – SDR and DDR Read Starting at Any Byte Address	21
Table 9: Clock Frequencies – SDR and DDR Read 4-Byte Aligned	22
Table 10: Sequence of Bytes During Wrap	22
Table 11: Sector Protection Register	24
Table 12: Global Freeze Bit	24
Table 13: Nonvolatile and Volatile Lock Bits	25
Table 14: Nonvolatile Lock Bit Register	26
Table 15: Volatile Lock Bit Register	26
Table 16: Protection Management Register	27
Table 17: Protection Management Register Operations	28
Table 18: Device ID Data	29
Table 19: Extended Device ID Data, First Byte	29
Table 20: Device Configuration Information Data	29
Table 21: Command Set	31
Table 22: RESET ENABLE and RESET MEMORY Operations	34
Table 23: READ ID Operation	35
Table 24: READ MEMORY Operations	37
Table 25: 4-BYTE READ MEMORY Operations	37
Table 26: WRITE ENABLE/DISABLE Operations	41
Table 27: READ REGISTER Operations	42
Table 28: WRITE REGISTER Operations	43
Table 29: CLEAR FLAG STATUS REGISTER Operation	44
Table 30: PROGRAM Operations	46
Table 31: 4-BYTE PROGRAM Operations	46
Table 32: ERASE Operations	48
Table 33: SUSPEND/RESUME Operations	50
Table 34: OTP Control Byte (Byte 64)	53
Table 35: ENTER and EXIT 4-BYTE ADDRESS MODE Operations	54
Table 36: CRC Command Sequence on Entire Device	55
Table 37: CRC Command Sequence on a Range	56
Table 38: Operations Allowed/Disallowed During Device States	57
Table 39: XIP Confirmation Bit	59
Table 40: Effects of Running XIP in Different Protocols	59
Table 41: Power-Up Timing and V_{WI} Threshold	61
Table 42: Absolute Ratings	64
Table 43: Operating Conditions	64
Table 44: I/O Capacitance	64
Table 45: AC Timing I/O Conditions	65
Table 46: DC Current Characteristics and Operating Conditions	66
Table 47: DC Voltage Characteristics and Operating Conditions	67
Table 48: AC Characteristics and Operating Conditions	68
Table 49: AC Reset Conditions	70
Table 50: Program/Erase Specifications	74



512Mb, 1.8V Xccela Flash Memory Device Description

Device Description

The Micron Xccela flash is a high-performance, multiple I/O, SPI-compatible flash memory device. It features a high-speed, low pin count Xccela bus interface with a DDR clock frequency of up to 200 MHz for 1.8V parts and up to 133 MHz for 3.0 V parts, using eight I/O signals and a data strobe (DQS pin).

SUSPEND and RESUME commands provide the ability to pause and resume PROGRAM/ERASE operations. Nonvolatile and volatile configuration registers enable respective default and temporary settings such as READ operation dummy clock cycles and wrap modes, memory protection, output buffer impedance, SPI protocol type, and XiP mode.

Memory is organized as uniform 128KB sectors, 4KB and 32KB sub-sectors, and 256 byte pages. The device also includes a 64-byte one-time-programmable (OTP) memory area that can be permanently locked.

Direct boot in octal DDR protocol provides high performance and ease of use, enabling communication between the host and flash device without need to configure extended SPI protocol operations. However, the device still supports both extended SPI and octal DDR protocols to ensure legacy system support and an easy migration path. The extended SPI protocol supports address and data transmission on one or eight data lines, depending on the command.

Note: XiP feature is supported in extended-SPI because its commands are sent through DQ0 only.

Information in octal DDR protocol is always transmitted by eight data lines on both rising and falling clock edges. Most legacy x1 SPI commands are supported, but require only one clock cycle because the command is latched on both the rising and falling edges of the clock. Address cycles are fixed at 4-byte READ operations from the flash array.

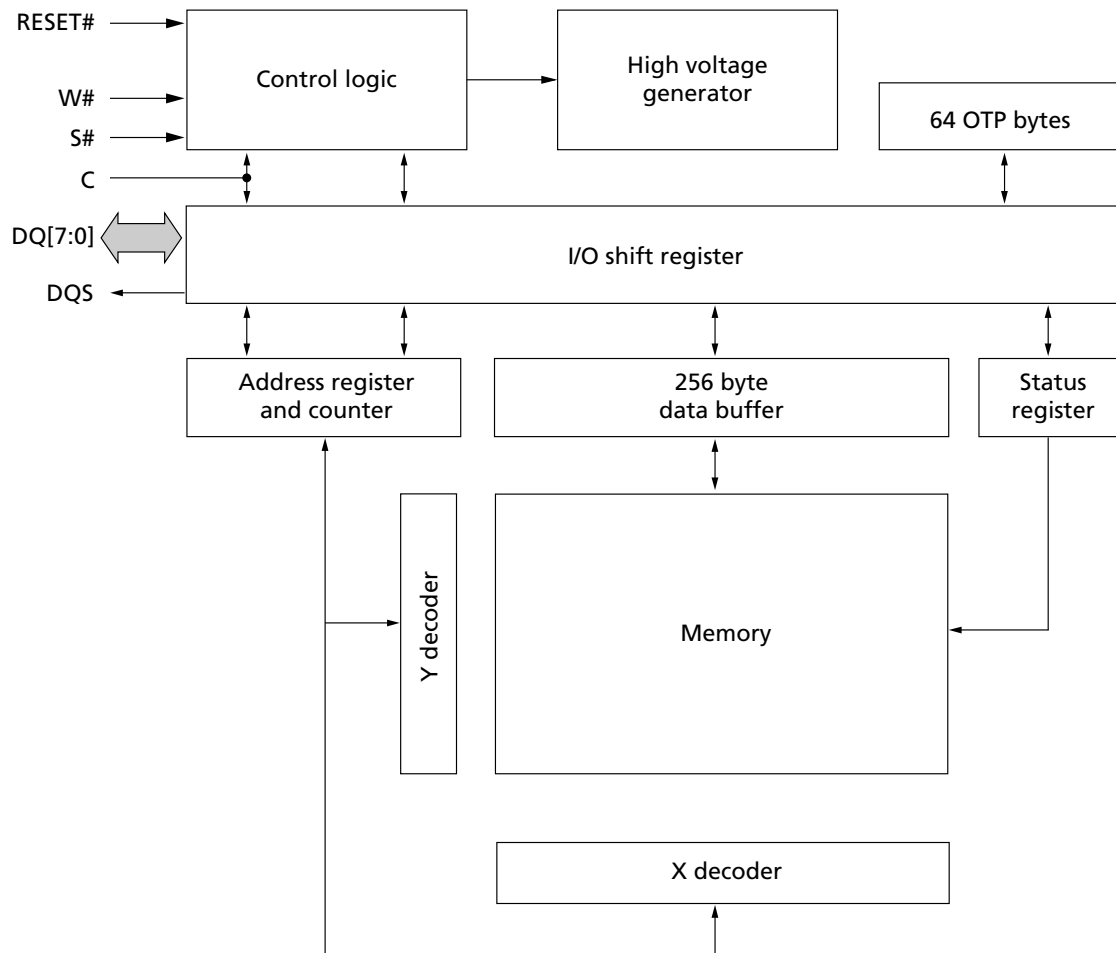
The host does not need to drive DQS during the input operation to the memory. The data input (DQ) to the memory still relies on clock (C) to latch all address and data operations. Most register outputs require dummy clock cycles due to the critical timing from command decoding. With the help of DQS for data latching, the number of dummy clocks is transparent to the host.



512Mb, 1.8V Xcela Flash Memory Device Description

Block Diagram

Figure 2: Block Diagram – Components and Signals



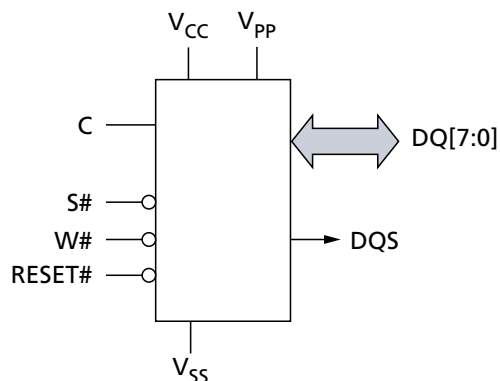
Note: 1. Each page of memory can be individually programmed, but the device is not page-erasable.



512Mb, 1.8V Xccela Flash Memory Device Description

Device Logic Diagram

Figure 3: Logic Diagram



Advanced Security Protection

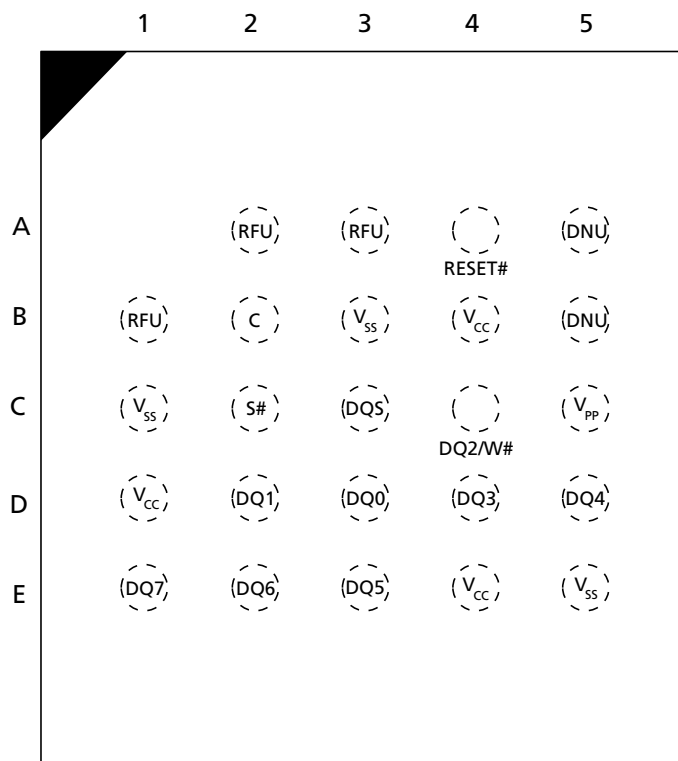
The device offers an advanced security protection scheme where each sector can be independently locked, by either volatile or nonvolatile locking features. The nonvolatile locking configuration can also be locked, as well password-protected. See Block Protection Settings and Sector and Password Protection for more details.



512Mb, 1.8V Xcelera Flash Memory Signal Assignments

Signal Assignments

Figure 4: 24-Ball TBGA, 5 × 5 (Balls Down)



Note: 1. See Part Number Ordering Information for complete package names and details.



512Mb, 1.8V Xccela Flash Memory Signal Descriptions

Signal Descriptions

The table below is a comprehensive list of device signals. All signals listed may not be supported. See Signal Assignments for device-specific information.

Table 1: Signal Descriptions

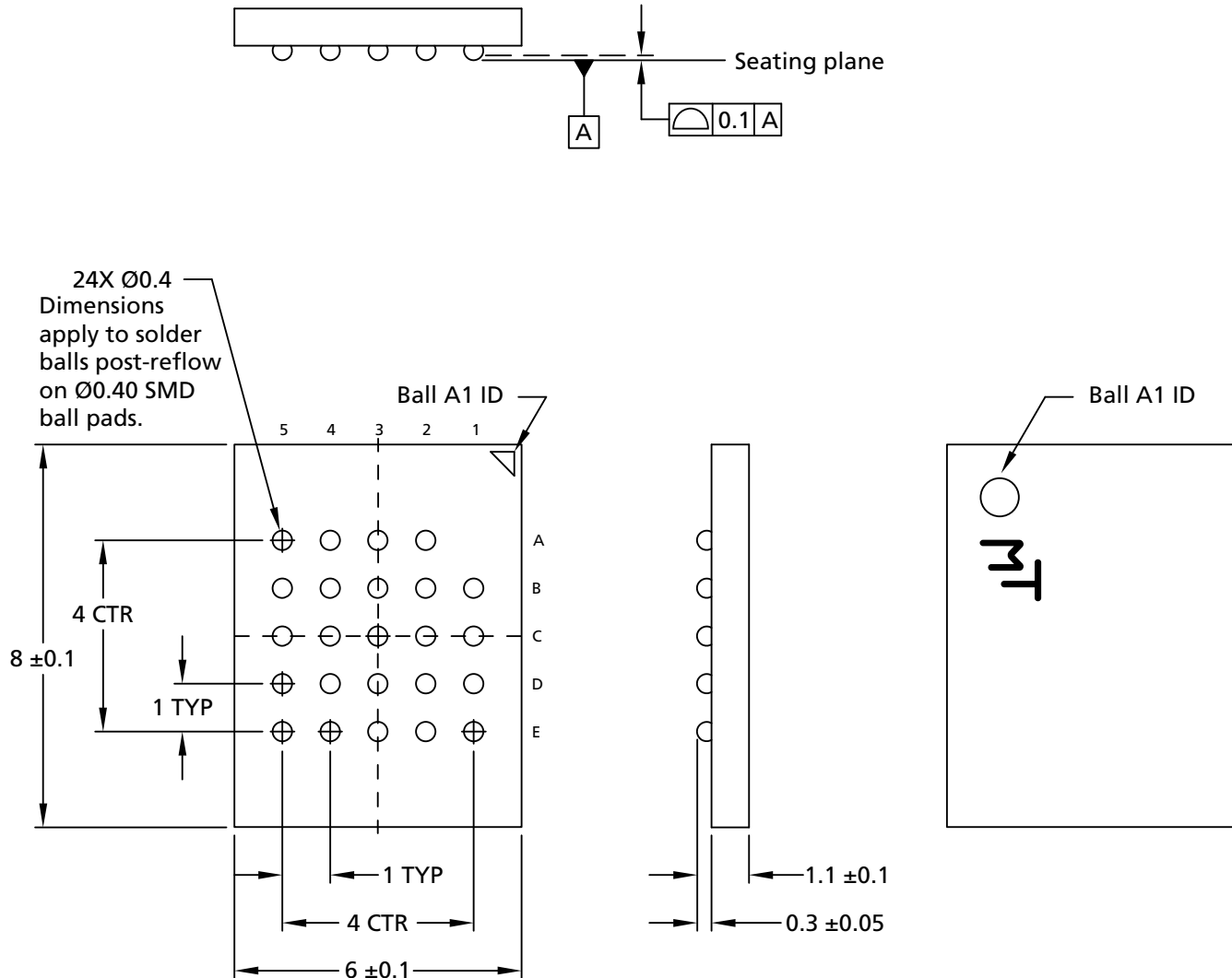
Symbol	Type	Description
C	Input	Clock: Provides timing for the serial interface. Command, address, or data inputs are latched on the rising edge of C. Data is shifted out on the falling edge of C.
S#	Input	Chip select: When S# is LOW, device is selected and in active power mode. Operations are initiated on the falling edge of S#. When S# is HIGH, device is deselected, DQ pins are tri-stated, and unless an internal WRITE operation is in progress, device enters standby mode.
RESET#	Input	RESET: Resets device to its default settings, such as after a volatile configuration register setting which then requires a return to the device default setting. Reset is optional when device settings are fixed by nonvolatile configuration register settings and always synchronized with the host. This pad is internally tied to weak pull-up so the pin can be floated.
W#	Input	Write protect: This input signal is used to freeze the status register in conjunction with the enable/disable bit of the status register. When the enable/disable bit of the status register is set to 1 and the W# signal is driven LOW, the status register nonvolatile bits become read-only and the WRITE STATUS REGISTER operation will not be executed. During the extended-SPI protocol with OCTAL READ/PROGRAM instructions, and during octal DDR protocol, this pin functions are an input/output (DQ2 functionality). This signal does not have internal pull-ups, it should not be left floated and must be driven, even if none of W#/DQ2 function is used.
DQ[7:0]	I/O	Serial I/O: Bidirectional signals that transfer address, data, and command information. In extended-SPI protocol, DQ0 functions as input and DQ1 as output. DQ[7:2] are not used. In octal protocol, input/output on DQ[7:0] depends on the command. Input can be latched on the rising edge of C (SDR) or on both edges of C (DDR). Data can be shifted out on the falling edge of C (SDR) or on both edges of C (DDR). In octal DDR, DQ[7:0] always function as I/O, input is latched on both edges of C, and output is shifted out on both edges of C. DQ2 is used also as write protection control.
DQS	Output	Data strobe: Indicates output data valid for DDR modes and is required to support high speed data output. Not required in extended-SPI protocol except to achieve high frequency for specific DDR commands. Used for READ but not for WRITE operations. Configured by nonvolatile and volatile configuration register bit 5 at address 00h. When enabled, DQS is driven to ground at S# LOW and until the device is driving output data, in which case DQS toggles to synchronize data output. When not enabled, DQS is not driven.
V _{CC}	Supply	Supply voltage: Core and I/O supply.
V _{PP}	Supply	Supply voltage: If V _{PP} is in the voltage range of V _{PPH} , the signal acts as an additional power supply for programming operation, as defined in the Operating Conditions table. The V _{PP} pad will be internally pulled up to V _{CC} , so customer can leave V _{PP} pin floated if not used.
V _{SS}	Supply	Ground: Core and I/O ground connection. V _{SS} is the reference for the V _{CC} supply voltage.
DNU	–	Do not use: Must be left floating.
RFU	–	Reserved for future use: Must be left floating.



512Mb, 1.8V Xcelera Flash Memory Package Dimensions – Package Code: 12

Package Dimensions – Package Code: 12

Figure 5: 24-Ball T-PBGA (5 × 5 ball grid array) – 6mm × 8mm



- Notes: 1. All dimensions are in millimeters.
2. See Part Number Ordering Information for complete package names and details.



512Mb, 1.8V Xccela Flash Memory Memory Map – 512Mb Density

Memory Map – 512Mb Density

Table 2: Sectors[511:0]

Sector	Subsector (4KB)	Address Range	
		Start	End
511	16,383	03FF F000h	03FF FFFFh
	⋮	⋮	⋮
	16,353	03FE 1000h	03FE 1FFFh
	16,352	03FE 0000h	03FE 0FFFh
⋮	⋮	⋮	⋮
1	63	0003 F000h	0003 FFFFh
	⋮	⋮	⋮
	33	0002 1000h	0002 1FFFh
	32	0002 0000h	0002 0FFFh
0	31	0001 F000h	0001 FFFFh
	⋮	⋮	⋮
	1	0000 1000h	0000 1FFFh
	0	0000 0000h	0000 0FFFh



512Mb, 1.8V Xcelera Flash Memory Status Register

Status Register

Status register bits can be read from or written to using READ STATUS REGISTER or WRITE STATUS REGISTER commands, respectively. When the status register enable/disable bit (bit 7) is set to 1 and W# is driven LOW, the status register nonvolatile bits become read-only and the WRITE STATUS REGISTER operation will not execute. The only way to exit this hardware-protected mode is to drive W# HIGH.

Table 3: Status Register

Bit	Name	Settings	Description	Notes
7	Status register write enable/disable	0 = Enabled (Default) 1 = Disabled	Nonvolatile control bit: Used with W# to enable or disable writing to the status register.	
5	Top/bottom	0 = Top (Default) 1 = Bottom	Nonvolatile control bit: Determines whether the protected memory area defined by the block protect bits starts from the top or bottom of the memory array.	
6, 4:2	BP[3:0]	See Protected Area tables	Nonvolatile control bit: Defines memory to be software protected against PROGRAM or ERASE operations. When one or more block protect bits is set to 1, a designated memory area is protected from PROGRAM and ERASE operations.	1
1	Write enable latch	0 = Clear (Default) 1 = Set	Volatile control bit: The device always powers up with this bit cleared to prevent inadvertent WRITE, PROGRAM, or ERASE operations. To enable these operations, the WRITE ENABLE operation must be executed first to set this bit.	
0	Write in progress	0 = Ready (Default) 1 = Busy	Volatile status bit: Indicates if one of the following command cycles is in progress: WRITE STATUS REGISTER WRITE NONVOLATILE CONFIGURATION REGISTER PROGRAM ERASE	2

- Notes:
1. The BULK ERASE command is executed only if all bits = 0.
 2. Status register bit 0 is the inverse of flag status register bit 7.



512Mb, 1.8V Xcela Flash Memory Status Register

Block Protection Settings

Table 4: Protected Area – 128KB Sectors

Status Register Content					Protected Area	Unprotected Area
Top/Bottom	BP3	BP2	BP1	BP0		
0	0	0	0	0	None	0:511
0	0	0	0	1	511	0:510
0	0	0	1	0	510:511	0:509
0	0	0	1	1	508:511	0:507
0	0	1	0	0	504:511	0:503
0	0	1	0	1	496:511	0:495
0	0	1	1	0	480:511	0:479
0	0	1	1	1	448:511	0:447
0	1	0	0	0	384:511	0:383
0	1	0	0	1	256:511	0:255
0	1	0	1	0	0:511	None
0	1	0	1	1	0:511	None
0	1	1	0	0	0:511	None
0	1	1	0	1	0:511	None
0	1	1	1	0	0:511	None
0	1	1	1	1	0:511	None
1	0	0	0	0	None	0:511
1	0	0	0	1	0	1:511
1	0	0	1	0	0:1	2:511
1	0	0	1	1	0:3	4:511
1	0	1	0	0	0:7	8:511
1	0	1	0	1	0:15	16:511
1	0	1	1	0	0:31	32:511
1	0	1	1	1	0:63	64:511
1	1	0	0	0	0:127	128:511
1	1	0	0	1	0:255	256:511
1	1	0	1	0	0:511	None
1	1	0	1	1	0:511	None
1	1	1	0	0	0:511	None
1	1	1	0	1	0:511	None
1	1	1	1	0	0:511	None
1	1	1	1	1	0:511	None
1	1	1	1	1	0:511	None



512Mb, 1.8V Xcela Flash Memory Flag Status Register

Flag Status Register

Flag status register bits are read by using READ FLAG STATUS REGISTER command. All bits are volatile and are reset to zero on power-up.

Status bits are set and reset automatically by the internal controller. Error bits must be cleared through the CLEAR STATUS REGISTER command.

Table 5: Flag Status Register

Bit	Name	Settings	Description
7	Program or erase controller	0 = Busy 1 = Ready	Status bit: Indicates whether one of the following command cycles is in progress: WRITE STATUS REGISTER, WRITE NONVOLATILE CONFIGURATION REGISTER, PROGRAM, or ERASE.
6	Erase suspend	0 = Clear 1 = Suspend	Status bit: Indicates whether an ERASE operation has been or is going to be suspended.
5	Erase	0 = Clear 1 = Failure or protection error	Error bit: Indicates whether an ERASE operation has succeeded or failed.
4	Program	0 = Clear 1 = Failure or protection error	Error bit: Indicates whether a PROGRAM operation has succeeded or failed. It indicates, also, whether a CRC check has succeeded or failed.
3	Reserved	0	Reserved
2	Program suspend	0 = Clear 1 = Suspend	Status bit: Indicates whether a PROGRAM operation has been or is going to be suspended.
1	Protection	0 = Clear 1 = Failure or protection error	Error bit: Indicates whether an ERASE or PROGRAM operation has attempted to modify the protected array sector, or whether a PROGRAM operation has attempted to access the locked OTP space.
0	Addressing	0 = 3-byte addressing 1 = 4-byte addressing	Status bit: Indicates whether 3-byte or 4-byte address mode is enabled.



512Mb, 1.8V Xcela Flash Memory Internal Configuration Register

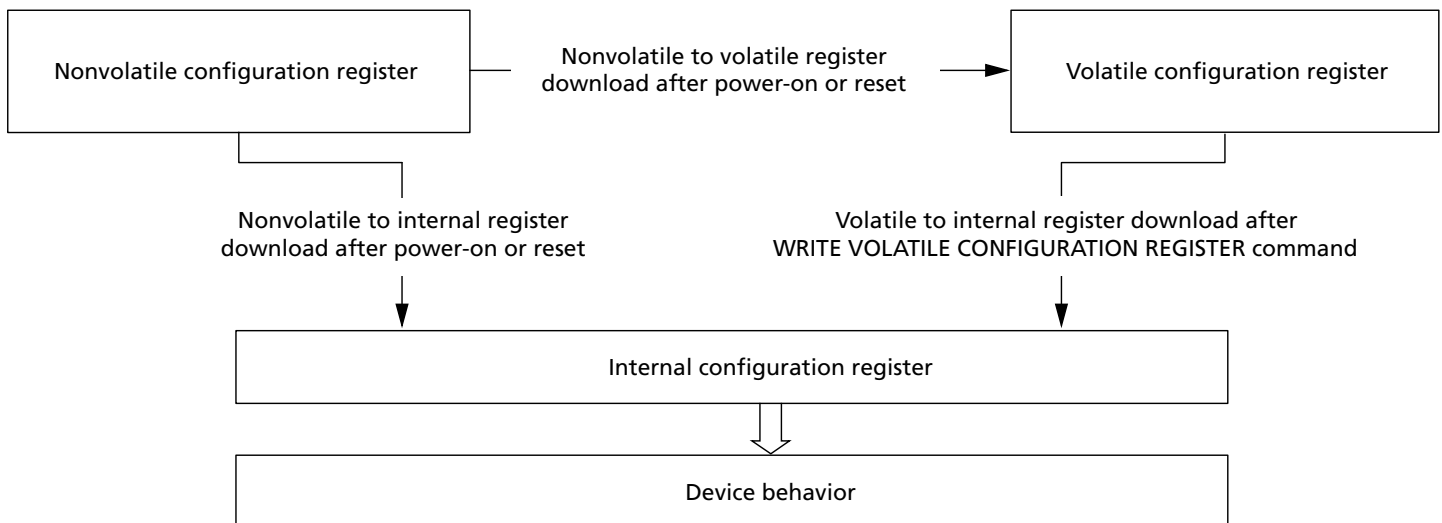
Internal Configuration Register

The memory configuration is set by an internal configuration register that is not directly accessible to users.

The user can change the default configuration at power-up by using the WRITE NON-VOLATILE CONFIGURATION REGISTER. Information from the nonvolatile configuration register overwrites the internal configuration register during power-on or after a reset.

The user can change the configuration during device operation using the WRITE VOLATILE CONFIGURATION REGISTER command. Information from the volatile configuration registers overwrite the internal configuration register immediately after the WRITE command completes.

Figure 6: Internal Configuration Register





512Mb, 1.8V Xcela Flash Memory Nonvolatile Configuration Register

Nonvolatile Configuration Register

Nonvolatile configuration register bits set the device configuration after power-up or reset. All bits are erased (FFh) unless stated otherwise. This register is read from and written to using the READ NONVOLATILE CONFIGURATION REGISTER and the WRITE NONVOLATILE CONFIGURATION REGISTER commands, respectively. The commands use the main array address scheme, but only the LSB is used to access different register settings, thereby providing up to 256 bytes of registers (See the table below for the details). A READ command from a reserved address returns FFh. A WRITE command to a reserved setting is ignored, flag status register bit 1 is set, and the write enable latch bit is cleared.

Table 6: Nonvolatile Configuration Register

Address	Name	Settings	Description	Notes
255h:08h	Reserved	Reserved	Reserved	
07h	Wrap configuration	FFh = Continuous (Default) FEh = 64-byte wrap FDh = 32-byte wrap FCh = 16-byte wrap Others = Reserved	Enables the device to read from memory sequentially or to wrap within 16-, 32-, or 64-byte boundaries.	
06h	XIP configuration	FFh = XIP disabled (Default) FEh = 8IOFR XIP FDh = 8OFR XIP F8h = FAST READ XIP Others = Reserved	Enables the device to operate in the selected XIP mode immediately after power-on reset.	
05h	Beyond 128Mb address configuration	FFh = 3-byte address (Default) FEh = 4-byte address Others = Reserved	Defines the number of address bytes for a command.	
04h	Reserved	Reserved	Reserved	
03h	Programmable output drive strength	FFh = 50Ω (Default) FEh = 35Ω FDh = 25Ω FCh = 18Ω Others = Reserved	Optimizes the impedance at $V_{CC}/2$ output voltage.	
02h	Reserved	Reserved	Reserved	
01h	Dummy cycle configuration	00h = Identical to 1Fh 01h = 1 dummy cycle 02h = 2 dummy cycles 03h to 1Dh = 3 to 29 dummy cycles 1Eh = 30 dummy cycles 1Fh = Default Others = Reserved	Sets the number of dummy clock cycles subsequent to all FAST READ commands (See the Command Set Table for default setting values).	1



512Mb, 1.8V Xcelera Flash Memory Nonvolatile Configuration Register

Table 6: Nonvolatile Configuration Register (Continued)

Address	Name	Settings	Description	Notes
00h	I/O mode	FFh = Extended SPI (Default) DFh = Extended SPI without DQS E7h = Octal DDR C7h = Octal DDR without DQS Others = Reserved	Sets the device to work in different I/O modes such as DDR mode or DQS mode (strobe enabled).	2

- Notes:
1. The number of cycles must be set to accord with the clock frequency, which varies by the type of FAST READ command (See Supported Clock Frequencies table). Insufficient dummy clock cycles for the operating frequency causes the memory to read incorrect data.
 2. For parts configured with pin configuration option "Boot in DDR x8" the default value of this byte is FFh. On those parts it's not possible to configure the parts to work in extended SPI using NVCR.



512Mb, 1.8V Xccela Flash Memory Volatile Configuration Register

Volatile Configuration Register

Volatile configuration register bits temporarily set the device configuration after power-up or reset. All bits are erased (FFh) unless stated otherwise. This register is read from and written to using the READ NONVOLATILE CONFIGURATION REGISTER and the WRITE NONVOLATILE CONFIGURATION REGISTER commands, respectively. The commands use the main array address scheme; however, only the LSB is used to access different register settings to provide up to 256 bytes of registers (See the table below for the details). A READ command from a reserved address returns FFh. A WRITE command to a reserved setting is ignored, flag status register bit 1 is set, and the write enable latch bit is cleared.

Table 7: Volatile Configuration Register

Address	Name	Settings	Description	Notes
255h:08h	Reserved	Reserved	Reserved	
07h	Wrap configuration	FFh = Continuous (Default) FEh = 64-byte wrap FDh = 32-byte wrap FCh = 16-byte wrap Others = Reserved	Enables the device to read from memory sequentially or to wrap within 16-, 32-, or 64-byte boundaries.	
06h	XiP configuration	FFh = XiP disabled (Default) FEh = XiP enabled Others = Reserved	Enables the device to operate in the selected XiP mode. It is first required to enable XiP and then enter XiP mode using the XiP confirmation bit	
05h	Beyond 128Mb address configuration	FFh = 3-byte address (Default) FEh = 4-byte address Others = Reserved	Defines the number of address bytes for a command.	
04h	Reserved	Reserved	Reserved	
03h	Programmable output drive strength	FFh = 50Ω (Default) FEh = 35Ω FDh = 25Ω FCh = 18Ω Others = Reserved	Optimizes the impedance at $V_{CC}/2$ output voltage.	
02h	Reserved	Reserved	Reserved	
01h	Dummy cycle configuration	00h = Identical to 1Fh 01h = 1 dummy cycle 02h = 2 dummy cycles 03h to 1Dh = 3 to 29 dummy cycles 1Eh = 30 dummy cycles 1Fh = Default Others = Reserved	Sets the number of dummy clock cycles subsequent to all FAST READ commands (See the Command Set Table for default setting values).	1



512Mb, 1.8V Xccela Flash Memory Volatile Configuration Register

Table 7: Volatile Configuration Register (Continued)

Address	Name	Settings	Description	Notes
00h	I/O mode	FFh = Extended SPI (Default) DFh = Extended SPI without DQS E7h = Octal DDR C7h = Octal DDR without DQS Others = Reserved	Sets the device to work in different I/O modes such as DDR mode or DQS mode (strobe enabled).	

Note: 1. The number of cycles must be set to accord with the clock frequency, which varies by the type of FAST READ command (See Supported Clock Frequencies table). Insufficient dummy clock cycles for the operating frequency causes the memory to read incorrect data.

Supported Clock Frequencies

Table 8: Clock Frequencies – SDR and DDR Read Starting at Any Byte Address

Note 1 applies to entire table

Number of Dummy Clock Cycles	FAST READ	Octal OUTPUT FAST READ		Octal I/O FAST READ		OCTAL DDR
	SDR	SDR	DDR	SDR	DDR	
1	100	16	NA	NA	NA	NA
2	116	33	16	NA	NA	NA
3	133	50	33	16	16	16
4	150	66	50	33	33	33
5	166	83	66	50	50	50
6	166	100	83	66	66	66
7	166	116	95	76	76	76
8	166	133	105	86	86	86
9	166	143	114	95	95	95
10	166	152	124	105	105	105
11	166	162	133	114	114	114
12	166	166	143	124	124	124
13	166	166	152	133	133	133
14	166	166	162	143	143	143
15	166	166	171	152	152	152
16	166	166	181	162	162	162
17	166	166	191	166	171	171
18	166	166	200	166	181	181
19	166	166	200	166	191	191
20 and above	166	166	200	166	200	200

Note: 1. Values are guaranteed by characterization and not 100% tested in production.



512Mb, 1.8V Xccela Flash Memory Volatile Configuration Register

Table 9: Clock Frequencies – SDR and DDR Read 4-Byte Aligned

Note 1 applies to entire table

Number of Dummy Clock Cycles	FAST READ	Octal OUTPUT FAST READ		Octal I/O FAST READ		OCTAL DDR
	SDR	SDR	DDR	SDR	DDR	
1	100	16	NA	NA	NA	NA
2	116	33	16	NA	NA	NA
3	133	50	33	16	16	16
4	150	66	50	33	33	33
5	166	83	66	50	50	50
6	166	100	83	66	66	66
7	166	116	100	83	83	83
8	166	133	114	100	95	95
9	166	150	124	116	105	105
10	166	166	133	133	114	114
11	166	166	143	143	124	124
12	166	166	152	152	133	133
13	166	166	162	162	143	143
14	166	166	171	166	152	152
15	166	166	181	166	162	162
16	166	166	191	166	171	171
17	166	166	200	166	181	181
18	166	166	200	166	191	191
19 and above	166	166	200	166	200	200

Note: 1. Values are guaranteed by characterization and not 100% tested in production.

Data Sequence Wraps by Density

Table 10: Sequence of Bytes During Wrap

Starting Address	16-Byte Wrap	32-Byte Wrap	64-Byte Wrap
0	0-1-2- . . . -15-0-1- . .	0-1-2- . . . -31-0-1- . .	0-1-2- . . . -63-0-1- . .
1	1-2- . . . -15-0-1-2- . .	1-2- . . . -31-0-1-2- . .	1-2- . . . -63-0-1-2- . .
....
15	15-0-1-2-3- . . . -15-0-1- . .	15-16-17- . . . -31-0-1- . .	15-16-17- . . . -63-0-1- . .
....
31	–	31-0-1-2-3- . . . -31-0-1- . .	31-32-33- . . . -63-0-1- . .
....
63	–	–	63-0-1- . . . -63-0-1- . .

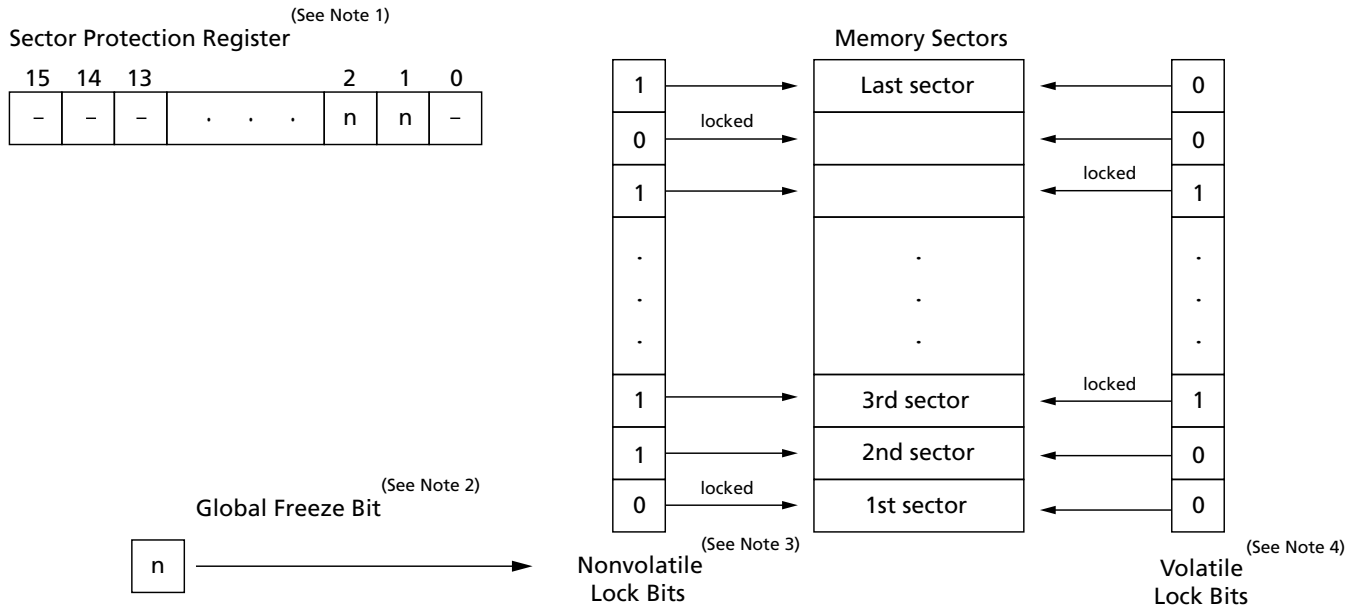


512Mb, 1.8V Xcelera Flash Memory Security Registers

Security Registers

Security registers enable sector and password protection on multiple levels using non-volatile and volatile register and bit settings (shown below). The applicable register tables follow.

Figure 7: Sector and Password Protection



- Notes:
- Sector protection register.** This 16-bit nonvolatile register includes two active bits[2:1] to enable sector and password protection.
 - Global freeze bit.** This volatile bit protects the settings in all nonvolatile lock bits.
 - Nonvolatile lock bits.** Each nonvolatile bit corresponds to and provides nonvolatile protection for an individual memory sector, which remains locked (protection enabled) until its corresponding bit is cleared to 1.
 - Volatile lock bits.** Each volatile bit corresponds to and provides volatile protection for an individual memory sector, which is locked temporarily (protection is cleared when the device is reset or powered down).



512Mb, 1.8V Xcela Flash Memory Sector Protection Security Register

Sector Protection Security Register

Table 11: Sector Protection Register

Bits	Name	Settings	Description	Notes
15:3	Reserved	1 = Default	—	
2	Password protection lock	1 = Disabled (Default) 0 = Enabled	Nonvolatile bit: When set to 1, password protection is disabled. When set to 0, password protection is enabled permanently; the 64-bit password cannot be retrieved or reset.	1, 2
1	Sector protection lock	1 = Enabled, with password protection (Default) 0 = Enabled, without password protection	Nonvolatile bit: When set to 1, nonvolatile lock bits can be set to lock/unlock their corresponding memory sectors; bit 2 can be set to 0, enabling password protection permanently. When set to 0, nonvolatile lock bits can be set to lock/unlock their corresponding memory sectors; bit 2 must remain set to 1, disabling password protection permanently.	1, 3, 4
0	Reserved	1 = Default	—	

- Notes:
- Bits 2 and 1 are user-configurable, one-time-programmable, and mutually exclusive in that only one of them can be set to 0. It is recommended that one of the bits be set to 0 when first programming the device.
 - The 64-bit password must be programmed and verified before this bit is set to 0 because after it is set, password changes are not allowed, thus providing protection from malicious software. When this bit is set to 0, a 64-bit password is required to reset the global freeze bit from 0 to 1. In addition, if the password is incorrect or lost, the global freeze bit can no longer be set and nonvolatile lock bits cannot be changed. (See the Sector and Password Protection figure and the Global Freeze Bit Definition table).
 - Whether this bit is set to 1 or 0, it enables programming or erasing nonvolatile lock bits (which provide memory sector protection). The password protection bit must be set beforehand because setting this bit will either enable password protection permanently (bit 2 = 0) or disable password protection permanently (bit 1 = 0).
 - By default, all sectors are unlocked when the device is shipped from the factory. Sectors are locked, unlocked, read, or locked down as explained in the Nonvolatile and Volatile Lock Bits table and the Volatile Lock Bit Register Bit Definitions table.

Table 12: Global Freeze Bit

Bits	Name	Settings	Description
7:1	Reserved	0	Bit values are 0
0	Global freeze bit	1 = Disabled (Default) 0 = Enabled	Volatile bit: When set to 1, all nonvolatile lock bits can be set to enable or disable locking their corresponding memory sectors. When set to 0, nonvolatile lock bits are protected from PROGRAM or ERASE commands. This bit should not be set to 0 until the nonvolatile lock bits are set.

- Note:
- The READ GLOBAL FREEZE BIT command enables reading this bit. When password protection is enabled, this bit is locked upon device power-up or reset. It cannot be changed without the password. After the password is entered, the UNLOCK PASSWORD command resets this bit to 1, enabling programming or erasing the nonvolatile lock bits. After the bits are changed, the WRITE GLOBAL FREEZE BIT command sets this bit to 0, protecting the nonvolatile lock bits from PROGRAM or ERASE operations.



512Mb, 1.8V Xcela Flash Memory Nonvolatile and Volatile Sector Lock Bits Security

Nonvolatile and Volatile Sector Lock Bits Security

Table 13: Nonvolatile and Volatile Lock Bits

Bit Details	Nonvolatile Lock Bit	Volatile Lock Bit
Description	Each sector of memory has one corresponding non-volatile lock bit	Each sector of memory has one corresponding volatile lock bit; this bit is the sector write lock bit described in the Volatile Lock Bit Register table.
Function	When set to 0, locks and protects its corresponding memory sector from PROGRAM or ERASE operations. Because this bit is nonvolatile, the sector remains locked, protection enabled, until the bit is cleared to 1.	When set to 1, locks and protects its corresponding memory sector from PROGRAM or ERASE operations. Because this bit is volatile, protection is temporary. The sector is unlocked, protection disabled, upon device reset or power-down.
Settings	1 = Lock disabled 0 = Lock enabled	0 = Lock disabled 1 = Lock enabled
Enabling protection	The bit is set to 0 by the WRITE NONVOLATILE LOCK BITS command, enabling protection for designated locked sectors. Programming a sector lock bit requires the typical byte programming time.	The bit is set to 1 by the WRITE VOLATILE LOCK BITS command, enabling protection for designated locked sectors.
Disabling protection	All bits are cleared to 1 by the ERASE NONVOLATILE LOCK BITS command, unlocking and disabling protection for all sectors simultaneously. Erasing all sector lock bits requires typical sector erase time.	All bits are set to 0 upon reset or power-down, unlocking and disabling protection for all sectors.
Reading the bit	Bits are read by the READ NONVOLATILE LOCK BITS command.	Bits are read by the READ VOLATILE LOCK BITS command.



512Mb, 1.8V Xcela Flash Memory Nonvolatile Lock Bit Security Register

Nonvolatile Lock Bit Security Register

For nonvolatile sector locking, the nonvolatile lock bits are stored in flash cells within an erasable sector lock-bit array, hence, making this a nonvolatile locking scheme. An erased flash cell corresponds to an unlocked sector and a programmed flash cell corresponds to a locked sector.

One of nonvolatile lock bits is related to each sector, the nonvolatile lock bits are programmed individually but must be erased as a group.

Programming nonvolatile lock bits requires the typical byte programming time. Erasing all the nonvolatile lock bits requires typical sector erase time.

Table 14: Nonvolatile Lock Bit Register

Nonvolatile Lock Bit Value	Protection Status
00h	Sector protected from modify operations
FFh	Sector unprotected from modify operations (default).

Volatile Lock Bit Security Register

One volatile lock bit register is associated with each sector of memory. It enables the sector to be locked, unlocked, or locked-down with the WRITE VOLATILE LOCK BITS command, which executes only when sector lock down (bit 1) is set to 0. Each register can be read with the READ VOLATILE LOCK BITS command. This register is compatible with and provides the same locking capability as the lock register in the Micron N25Q SPI NOR family.

Table 15: Volatile Lock Bit Register

Bit	Name	Settings	Description
7:2	Reserved	0	Bit values are 0.
1	Sector lock down	0 = Lock-down disabled (Default) 1 = Lock-down enabled	Volatile bit: Device always powers up with this bit set to 0 so that sector lock down and sector write lock bits can be set to 1. When this bit set to 1, neither of the two volatile lock bits can be written to until the next power cycle, hardware, or software reset.
0	Sector write lock	0 = Write lock disabled (Default) 1 = Write lock enabled	Volatile bit: Device always powers up with this bit set to 0 so that PROGRAM and ERASE operations in this sector can be executed and sector content modified. When this bit is set to 1, PROGRAM and ERASE operations in this sector are not executed.



512Mb, 1.8V Xcelia Flash Memory Protection Management Register

Protection Management Register

MT35X offers enhanced security features that can be enabled by properly setting the protection management register (PMR).

The PMR bits can be read from or written to using the READ PROTECTION MANAGEMENT REGISTER and WRITE PROTECTION MANAGEMENT REGISTER commands.

When the PMR lockdown bit (bit 2) is set to 0, the device will no longer respond to WRITE PROTECTION MANAGEMENT REGISTER commands. If this command is issued, the register will remain unchanged and the device will set an error code in flag status register bits 1 and 4.

Note: If the enhanced security features (activated through the PMR) are not going to be used, programming bit 2 of the PMR to 0 is strongly recommended. This prevents any future unintentional or malicious operation on this register that could result in permanent and irreversible locking of the memory sectors.

Table 16: Protection Management Register

Bit	Name	Settings	Description	Notes
7	Reserved	Reserved	Reserved	
6	Reserved	Reserved	Reserved	
5	Data protection at power up	0 = Lock 1 = Unlock (default)	OTP control bit: Enabling this bit sets all sector lock bits, eliminating the possibility of data corruption from errant instructions sent to the memory. The sector lock bits remain set from the time external power is available.	
4	Status Register Lock	0 = Lock 1 = Unlock (default)	OTP control bit: Permanently locks the status register, further writes to SR not allowed regardless of the state of W# pin and write enable/disable bit of the status register.	
3	Reserved	Reserved	Reserved	
2	PMR lockdown	0 = Lock 1 = Unlock (default)	OTP control bit: Permanently locks the protection management register.	
1	Nonvolatile sector lock bit register lockdown	0 = Lock 1 = Unlock (default)	OTP control: Permanently locks the contents of the nonvolatile sector lock bit register.	1
0	Nonvolatile sector lock bit erase lock	0 = Lock 1 = Unlock (default)	OTP control: When this bit is set to 1, the nonvolatile sector lock bit register array is erasable; otherwise, it is unerasable.	

Note: 1. When this bit is set to 0, the nonvolatile lock bits are locked from PROGRAM and ERASE operations. Nonvolatile lock bits cannot be unlocked.



512Mb, 1.8V Xcela Flash Memory Protection Management Register Operations

Protection Management Register Operations

Protection management register bits can be read with the READ PROTECTION MANAGEMENT REGISTER (2Bh) command. They can be programmed independently or collectively with the WRITE PROTECTION MANAGEMENT REGISTER command (68h). The bits are one-time programmable and cannot be erased.

To initiate a READ PROTECTION MANAGEMENT REGISTER command, S# is driven LOW. For extended SPI protocol, input is on DQ0, output on DQ1. For dual SPI protocol, input/output is on DQ[1:0]. For Octal DDR protocol, input/output is on DQ[7:0]. The operation is terminated by driving S# HIGH at any time during data output.

Before a WRITE PROTECTION MANAGEMENT REGISTER command is initiated, the WRITE ENABLE command must be executed to set the write enable latch bit to 1. To initiate a command, S# is driven LOW and held LOW until the eighth bit of the last data byte has been latched in, after which it must be driven HIGH. For the extended SPI and Octal DDR protocols, input is on DQ0, and DQ[7:0], respectively, followed by the data bytes. . If S# is not driven HIGH, the command is not executed, error bits are not set, and the write enable latch remains set to 1. The operation is self-timed and its duration is ^tPPMR.

Table 17: Protection Management Register Operations

Operation Name	Description/Conditions
READ PROTECTION MANAGEMENT REGISTER (2Bh)	The command does not require dummy cycles in extended SPI protocol, while 8 dummy cycles are necessary in Octal DDR protocol. When the register is read continuously, the same byte is output repeatedly.
WRITE PROTECTION MANAGEMENT REGISTER (68h)	When an operation is in progress, the write in progress bit is set to 1. The write enable latch bit is cleared to 0, whether the operation is successful or not. The status register and flag status register can be polled for the operation status. When the operation completes, the write in progress bit is cleared to 0, whether the operation is successful or not. For stacked devices (1Gb and 2Gb) it is possible to obtain the operation status by reading the flag status register a number of times corresponding to the die stacked, with S# toggled in between the READ FLAG STATUS REGISTER commands. When the operation completes, the program or erase controller bit of the flag status register is cleared to 1. The end of operation can be detected when the program or erase controller bit of the flag status register outputs 1 for all the die of the stack. When a 0 is written to any reserved field, the operation is initiated; however, uCode aborts the operation without programming any bits. Then the write enable latch bit is cleared, and the program error bit and protection error bits are set to 1. When protection management bit 2 is set to 0 (locked), the command is not executed, the write enable latch remains set to 1, and flag status register and protection error bits are set to 1.



512Mb, 1.8V Xccela Flash Memory Device ID Data

Device ID Data

The device ID data shown in the tables here is read by the READ ID and MULTIPLE I/O READ ID operations.

Table 18: Device ID Data

Byte#	Name	Content Value	Assigned By
Manufacturer ID (1 Byte total)			
1	Manufacturer ID (1 Byte)	2Ch	JEDEC
Device ID (2 bytes total)			
2	Memory type (1 Byte)	5Ah = 3V	Manufacturer
		5Bh = 1.8V	
3	Memory capacity (1 byte)	1Ch = 2Gb	
		1Bh = 1Gb	
		1Ah = 512Mb	
		19h = 256Mb	
Unique ID (17 bytes total)			
4	Indicates the number of remaining ID bytes (1 byte)	10h	Factory
5	Extended device ID (1 byte)	See Extended Device ID table	
6	Device configuration information (1 byte)	See Device Configuration In-formation table	
7:20	Customized factory data (14 bytes)	Unique ID code (UID)	

Table 19: Extended Device ID Data, First Byte

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Device generation 1 = 2nd generation	Reserved	Reserved	Reserved	Reserved	Sector size: 01 = Uniform 128KB	

Table 20: Device Configuration Information Data

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	Boot up protocol: 0 = Boot in SDR x1 1 = Boot in DDR x8	Reserved	



512Mb, 1.8V Xcela Flash Memory Serial Flash Discovery Parameter Data

Serial Flash Discovery Parameter Data

The serial flash discovery parameter (SFDP) provides a standard, consistent method to describe serial flash device functions and features using internal parameter tables. The parameter tables can be interrogated by host system software, enabling adjustments to accommodate divergent features from multiple vendors. The SFDP standard defines a common parameter table that describes important device characteristics and serial access methods used to read the parameter table data. Micron's SFDP table information aligns with JEDEC-standard JESD216 for serial flash discoverable parameters. The latest JEDEC standard includes revision 1.6. Refer to JEDEC-standard JESD216B for a complete overview of the SFDP table definition. Data in the SFDP tables is read by the READ SERIAL FLASH DISCOVERY PARAMETER operation. See Micron TN-12-35: Serial Flash Discovery Parameters for MT35X Family for serial flash discovery parameter data.



512Mb, 1.8V Xccela Flash Memory Command Definitions

Command Definitions

Table 21: Command Set

Command	Code	Extended SPI		Octal SPI		Address Bytes	Data Bytes
		Command-Address-Data	Dummy Clock Cycles	Command-Address-Data	Dummy Clock Cycles		
Software RESET Operations							
RESET ENABLE	66h	1-0-0	0	8-0-0	0	0	0
RESET MEMORY	99h	1-0-0	0	8-0-0	0	0	0
READ ID Operations							
READ ID	9E/9Fh	1-0-1	0	8-0-8	8	0	1 to 20
READ SERIAL FLASH DISCOVERY PARAMETER	5Ah	1-1-1	8	8-8-8	8	3 ¹	1 to ∞
READ MEMORY Operations							
READ	03h	1-1-1	0	–	–	3 ²	1 to ∞
FAST READ	0Bh	1-1-1	8	8-8-8	16	3 ²	1 to ∞
OCTAL OUTPUT FAST READ	8Bh	1-1-8	8	8-8-8	16	3 ²	1 to ∞
OCTAL I/O FAST READ	CBh	1-8-8	16	8-8-8	16	3 ²	1 to ∞
DDR OCTAL OUTPUT FAST READ	9Dh	1-1-8	8	8-8-8	16	3 ²	1 to ∞
DDR OCTAL I/O FAST READ	FDh	1-8-8	16	8-8-8	16	4	1 to ∞
READ MEMORY Operations with 4-Byte Address							
4-BYTE READ	13h	1-1-1	0	–	–	4	1 to ∞
4-BYTE FAST READ	0Ch	1-1-1	8	8-8-8	16	4	1 to ∞
4-BYTE OCTAL OUTPUT FAST READ	7Ch	1-1-8	8	8-8-8	16	4	1 to ∞
4-BYTE OCTAL I/O FAST READ	CCh	1-8-8	16	8-8-8	16	4	1 to ∞
WRITE Operations							
WRITE ENABLE	06h	1-0-0	0	8-0-0	0	0	0
WRITE DISABLE	04h	1-0-0	0	8-0-0	0	0	0
READ REGISTER Operations							
READ STATUS REGISTER	05h	1-0-1	0	8-0-8	8	0	1 to ∞
READ FLAG STATUS REGISTER	70h	1-0-1	0	8-0-8	8	0	1 to ∞
READ NONVOLATILE CONFIGURATION REGISTER	B5h	1-1-1	8	8-8-8	8	3 ²	1 to ∞
READ VOLATILE CONFIGURATION REGISTER	85h	1-1-1	8	8-8-8	8	3 ²	1 to ∞
READ PROTECTION MANAGEMENT REGISTER	2Bh	1-0-1	0	8-0-8	8	0	1 to ∞
READ GENERAL PURPOSE READ REGISTER	96h ^{3, 4}	1-0-1	8	8-0-8	8	0	1 to ∞



512Mb, 1.8V Xccela Flash Memory Command Definitions

Table 21: Command Set (Continued)

Command	Code	Extended SPI		Octal SPI		Address Bytes	Data Bytes
		Command-Address-Data	Dummy Clock Cycles	Command-Address-Data	Dummy Clock Cycles		
WRITE REGISTER Operations							
WRITE STATUS REGISTER	01h	1-0-1	0	8-0-8	0	0	1
WRITE NONVOLATILE CONFIGURATION REGISTER	B1h	1-1-1	0	8-8-8	0	3 ²	1
WRITE VOLATILE CONFIGURATION REGISTER	81h	1-1-1	0	8-8-8	0	3 ²	1
WRITE PROTECTION MANAGEMENT REGISTER	68h	1-0-1	0	8-0-8	0	0	1
CLEAR FLAG STATUS REGISTER Operation							
CLEAR FLAG STATUS REGISTER	50h	1-0-0	0	8-0-0	0	0	0
PROGRAM Operations							
PAGE PROGRAM	02h	1-1-1	0	8-8-8	0	3 ²	1 to 256
OCTAL INPUT FAST PROGRAM	82h	1-1-8	0	8-8-8	0	3 ²	1 to 256
EXTENDED OCTAL INPUT FAST PROGRAM	C2h	1-8-8	0	8-8-8	0	3 ²	1 to 256
PROGRAM Operations with 4-Byte Address							
4-BYTE PAGE PROGRAM	12h	1-1-1	0	8-8-8	0	4	1 to 256
4-BYTE OCTAL INPUT FAST PROGRAM	84h	1-1-8	0	8-8-8	0	4	1 to 256
4-BYTE OCTAL INPUT EXTENDED FAST PROGRAM	8Eh	1-8-8	0	8-8-8	0	4	1 to 256
ERASE Operations							
32KB SUBSECTOR ERASE	52h	1-1-0	0	8-8-0	0	3 ²	0
4KB SUBSECTOR ERASE	20h	1-1-0	0	8-8-0	0	3 ²	0
SECTOR ERASE	D8h	1-1-0	0	8-8-0	0	3 ²	0
BULK ERASE	C7h/60h	1-0-0	0	8-0-0	0	0	0
ERASE Operations with 4-Byte Address							
4-BYTE SECTOR ERASE	DCh	1-1-1	0	8-8-8	0	4	0
4-BYTE 4KB SUBSECTOR ERASE	21h	1-1-1	0	8-8-8	0	4	0
4-BYTE 32KB SUBSECTOR ERASE	5Ch	1-1-1	0	8-8-8	0	4	0
SUSPEND/RESUME Operations							
PROGRAM/ERASE SUSPEND	75h	1-0-0	0	8-0-0	0	0	0
PROGRAM/ERASE RESUME	7Ah	1-0-0	0	8-0-0	0	0	0
ONE-TIME PROGRAMMABLE (OTP) Operations							
READ OTP ARRAY	4Bh	1-1-1	8	8-8-8	16	3 ²	1 to 65



512Mb, 1.8V Xccela Flash Memory Command Definitions

Table 21: Command Set (Continued)

Command	Code	Extended SPI		Octal SPI		Address Bytes	Data Bytes
		Command-Address-Data	Dummy Clock Cycles	Command-Address-Data	Dummy Clock Cycles		
PROGRAM OTP ARRAY	42h	1-1-1	0	8-8-8	0	3 ²	1 to 65
4-BYTE ADDRESS MODE Operations							
ENTER 4-BYTE ADDRESS MODE	B7h	1-0-0	0	8-0-0	0	0	0
EXIT 4-BYTE ADDRESS MODE	E9h	1-0-0	0	8-0-0	0	0	0
DEEP POWER-DOWN Operations							
ENTER DEEP POWER-DOWN	B9h	1-0-0	0	8-0-0	0	0	0
RELEASE FROM DEEP POWER-DOWN	ABh	1-0-0	0	8-0-0	0	0	0
ADVANCED SECTOR PROTECTION Operations							
READ SECTOR PROTECTION	2Dh	1-0-1	0	8-0-8	8	0	1 to ∞
PROGRAM SECTOR PROTECTION	2Ch	1-0-1	0	8-0-8	0	0	2
READ VOLATILE LOCK BITS	E8h	1-1-1	0	8-8-8	8	3 ²	1 to ∞
WRITE VOLATILE LOCK BITS	E5h	1-1-1	0	8-8-8	0	3 ²	1
READ NONVOLATILE LOCK BITS	E2h	1-1-1	0	8-8-8	8	4	1 to ∞
WRITE NONVOLATILE LOCK BITS	E3h	1-1-0	0	8-8-0	0	4	0
ERASE NONVOLATILE LOCK BITS	E4h	1-0-0	0	8-0-0	0	0	0
READ GLOBAL FREEZE BIT	A7h	1-0-1	0	8-0-8	8	0	1 to ∞
WRITE GLOBAL FREEZE BIT	A6h	1-0-0	0	8-0-0	0	0	0
READ PASSWORD	27h ⁵	1-0-1	0	8-0-8	8	0	1 to ∞
WRITE PASSWORD	28h	1-0-1	0	8-0-8	0	0	8
UNLOCK PASSWORD	29h	1-0-1	0	8-0-8	0	0	8
ADVANCED SECTOR PROTECTION Operations with 4-Byte Address							
4-BYTE READ VOLATILE LOCK BITS	E0h	1-1-1	0	8-8-8	8	4	1 to ∞
4-BYTE WRITE VOLATILE LOCK BITS	E1h	1-1-1	0	8-8-8	0	4	1
ADVANCED FUNCTION INTERFACE Operations							
CYCLIC REDUNDANCY CHECK	9Bh/27h	1-0-1	0	8-0-8	0	0	10 or 18

- Notes:
1. Read SFD instruction accepts only 3-byte address even if the device is configured to 4-byte address mode. In octal DDR mode, it will be fixed 4-byte address cycle.
 2. Requires 4 bytes of address if the device is configured to 4-byte address mode or Octal DDR protocol.



512Mb, 1.8V Xcelera Flash Memory Software RESET Operations

3. The number of dummy cycles for the READ GENERAL PURPOSE READ REGISTER command is fixed (8 dummy cycles) and is not affected by dummy cycle settings in the non-volatile configuration register and volatile configuration register.
4. The general purpose read register is 64 bytes. After the first 64 bytes, the device outputs wrap.
5. After the 8-bit instruction shifted in, the 64-bit data are shifted out, the least significant byte first, most significant bit of each byte first. The READ PASSWORD instruction is terminated by driving chip select (S#) HIGH at any time during data output. When read continuously, the device outputs the 64-bit data repeatedly.

Software RESET Operations

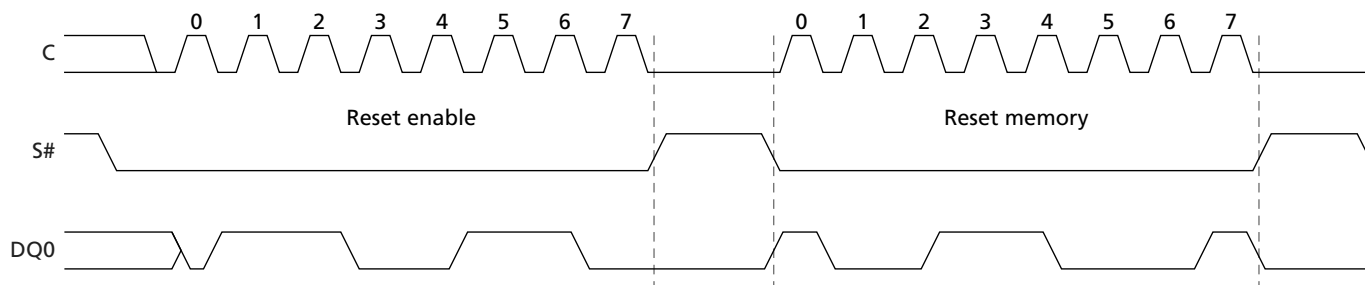
RESET ENABLE and RESET MEMORY Commands

To initiate these commands, S# is driven LOW and the command code is input on DQ0. A minimum deselection time of t_{SHSL2} must come between RESET ENABLE and RESET MEMORY or reset is not guaranteed. Then, S# must be driven HIGH for the device to enter power-on reset. A time of t_{SHSL3} is required before the device can be reselected by driving S# LOW.

Table 22: RESET ENABLE and RESET MEMORY Operations

Operation Name	Description/Conditions
RESET ENABLE (66h)	To reset the device, the RESET ENABLE command must be followed by the RESET MEMORY command. When the two commands are executed, the device enters a power-on reset condition. It is recommended to exit XIP mode before executing these two commands. All volatile lock bits and the volatile configuration register are reset to the power-on reset default condition according to nonvolatile configuration register settings. If a reset is initiated while a WRITE, PROGRAM, or ERASE operation is in progress or suspended, the operation is aborted and data may be corrupted. Reset is effective after the flag status register bit 7 outputs 1 with at least one byte output. A RESET ENABLE command is not accepted during WRITE STATUS REGISTER and WRITE NONVOLATILE CONFIGURATION REGISTER operations.
RESET MEMORY (99h)	

Figure 8: RESET ENABLE and RESET MEMORY – 66h and 99h



Note: 1. The octal DDR protocol uses eight data pins to transmit information.



512Mb, 1.8V Xcelera Flash Memory READ ID Operation

READ ID Operation

READ ID Command

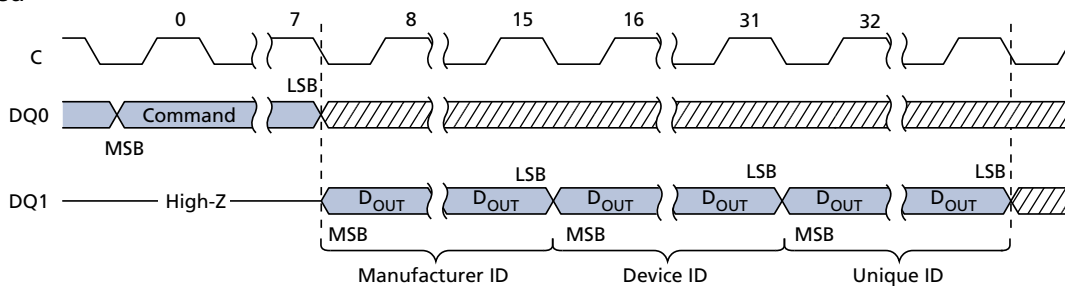
To initiate this command, S# is driven LOW and the command code is input on DQ_n. When S# is driven HIGH, the device goes to standby. The operation is terminated by driving S# HIGH at any time during data output.

Table 23: READ ID Operation

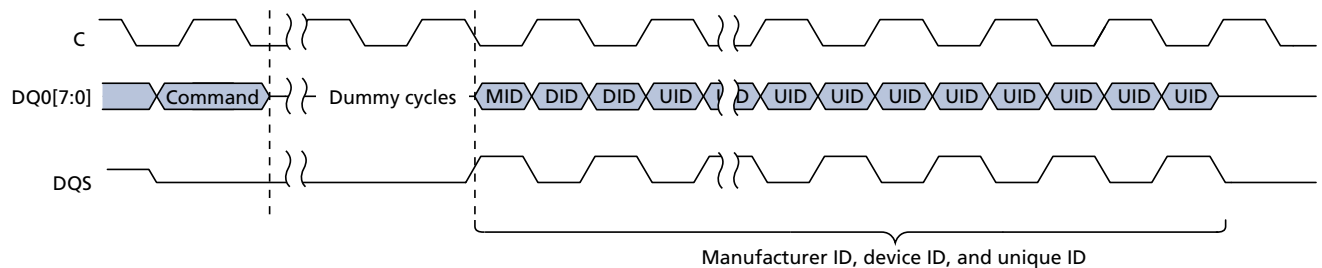
Operation Name	Description/Conditions
READ ID (9Eh/9Fh)	Outputs information shown in the Device ID Data tables. If an ERASE or PROGRAM cycle is in progress when the command is initiated, the command is not decoded and the command cycle in progress is not affected.

Figure 9: READ ID Command

Extended



Octal DDR



Note: 1. S# not shown.



512Mb, 1.8V Xcelera Flash Memory READ SERIAL FLASH DISCOVERY PARAMETER Operation

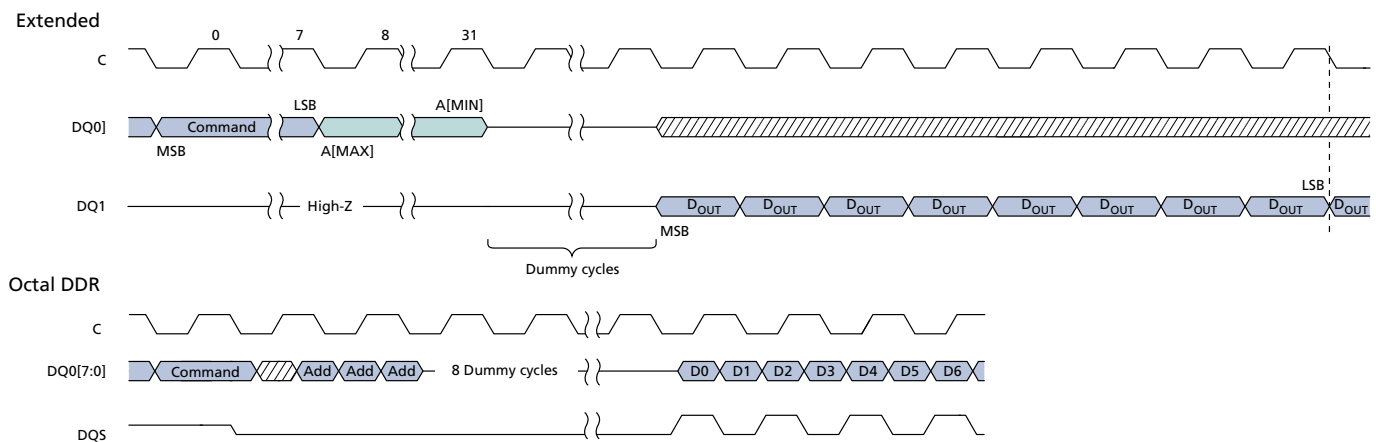
READ SERIAL FLASH DISCOVERY PARAMETER Operation

READ SERIAL FLASH DISCOVERY PARAMETER Command

To execute READ SERIAL FLASH DISCOVERY PARAMETER command, S# is driven LOW. The command code is input on DQ0, followed by three address bytes and eight dummy clock cycles. The device outputs the information starting from the specified address. When the 2048-byte boundary is reached, the data output wraps to address 0 of the Serial Flash Discovery Parameter Data table. The operation is terminated by driving S# HIGH at any time during data output.

Note: The operation always executes in continuous mode so the read burst wrap setting in the volatile configuration register does not apply.

Figure 10: READ SERIAL FLASH DISCOVERY PARAMETER Command – 5Ah



Note: 1. S# not shown.



512Mb, 1.8V Xccela Flash Memory READ MEMORY Operations

READ MEMORY Operations

To initiate a command, S# is driven LOW and the command code is input on DQ_n, followed by input of the address bytes on DQ_n. The operation is terminated by driving S# HIGH at any time during data output.

Table 24: READ MEMORY Operations

Operation Name	Description/Conditions
READ (03h)	The device supports 3-bytes addressing (default), with A[23:0] input during address cycle. After any READ command is executed, the device will output data from the selected address. After the boundary is reached, the device will start reading again from the beginning. Each address bit is latched in during the rising edge of the clock. The addressed byte can be at any location, and the address automatically increments to the next address after each byte of data is shifted out; therefore, a die can be read with a single command. FAST READ can operate at a higher frequency (^f C). DDR commands function in DDR protocol regardless of settings in the nonvolatile configuration register; other commands function in DDR protocol only after DDR protocol is enabled by the register settings. Due to the nature of DDR protocol, an even number of bytes is always transferred. The least significant bit of the byte address shall always be zero when using the DDR protocol. Please note that if the least significant bit of the address is set to one when using the DDR protocol, the results are indeterminate.
FAST READ (0Bh)	
OCTAL OUTPUT FAST READ (8Bh)	
OCTAL I/O FAST READ (CBh)	
DDR OCTAL OUTPUT FAST READ (9Dh)	
DDR OCTAL I/O FAST READ (FDh)	

4-BYTE READ MEMORY Operations

Table 25: 4-BYTE READ MEMORY Operations

Operation Name	Description/Conditions
4-BYTE READ (13h)	READ MEMORY operations can be extended to a 4-bytes address range, with [A31:0] input during address cycle. Selection of the 3-byte or 4-byte address range can be enabled in two ways: through the nonvolatile configuration register or through the ENABLE 4-BYTE ADDRESS MODE/EXIT 4-BYTE ADDRESS MODE commands. Each address bit is latched in during the rising edge of the clock. The addressed byte can be at any location, and the address automatically increments to the next address after each byte of data is shifted out; therefore, a die can be read with a single command. FAST READ can operate at a higher frequency (^f C).
4-BYTE FAST READ (0Ch)	
4-BYTE OCTAL OUTPUT FAST READ (7Ch)	
4-BYTE OCTAL I/O FAST READ (CCh)	



512Mb, 1.8V Xcela Flash Memory READ MEMORY Operations Timings

READ MEMORY Operations Timings

Figure 11: READ – 03h/13h²

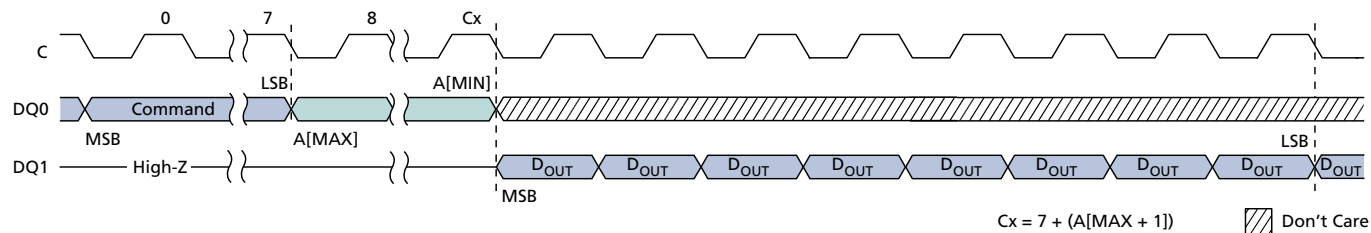
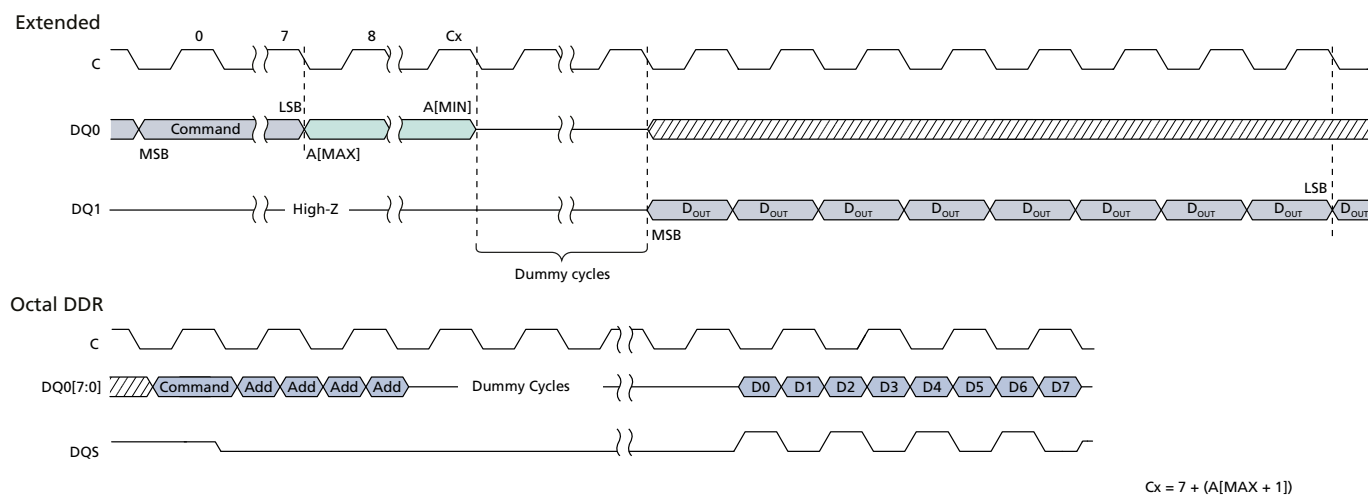


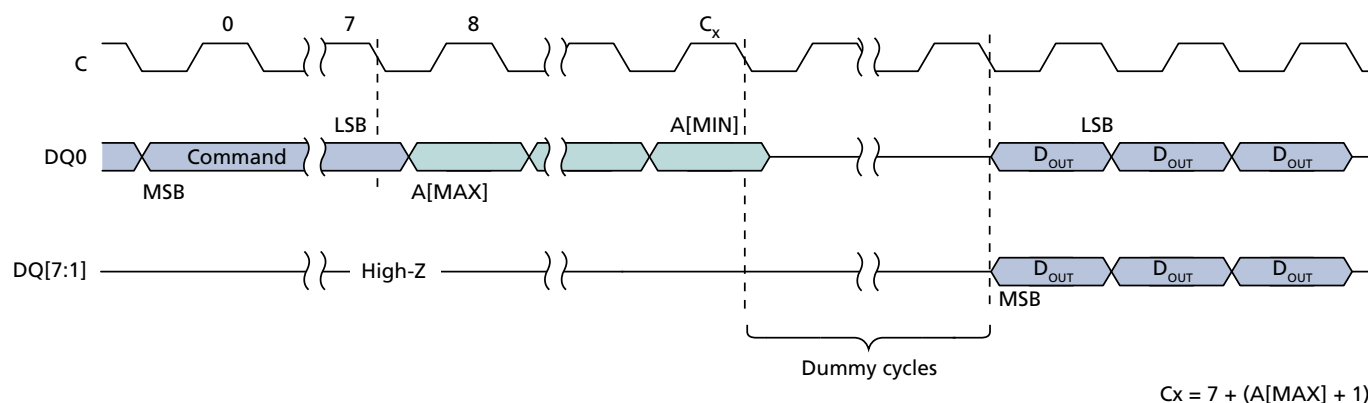
Figure 12: FAST READ – 0Bh/0Ch³





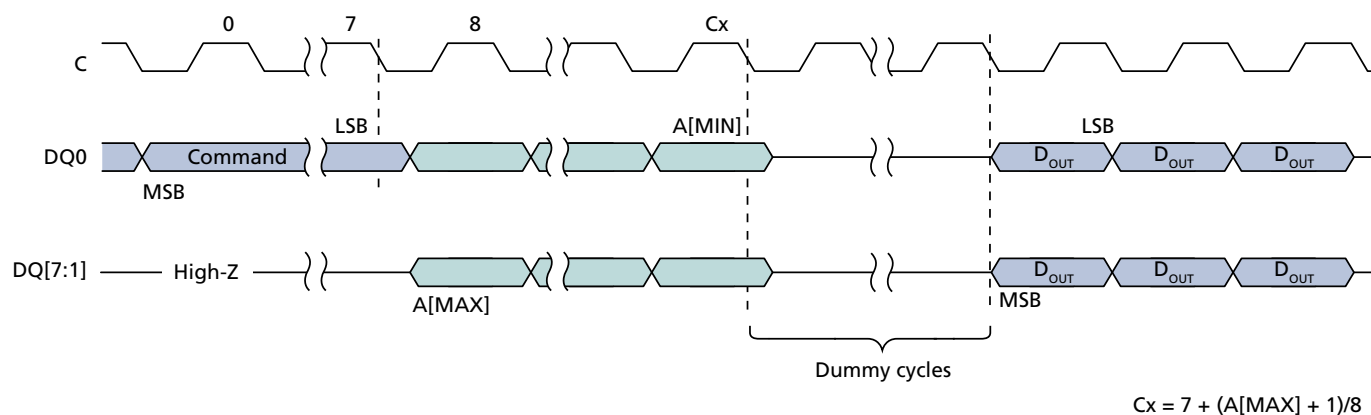
512Mb, 1.8V Xcela Flash Memory READ MEMORY Operations Timings

Figure 13: OCTAL OUTPUT FAST READ – 8Bh/7Ch³



- Notes:
1. Requires 32-bit address in 4-byte address configuration. In octal DDR protocol, the command, address, and data-out bits are transmitted on all eight data pins in DDR mode. The address is fixed with 4-byte.
 2. S# not shown.
 3. FAST READ and 4-BYTE FAST READ commands.

Figure 14: OCTAL I/O FAST READ – CBh/CCh³

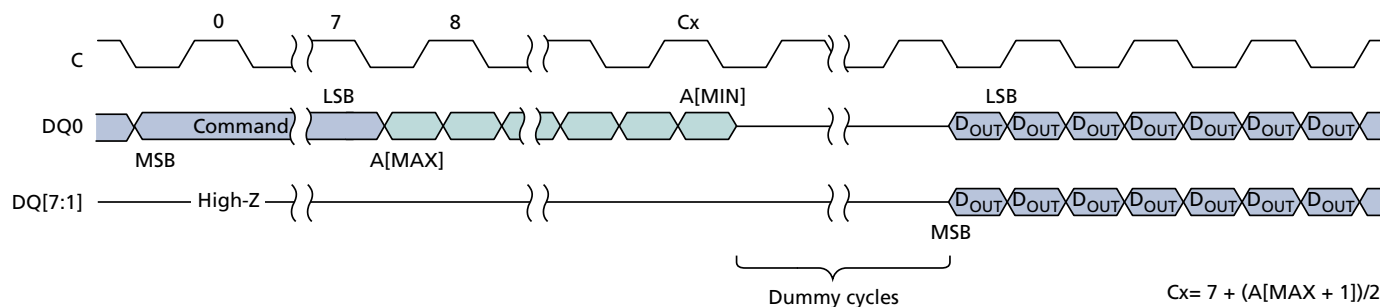


- Notes:
1. Requires 32-bit address in 4-byte address configuration. In octal DDR protocol, the command, address, and data-out bits are transmitted on all eight data pins in DDR mode. The address is fixed with 4-byte.
 2. S# not shown.
 3. FAST READ and 4-BYTE FAST READ commands.



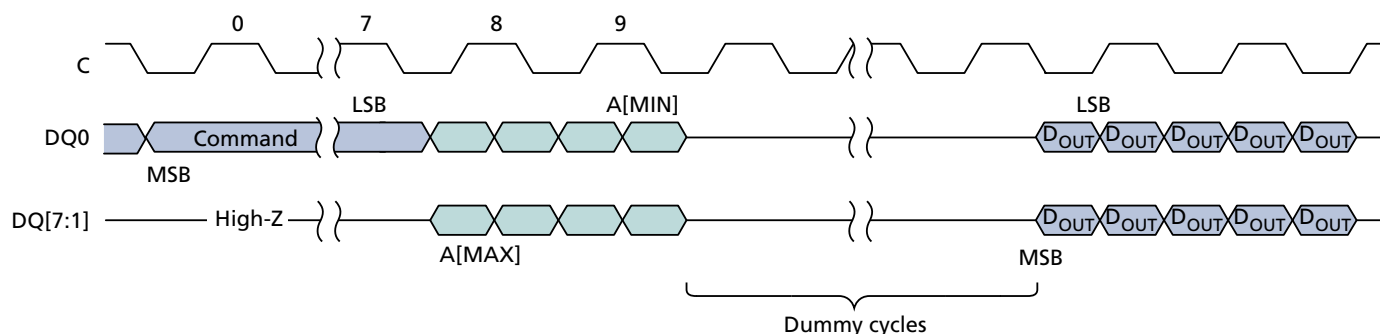
512Mb, 1.8V Xcela Flash Memory READ MEMORY Operations Timings

Figure 15: OCTAL OUTPUT FAST READ with DDR ADDRESS and DATA – 9Dh



- Notes:
1. Requires 32-bit address in 4-byte address configuration. In octal DDR protocol, the command, address, and data-out bits are transmitted on all eight data pins in DDR mode. The address is fixed with 4-byte.
 2. S# not shown.

Figure 16: OCTAL I/O FAST READ with DDR ADDRESS and DATA – FDh



- Notes:
1. Requires 32-bit address in 4-byte address configuration. In octal DDR protocol, the command, address, and data-out bits are transmitted on all eight data pins in DDR mode. The address is fixed with 4-byte.
 2. S# not shown.



512Mb, 1.8V Xcelera Flash Memory WRITE ENABLE/DISABLE Operations

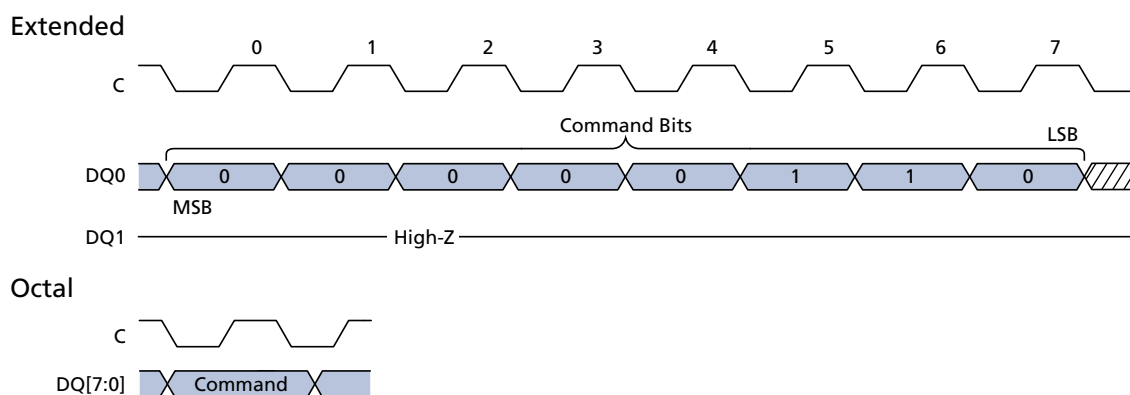
WRITE ENABLE/DISABLE Operations

To initiate a command, S# is driven LOW and held LOW until the eighth bit of the command code has been latched in, after which it must be driven HIGH. For extended and octal SPI protocols respectively, the command code is input on DQ0 and DQ[7:0], respectively. If S# is not driven HIGH after the command code has been latched in, the command is not executed, flag status register error bits are not set, and the write enable latch remains cleared to its default setting of 0, providing protection against errant data modification.

Table 26: WRITE ENABLE/DISABLE Operations

Operation Name	Description/Conditions
WRITE ENABLE (06h)	Sets the write enable latch bit before each PROGRAM, ERASE, and WRITE command.
WRITE DISABLE (04h)	Clears the write enable latch bit. In case of a protection error, WRITE DISABLE will not clear the bit. Instead, a CLEAR FLAG STATUS REGISTER command must be issued to clear both flags.

Figure 17: WRITE ENABLE and WRITE DISABLE Timing



Note: 1. WRITE ENABLE command sequence and code, shown here, is 06h (0000 0110 binary);
WRITE DISABLE is identical, but its command code is 04h (0000 0100 binary).



512Mb, 1.8V Xcelera Flash Memory READ REGISTER Operations

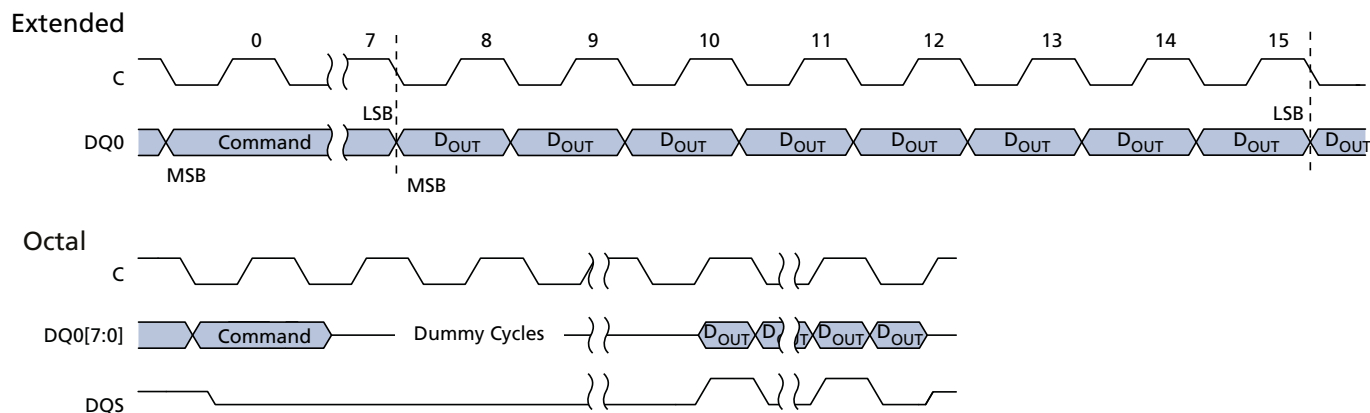
READ REGISTER Operations

To initiate a command, S# is driven LOW. For extended SPI protocol, input is on DQ0, output on DQ1. For octal SPI protocol, I/O is on DQ[7:0]. The operation is terminated by driving S# HIGH at any time during data output.

Table 27: READ REGISTER Operations

Operation Name	Description/Conditions
READ STATUS REGISTER (05h)	Can be read continuously and at any time, including during a PROGRAM, ERASE, or WRITE operation. If one of these operations is in progress, checking the write in progress bit or P/E controller bit is recommended before executing the command.
READ FLAG STATUS REGISTER (70h)	
READ NONVOLATILE CONFIGURATION REGISTER (B5h)	When continuously read, the device outputs the same byte repeatedly. All reserved fields output a value of 1.
READ VOLATILE CONFIGURATION REGISTER (85h)	When continuously read, the device outputs the same byte repeatedly. All reserved fields output a value of 1.

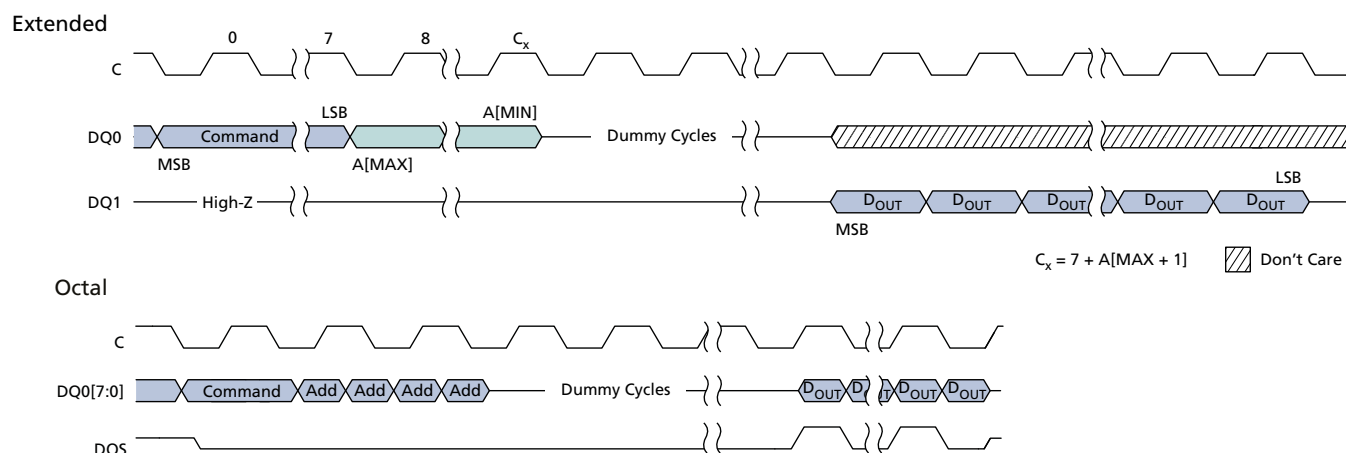
Figure 18: READ STATUS REGISTER – 05h





512Mb, 1.8V Xcelera Flash Memory WRITE REGISTER Operations

Figure 19: READ CONFIGURATION REGISTER – B5h/85h



WRITE REGISTER Operations

Before a WRITE REGISTER command is initiated, the WRITE ENABLE command must be executed to set the write enable latch bit to 1. To initiate a command, S# is driven LOW and held LOW until the eighth bit of the last data byte has been latched in, after which it must be driven HIGH; for the WRITE NONVOLATILE CONFIGURATION REGISTER command. For the extended and octal SPI protocols respectively, input is on DQ0 and DQ[7:0], followed by the data bytes. If S# is not driven HIGH, the command is not executed, flag status register error bits are not set, and the write enable latch remains set to 1. The operation is self-timed and its duration is t_W for WRITE STATUS REGISTER and t_{WVCR} for WRITE NONVOLATILE CONFIGURATION REGISTER.

Table 28: WRITE REGISTER Operations

Operation Name	Description/Conditions
WRITE STATUS REGISTER (01h)	The WRITE STATUS REGISTER command writes new values to status register bits 7:2, enabling software data protection. The status register can also be combined with the W# signal to provide hardware data protection. This command has no effect on status register bits 1:0.
WRITE NONVOLATILE CONFIGURATION REGISTER (B1h)	For the WRITE STATUS REGISTER and WRITE NONVOLATILE CONFIGURATION REGISTER commands, when the operation is in progress, the write in progress bit is set to 1. The write enable latch bit is cleared to 0, whether the operation is successful or not. The status register and flag status register can be polled for the operation status. When the operation completes, the write in progress bit is cleared to 0, whether the operation is successful or not.
WRITE VOLATILE CONFIGURATION REGISTER (81h)	Because register bits are volatile, change to the bits is immediate. Reserved bits are not affected by this command.



512Mb, 1.8V Xcelera Flash Memory CLEAR FLAG STATUS REGISTER Operation

Figure 20: WRITE STATUS REGISTER – 01h

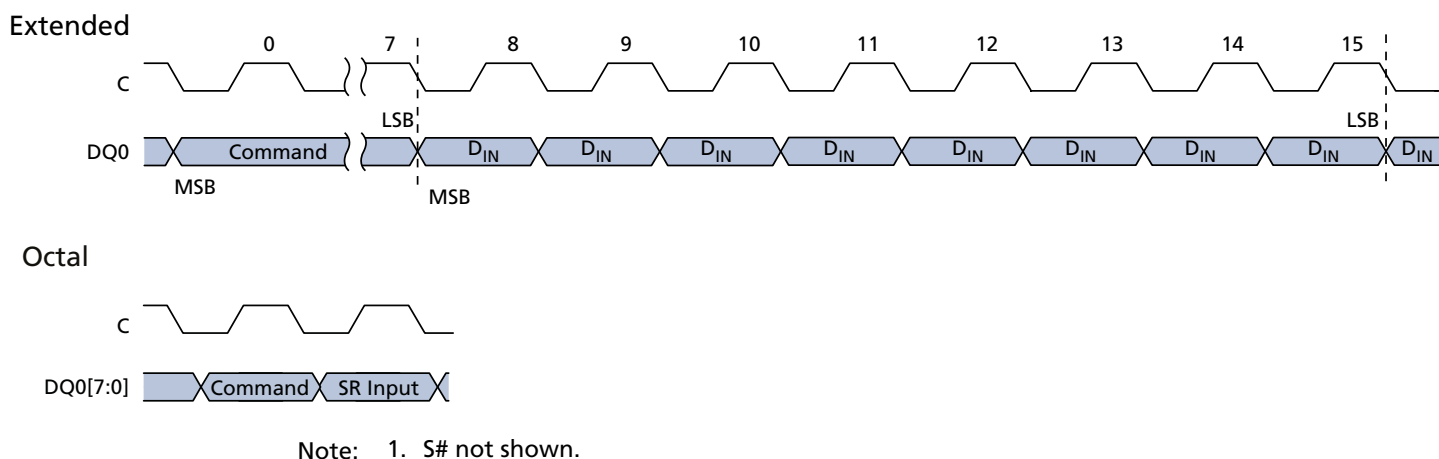
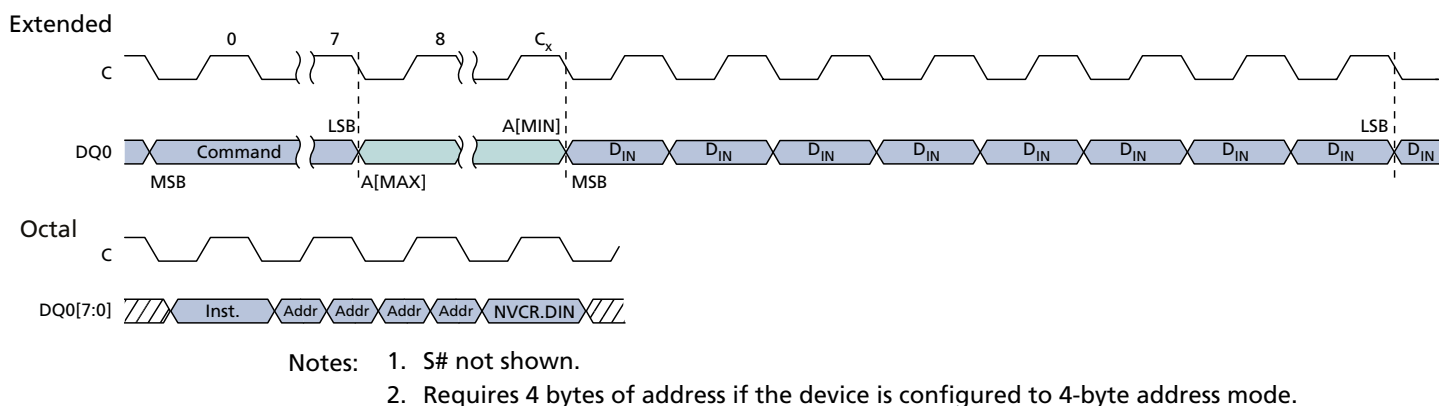


Figure 21: WRITE CONFIGURATION REGISTER – B1h/81h



CLEAR FLAG STATUS REGISTER Operation

To initiate a command, S# is driven LOW. For the extended and octal SPI protocols respectively, input is on DQ0 and DQ[7:0]. The operation is terminated by driving S# HIGH at any time.

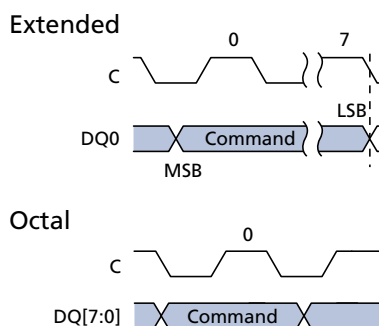
Table 29: CLEAR FLAG STATUS REGISTER Operation

Operation Name	Description/Conditions
CLEAR FLAG STATUS REGISTER (50h)	Resets the error bits (erase, program, and protection)



512Mb, 1.8V Xccela Flash Memory PROGRAM Operations

Figure 22: CLEAR FLAG STATUS REGISTER Timing



Note: 1. S# not shown.

PROGRAM Operations

Before a PROGRAM command is initiated, the WRITE ENABLE command must be executed to set the write enable latch bit to 1. To initiate a command, S# is driven LOW and held LOW until the eighth bit of the last data byte has been latched in, after which it must be driven HIGH. If S# is not driven HIGH, the command is not executed, flag status register error bits are not set, and the write enable latch remains set to 1. Each address bit is latched in during the rising edge of the clock. When a command is applied to a protected sector, the command is not executed, the write enable latch bit remains set to 1, and flag status register bits 1 and 4 are set. If the operation times out, the write enable latch bit is reset and the program fail bit is set to 1.

Note: The manner of latching data shown and explained in the timing diagrams ensures that the number of clock pulses is a multiple of one byte before command execution, helping reduce the effects of noisy or undesirable signals and enhancing device data protection.



512Mb, 1.8V Xccela Flash Memory 4-BYTE PROGRAM Operations

Table 30: PROGRAM Operations

Operation Name	Description/Conditions
PAGE PROGRAM (02h)	<p>A PROGRAM operation changes a bit from 1 to 0.</p> <p>When the operation is in progress, the write in progress bit is set to 1. The write enable latch bit is cleared to 0, whether the operation is successful or not. The status register and flag status register can be polled for the operation status. When the operation completes, the write in progress bit is cleared to 0. An operation can be paused or resumed by the PROGRAM/ERASE SUSPEND or PROGRAM/ERASE RESUME command, respectively.</p> <p>If the bits of the least significant address, which is the starting address, are not all zero, all data transmitted beyond the end of the current page is programmed from the starting address of the same page. If the number of bytes sent to the device exceed the maximum page size, previously latched data is discarded and only the last maximum page-size number of data bytes are guaranteed to be programmed correctly within the same page. If the number of bytes sent to the device is less than the maximum page size, they are correctly programmed at the specified addresses without any effect on the other bytes of the same page. Due to its nature, Octal DDR operation requires bus transition in even number, therefore for program operation the following restrictions apply:</p> <ul style="list-style-type: none"> – If there is a need to program from odd starting address, keep the even input address and the input data shall start with "FFh" – If there is a need to program with odd ending address, simply provide an extra data with "FFh" in the last falling edge of clock
OCTAL INPUT FAST PROGRAM (82h)	
EXTENDED OCTAL INPUT FAST PROGRAM (C2h)	

4-BYTE PROGRAM Operations

Table 31: 4-BYTE PROGRAM Operations

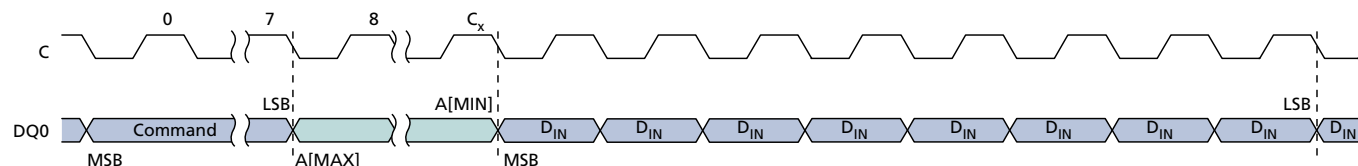
Operation Name	Description/Conditions
4-BYTE PAGE PROGRAM (12h)	<p>PROGRAM operations can be extended to a 4-bytes address range, with [A31:0] input during address cycle.</p> <p>Selection of the 3-byte or 4-byte address range can be enabled in two ways: through the nonvolatile configuration register or through the ENABLE 4-BYTE ADDRESS MODE/EXIT 4-BYTE ADDRESS MODE commands.</p>
4-BYTE OCTAL INPUT FAST PROGRAM (84h)	
4-BYTE EXTENDED OCTAL INPUT FAST PROGRAM (8Eh)	



512Mb, 1.8V Xcelera Flash Memory PROGRAM Operations Timings

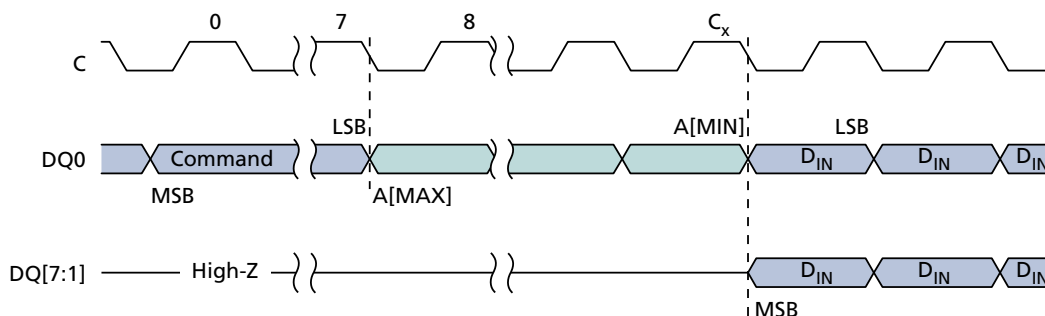
PROGRAM Operations Timings

Figure 23: PAGE PROGRAM – 02h/12h



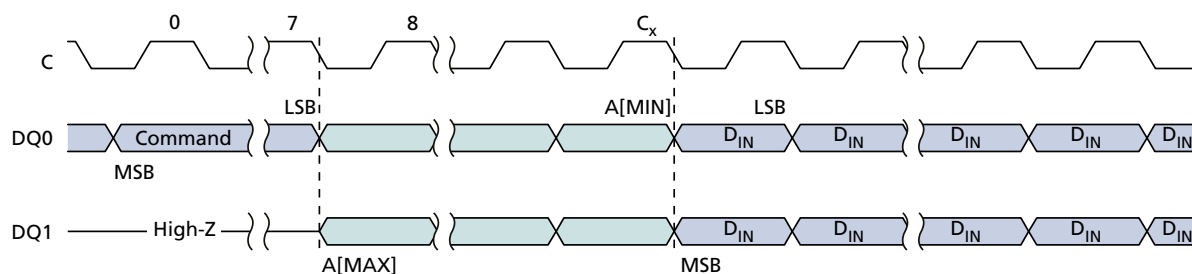
- Notes:
1. $C_x = 7 + (A[MAX]) + 1$. Requires 32-bit address in 4-byte address configuration.
 2. In octal DDR protocol, command, address, and data-out bits are transmitted on all eight data pins in DDR mode, and address is fixed with 4-byte.
 3. S# not shown. The operation is self-timed, and its duration is t_{PP} .

Figure 24: OCTAL INPUT FAST PROGRAM – 82h/84h



- Notes:
1. $C_x = 7 + (A[MAX]) + 1$. Requires 32-bit address in 4-byte address configuration.
 2. In octal DDR protocol, command, address, and data-out bits are transmitted on all eight data pins in DDR mode, and address is fixed with 4-byte.
 3. S# not shown. The operation is self-timed, and its duration is t_{PP} .

Figure 25: EXTENDED OCTAL INPUT FAST PROGRAM – C2h/8Eh



- Notes:
1. $C_x = 7 + (A[MAX]) + 1/8$. Requires 32-bit address in 4-byte address configuration.
 2. In octal DDR protocol, command, address, and data-out bits are transmitted on all eight data pins in DDR mode, and address is fixed with 4-byte.
 3. S# not shown. The operation is self-timed, and its duration is t_{PP} .



512Mb, 1.8V Xccela Flash Memory ERASE Operations

ERASE Operations

An ERASE operation changes a bit from 0 to 1. Before any ERASE command is initiated, the WRITE ENABLE command must be executed to set the write enable latch bit to 1; if not, the device ignores the command and no error bits are set to indicate operation failure. S# is driven LOW and held LOW until the eighth bit of the last data byte has been latched in, after which it must be driven HIGH. The operations are self-timed, and duration is ^tSSE, ^tSE, or ^tBE according to command.

If S# is not driven HIGH, the command is not executed, flag status register error bits are not set, and the write enable latch remains set to 1. A command applied to a protected subsector is not executed. Instead, the write enable latch bit remains set to 1, and flag status register bits 1 and 5 are set.

When the operation is in progress, the program or erase controller bit of the flag status register is set to 0. In addition, the write in progress bit is set to 1. When the operation completes, the write in progress bit is cleared to 0. The write enable latch bit is cleared to 0, whether the operation is successful or not. If the operation times out, the write enable latch bit is reset and the erase error bit is set to 1.

The status register and flag status register can be polled for the operation status. When the operation completes, these register bits are cleared to 1.

Note: For all ERASE operations, noisy or undesirable signal effects can be reduced and device data protection enhanced by holding S# LOW until the eighth bit of the last data byte has been latched in; this ensures that the number of clock pulses is a multiple of one byte before command execution.

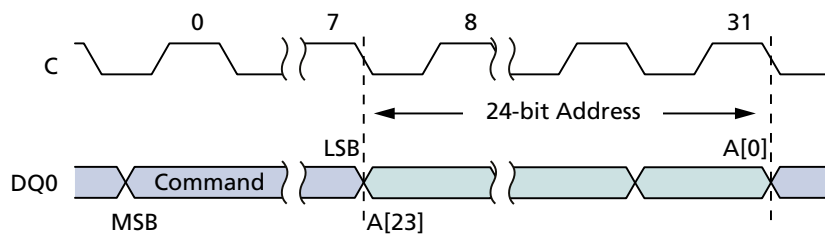
Table 32: ERASE Operations

Operation Name	Description/Conditions
SUBSECTOR ERASE (52h/20h)	Sets the selected subsector or sector bits to FFh. Any address within the subsector is valid for entry. Each address bit is latched in during the rising edge of the clock. The operation can be suspended and resumed by the PROGRAM/ERASE SUSPEND and PROGRAM/ERASE RESUME commands, respectively.
SECTOR ERASE (D8h)	
BULK ERASE (C7h/60h)	Sets the device bits to FFh. The command is not executed if any sector is locked. Instead, the write enable latch bit remains set to 1, and flag status register bits 1 and 5 are set.



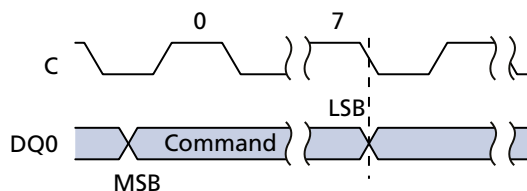
512Mb, 1.8V Xcelera Flash Memory ERASE Operations

Figure 26: SUBSECTOR and SECTOR ERASE Timing



- Notes:
1. Requires 32-bit address in 4-byte address configuration.
 2. In octal DDR protocol, command, address, and data-out bits are transmitted on all eight data pins in DDR mode, and address is fixed with 4-byte.
 3. S# not shown. The operation is self-timed, and its duration is t_{SSE}/t_{SE} .

Figure 27: BULK ERASE Timing



- Notes:
1. In octal DDR protocol, command is transmitted on all eight data pins in DDR mode.
 2. S# not shown. The operation is self-timed, and its duration is t_{BE} .



512Mb, 1.8V Xcella Flash Memory SUSPEND/RESUME Operations

SUSPEND/RESUME Operations

PROGRAM/ERASE SUSPEND Operations

A PROGRAM/ERASE SUSPEND command enables the memory controller to interrupt and suspend an array PROGRAM or ERASE operation within the program/erase latency. To initiate the command, S# is driven LOW, and the command code is input on DQn. The operation is terminated by the PROGRAM/ERASE RESUME command.

For a PROGRAM SUSPEND, the flag status register bit 2 is set to 1. For an ERASE SUSPEND, the flag status register bit 6 is set to 1.

After an erase/program latency time, the flag status register bit 7 is also set to 1, but the device is considered in suspended state once bit 7 of the flag status register outputs 1 with at least one byte output. In the suspended state, the device is waiting for any operation.

If the time remaining to complete the operation is less than the suspend latency, the device completes the operation and clears the flag status register bits 2 or 6, as applicable. Because the suspend state is volatile, if there is a power cycle, the suspend state information is lost and the flag status register powers up as 80h.

It is possible to nest a PROGRAM/ERASE SUSPEND operation inside a PROGRAM/ERASE SUSPEND operation just once. Issue an ERASE command and suspend it. Then issue a PROGRAM command and suspend it also. With the two operations suspended, the next PROGRAM/ERASE RESUME command resumes the latter operation, and a second PROGRAM/ERASE RESUME command resumes the former (or first) operation.

PROGRAM/ERASE RESUME Operations

To initiate the command, S# is driven LOW, and the command code is input on DQn. The operation is terminated by driving S# HIGH.

Table 33: SUSPEND/RESUME Operations

Operation Name	Description/Conditions
PROGRAM SUSPEND (75h)	A READ operation is possible in any page except the one in a suspended state. Reading from a sector that is in a suspended state will output indeterminate data.
ERASE SUSPEND (75h)	<p>A PROGRAM or READ operation is possible in any sector except the one in a suspended state. Reading from a sector that is in a suspended state will output indeterminate data. During a SUSPEND SUBSECTOR ERASE operation, reading an address in the sector that contains the suspended subsector could output indeterminate data.</p> <p>The device ignores a PROGRAM command to a sector that is in an erase suspend state; it also sets the flag status register bit 4 to 1 (program failure/protection error) and leaves the write enable latch bit unchanged.</p> <p>When the ERASE resumes, it does not check the new lock status of the WRITE VOLATILE LOCK BITS command.</p>



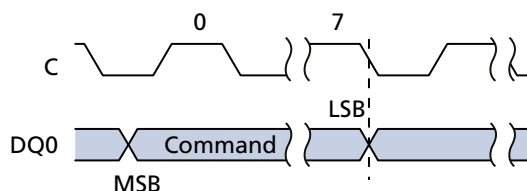
512Mb, 1.8V Xccela Flash Memory SUSPEND/RESUME Operations

Table 33: SUSPEND/RESUME Operations (Continued)

Operation Name	Description/Conditions
PROGRAM RESUME (7Ah)	<p>The status register write in progress bit is set to 1 and the flag status register program erase controller bit is set to 0. The command is ignored if the device is not in a suspended state.</p> <p>When the operation is in progress, the program or erase controller bit of the flag status register is set to 0. The flag status register can be polled for the operation status. When the operation completes, that bit is cleared to 1.</p>
ERASE RESUME (7Ah)	

Note: 1. See the Operations Allowed/Disallowed During Device States table.

Figure 28: PROGRAM/ERASE SUSPEND or RESUME Timing



- Notes:
1. In octal DDR protocol command is transmitted on all eight data pins.
 2. S# not shown.



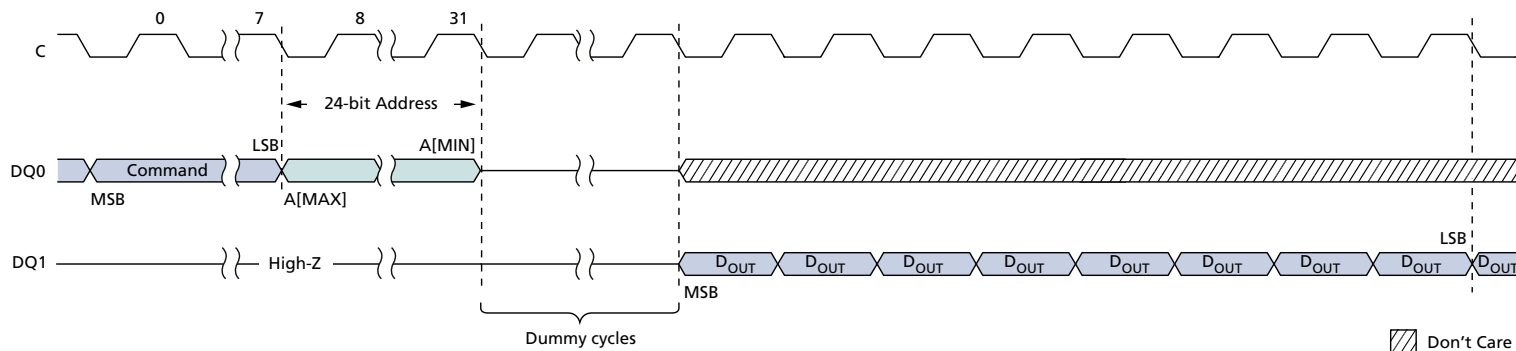
512Mb, 1.8V Xcelera Flash Memory ONE-TIME PROGRAMMABLE Operations

ONE-TIME PROGRAMMABLE Operations

READ OTP ARRAY Command

To initiate a READ OTP ARRAY command, S# is driven LOW. The command code is input on DQ0, followed by address bytes and dummy clock cycles. Each address bit is latched in during the rising edge of C. Data is shifted out on DQ1, beginning from the specified address and at a maximum frequency of f_C (MAX) on the falling edge of the clock. The address increments automatically to the next address after each byte of data is shifted out. There is no rollover mechanism; therefore, if read continuously, after location 0x40, the device continues to output data at location 0x40. The operation is terminated by driving S# HIGH at any time during data output.

Figure 29: READ OTP Command



- Notes:
1. Requires 32-bit address in 4-byte address configuration.
 2. In octal DDR protocol, command, address, and data-out bits are transmitted on all eight data pins in DDR mode, and address is fixed with 4-byte.
 3. S# not shown.

PROGRAM OTP ARRAY Command

To initiate the PROGRAM OTP ARRAY command, the WRITE ENABLE command must be issued to set the write enable latch bit to 1; otherwise, the PROGRAM OTP ARRAY command is ignored and flag status register bits are not set. S# is driven LOW and held LOW until the eighth bit of the last data byte has been latched in, after which it must be driven HIGH. The command code is input on DQ0, followed by address bytes and at least one data byte. Each address bit is latched in during the rising edge of the clock. When S# is driven HIGH, the operation, which is self-timed, is initiated; its duration is t_{POTP} . There is no rollover mechanism; therefore, after a maximum of 65 bytes are latched in the subsequent bytes are discarded.

PROGRAM OTP ARRAY programs, at most, 64 bytes to the OTP memory area and one OTP control byte. When the operation is in progress, the write in progress bit is set to 1. The write enable latch bit is cleared to 0, whether the operation is successful or not, and the status register and flag status register can be polled for the operation status. When the operation completes, the write in progress bit is cleared to 0.

If the operation times out, the write enable latch bit is reset and the program fail bit is set to 1. If S# is not driven HIGH, the command is not executed, flag status register error



512Mb, 1.8V Xccela Flash Memory ONE-TIME PROGRAMMABLE Operations

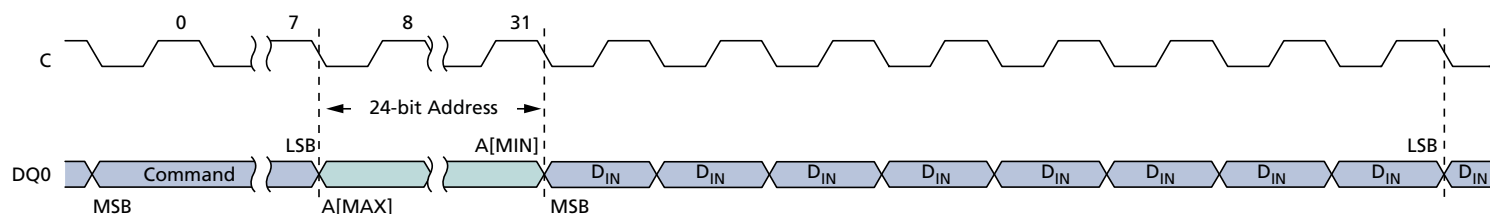
bits are not set, and the write enable latch remains set to 1. The operation is considered complete once bit 7 of the flag status register outputs 1 with at least one byte output.

The OTP control byte (byte 64) is used to permanently lock the OTP memory array.

Table 34: OTP Control Byte (Byte 64)

Bit	Name	Settings	Description
0	OTP control byte	0 = Locked 1 = Unlocked (Default)	Used to permanently lock the 64-byte OTP array. When bit 0 = 1, the 64-byte OTP array can be programmed. When bit 0 = 0, the 64-byte OTP array is read only. Once bit 0 has been programmed to 0, it can no longer be changed to 1. Program OTP array is ignored, the write enable latch bit remains set, and flag status register bits 1 and 4 are set.

Figure 30: PROGRAM OTP Command



- Notes:
1. Requires 32-bit address in 4-byte address configuration.
 2. In octal DDR protocol, command, address, and data-out bits are transmitted on all eight data pins in DDR mode, and address is fixed with 4-byte.
 3. S# not shown.

**512Mb, 1.8V Xcelera Flash Memory
ADDRESS MODE Operations****ADDRESS MODE Operations****ENTER and EXIT 4-BYTE ADDRESS MODE Command**

To initiate these commands, $S\#$ is driven LOW, and the command is input on DQn .

Table 35: ENTER and EXIT 4-BYTE ADDRESS MODE Operations

Operation Name	Description/Conditions
ENTER 4-BYTE ADDRESS MODE (B7h)	The effect of the command is immediate. The default address mode is three bytes, and the device returns to the default upon exiting the 4-byte address mode.
EXIT 4-BYTE ADDRESS MODE (E9h)	



512Mb, 1.8V Xccela Flash Memory CYCLIC REDUNDANCY CHECK Operations

CYCLIC REDUNDANCY CHECK Operations

A CYCLIC REDUNDANCY CHECK (CRC) operation is a hash function designed to detect accidental changes to raw data and is used commonly in digital networks and storage devices such as hard disk drives. A CRC-enabled device calculates a short, fixed-length binary sequence, known as the CRC code or just CRC, for each block of data. CRC can be a higher performance alternative to reading data directly in order to verify recently programmed data. Or, it can be used to check periodically the data integrity of a large block of data against a stored CRC reference over the life of the product. CRC helps improve test efficiency for programmer or burn-in stress tests. No system hardware changes are required to enable CRC.

The CRC-64 operation follows the ECMA standard. The generating polynomial is:

$$G(x) = x^{64} + x^{62} + x^{57} + x^{55} + x^{54} + x^{53} + x^{52} + x^{47} + x^{46} + x^{45} + x^{40} + x^{39} + x^{38} + x^{37} + x^{35} + x^{33} + x^{32} + x^{31} + x^{29} + x^{27} + x^{24} + x^{23} + x^{22} + x^{21} + x^{19} + x^{17} + x^{13} + x^{12} + x^{10} + x^9 + x^7 + x^4 + x + 1$$

Note: The data stream sequence is from LSB to MSB and the default initial CRC value is all zero.

The device CRC operation generates the CRC result of the entire device or of an address range specified by the operation. Then the CRC result is compared with the expected CRC data provided in the sequence. Finally the device indicates a pass or fail through the bit #4 of FLAG STATUS REGISTER. If the CRC fails, it is possible to take corrective action such as verifying with a normal read mode or by rewriting the array data.

CRC operation supports CRC data read back when CRC check fails; the CRC data generated from the target address range or entire device will be stored in a dedicated register GPRR (general purpose read register) only when CRC check fails, and it can be read out through the GPRR read sequence with command 96h, least significant byte first. GPRR is reset to default all 0 at the beginning of the CRC operation, and so customer will read all 0 if CRC operation pass.

Note that the GPRR is a volatile register. It is cleared to all 0s on power-up and hardware/software reset. Read GPRR starts from the first location, when clocked continuously, will wrap after location 64.

The CYCLIC REDUNDANCY CHECK operation command sequences are shown in the tables below, for an entire die or for a selected range.

Table 36: CRC Command Sequence on Entire Device

Command Sequence		Description
Byte#	Data	
1	9Bh	Command code for interface activation
2	27h	Sub-command code for CRC operation
3	FFh	CRC operation option selection (CRC operation on entire device)
4	CRC[7:0]	1st byte of expected CRC value
5–10	CRC[55:8]	2nd to 7th byte of expected CRC value
11	CRC[63:56]	8th byte of expected CRC value
12	FFh	Data fill in only in DDR protocol
Drive S# HIGH		Operation sequence confirmed; CRC operation starts



512Mb, 1.8V Xccela Flash Memory CYCLIC REDUNDANCY CHECK Operations

Table 37: CRC Command Sequence on a Range

Command Sequence		Description
Byte#	Data	
1	9Bh	Command code for interface activation
2	27h	Sub-command code for CRC operation
3	FEh	CRC operation option selection (CRC operation on a range)
4	CRC[7:0]	1st byte of expected CRC value
5 to 10	CRC[55:8]	2nd to 7th byte of expected CRC value
11	CRC[63:56]	8th byte of expected CRC value
12	Start Address [7:0]	Specifies the starting byte address for CRC operation
13 to 14	Start Address [23:8]	
15	Start Address [31:24]	
16	Stop Address [7:0]	Specifies the ending byte address for CRC operation
17 to 18	Stop Address [23:8]	
19	Stop Address [31:24]	
20	FFh	
Drive S# HIGH		Operation sequence confirmed; CRC operation starts



512Mb, 1.8V Xcelera Flash Memory State Table

State Table

The device can be in only one state at a time. Depending on the state of the device, some operations as shown in the table below are allowed (Yes) and others are not (No). For example, when the device is in the standby state, all operations except SUSPEND are allowed in any sector. For all device states except the erase suspend state, if an operation is allowed or disallowed in one sector, it is allowed or disallowed in all other sectors. In the erase suspend state, a PROGRAM operation is allowed in any sector except the one in which an ERASE operation has been suspended.

Table 38: Operations Allowed/Disallowed During Device States

Operation	Standby State	Program or Erase State	Subsector Erase Suspend or Program Suspend State	Erase Suspend State	Notes
READ	Yes	No	Yes	Yes	1
READ (status/flag status registers)	Yes	Yes	Yes	Yes	6
PROGRAM	Yes	No	No	Yes/No	2
ERASE (sector/subsector)	Yes	No	No	No	3
WRITE	Yes	No	No	No	4
WRITE	Yes	No	Yes	Yes	5
SUSPEND	No	Yes	No	No	7

- Notes:
1. All READ operations except READ STATUS REGISTER and READ FLAG REGISTER. When issued to a sector or subsector that is simultaneously in an erase suspend state, the READ operation is accepted, but the data output is not guaranteed until the erase has completed.
 2. All PROGRAM operations except PROGRAM OTP. In the erase suspend state, a PROGRAM operation is allowed in any sector (Yes) except the sector (No) in which an ERASE operation has been suspended.
 3. Applies to the SECTOR ERASE or SUBSECTOR ERASE operation.
 4. Applies to the following operations: WRITE STATUS REGISTER, WRITE NONVOLATILE CONFIGURATION REGISTER, PROGRAM OTP, and BULK ERASE.
 5. Applies to the WRITE VOLATILE CONFIGURATION REGISTER, WRITE ENABLE, WRITE DISABLE, CLEAR FLAG STATUS REGISTER, or WRITE LOCK REGISTER operation.
 6. Applies to the READ STATUS REGISTER or READ FLAG STATUS REGISTER operation.
 7. Applies to the PROGRAM SUSPEND or ERASE SUSPEND operation.



512Mb, 1.8V Xcelia Flash Memory XIP Mode

XIP Mode

Execute-in-place (XIP) mode allows the memory to be read by sending an address to the device and then receiving the data on one or eight pins in parallel, depending on the customer requirements. XIP mode offers maximum flexibility to the application, saves instruction overhead, and reduces random access time.

Activate or Terminate XIP Using Volatile Configuration Register

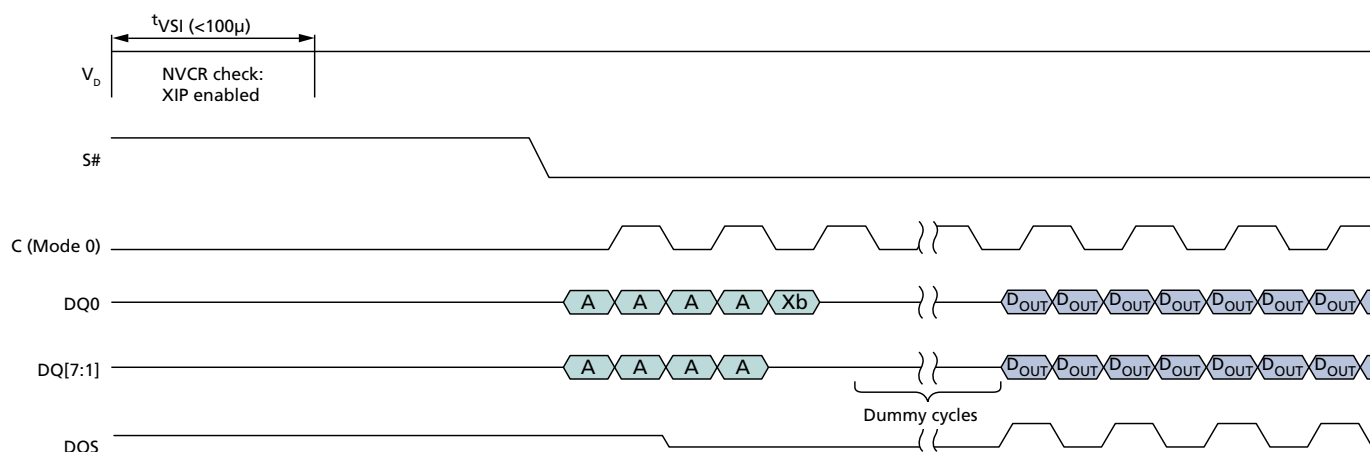
Applications that boot in SPI and must switch to XIP use the volatile configuration register. XIP provides faster memory READ operations by requiring only an address to execute, rather than a command code and an address.

To activate XIP requires two steps. First, enable XIP by setting volatile configuration register (byte 6). Next, drive the XIP confirmation bit to 0 during the next FAST READ operation. XIP is then active. Once in XIP, any command that occurs after S# is toggled requires only address bits to execute; a command code is not necessary, and device operations use the SPI protocol that is enabled. XIP is terminated by driving the XIP confirmation bit to 1. The device automatically resets the XIP volatile configuration register to FFh.

Activate or Terminate XIP Using Nonvolatile Configuration Register

Applications that must boot directly in XIP use the nonvolatile configuration register. To enable a device to power-up in XIP using this register, set nonvolatile configuration register (byte 6). Settings vary according to protocol, as explained in the Nonvolatile Configuration Register section. Because the device boots directly in XIP, after the power cycle, no command code is necessary. XIP is terminated by driving the XIP confirmation bit to 1.

Figure 31: XIP Mode Entered at Power-On

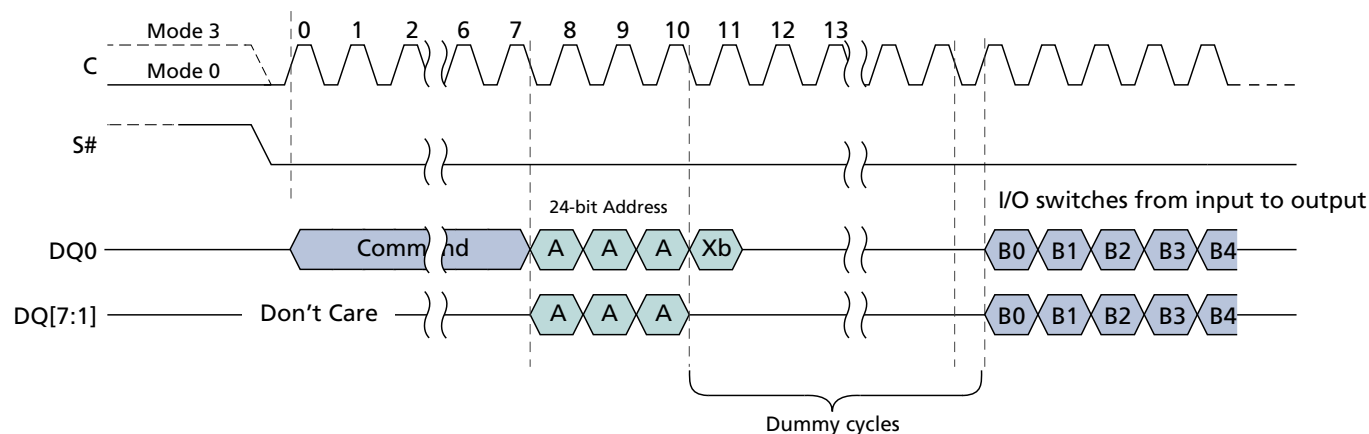


- Notes:
1. Xb is the XIP confirmation bit and should be set as follows: 0 to keep XIP state; 1 to exit XIP mode and return to standard read mode.
 2. Example of NVCR.06h = FEh; 8IOFR XIP in octal DDR protocol.



512Mb, 1.8V Xcelera Flash Memory XIP Mode

Figure 32: XIP Mode Entry by Volatile Configuration Register



Note: 1. Xb is the XIP confirmation bit and should be set as follows: 0 to keep XIP state; 1 to exit XIP mode and return to standard read mode.

Confirmation Bit Settings Required to Activate or Terminate XIP

The XIP confirmation bit setting activates or terminates XIP after it has been enabled or disabled. This bit is the value on DQ0 during the first dummy clock cycle in the FAST READ operation. In octal I/O XIP mode, the values of DQ[7:1] during the first dummy clock cycle after the addresses are always "Don't Care."

Table 39: XIP Confirmation Bit

Bit Value	Description
0	Activates XIP: While this bit is 0, XIP remains activated.
1	Terminates XIP: When this bit is set to 1, XIP is terminated and the device returns to SPI.

Table 40: Effects of Running XIP in Different Protocols

Protocol	Effect
Extended I/O	A LOW pulse on RESET# pin resets XIP and the device to the state it was in previous to the last power-up, as defined by the nonvolatile configuration register.
Octal I/O	Values of DQ[7:1] during the first dummy clock cycle are "Don't Care."



512Mb, 1.8V Xcela Flash Memory Power-Up and Power-Down

Terminating XIP After a Controller and Memory Reset

The system controller and the device can become out of synchronization if, during the life of the application, the system controller is reset without the device being reset. In such a case, the controller can reset the memory to power-on reset by using RESET# pin.

The following sequences cause the controller to set the XIP confirmation bit to 1, thereby terminating XIP. However, it does not reset the device or interrupt PROGRAM/ERASE operations that may be in progress. After terminating XIP, the controller must execute RESET ENABLE and RESET MEMORY to implement a software reset and reset the device. It's required to have DQ0 equal to 1 for the situations listed here:

- 3 clock cycles within S# LOW (S# becomes HIGH before 4th clock cycle) +
- 4 clock cycles within S# LOW (S# becomes HIGH before 5th clock cycle) +
- 5 clock cycles within S# LOW (S# becomes HIGH before 6th clock cycle) +
- 25 clock cycles within S# LOW (S# becomes HIGH before 26th clock cycle) +
- 33 clock cycles within S# LOW (S# becomes HIGH before 34th clock cycle)

Power-Up and Power-Down

Power-Up and Power-Down Requirements

At power-up and power-down, the device must not be selected; that is, S# must follow the voltage applied on V_{CC} until V_{CC} reaches the correct values: $V_{CC,min}$ at power-up and V_{SS} at power-down.

To provide device protection and prevent data corruption and inadvertent WRITE operations during power-up, a power-on reset circuit is included. The logic inside the device is held to RESET while V_{CC} is less than the power-on reset threshold voltage shown here; all operations are disabled, and the device does not respond to any instruction. During a standard power-up phase, the device ignores all commands except READ STATUS REGISTER and READ FLAG STATUS REGISTER. These operations can be used to check the memory internal state. After power-up, the device is in standby power mode; the write enable latch bit is reset; the write in progress bit is reset; and the dynamic protection register is configured as (write lock bit, lock down bit) = (0,0).

Normal precautions must be taken for supply line decoupling to stabilize the V_{CC} supply. Each device in a system should have the V_{CC} line decoupled by a suitable capacitor (typically 100nF) close to the package pins. At power-down, when V_{CC} drops from the operating voltage to below the power-on-reset threshold voltage shown here, all operations are disabled and the device does not respond to any command.

When the operation is in progress, the program or erase controller bit of the status register is set to 0. To obtain the operation status, the flag status register must be polled. When the operation completes, the program or erase controller bit is cleared to 1. The cycle is complete after the flag status register outputs the program or erase controller bit to 1.

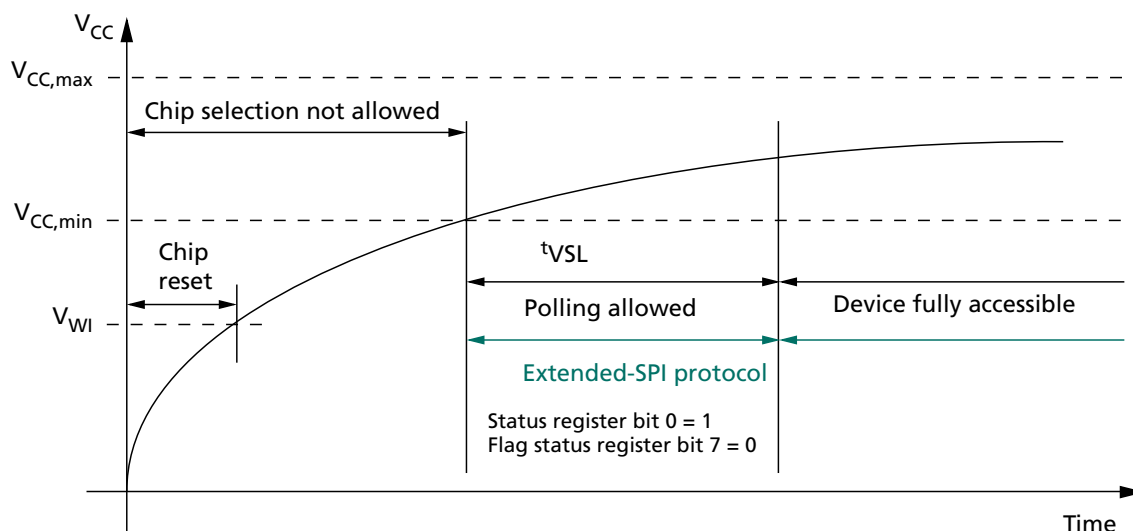
Note: If power-down occurs while a WRITE, PROGRAM, or ERASE cycle is in progress, data corruption may result.

V_{PPH} must be applied only when V_{CC} is stable and in the $V_{CC,min}$ to $V_{CC,max}$ voltage range.



512Mb, 1.8V Xcelera Flash Memory Power-Up and Power-Down

Figure 33: Power-Up Timing



- Notes:
1. t_{VSL} polling has to be in extended-SPI protocol and SDR mode.
 2. During t_{VSL} period, output strength is default setting and DQS is disabled.
 3. In a system that uses a fast V_{CC} ramp rate, current design requires a minimum 100 μ s after V_{CC} reaches V_{WI} , and before the polling is allowed, even though $V_{CC,min}$ is achieved.

Table 41: Power-Up Timing and V_{WI} Threshold

Note 1 applies to entire table

Symbol	Parameter	Min	Max	Unit	Notes
t_{VSL}	$V_{CC,min}$ to device fully accessible	–	300	μ s	2, 3
V_{WI}	Write inhibit voltage	1.0	1.5	V	2

- Notes:
1. When V_{CC} reaches $V_{CC,min}$, to determine whether power-up initialization is complete, the host can poll status register bit 0 or flag status register bit 7 only in extended SPI protocol because the device will accept commands only on DQ0 and output data only on DQ1. When the device is ready, the host has full access using the protocol configured in the nonvolatile configuration register. If the host cannot poll the status register in $\times 1$ SPI mode, it is recommended to wait t_{VSL} before accessing the device.
 2. Parameters listed are characterized only.
 3. On the first power-up after an event causing a sub-sector ERASE operation interrupt (for example, due to power-loss), the maximum time for t_{VSL} will be up to 4.5ms in case of 4KB subsector erase interrupt and up to 36ms in case of 32KB sub-sector erase interrupt; this accounts for erase recovery embedded operation.



512Mb, 1.8V Xcelera Flash Memory Power Loss and Interface Rescue

Power Loss and Interface Rescue

If a power loss occurs during a WRITE NONVOLATILE CONFIGURATION REGISTER command, after the next power-on, the device might begin in an undetermined state (XIP mode or an unnecessary protocol). If this occurs, a power loss recovery sequence must reset the device to a fixed state (default SPI protocol without XIP) until the next power-up.

If the controller and memory device get out of synchronization, the controller can follow an interface rescue sequence to reset the memory device interface to power-up to the last reset state (as defined by latest nonvolatile configuration register). This resets only the interface, not the entire memory device, and any ongoing operations are not interrupted.

After each sequence, the issue should be resolved definitively by running the WRITE NONVOLATILE CONFIGURATION REGISTER command again.

Note: The two steps in each sequence must be in the correct order.

First Step – Power Loss Recovery and Interface Rescue

The first step in both the power loss recovery and interface rescue sequences is DQ0 (PAD DATA) equal to 1 for the situations listed here:

- 3 clock cycles within S# LOW (S# becomes HIGH before 4th clock cycle) +
- 4 clock cycles within S# LOW (S# becomes HIGH before 5th clock cycle) +
- 5 clock cycles within S# LOW (S# becomes HIGH before 6th clock cycle) +
- 25 clock cycles within S# LOW (S# becomes HIGH before 26th clock cycle) +
- 33 clock cycles within S# LOW (S# becomes HIGH before 34th clock cycle)

Second Step – Power Loss Recovery

For power loss recovery, the second step in the sequence is exiting from present SPI protocol by using the following FFh sequence: DQ[7:0] equal to 1 for 8 clock cycles within S# LOW; S# becomes HIGH before 9th clock cycle. DQ[7:0] equal "1" should be driven on both edges of clock for 8 cycles with S# LOW. After this two-part sequence the default SPI protocol is active.

Second Step – Interface Rescue

For interface rescue, the second step in the sequence is exiting from present SPI protocol by using the following FFh sequence: DQ[7:0] equal to 1 for 16 clock cycles within S# LOW; S# becomes HIGH before 17th clock cycle. DQ[7:0] equal "1" should be driven on both edges of clock for 16 cycles with S# LOW. After this two-part sequence the device will be in the protocol defined by NVCR setting from latest power-up or reset.



512Mb, 1.8V Xccela Flash Memory Initial Delivery Status

Initial Delivery Status

The device is delivered as the following:

- Memory array erased: all bits are set to 1 (each byte contains FFh)
- All sectors un-protected
- Status register contains 00h (all status register bits are 0)
- Nonvolatile configuration register in default state



512Mb, 1.8V Xcelera Flash Memory Absolute Ratings and Operating Conditions

Absolute Ratings and Operating Conditions

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only. Exposure to absolute maximum rating for extended periods may adversely affect reliability. Stressing the device beyond the absolute maximum ratings may cause permanent damage.

Table 42: Absolute Ratings

Symbol	Parameter	Min	Max	Units	Notes
T _{STG}	Storage temperature	-65	150	°C	
T _{LEAD}	Lead temperature during soldering	–	See note 1	°C	
V _{CC}	Supply voltage	-0.6	2.4	V	2
V _{PP}	Fast program voltage	-0.2	10	V	
V _{IO}	I/O voltage with respect to ground	-0.6	V _{CC} + 0.6	V	2
V _{ESD}	Electrostatic discharge voltage (human body model)	-2000	2000	V	2, 3

- Notes:
1. Compliant with JEDEC Standard J-STD-020C (for small-body, Sn-Pb or Pb assembly), RoHS, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.
 2. All specified voltages are with respect to V_{SS}. During infrequent, nonperiodic transitions, the voltage potential between V_{SS} and the V_{CC} may undershoot to -2.0V for periods less than 20ns, or overshoot to V_{CC,max} + 2.0V for periods less than 20ns.
 3. JEDEC Standard JESD22-A114A (C1 = 100pF, R1 = 1500Ω, R2 = 500Ω).

Table 43: Operating Conditions

Symbol	Parameter	Min	Max	Units
V _{CC}	Supply voltage	1.7	2.0	V
V _{PPH}	Supply voltage on V _{PP}	8.5	9.5	V
T _A	Ambient operating temperature	-40	85	°C
T _A	Ambient operating temperature (automotive)	-40	105	°C

Table 44: I/O Capacitance

Note 1 applies to entire table

Symbol	Description	Min	Max	Units
C _{IN/OUT}	I/O capacitance DQ[7:0], DQS, RESET#	–	5	pF
C _{IN}	Input capacitance (other pins)	–	3	pF
C _{IN/S#}	Input/Chip select	–	4	pF

- Note:
1. Verified in device characterization; not 100% tested. These parameters are not subject to a production test; they are verified by design and characterization. The capacitance is measured according to JEP147, "PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER (VNA)," with V_{CC} and V_{SS} applied and all other pins floating (except the pin under test), V_{BIAS} = V_{CC}/2, T_A = 25°C, frequency = 54 MHz.



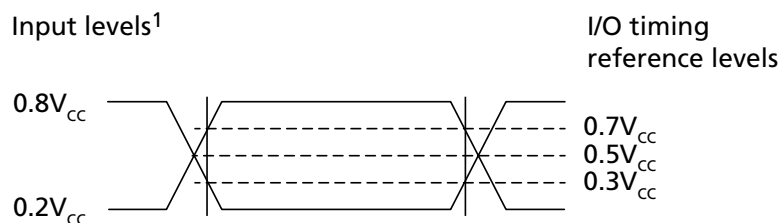
512Mb, 1.8V Xcela Flash Memory Absolute Ratings and Operating Conditions

Table 45: AC Timing I/O Conditions

Symbol	Description	Min	Max	Units	Notes
C_L	Load capacitance	–	12	pF	1
–	Input rise and fall times	–	1.2	ns	
	Input pulse voltages	$0.2V_{CC}$ to $0.8V_{CC}$		V	
	Input timing reference voltages	$0.3V_{CC}$ to $0.7V_{CC}$		V	
	Output timing reference voltages	$V_{CC}/2$		V	

Note: 1. Output buffers are configurable by user.

Figure 34: AC Timing I/O Reference Levels





512Mb, 1.8V Xcelera Flash Memory DC Characteristics and Operating Conditions

DC Characteristics and Operating Conditions

Table 46: DC Current Characteristics and Operating Conditions

Note 1 applies to entire table

Parameter	Symbol	Test Conditions	Typ	Max	Unit	Notes
Input leakage current	I_{LI}	–	–	± 2	μA	
Output leakage current	I_{LO}	–	–	± 2	μA	
Standby current	I_{CC1}	$S = V_{CC}, V_{IN} = V_{SS} \text{ or } V_{CC}$	25	100	μA	2
Standby current (Automotive)	I_{CC1}	$S = V_{CC}, V_{IN} = V_{SS} \text{ or } V_{CC}$	25	200	μA	2
Deep power-down current	I_{CC2}	$S = V_{CC}, V_{IN} = V_{SS} \text{ or } V_{CC}$	2	50	μA	3
Deep power-down current (Automotive)	I_{CC2}	$S = V_{CC}, V_{IN} = V_{SS} \text{ or } V_{CC}$	2	100	μA	3
Operating current (FAST READ EXTENDED I/O)	I_{CC3}	$C = 0.1V_{CC}/0.9V_{CC}$ at 133 MHz, DQ1 = open	–	16	mA	4
		$C = 0.1V_{CC}/0.9V_{CC}$ at 54 MHz, DQ1 = open	–	8	mA	4
		$C = 0.1V_{CC}/0.9V_{CC}$ at 166 MHz, DQ = open	–	60	mA	
		$C = 0.1V_{CC}/0.9V_{CC}$ at 200 MHz, DQ = open	–	70	mA	
Operating current (Octal SDR command)						
Operating current (Octal DDR command)						
Operating current (PROGRAM operations)	I_{CC4}	$S\# = V_{CC}$	–	40	mA	5
Operating current (WRITE operations)	I_{CC5}	$S\# = V_{CC}$	–	24	mA	
Operating current (ERASE operations)	I_{CC6}	$S\# = V_{CC}$	–	35	mA	

- Notes:
1. Currents are RMS unless noted. Typical values are at V_{CC} (3V); $V_{IO} = 0V/V_{CC}$; $T_C = +25^\circ C$.
 2. Standby current is an average calculated 5 μs after $S\#$ deassertion and completion of any internal operation.
 3. Deep power-down current is an average calculated during a 5ms time interval 100 μs after completion of any internal operation.
 4. Read current is an average calculated during a 1KB continuous READ operation without load, in a checker-board pattern.
 5. Program current is an average measured over a 256-byte data PROGRAM operation.



512Mb, 1.8V Xcela Flash Memory DC Characteristics and Operating Conditions

Table 47: DC Voltage Characteristics and Operating Conditions

Note applies to entire table

Parameter	Symbol	Conditions	Min	Max	Unit
Input low voltage (DC)	V_{IL}	–	–0.3	$0.3V_{CC}$	V
Input low voltage (AC)		–	–0.3	$0.2V_{CC}$	V
Input high voltage (DC)	V_{IH}	–	$0.7V_{CC}$	$V_{CC} + 0.3$	V
Input high voltage (AC)		–	$0.8V_{CC}$	$V_{CC} + 0.3$	V
Output low voltage	V_{OL}	$I_{OL} = 1.6\text{mA}$	–	$0.15 \times V_{CC}$	V
Output high voltage	V_{OH}	$I_{OH} = -100\mu\text{A}$	$0.85 \times V_{CC}$	–	V

Note: 1. V_{IL} can undershoot to -1.0V for periods less than 2ns ; V_{IH} can overshoot to $V_{CC,\text{max}} + 1.0\text{V}$ for periods less than 2ns .



512Mb, 1.8V Xcelera Flash Memory AC Characteristics and Operating Conditions

AC Characteristics and Operating Conditions

Table 48: AC Characteristics and Operating Conditions

Parameter	Symbol	Data Transfer Rate	Min	Typ	Max	Unit	Notes
Clock frequency for all commands other than READ	f_C	SDR	DC	–	166	MHz	
		DDR	DC	–	200		
Clock frequency for READ command (03h)	f_R	SDR	DC	–	54	MHz	
Clock HIGH time	t_{CH}	SDR	2.7	–	3.3	ns	2
		DDR	2.25	–	2.75		
Clock LOW time	t_{CL}	SDR	2.7	–	3.3	ns	2
		DDR	2.25	–	2.75		
Clock rise time (peak-to-peak)	t_{CLCH}	SDR/DDR	1/1.2	–	–	V/ns	3, 4
Clock fall time (peak-to-peak)	t_{CHCL}	SDR/DDR	1/1.2	–	–	V/ns	3, 4
S# active setup time (relative to clock)	t_{SLCH}	SDR/DDR	2.25	–	–	ns	
S# not active hold time (relative to clock)	t_{CHSL}	SDR/DDR	2	–	–	ns	
Data in setup time	t_{DVCH}	SDR/DDR	1.8/0.4	–	–	ns	
	t_{DVCL}	DDR only	0.4	–	–	ns	
Data in hold time	t_{CHDX}	SDR/DDR	1.8/0.4	–	–	ns	
	t_{CLDX}	DDR only	0.4	–	–	ns	
S# active hold time (relative to clock)	t_{CHSH}	SDR	2	–	–	ns	
		DDR	2	–	–		
S# not active setup time (relative to clock)	t_{SHCH}	SDR	2	–	–	ns	
		DDR	2	–	–	ns	
S# deselect time after a READ command	t_{SHSL1}	SDR/DDR	10	–	–	ns	
S# deselect time after a nonREAD command	t_{SHSL2}	SDR/DDR	30	–	–	ns	
Output disable time	t_{SHQZ}	SDR/DDR	–	–	6	ns	3
Data Valid Window	t_{DVW}	DDR	1.3	–	–	ns	
Clock low to output valid (Cload = 12pf)	t_{CLQV}	SDR/DDR	–	–	6	ns	5
Clock high to output valid (Cload = 12pf)	t_{CHQV}	DDR	–	–	6	ns	5
Output hold skew	t_{QHS}	DDR	–	–	0.5	ns	
DQS to last DQ valid	t_{DQSQ}	DDR	–	–	0.4	ns	
DQS low after first clock	t_{CLQSL}	DDR	–	–	10	ns	6
S# to DQS High-Z	t_{SHQSZ}	DDR	–	–	6	ns	
Output hold time	t_{CLQX}	SDR/DDR	1.3	–	–	ns	5
Output hold time	t_{CHQX}	DDR only	1.3	–	–	ns	5
Write protect setup time	t_{WHSL}	SDR/DDR	20	–	–	ns	7
Enhanced V_{ppH} HIGH to S# LOW	t_{VPPHSL}	SDR/DDR	200	–	–	ns	7
S# HIGH to deep power-down	t_{DP}	SDR/DDR	3	–	–	μ s	



512Mb, 1.8V Xcelera Flash Memory AC Characteristics and Operating Conditions

Table 48: AC Characteristics and Operating Conditions (Continued)

Parameter	Symbol	Data Transfer Rate	Min	Typ	Max	Unit	Notes
S# HIGH to standby mode (DPD exit time)	t_{RDP}	SDR/DDR	30	–	–	μs	
WRITE STATUS REGISTER cycle time	t_W	SDR/DDR	–	1.3	8	ms	
WRITE NONVOLATILE CONFIGURATION REGISTER cycle time	t_{WNVCR}	SDR/DDR	–	0.2	1	s	
WRITE PROTECTION MANAGEMENT REGISTER timing	t_{PPMR}	SDR/DDR	–	0.1	0.5	ms	
Nonvolatile sector lock time	t_{PPBP}	SDR/DDR	–	0.1	2.8	ms	
Program ASP register	t_{ASPP}	SDR/DDR	–	0.1	0.5	ms	
Program password	t_{PASSP}	SDR/DDR	–	0.2	0.8	ms	
Erase nonvolatile sector lock array	t_{PPBE}	SDR/DDR	–	0.2	1	s	
Page program time (256 bytes)	t_{PP}	SDR/DDR	–	120	1800	μs	8
Page program time with $V_{pp}=V_{PPH}$ (256 bytes)	t_{PP}	SDR/DDR	–	80	1800	μs	8
PROGRAM OTP cycle time (64 bytes)	t_{POTP}	SDR/DDR	–	0.2	0.8	ms	
Sector erase time	t_{SE}	SDR/DDR	–	0.2	1	s	
4KB subsector erase time	t_{SSE}	SDR/DDR	–	20	400	ms	
32KB subsector erase time	t_{SSE}	SDR/DDR	–	0.1	1	s	
512Mb bulk erase time	t_{BE}	SDR/DDR	–	80	400	s	

- Notes:
1. Typical values given for $T_A = 25\text{ }^{\circ}\text{C}$.
 2. $t_{CH} + t_{CL}$ must add up to $1/f_C$.
 3. Value guaranteed by characterization; not 100% tested.
 4. Expressed as a slew-rate.
 5. The specification only applies when DQS is disabled.
 6. DQS will be driven with the first clock falling edge after S# LOW.
 7. Only applicable as a constraint for a WRITE STATUS REGISTER command when STATUS REGISTER WRITE is set to 1.
 8. Typical value is applied for pattern: 50% "0" and 50% "1."



512Mb, 1.8V Xcelera Flash Memory AC Reset Specifications

AC Reset Specifications

Table 49: AC Reset Conditions

Note 1 applies to entire table

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reset pulse width	t_{RLRH}^2		50	–	–	ns
Reset recovery time	t_{RHSL}	Device deselected (S# HIGH) and is in XIP mode	40	–	–	ns
		Device deselected (S# HIGH) and is in standby mode	40	–	–	ns
		Commands are being decoded, any READ operations are in progress or any WRITE operation to volatile registers are in progress	40	–	–	ns
		Any device array PROGRAM/ERASE/SUSPEND/RESUME, PROGRAM OTP, NONVOLATILE SECTOR LOCK, and ERASE NONVOLATILE SECTOR LOCK ARRAY operations are in progress	30	–	–	μ s
		While a WRITE STATUS REGISTER operation is in progress	–	t_W	–	ms
		While a WRITE NONVOLATILE CONFIGURATION REGISTER operation is in progress	–	t_{WNVCR}	–	ms
		On completion or suspension of a SUBSECTOR ERASE operation	–	t_{SSE}	–	s
		Device in deep power-down mode	–	t_{RDP}	–	ms
		While ADVANCED SECTOR PROTECTION PROGRAM operation is in progress	–	t_{ASPP}	–	ms
		While PASSWORD PROTECTION PROGRAM operation is in progress	–	t_{PASSP}	–	ms
Software reset recovery time	t_{SHSL3}	Device deselected (S# HIGH) and is in standby mode	40	–	–	ns
		Any flash array PROGRAM/ERASE/SUSPEND/RESUME, PROGRAM OTP, NONVOLATILE SECTOR LOCK, and ERASE NONVOLATILE SECTOR LOCK ARRAY operations are in progress	30	–	–	μ s
		While WRITE STATUS REGISTER operation is in progress	–	t_W	–	ms
		While a WRITE NONVOLATILE CONFIGURATION REGISTER operation is in progress	–	t_{WNVCR}	–	ms
		On completion/suspension of SUBSECTOR ERASE operation	–	t_{SSE}	–	s
		Device in deep power-down mode	–	t_{RDP}	–	ms
		While ADVANCED SECTOR PROTECTION PROGRAM operation is in progress	–	t_{ASPP}	–	ms
		While PASSWORD PROTECTION PROGRAM operation is in progress	–	t_{PASSP}	–	ms
Chip select high to reset high	t_{SHRH}	Chip must be deselected before reset is de-asserted	10	–	–	ns

- Notes: 1. Values are guaranteed by characterization; not 100% tested.
2. The device reset is possible but not guaranteed if $t_{RLRH} < 50$ ns.



512Mb, 1.8V Xcelera Flash Memory AC Reset Specifications

Figure 35: Reset AC Timing During PROGRAM or ERASE Cycle

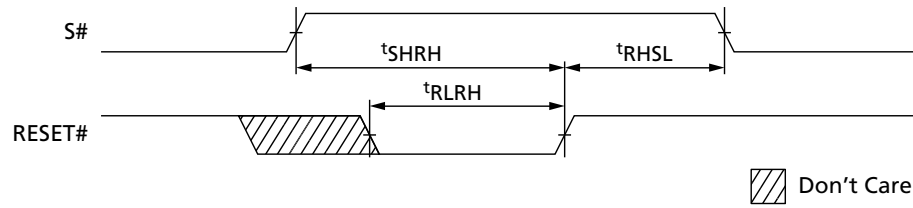


Figure 36: Serial Input Timing

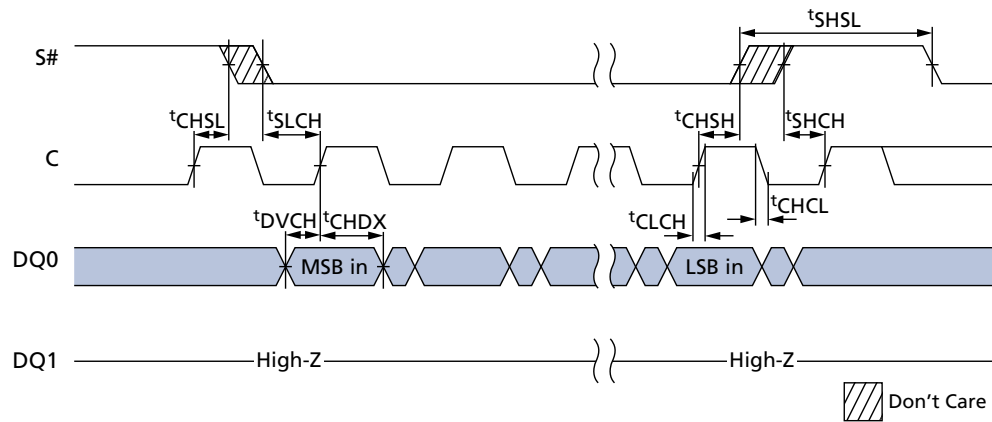
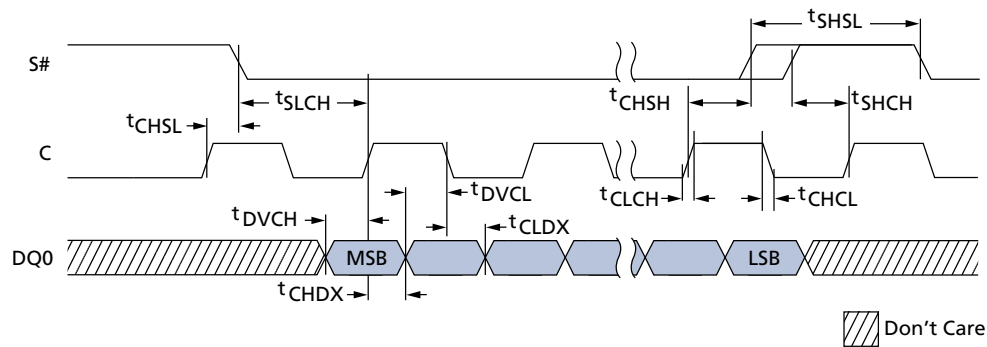


Figure 37: Serial Input Timing – DDR





512Mb, 1.8V Xcelera Flash Memory AC Reset Specifications

Figure 38: Write Protect Setup and Hold During WRITE STATUS REGISTER Operation (SRWD = 1)

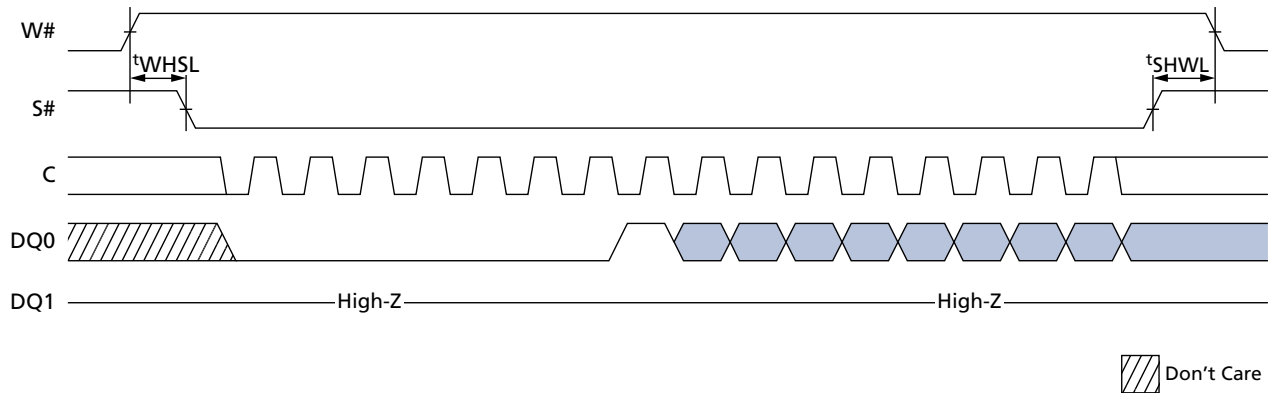


Figure 39: Output Timing – SDR

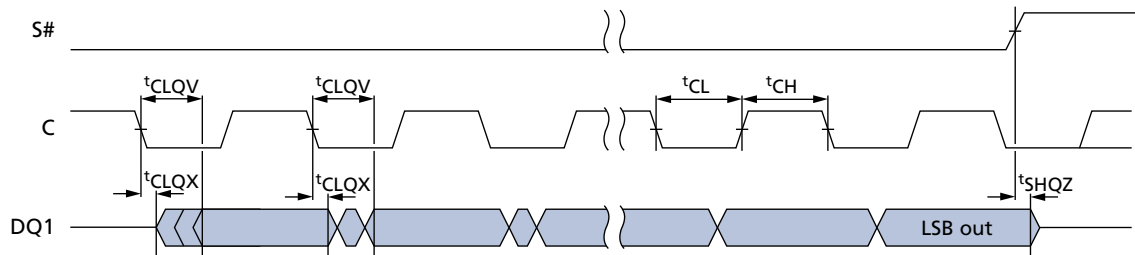
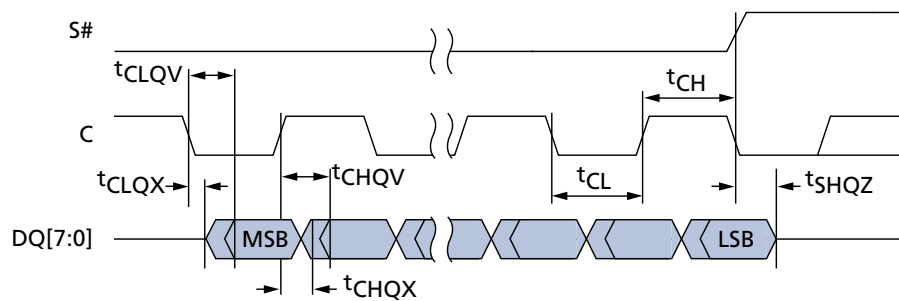


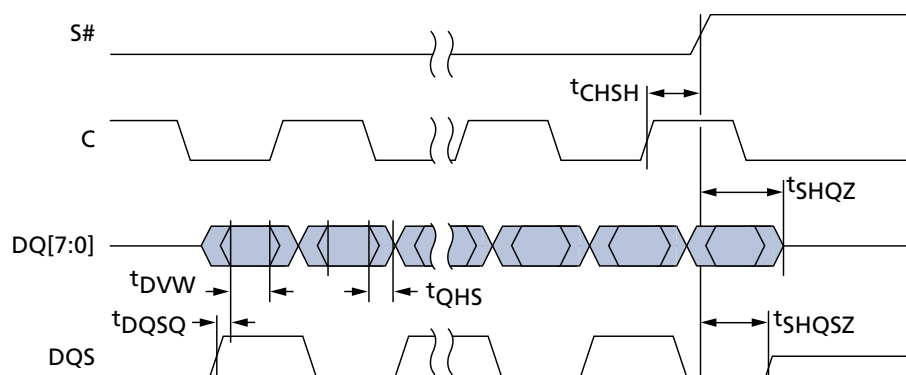
Figure 40: Output Timing – DDR





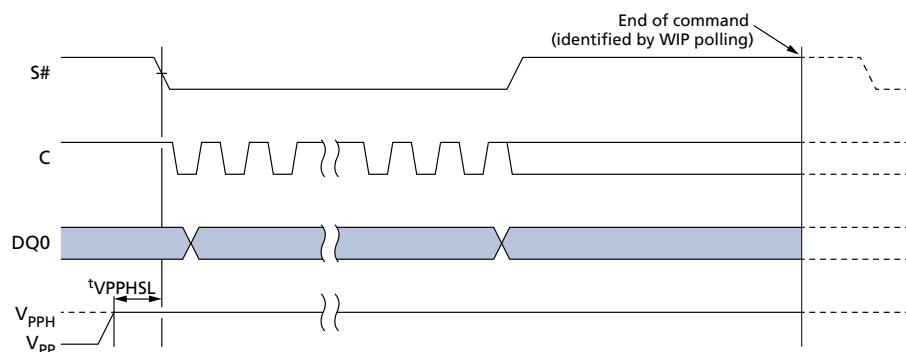
512Mb, 1.8V Xcelera Flash Memory AC Reset Specifications

Figure 41: Output Timing – DDR with DQS



Note: 1. The device will be de-selected while clock is HIGH to get even counts of output data. Next DQ (or DQS) output could be observed if clock falling edge is received before S# goes HIGH.

Figure 42: V_{PPH} Timing





512Mb, 1.8V Xcela Flash Memory Program/Erase Specifications

Program/Erase Specifications

Table 50: Program/Erase Specifications

Parameter	Condition	Typ	Max	Units	Notes
Erase to suspend	Sector erase or erase resume to erase suspend	150	–	μs	1
Program to suspend	Program resume to program suspend	5	–	μs	1
Subsector erase to suspend	Subsector erase or subsector erase resume to erase suspend	50	–	μs	1
Suspend latency	Program	7	25	μs	2
Suspend latency	Subsector erase	15	30	μs	2
Suspend latency	Erase	15	30	μs	3

- Notes:
1. Timing is not internally controlled.
 2. Any READ command accepted.
 3. Any command except the following are accepted: SECTOR, SUBSECTOR, or BULK ERASE; WRITE STATUS REGISTER; WRITE NONVOLATILE CONFIGURATION REGISTER; and PROGRAM OTP.



512Mb, 1.8V Xccela Flash Memory Revision History

Revision History

Rev. F – 06/17

- Updated Serial Flash Discovery Parameter Data section: Reviewed paragraph
- Added automotive I_{CC} currents in DC Current Characteristics and Operating Conditions table
- Changed document number from 09005aef864b038a to CCMTD-1725822587-3962

Rev. E – 12/16

- General review
- Changed XTRMFlash™ to Xccela™ flash

Rev. D – 08/16

- Added Nonvolatile Lock Bit Security Register
- Added Protection Management Register
- Updated Device ID Data table in Device ID Data section
- Added general purpose read register notes to Command Definitions table
- Modified octal figure of READ STATUS REGISTER – 05h in READ REGISTER Operations section
- Added octal figure of WRITE CONFIGURATION REGISTER in WRITE REGISTER Operations section
- Added Initial Delivery Status
- Change I_{CC3}, I_{CC4}, and I_{CC5} values
- Added output hold time - t_{CVQX} in AC Characteristics and Operating Conditions table

Rev. C – 01/16

- Removed SO16W package
- Added V_{PP} for program
- Changed status from Advanced to Preliminary

Rev. B – 10/15

- Updated language for XTRMFlash memory

Rev. A – 04/15

- Initial release

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-4000

www.micron.com/products/support Sales inquiries: 800-932-4992

Micron and the Micron logo are trademarks of Micron Technology, Inc.

All other trademarks are the property of their respective owners.

This data sheet contains initial characterization limits that are subject to change upon full characterization of production devices.