INNOLUX 群創光電

INNOLUX DISPLAY CORPORATION

Application Notes

Type : FOG

Customer:

Model Name: P101JEA-3Z1

Date: 2015/05/20

Version: V02

Approved by	Reviewed by	Prepared by
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INNOLUX 群創光電

REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver 01	2014/10/01	All	All	Initial Release
Ver 02	2015/05/20	15	7.3	新增靜電防護建議項目

INNOLUX 群創光電

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1. Module Introduction

Model name	Module photo	
	Top side	Bottom side
P101JEA-3Z1		

2. Pin Assignment

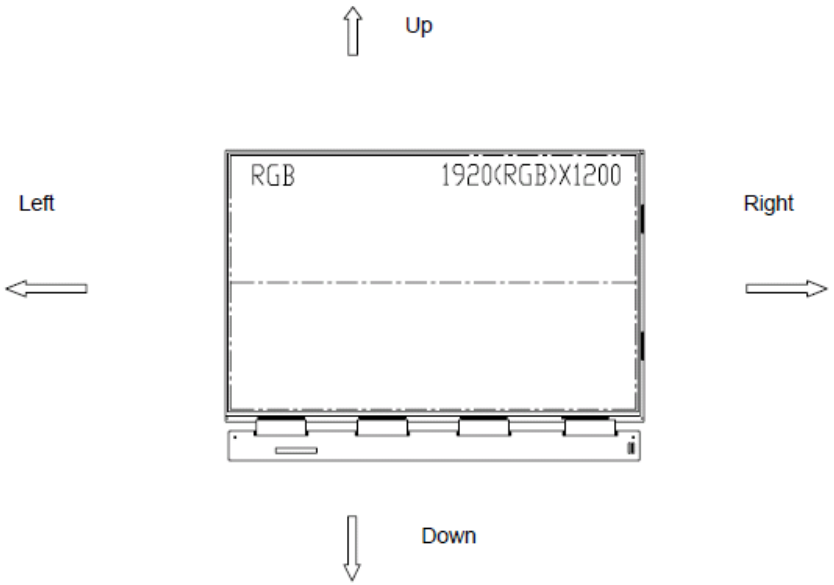
A 40pin connector is used for the module electronics interface. In this model used "FH33J-40S-0.5SH(10)" manufactured by Vigorconn.

Pin No.	Symbol	Description	Remark
1	VCOM	Common Voltage type:3.69 V	3.32~4.04V
2	VDD	Power supply for interface system except MIPI interface pin, VDDIN=3.3V	
3	VDD		
4	NC	NC	
5	Reset	Device reset signal(1.8V)	
6	NC	NC	
7	GND	GROUND	
8	RXIN0-	MIPI Negative data signal (-)	
9	RXIN0+	MIPI Positive data signal (+)	
10	GND	GROUND	
11	RXIN1-	MIPI Negative data signal (-)	
12	RXIN1+	MIPI Positive data signal (+)	
13	GND	GROUND	
14	RXCLKIN-	MIPI Negative clock signal (-)	
15	RXCLKIN+	MIPI Positive clock signal (+)	
16	GND	GROUND	
17	RXIN2-	MIPI Negative data signal (-)	
18	RXIN2+	MIPI Positive data signal (+)	
19	GND	GROUND	
20	RXIN3-	MIPI Negative data signal (-)	

21	RXIN3+	MIPI Negative data signal (+)	
22	GND	GROUND	
23	NC	No connection	
24	NC	No connection	
25	GND	GROUND	
26	PWMI	PWM input signal	
27	PWMO	PWM output signal	
28	NC	No connection	
29	AVDD	Power supply for analog circuits(9.89V)	
30	GND	GROUND	
31	LED-	LED cathode	
32	LED-		
33	NC	No connection	
34	NC	No connection	
35	VGL	Gate OFF Voltage(-6.8V)	
36	NC	No connection	
37	NC	No connection	
38	VGH	Gate ON Voltage(21.88V)	
39	LED+	LED anode	
40	LED+		

Note: Definition of scanning direction.

Refer to the figure as below:



3. Power Operation Conditions

3.1 Absolute Maximum Ratings

(Note 1)

Item	Symbol	Values		Unit	Remark
		Min.	Max.		
Power voltage	V_{CC}	-0.3	5.0	V	
	AV_{DD}	6.5	13.5	V	
	V_{GH}	-0.3	42	V	
	V_{GL}	VGH-42	0.3	V	
	V_{GH}-V_{GL}	-	42	V	
Operation Temperature	T_{OP}	-10	50	℃	
Storage Temperature	T_{ST}	-20	60	℃	

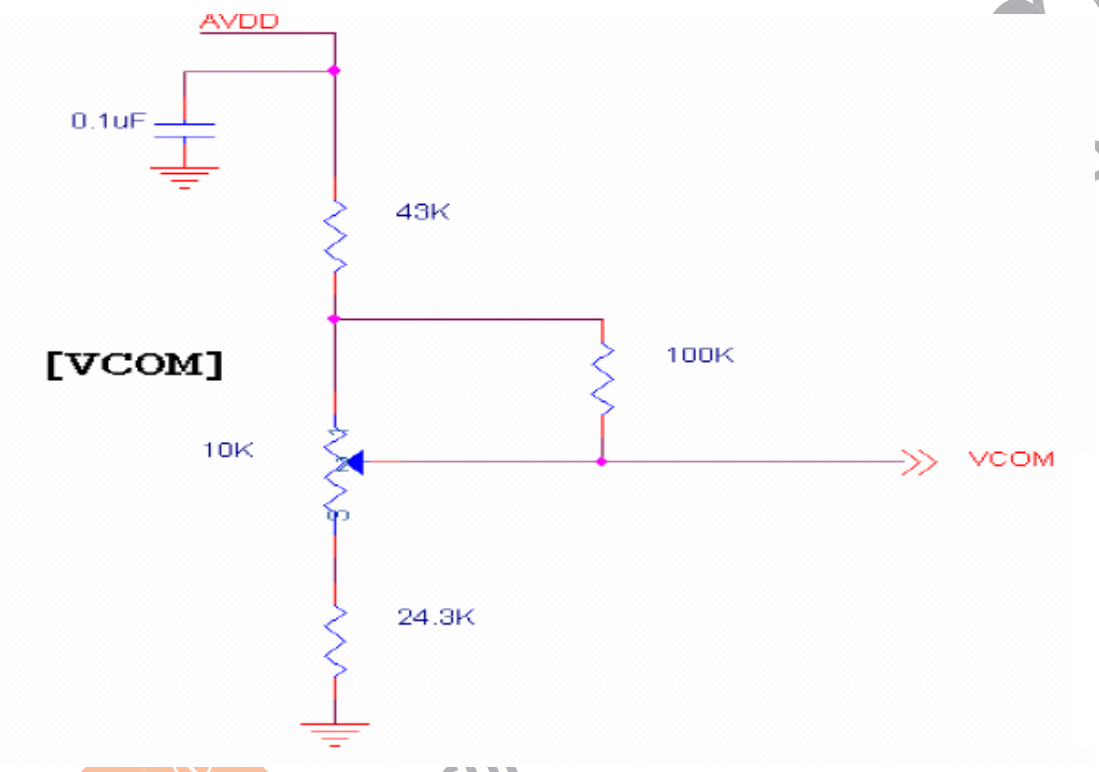
Note 1: The absolute maximum rating values of this product are not allowed to be exceeded at any times. Should a module be used with any of the absolute maximum ratings exceeded, the characteristics of the module may not be recovered, or in an extreme case, the module may be permanently destroyed.

3.2 Typical Operation Conditions

(Note 1)

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Power voltage	V_{CC}	3.0	3.3	3.6	V	Note2
	AV_{DD}	9.69	9.89	10.09	V	
	V_{GH}	21.58	21.88	22.18	V	
	V_{GL}	-7.1	-6.8	-6.5	V	
Input signal voltage	V_{COM}	3.32	3.69	4.04	V	Note3
Input logic high voltage	V_{IH}	0.7V_{DD}	-	V_{DD}	V	
Input logic low voltage	V_{IL}	0	-	0.3V_{DD}	V	

Note 1: Be sure to apply VDD and VGL to the LCD first, and then apply VGH.
Note 2: VDD setting should match the signals output voltage (refer to Note 3) of customer's system board.
Note 4: Typical VCOM is only a reference value, it must be optimized according to each LCM. Be sure to use VR.



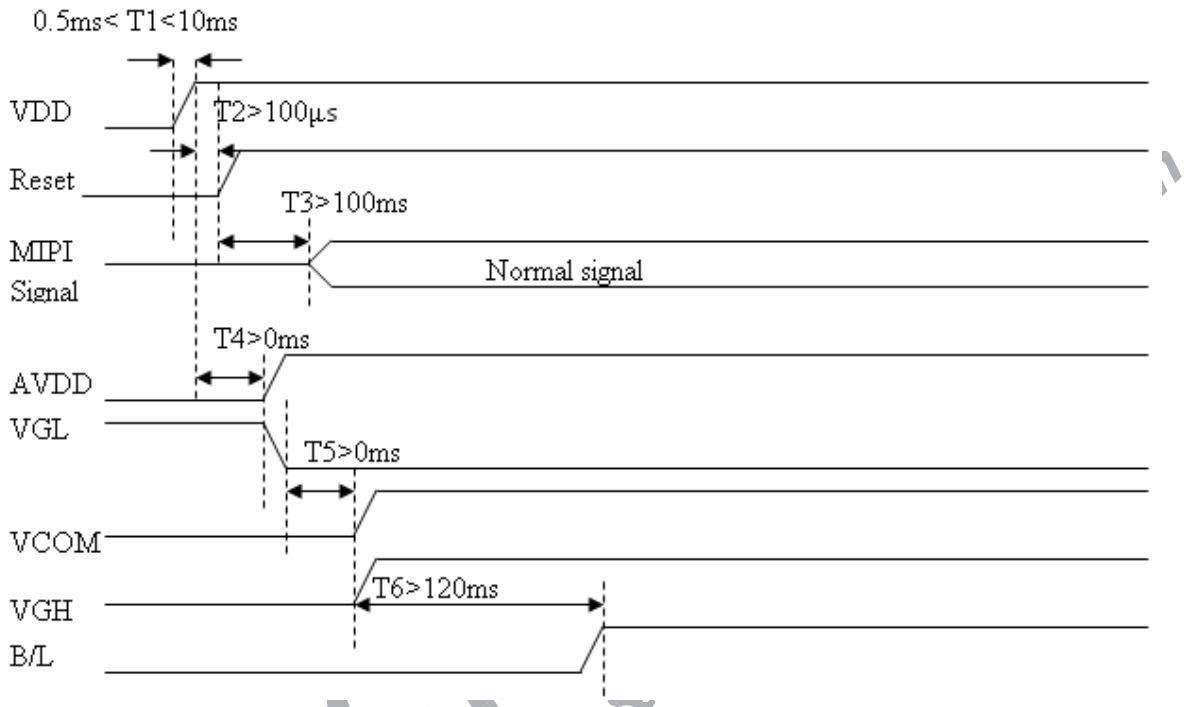
3.3 Current Consumption

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Current for Driver	I_{GH}	-	1.0	-	mA	VGH=21.88 V
	I_{GL}	-	3.0	-	mA	VGL=-6.8 V
	I_{CC}	-	100	-	mA	V_{DD}=3.3V
	IAV_{DD}	-	55	-	mA	AVDD=9.89V V

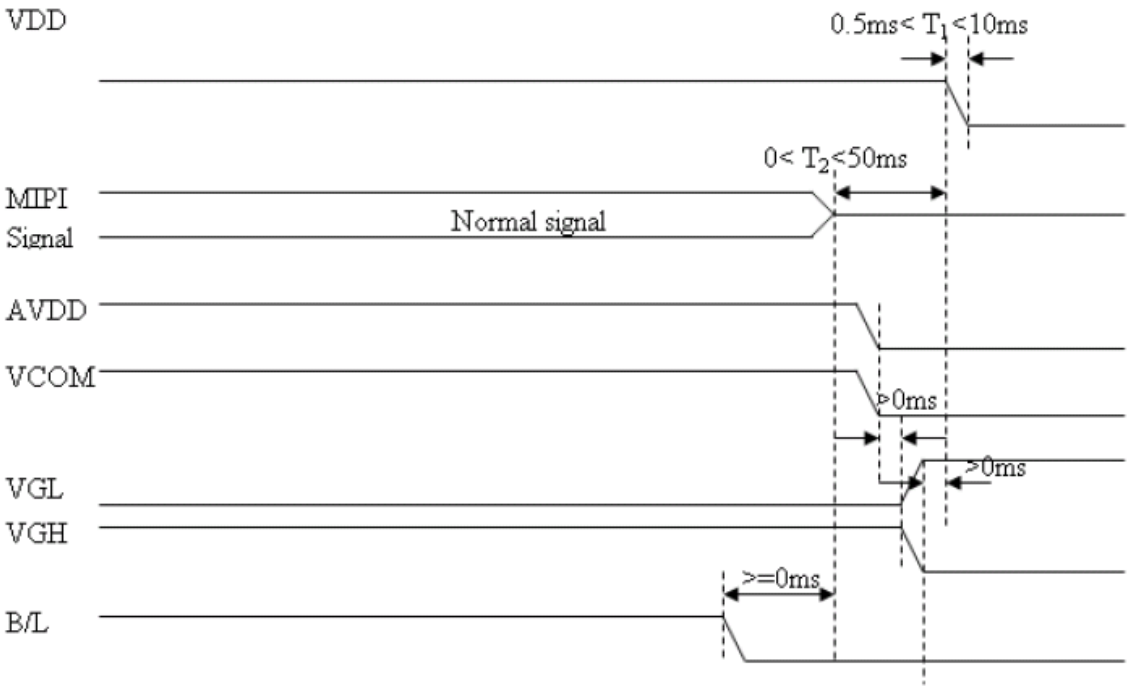
4. Power Sequence

請確實依照規範之Power Sequence進行設計，以避免造成顯示異常或產品損壞等問題。

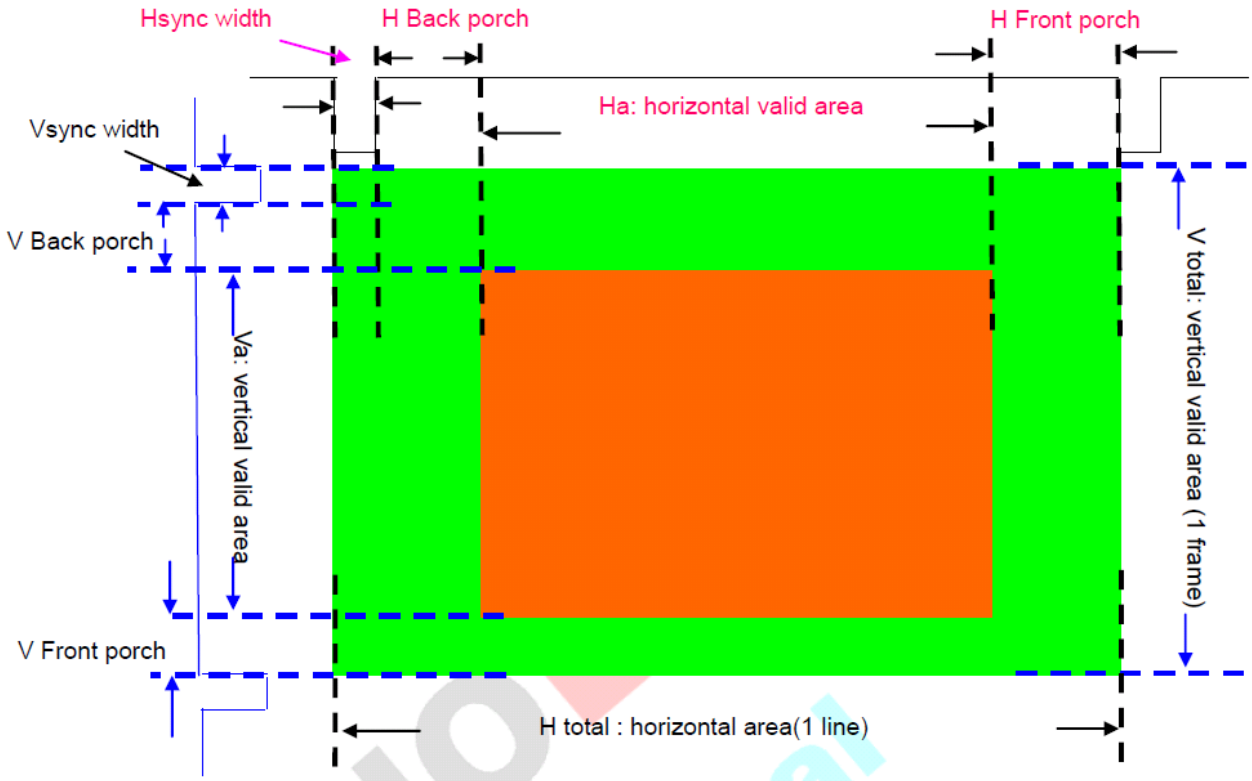
4.1 Power on:



4.2 Power off



5. Timing Characteristics



Timing Formula:

DCLK = (Hw + Hbp + Ha +Hfp)*(Vw + Vbp + Va +Vfp)*Fvsync (Unit : Hz)

Fhsync = (Vw+ Vbp + Va +Vfp)*Fvsync (Unit: Hz)

Remark: 1. Fhsync is Hsync frequency, and Fvsync is Vsync frequency.
2. Parameter Table .

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Clock Frequency	fclk		150.11		MHz	Frame rate =60
Horizontal display area	thd		1920			
HS period time	th		2044		DCLK	
HS Blanking	thb+thfp		124		DCLK	
Vertical display area	tvd		1200			
VS period time	tv		1224		H	
VS Blanking	tvb+tvfp		24		H	

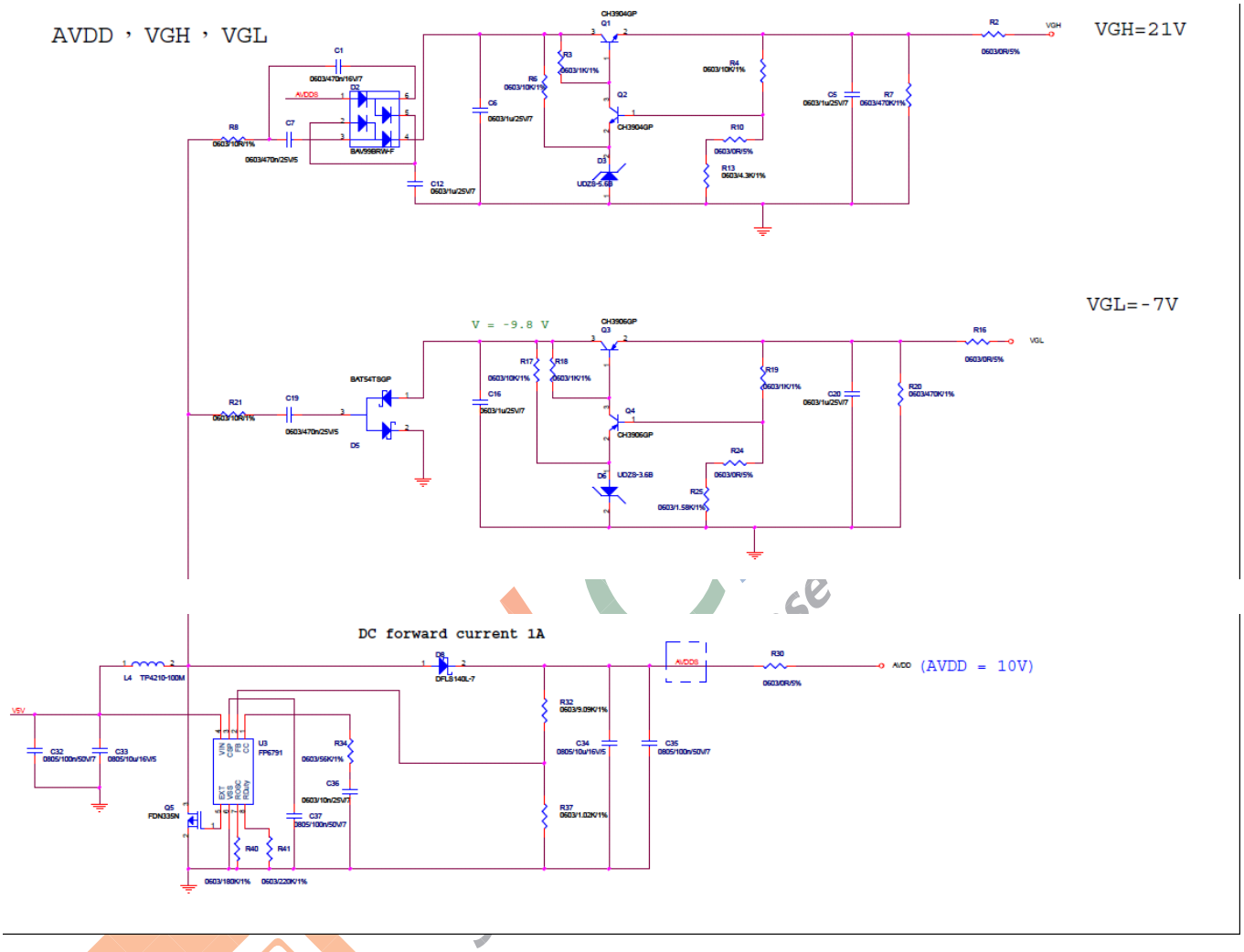
Notes 2. EDID code 參考值

Item	Description	EDID
1	Pixel clock	08
2	Pixel clock	39
3	H active	80
4	H blank	2D
5	H active H blank	70
6	V active	B0
7	V blank	2D
8	V active V blank	40
9	H sync offset	14
10	H sync pulse width	05
11	V sync offset V sync pulse width	45
12	H sync offset : H sync pulse width : V sync offset : V sync width	04
13	H image size	D9
14	V image size	87
15	H image size : V image size	00
16	H boarder	00
17	V boarder	00
18	Non-interlaced, Normal,no stereo,Separate sync,H/V pol Negatives	18

根據 EDID Code 所設定視窗準位參數:

CLK=146.78MHz	
HFP= 20	VFP= 20
HBP= 20	VBP= 20
HPW= 5	VPW= 5
HVD= 1920	VVD= 1200

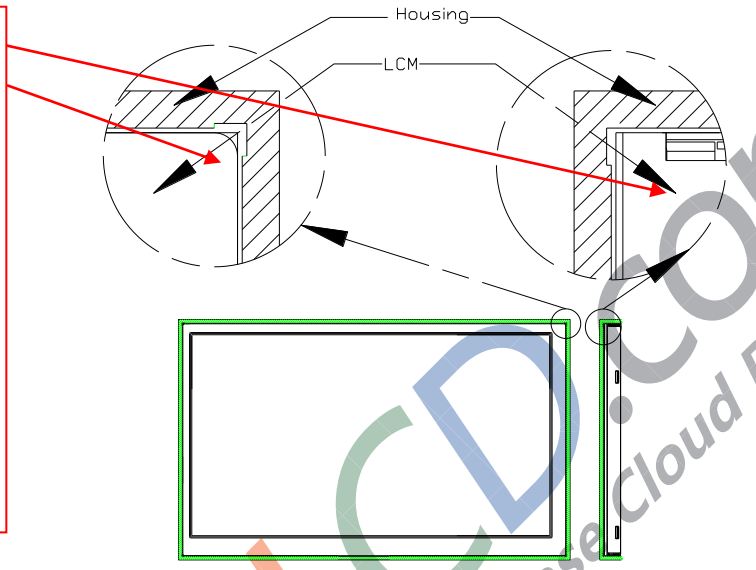
6. Reference Circuit



7. Suggestion for housing design

7.1 LCM corner /edge avoidable cutting.

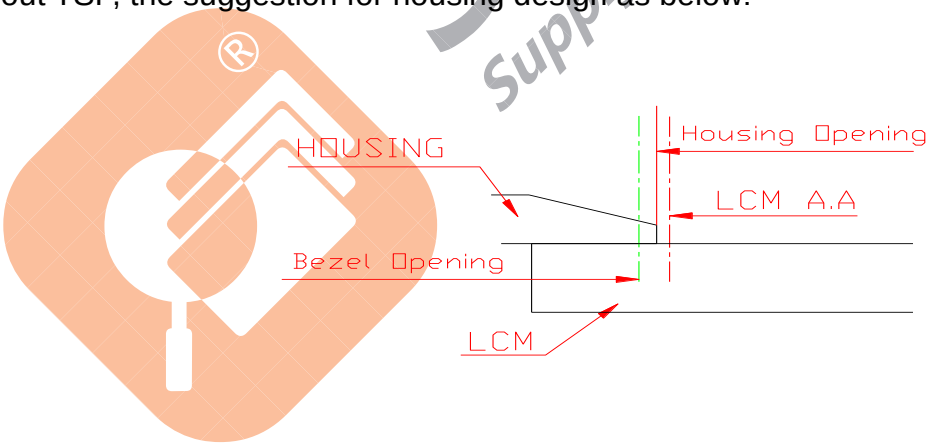
If you design a avoidable cutting as the right drawing. LCM will easier to assemble in the housing.
When you use the LCM with TSP, the cutting will avoid damage the edge or corner of TSP during the assembly.



7.2 Housing opening design guide.

7.2.1 Without TSP

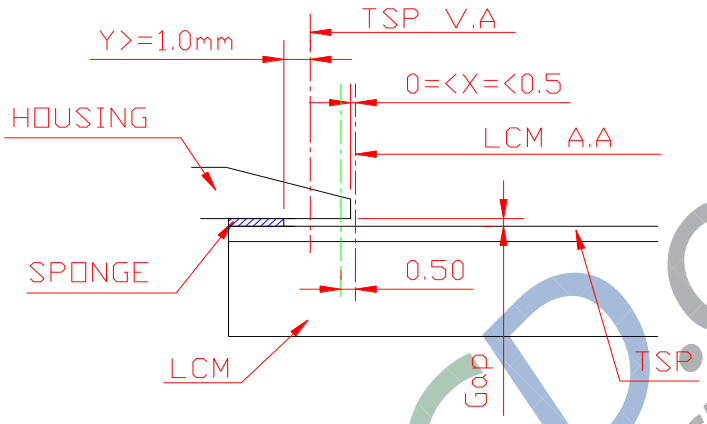
If without TSP, the suggestion for housing design as below:



Notes: 1. Housing opening mast bigger than LCMA.A and cover the bezel .
2. If you want to provide more protection for LCM, you can add same buffer material on the top or bottom of LCM

7.2.2 4-Wire Resistive Touch Screen Panel

Because touch film is made of flexible PET, any unexpected touch with it would cause malfunction of touch panel. So here a sponge between touch panel and plastic housing is recommended for users. And the drawing will show you how to design the housing and sponge.

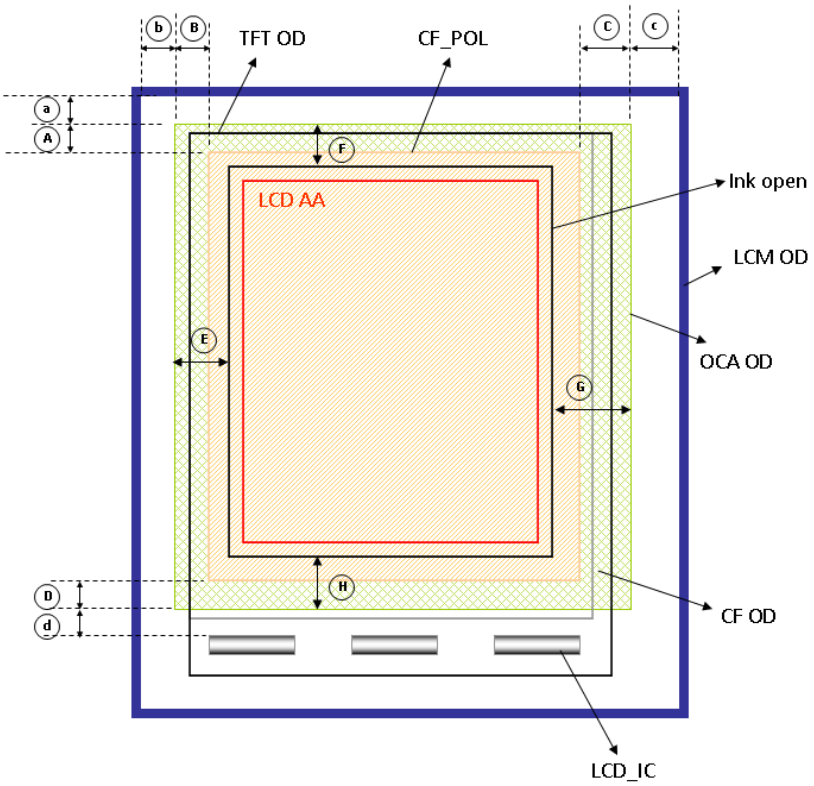


Section sketch (with TSP)

Notes: 1. X is the distance from LCM A.A to housing opening.
2. Y is the distance from TSP V.A to Sponge opening.
3. The active force will be bigger when you touch the area near the housing opening.
4. If you want to provide more protection for LCM, you can add same buffer material on the bottom of LCM.

7.2.3 Capacitive Touch Screen Panel (OGS)

If customer add the CTP on the LCM, the CTP Ink open window design guide as below:

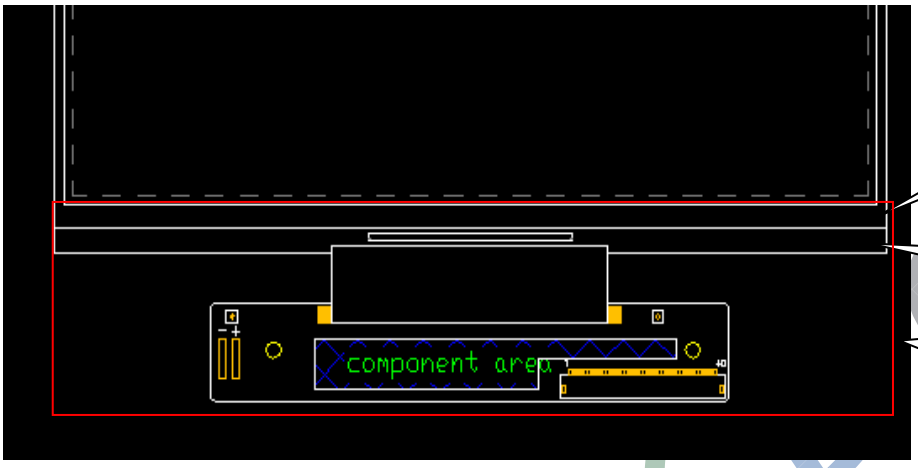


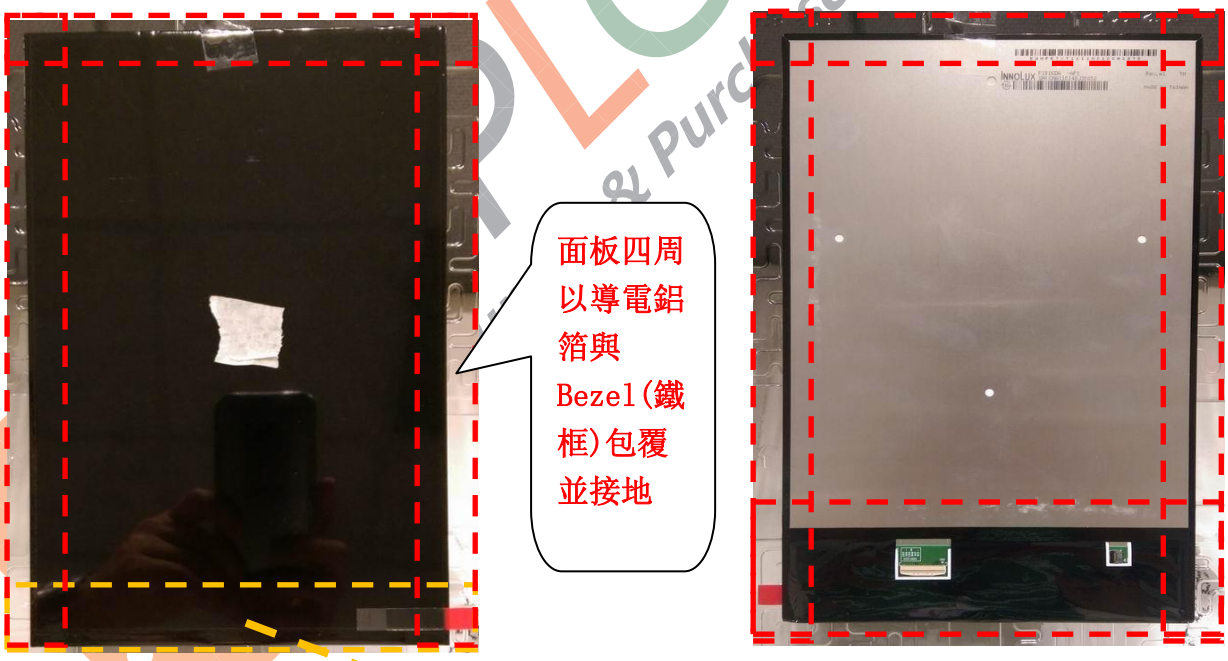
		Standard Value	Tolerance	Remark
A	CF_POL edge → OCA edge	See remark	-	取 CF_POL edge → LCM OD (inner edge) 的中心線定義為 OCA 的外型邊界。因此， (A)=(a), (B)=(b), (C)=(c)
B	CF_POL edge → OCA edge	See remark	-	
C	CF_POL edge → OCA edge	See remark	-	
D	CF_POL edge → OCA edge	See remark	-	取 CF_POL edge → LCD IC (Top edge) 的中心線定義為 OCA 的外型邊界。因此， (D)=(d)
E	Ink open area → OCA edge	> 1350um	±350um	避免 OCA 貼覆不佳出現的氣泡出現在可視區內(Ink open area)。 考量因素， (1) OCA 材切精度:±200um (2) Ink 印刷精度: OGS type：±50um (photo process) TOD type：±150um (mask process) (3) 貼覆精度(軟對硬): :±150um (J001)
F	Ink open area → OCA edge	> 1350um	±350um	
G	Ink open area → OCA edge	> 1350um	±350um	
H	Ink open area → OCA edge	> 1350um	±350um	
*	OCA 是否有完全覆蓋觸控走線區域	See remark		考量， (1) 空間允許下請完全覆蓋 (2) 若被要求降低成本則需重新討論

7.3 ESD 防護建議

針對 IPS 機種，建議將 CF 靜電導出。

A: CF 與 Bezel(背鐵框) 通過導電膠帶導通；(需注意與 TFT 線路，PCBA 元器件絕緣處理)

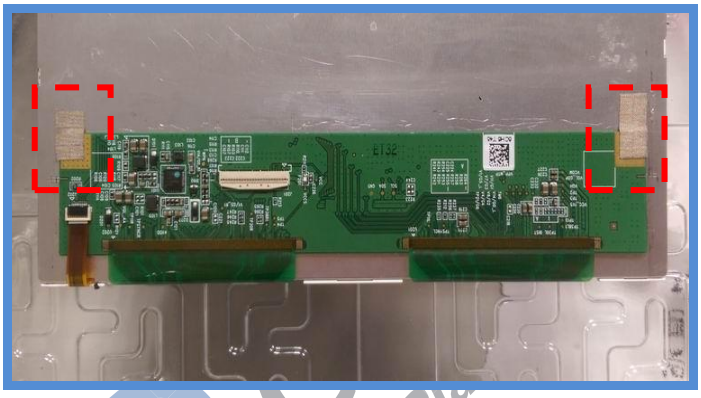




B: FOG PCBA 接地與背光鐵框接地，增強靜電防護。
(靜電規格與模組(背光)設計強相關 ，FOG 單體無法保證 Human Body mode 靜電測試規格。)

導電雙面膠

或



導電膠帶