Monolithic Digital UHF-band Transmitter Wireless-Mic-on-a-Chip™

KT0626M

▪ Features

Fully integration
- **Low noise Microphone interface**
- **High fidelity digital audio processing**
- **Ultra Low noise frequency synthesizer**
- **High power output PA**

Worldwide full band support
- **UHF: 470MHz~960MHz**

Professional Grade Performance:
- **Audio DR ⩾ 100 dB**
- **Flat audio response: 20Hz~18KHz**
- **Low Distortion: <0.5%**
- **Low Spurious Emissions: <-60dBc**
- **High power output capacity: ⩾40mW**

Ultra-Low Power Consumption:
- **< 110 mA operation current**
- **< 10 µA standby current**

Advanced Features:
- **Digital Auxiliary Channel**
- **Programmable Microphone sensitivity**
- **Programmable Transmit Power**
- **Programmable Compandor Time-Constant**
- **Optional pilot**
- **Configurable pilot frequency**
- **Built-in 75us pre-emphasis**
- **Built-in Low-Battery Detector**
- **No on/off noise**
- **No disturbing noise**

Small Form Factor:
- **24-pins QFN 4x4**

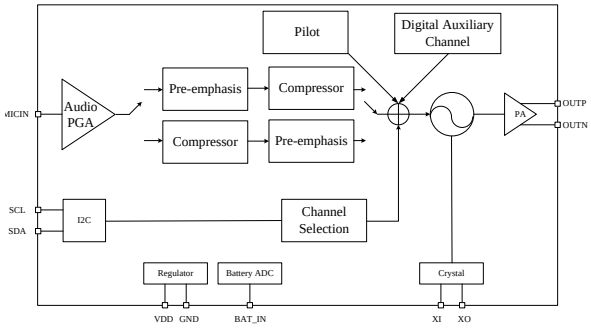
Simple Interface:
- **Single power supply**
- **Standard 2-wire I²C MCU interface**

2.2V ~ 3.6V supply

Pb-free and RoHS Compliant

▪ Applications

Wireless Microphone
Wireless Speaker



KT0626M System Diagram

▪ Description

The KT0626M is a chip of our full suite of the revolutionary wireless microphone chips, KT06xx, which replace hundreds of discrete components in a wireless microphone system while keeping the high standard of sound quality and functionality.

The KT0626M is a UHF band transmitter that includes audio amplifier, pre-emphasis, compressor, PLL and programmable power amplifier. It is designed to process microphone audio signal and transmit modulated FM signal in UHF band.

The KT0626M only requires a single low-voltage supply thanks to a built-in regulator. For a microphone built with a KT0626M, no external tuning is required that makes design-in effort minimum. And the KT0626M support digital auxiliary channel function.

The KT0626M is configured as an I²C slave and programmed through the industry standard 2-wire MCU interface. It is packaged in generic 24-pin QFN.

Rev. 1.1

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1. Electrical Specification

Table 1: Operation Condition

Parameter	Symbol	Operating Condition	Min	Typ	Max	Units
Analog Power Supply	AVDD	Relative to GND	2.2		3.6	V
Digital Power Supply	DVDD		2.2		3.6	V
Ambient Temperature	T_A		-30	25	70	℃
Electrostatic discharge maximum to MIL-Standard 883 C method 3015	Vmax				2000	V

Table 2: DC Characteristics

Parameter		Symbol	Test/Operating Condition	Min	Typ	Max	Units
Current Consumption	P_{OUT}=16dBm	I_{VDD}		-	110	-	mA
	P_{OUT}=13dBm	I_{VDD}		-	85	-	mA
	P_{OUT}=0dBm	I_{VDD}			60		mA
Standby Current		I_{APD}			5	10	μA

Table 3: UHF Band Transmitter Characteristics

(Unless otherwise noted Ta = -30~70℃, AVDD=DVDD= 2.2V to 3.6V)

Parameter	Symbol	Test/Operating Condition	Min	Typ	Max	Units
RF Frequency Range	F_{tx}		470		960	MHz
Audio Dynamic Range[1,2,3]	DR	A-weighted		100		dB
Total Harmonic Distortion[1,2,3]	THD	V_{in} = 1 V_{p-p}	-	0.3	0.5	%
Audio Input Swing	V_{in}		-		0.5	V_{RMS}
Audio Input Resistance	R_{in}			5		kΩ
Audio Frequency Response	F_{in}	Within 3dB	20	-	18k	Hz
Maximum Transmit Power	P_{out}			10		dBm
Spurious Emission	P_{out}				-60	dBc
Channel Step Resolution	STEP		-	25		KHz
Pilot frequency		24MHz Crystal 24.576MHz Crystal	- -	30 30.72	- -	KHz KHz
Pilot Deviation			2.5		10	KHz
Maximum Frequency Deviation					75	KHz
Pre-emphasis Time Constant	T_{pre}	PHTCNST = 1	-	75	-	μs
Crystal	CLK	Input clock		24/ 24.576		MHz
2-wire I^2C Clock	SCL		0	100	400	KHz

Notes:
1. FMOD=1KHz
2. △F=50KHz
3. V_{EMF}=1mV, Frequency=470MHz~960MHz

2. Pin List

Table 4: Pin list

Pin Index	Name	I/O Type	Function
1	XO1	Analog I/O	First crystal output.
2	XI	Analog I/O	Crystal output.
3	VREF	Analog Output	VREF output. Should be decoupled by a 1uF cap.
4	MICIN	Analog Input	Microphone signal input.
5	VCM	Analog Output	Common-mode reference. Should be decoupled by a 10uF cap.
6	GPIO	Digital I/O	General purpose IO.
7	NC1	Reserved	No connection.
8	SDA	Digital I/O	Serial data I/O.
9	SCL	Digital I/O	Serial clock input.
10	DVDD	Power	Digital power supply.
11	NC2	Reserved	No connection.
12	NC3	Reserved	No connection.
13	AVSS	Ground	Analog ground.
14	OUTP	Analog Output	RF positive output.
15	OUTN	Analog Output	RF negative output.
16	AVSS	Ground	Analog ground.
17	AVDD	Power	Analog power supply.
18	VREF	Analog Output	VREF output. Should be decoupled by a 0.1uF cap.
19	AVSS	Ground	Analog ground.
20	INDN	Analog IO	Inductor connection for VCO.
21	INDP	Analog IO	Inductor connection for VCO.
22	AVSS	Ground	Analog ground.
23	XO2	Analog I/O	Second crystal output.
24	AVDD	Power	Analog power supply.

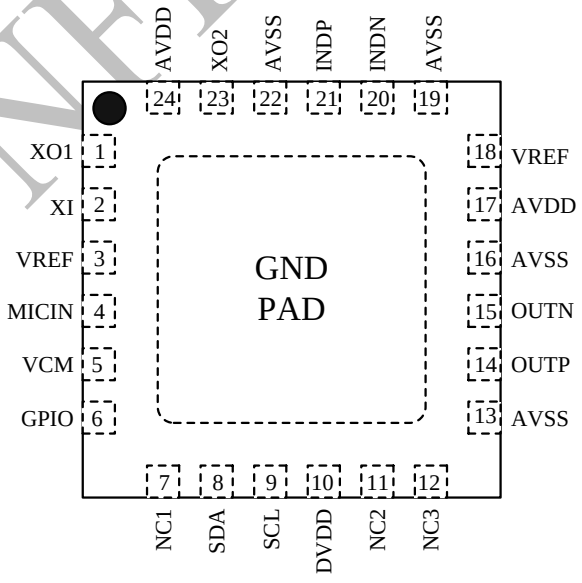


Figure 1: KT0626M Pin assignment (Top view)

3. Function Description

3.1. Overview

KT0626M offers a true single-chip, UHF-band wireless-microphone transmitter solution by minimizing the external components and offering the compatibility with state-of-art receiver solutions. It integrates a low-noise microphone pre-amplifier, a high fidelity audio frontend together with patent pending compandor technology to provide an audio dynamic range as high as 100dB. The fully integrated PLL modulates compressed audio signal to carrier frequency directly. The excellent PLL with ultra low level phase noise and spur emissions, reduces interference of other stations and ensure that more transmitters can operate simultaneously. A pilot signal could also be added to transmitted signal concurrently, which makes KT0626M compatible with current squelch technique used by high-end receivers. A battery meter is provided for MCU generating low-battery warning signal to user. MCU can configure KT0626M through a simple I2C interface.

3.2. Power-up and Standby

KT0626M enters normal operation mode about 100ms after power-supply is added to AVDD and DVDD pins and the working clock is stable. Audio link and PLL are power-up automatically, but PA must be power-on by setting register PA_ON to 1 separately. To enter the power-saving standby mode, MCU should write PA_ON to 0 firstly and then set register STANDBY to 1. Setting register STANDBY back to 0 will wake up KT0626M to normal operation mode.

3.3. Crystal

KT0626M supports 24MHz/24.576MHz crystal to providing the working clock of the chip. The register XTAL_SEL is used to select crystal between 24MHz and 24.576MHz. When a 24MHz crystal is used, the register XTAL_SEL should be set to 0.

3.4. Microphone Interface

KT0626M integrates a low-noise microphone interface as shown in Figure 2. The audio signal from microphone enters KT0626M through the pin MICIN. An AC-coupling cap Cc is needed in series of MICIN when the DC bias of microphone does not equal the internal VCM, about 0.9V. The value of the coupling cap should be chosen properly to guarantee a good enough frequency response at the low end of audio band. A decoupling cap with the same value should be placed outside VCM pin. The sensitivity of microphone can be adjusted within a wide range by setting register MIC_SENS.

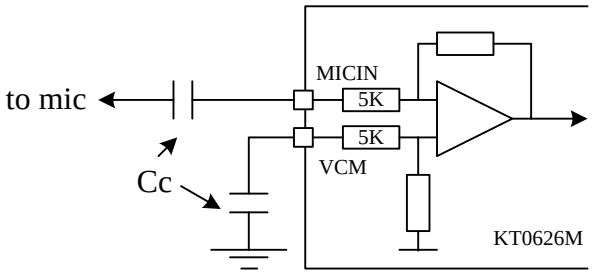


Figure 2: Audio Interface

3.5. Compandor

KT0626M compresses audio signal by a patent pending compandor circuit, which guarantees perfectly consistent performance compared with discrete solutions, whose performance is determined by the variant values of off-chip capacitors and resistors. The dynamic of audio signal is compressed by compandor at a precise 2 to 1 ratio. The time-constant of rectifier is set by register COMP_TC<2:0>. Setting COMP_DIS to 1 will disable the compandor.

3.6. Pilot generator

KT0626M provides a feature of adding a pilot to the transmitted audio signal to be compatible with the squelch algorithm widely used by high-end receivers. The pilot can be enabled by setting register AUXCH_EN to 1 and the frequency deviation of the pilot is determined by register AUX_FDEV<1:0>.

3.7. Digital Auxiliary Channel

KT0626M provides a special feature named “digital auxiliary channel”, which allowing user define specific information transmitted together with the audio signal. The carrier frequency of the digital auxiliary channel is fixed to 30KHz and can be enabled by AUXCH_EN bit. To enable the data transmission, AUXDATA_EN bits must be set to 1. The deviation of the carrier frequency can be adjusted through AUX_FDEV<1:0> bits.
There are two application modes for digital auxiliary channel function:

Sequential mode. In this mode, maximum 4 internal registers can be transmitted sequentially through AUX_ADDRA<7:0>, AUX_ADDRB<7:0>, AUX_ADDRC<7:0>, AUX_ADDRD<7:0>, which define the address of the registers to be transmitted. The quantity of the transmitted register can be defined through AUX_REG_NUM<1:0> bits.

Burst mode. In this mode, the transmitted register can be defined in BURST_DATA<15:0>. If the register value is changed, KT0626M will transmit the value of BURST_DATA<15:0>.

3.8. Channel selection

KT0626M supports UHF 470MHz~960MHz operating frequency range. An off-chip inductor, connected to pins INDN and INDP, determines the center frequency of band

specified by manufacturer. The actual carrier frequency can be configured by user within the range of ±24MHz from center frequency after the inductor is fixed. To guarantee noise performance, high-Q multi-layer chip inductor is recommended if the inductor value exceeds 1nH. Otherwise, routing the inductance by PCB trace is recommended.
The actual transmitted carrier frequency is configured by register CHAN_REGA<15:0> and CHAN_REGB<15:0>, whose values could be obtained from the configuration software provided by KT Micro. Once CHAN_REGA or CHAN_REGB is written by a different value from the previous one, the PLL starts to lock to the new carrier frequency. Within 50ms, the register PLL_READY will go high, indicating the PLL is locked.
For more information about off-chip inductor and channel configuration, please refer to application notes.

3.9. Transmission Power

The transmission power can be adjusted by register PA_GAIN<3:0> in 3dB steps. To eliminate destructive emissions before the channel is configured properly, the PA is off by default after power-on. After the PLL is locked, user should write register PA_ON to 1 to enable PA output. When the chip is going to enter the standby mode or power-off, register PA_ON should be set to 0 first.
The PA of KT0626M outputs signal through two differential pins, OUTP and OUTN. To transfer RF power via a mono-pole antenna, a LC balun should be added to convert differential ports to a single-ended port. If the antenna is dipole type, the balun could be eliminated. For more information about LC balun and impedance matching circuits, please refer to application notes.

3.10.Battery Meter

KT0626M integrates a battery ADC, which is enabled by register BATT_EN and will quantize the voltage of GPIO with a fixed full-scale level of 1.2V. An example of interface circuit for batter meter is shown in Figure 3. The value of R1 and R2 should be chosen properly to guarantee the voltage at GPIO do not exceed the full-scale level. The quantization result of battery meter can be read from register BAT_CODE<10:0>, whose maximum value is 1023.

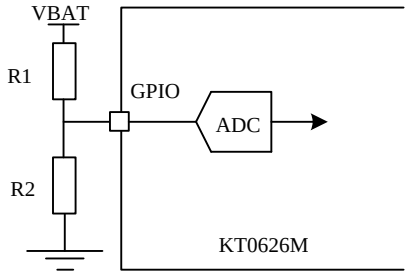


Figure 3: Battery Meter Interface

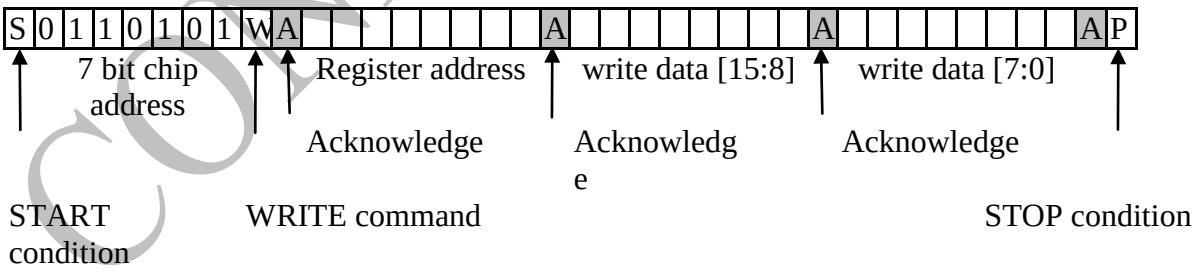
3.11.I2C interface

The serial interface (I2C mode) is used to read and write the device registers, the external controller can directly read and write a register without going through any other registers first. There is also an internal address counter that automatically moves the pointer forward after a read/write operation so that the external controller can continuously read/write desired number of chip registers starting from any of address. The MSB of a register data is transferred first.

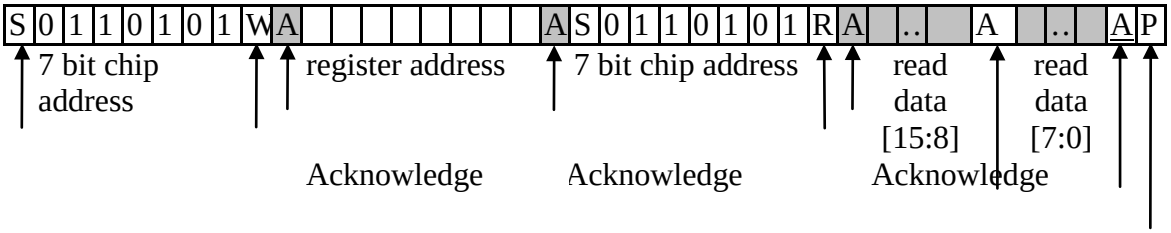
I2C bus mode uses SCL and SDA to transfer data. The device always drives data to SDA at the falling edge of SCL and captures data from SDA at the rising edge of SCL. The device acknowledges the external controller by driving SDA low at the falling edge of SCL. Data transfer always begins with START condition and ends with STOP condition. The external controller can read/write one 16-bits data at the specified address or read/write desired number of registers data continuously from the specified address till when STOP condition is occurred.
For write operations, external controller shall send command & data in the following sequence: START condition -> 7 bit chip address and Write command (“0”) -> 8 bit register address n -> write data n [15:8] -> write data n [7:0] -> write data n+1 [15:8] -> write data n+1 [7:0] -> …… -> STOP condition.
For read operations, external controller shall send command & data in the following sequence: START condition -> 7 bit chip address and Write command (“0”) -> 8 bit register address n -> 7 bit chip address and Read command (“1”) , then device will send read data n [15:8] -> read data n [7:0] -> read data n+1 [15:8] -> read data n+1 [7:0] -> …… till STOP condition.

Table 5: I2C Interface Protocol

RANDOM REGISTER WRITE PROCEDURE



RANDOM REGISTER READ PROCEDURE



START condition

WRITE command

READ command

NO Acknowledge

STOP condition

Note: The data bits in gray color are sent by KT0626M

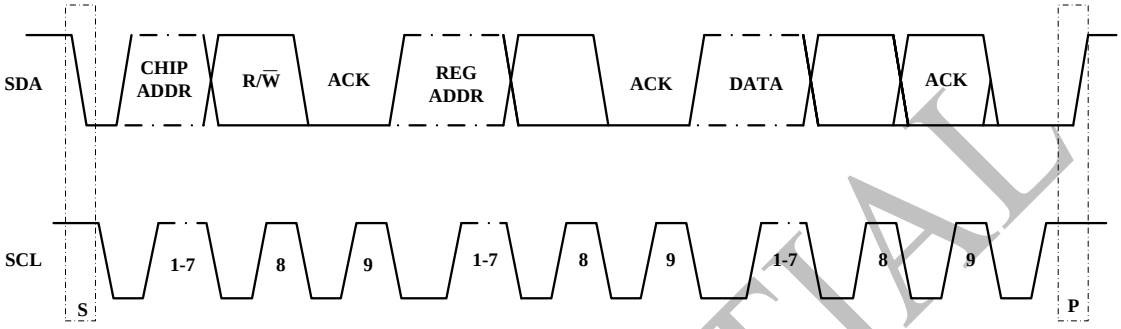


Figure 4: I2C interface timing diagram

3.12.Register Bank

Table 6: Configuration Registers Overview

Address	Register	Description
0x01	CHIP ID	
0x02	BURST_DATA	Burst Data Register
0x03	SYSCFG	System Configuration Register
0x07	BATTERY	Battery Meter Data Register
0x08	CHAN_REGA	Channel Configuration Register A
0x09	CHAN_REGB	Channel Configuration Register B
0x0B	CALI_CODE	Internal Calibration Code
0x0D	PLL_STATE	PLL Working State Register
0x0F	POWER_CFG	Power Control Register
0x18	MUTE_CFG	Mute Control Register
0x1B	AUDIO_CFG	Audio Control Register
0x1C	DSP_CFGA	Audio DSP Configuration Register A
0x1F	PILOT_CFG	Pilot Configuration Register
0x20	AUX ADDR1	Digital Auxiliary Channel Register A
0x21	AUX ADDR2	Digital Auxiliary Channel Register B
0x24	GPIO_CFG	GPIO Configuration Register
0x2B	DSP_CFGB	Audio DSP Configuration Register B

3.12.1. MANUFACTURER ID (Address 0x01)

Bit	Symbol	Access	Default	Functional Description
15:0	Chip ID	R	0x4B54	

3.12.2. BURST_DATA (Address 0x02)

Bit	Symbol	Access	Default	Functional Description
15:0	BURST_DATA<15:0>	R	0x0000	**Burst data for digital auxiliary channel function.**

3.12.3. SYSCFG (Address 0x03)

Bit	Symbol	Access	Default	Functional Description
15	STANDBY	RW	0	**Standby mode enable.** 1 = Standby mode 0 = Working mode
14:5	Reserved	RW	000_0000_000	**Reserved.**
4:1	PA_GAIN<3:0>	RW	0_000	**Output power control.**

				0000: Minimum power …… 1100: Maximum Power 1101: Reserved …… 1111: Reserved
0	PA_SEL	RW	0	**PA power control selection. Must be set to 1 after power-on.** 1: PA is controlled by PA_GAIN<3:0> 0: PA is un-controlled

3.12.4. BATTERY (Address 0x07)

Bit	Symbol	Access	Default	Functional Description
15:11	Reserved	RW	0	**Reserved.**
10:0	BAT_CODE<10:0>	R	0	**Battery meter results.**

3.12.5. CHAN_REGA (Address 0x08)

Bit	Symbol	Access	Default	Functional Description
15:0	CHAN_REGA<15:0>	RW	0x5900	**Channel configuration reg A.** Calculated by Config-Gen Software

3.12.6. CHAN_REGB (Address 0x09)

Bit	Symbol	Access	Default	Functional Description
15:0	CHAN_REGB<15:0>	RW	0x0000	**Channel configuration reg B.** Calculated by Config-Gen Software

3.12.7. CALI_CFG (Address 0x0A)

Bit	Symbol	Access	Default	Functional Description
15:6	Reserved	RW	0000_0000_00	**Reserved.**
5	TUNE	RW	0	**Tune Enable.**
4:0	Reserved	RW	0_0000	**Reserved.**

3.12.8. CALI_CODE (Address 0x0B)

Bit	Symbol	Access	Default	Functional Description
15:9	Reserved	RW	1000_000	**Reserved.**
8:3	BAND_CALI_RES	RW	0_0000	**Band calibration result.**
2:0	Reserved	RW	000	**Reserved.**

3.12.9. PLL_STATE (Address 0x0D)

Bit	Symbol	Access	Default	Functional Description
15:12	Reserved	R	0000	**Reserved.**
11	PLL_READY	R	0	**PLL ready flag.** 0: PLL is not locked 1: PLL is locked
10:6	Reserved	RW	000_00	**Reserved.**
5	Reserved	RW	1	**Must be set to 0 after power-on.**
4:0	Reserved	RW	0_0000	**Reserved.**

3.12.10. POWER_CFG (Address 0x0F)

Bit	Symbol	Access	Default	Functional Description
15:5	Reserved	RW	0000_0000_000	**Reserved.**
4	PA_ON	RW	0	**Power-on control for RF PA.** 0: PA is off 1: PA is on
3:0	Reserved	RW	0	**Reserved.**

3.12.11. MUTE_CFG (Address 0x18)

Bit	Symbol	Access	Default	Functional Description
15:12	Reserved	RW	0000	**Reserved.**
11	MUTE_PILOT_EN	RW	0	**Pilot disable control.** 0: Do not disable pilot. 1: Disable pilot when mute is enabled.
10	MUTE_PIN_EN	RW	1	**Mute enable input.** 0: Disable. 1: Enable.
9:0	Reserved	RW	00_0000_0000	**Reserved.**

3.12.12. AUDIO_CFG (Address 0x1B)

Bit	Symbol	Access	Default	Functional Description
15	MICPGA_GAIN	RW	0	**Microphone input Gain.** 0: 6dB 1: 0dB
14:0	Reserved	RW	100_0000_0010_0001	**Reserved.**

3.12.13. DSP_CFGA (Address 0x1C)

Bit	Symbol	Access	Default	Functional Description
15:12	FDEV_MON	R	0000	**Frequency Deviation Monitor.**
11:10	FDEV_MON_TC	RW	00	**Time-constant of Frequency Deviation Monitor.**
9	PRE_DIS	RW	0	**Pre-emphasis disable.** 0: Enable pre-emphasis 1: Disable pre-emphasis
8:5	MIC_SENS<3:0>	RW	0000	**Microphone sensitivity adjust.** 0000: 0dB 0001: 4dB 0010: 7dB 0011: 10dB 0100: 12dB 0101: 16dB 0110: 19dB 0111: 22dB 1000: 24dB 1001: 28dB 1010: 31dB 1011: 34dB 1100: 36dB 1101: 40dB 1110: 43dB 1111: 46dB
4	COMP_DIS	RW	0	**Compandor disable.** 0: Enable compressor 1: Disable compressor
3:1	COMP_TC<2:0>	RW	000	**Time-constant of compandor rectifier.** 000: 6ms 001: 12ms

				010: 24ms 011: 48ms 100: 93ms 101: 199ms 110: 398ms 111: 796ms
0	AUDIO_MUTE	RW	0	**Audio mute enable.** 0: Un-mute 1: Mute

3.12.14. PILOT_CFG (Address 0x1F)

Bit	Symbol	Access	Default	Functional Description
15	AUXCH_EN	RW	0	Enable the digital auxiliary channel function. 0 : Disable 1 : Enable
14	AUXDATA_EN	RW	0	Enable the data transmission for digital auxiliary channel function. 0 : Disable 1 : Enable
13:12	AUX_REG_NUM<1:0>	RW	00	The quantity of the transmitted register for digital auxiliary channel function. 2'b00: 1 2'b01: 2 2'b10: 3 2'b11: 4
11:9	Reserved	RW	000	**Reserved.**
8:7	AUX_FDEV<1:0>	RW	0_0	The deviation of digital auxiliary channel function: 2'b00: 2.5KHz 2'b01: 5KHz 2'b10: 7.5KHz 2'b11: 10KHz
6:0	Reserved	RW	000_0000	**Reserved.**

3.12.15. AUX ADDR1 (Address 0x20)

Bit	Symbol	Access	Default	Functional Description
15:8	AUX_ADDRB<7:0>	RW	0x00	**Second register address for digital auxiliary channel function.**

7:0	AUX_ADDRA<7:0>	RW	0x00	**First register address for digital auxiliary channel function.**

3.12.16. AUX ADDR2 (Address 0x21)

Bit	Symbol	Access	Default	Functional Description
15:8	AUX_ADDRD<7:0>	RW	0x00	**Fourth register address for digital auxiliary channel function.**
7:0	AUX_ADDRC<7:0>	RW	0x00	**Third register address for digital auxiliary channel function.**

3.12.17. GPIO_CFG (Address 0x24)

Bit	Symbol	Access	Default	Functional Description
15:13	Reserved	RW	000	**Reserved.**
12	BATT_EN	RW	0	**Battery meter enable.** 0: Disable battery meter 1: Enable battery meter
11:0	Reserved	RW	0000_0000_0000	**Reserved.**

3.12.18. DSP_CFGB (Address 0x2B)

Bit	Symbol	Access	Default	Functional Description
15:1	Reserved	RW	0000_0000_0000_000	**Reserved.**
0	PRE_FIRST	RW	1	**Sequence of pre-emphasis and compandor.** 0: Compandor→pre-emphasis 1: Pre-emphasis→compandor

3.12.19. STATUS_A (Address 0x3E)

Bit	Symbol	Access	Default	Functional Description
15	SOFT_RST	RW	000	**Soft Reset.** 3.13. 0: Normal mode. 1: Reset DSP part.
14:13	Reserved	RW	00	**Reserved.**
12	INF_DETECT_EN	RW	0	**Interferer Detect Enable.** 0: Disable. 1: Enable.

11:0	Reserved	RW	0000_0000_0000	**Reserved.**

3.13.20. SPARE_A (Address 0x3F)

Bit	Symbol	Access	Default	Functional Description
15:8	Reserved	RW	0000_0000	**Reserved.**
7	XTAL_SEL	RW	0	**Crystal Selection.** 0: Crystal 1. 1: Crystal 2.
6:0	Reserved	RW	000_0000	**Reserved.**

4. Typical Application Circuit

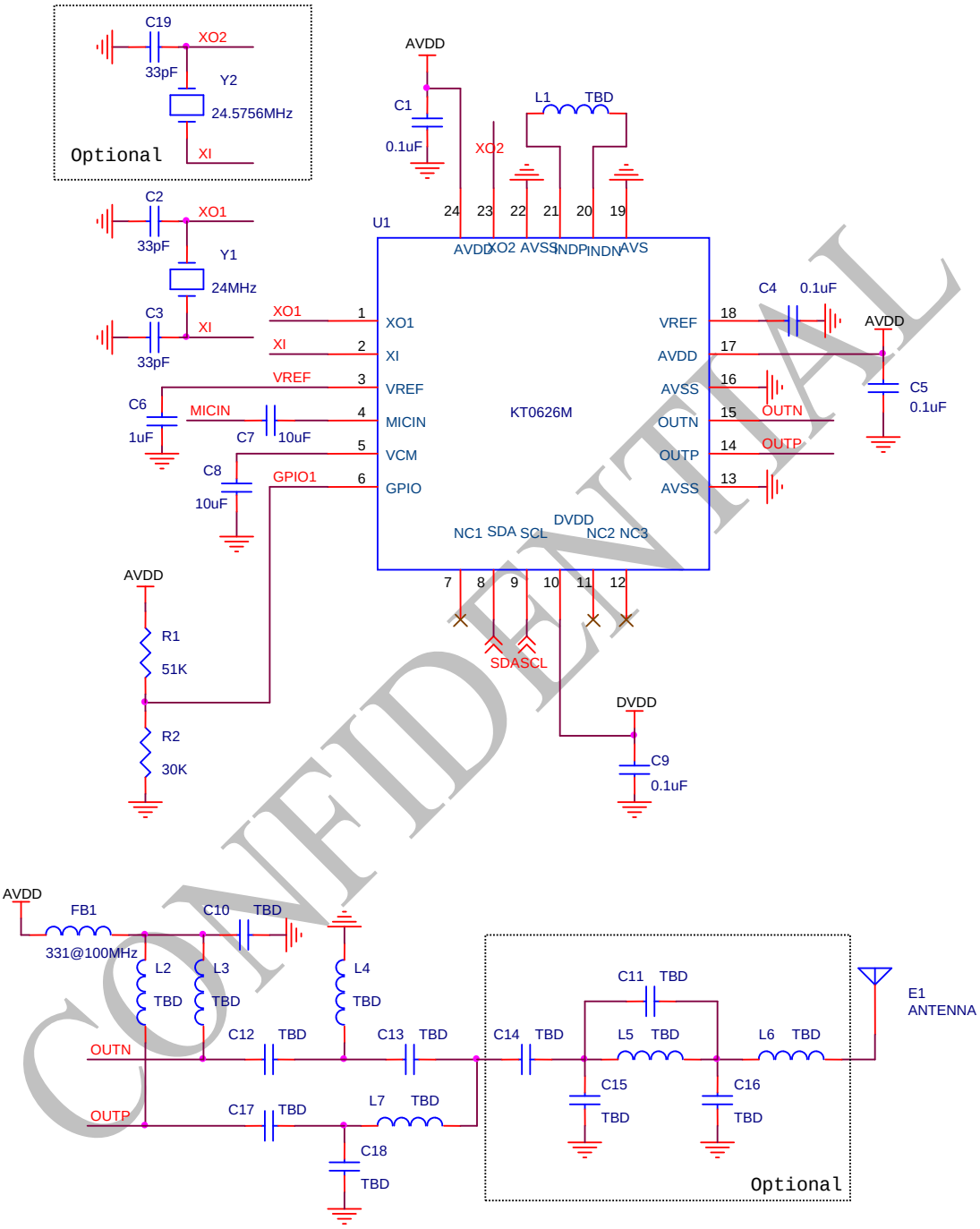
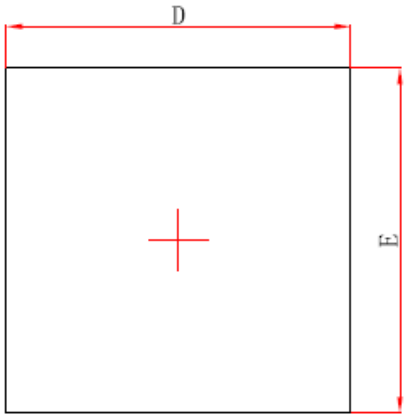


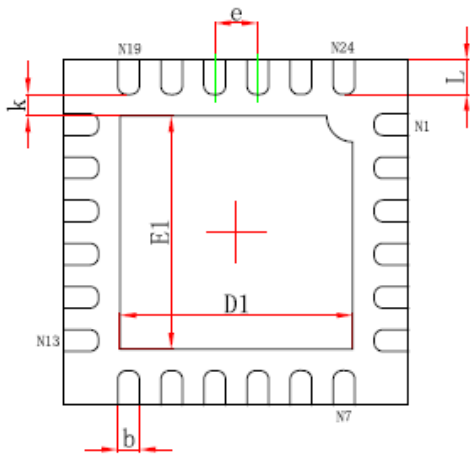
Figure 5: Typical application circuits

Components	Description	Value	Suppliers
C1,C6,C18	Supply decoupling capacitor	0.1uF	
C2,C3,C19	Crystal load capacitor	33pF	
C4	Decoupling capacitor	0.1uF	
C7	Decoupling capacitor	1uF	
C5	Decoupling capacitor	TBD	
C8,C13	Decoupling capacitor	10uF	
C9	Capacitor	TBD	
C10,C12,C16	Capacitor	TBD	
C11,C17	Capacitor	TBD	
C14	Capacitor	TBD	
C15	Capacitor	TBD	
E1	Antenna		
FB1	Ferrite bead	331@100MHz	
L1	Inductance	TBD	Murata LQG series
L2,L3	Inductance	TBD	Murata LQG series
L4,L7	Inductance	TBD	Murata LQG series
L5,L6	Inductance	TBD	Murata LQG series
R1	Resistor	51K	
R2	Resistor	30K	
Y1	Crystal	24MHz	
Y2	Crystal	24.576MHz	

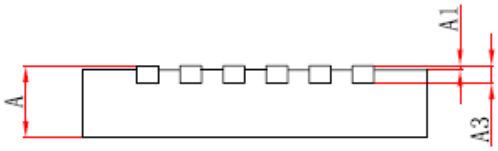
5. Package Outline



Top View



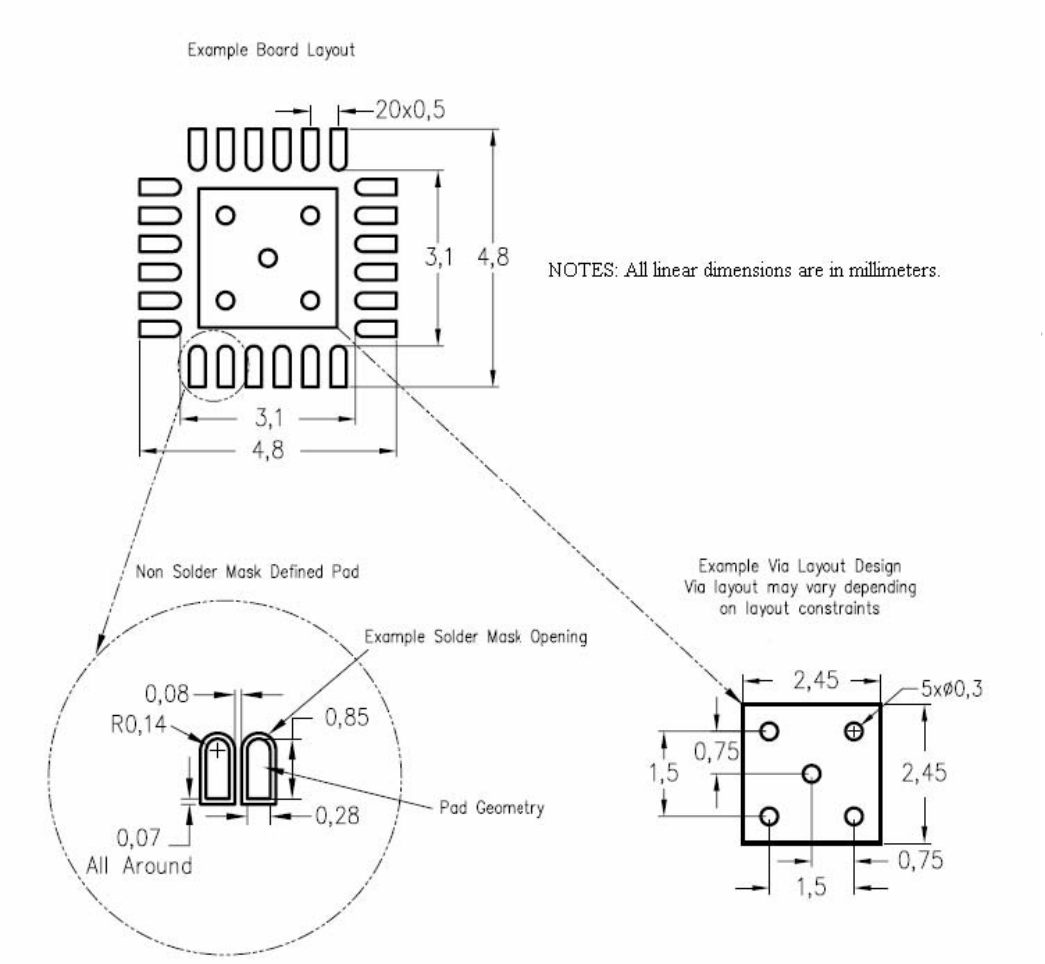
Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	3.900	4.100	0.154	0.161
E	3.900	4.100	0.154	0.161
D1	2.600	2.800	0.102	0.110
E1	2.600	2.800	0.102	0.110
k	0.200MIN.		0.008MIN.	
b	0.180	0.300	0.007	0.012
e	0.500TYP.		0.020TYP.	
L	0.300	0.500	0.012	0.020

6. PCB Land Pattern



7. Recommended Reflow Profile

The solder reflow profile should follow the paste manufacturer recommendation and the general JEDEC/IPC standard J-STD-20 guidelines. SnAgCu eutectic solder paste with melting temperature of 217℃ commonly used for lead-free solder reflow application. Figure 6 shows the range of temperature profiles of the J-STD-20 specification. The profile parameters and component peak temperature guidelines are listed in Table 7. Note all specified temperatures in Table 7 refer to the temperatures measured on the top surface of the package.

It is very important to control the peak reflow temperature below the maximum temperatures specified in Table 7 to prevent thermal damage to the package.

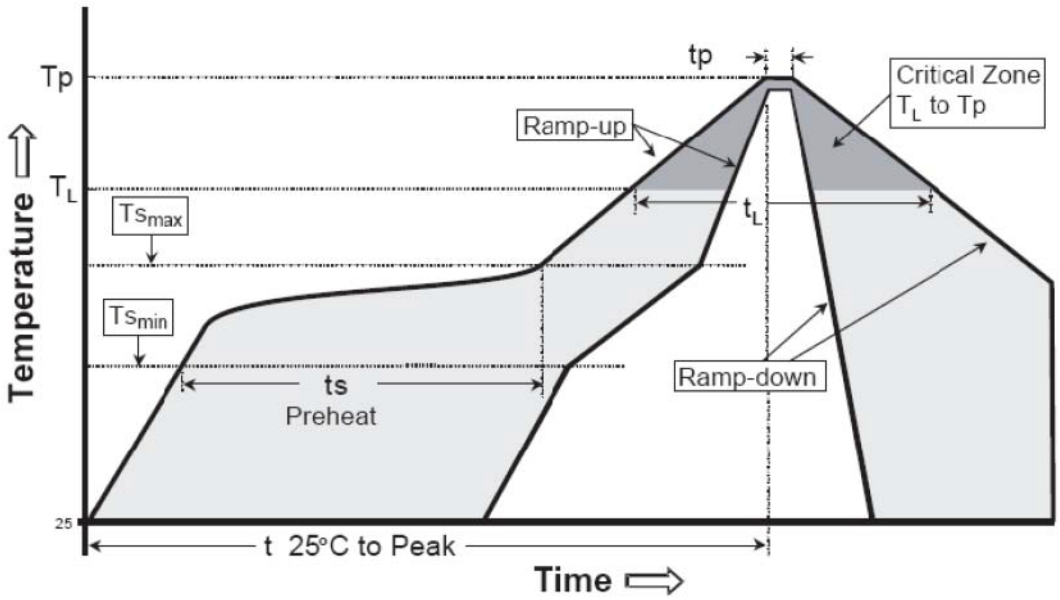


Figure 6: Typical reflow profile

Table 7: Reflow profile parameters

Profile Parameter	**Pb-FREE**
Average Ramp-Up Rate (TsMAX to Tp)	3℃/second maximum
Preheat: -Temperature Min (TsMIN) -Temperature Max (TsMAX) -Time (tsMIN to tsMAX)	 +150℃ +200℃ 60 to 180 seconds
Time maintained above: -Temperature (TL) -Time (tL)	 +217℃ 60 to 150 seconds
-Peak/Classification Temperature (Tp)	+260℃
Time within +5℃ of Actual Peak Temperature (tp)	20 to 40 seconds
Ramp-Down Rate	+6℃/second maximum
Time +25℃ to Peak Temperature	8 minutes maximum

8. Order Information

Part number	Description	Package
KT0626M	Monolithic Digital UHF-band Transmitter	QFN-24, Pb free, 4000 pcs per reel.

9. Revision History

V1.0 Official Release.
V1.1 Add Confidential

10. Contact Information

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