Monolithic Digital UHF-band Transmitter Wireless-Mic-on-a-Chip™

KT0603

▪ Features

Single-chip Wireless Mic solution
- **Built-in MCU**
- **Support up to 16 preset channels**

Fully integration
- **Low noise Microphone interface**
- **High fidelity digital audio processing**
- **Ultra Low noise frequency synthesizer**
- **High power output PA**

Worldwide full band support
- **UHF: 470MHz~960MHz**

Professional Grade Performance:
- **Audio Dynamic Range ≥ 100 dB**
- **Flat audio response: 20Hz~18KHz**
- **Low Distortion: <0.5%**
- **Low Spurious Emissions: <-60dBc**
- **High transmit power: ⩾10mW**

Ultra-Low Power Consumption:
- **< 80 mA operation current**
- **< 10 μA standby current**

Advanced Features:
- **Configurable Microphone sensitivity**
- **Configurable Transmit Power**
- **Configurable Compandor Time-Constant**
- **Optional pilot**
- **Built-in 75us pre-emphasis**
- **Built-in Low-Battery Detector**
- **No on/off noise**
- **No disturbing noise**

Small Form Factor:
- **QFN24 package**

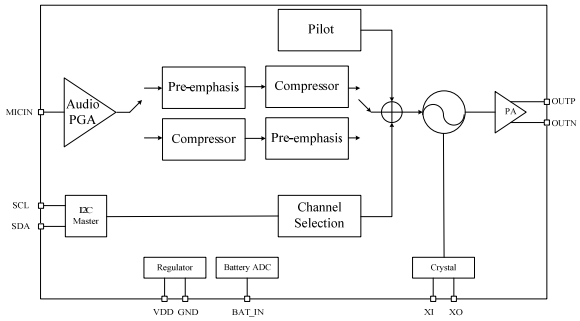
Simple Interface:
- **Single power supply (2.2V- 3.6V)**
- **2-wire I²C master interface**

Pb-free and RoHS Compliant

▪ Applications

Wireless Microphone
Wireless Speaker

Rev. 1.1



KT0603 System Diagram

▪ Description

The KT0603 is a UHF band chip of our full suite of the revolutionary wireless microphone chips, KT06xx, which replace hundreds of discrete components in a wireless microphone system while keeping the high standard of sound quality and functionality.

The KT0603 is a UHF band transmitter that includes audio amplifier, pre-emphasis, compressor, PLL and configurable power amplifier. It is designed to process microphone audio signal and transmit modulated FM signal in UHF band.

The KT0603 only requires a single low-voltage supply thanks to a built-in regulator. For a microphone built with a KT0603, no external tuning is required, which makes design-in effort minimum.

The KT0603 provides direct and simple interface to support mechanical tuning. A pre-programmed low cost EEPROM can be used to configure the radio settings to differentiate product designs and accommodate standards in various regions. No external MCU is required. It is packaged in generic QFN24.

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1. Electrical Specification

Table 1: Operation Condition

Parameter	Symbol	Operating Condition	Min	Typ	Max	Units
Analog Power Supply	AVDD	Relative to GND	2.2		3.6	V
Digital Power Supply	DVDD		2.2		3.6	V
Ambient Temperature	T_A		-30	25	70	℃
Electrostatic discharge maximum to MIL-Standard 883 C method 3015	Vmax				2000	V

Table 2: DC Characteristics

Parameter		Symbol	Test/Operating Condition	Min	Typ	Max	Units
Current Consumption	P_{OUT}=10dBm	I_{VDD}		-	80	-	mA
	P_{OUT}=0dBm	I_{VDD}			60		mA
Standby Current		I_{APD}			5	10	μA

Table 3: FM Receiver Characteristics

(Unless otherwise noted Ta = -30~70℃, AVDD= 2.2V to 3.6V)

Parameter	Symbol	Test/Operating Condition	Min	Typ	Max	Units
RF Frequency Range	F_{tx}		470		960	MHz
Audio Dynamic Range[1,2,3]	DR	A-weighted		100		dB
Total Harmonic Distortion[1,2,3]	THD	V_{in} = 1 V_{p-p}	-	0.3	0.5	%
Audio Input Swing	V_{in}		-		0.5	V_{RMS}
Audio Input Resistance	R_{in}			5		kΩ
Audio Frequency Response	F_{in}	Within 3dB	20	-	18k	Hz
Maximum Transmit Power	P_{out}			10		dBm
Spurious Emission	P_{out}				-60	dBc
Channel Step Resolution	STEP		-	25		KHz
Pilot frequency		24MHz crystal 24.576MHz crystal	- -	30 30.72	- -	KHz KHz
Pilot Deviation			2.5		10	KHz
Maximum Frequency Deviation					75	KHz
Pre-emphasis Time Constant	T_{pre}	PHTCNST = 1	-	75	-	μs
Crystal	CLK	Input clock		24/ 24.576		MHz
2-wire I^2C Clock	SCL			50		KHz

Notes:
1. FMOD=1KHz
2. △F=50KHz
3. V_{EMF}=1mV, Frequency=470MHz~960MHz

2. Pin List

Table 4: Pin list

Pin Index	Name	I/O Type	Function
1	XI	Analog I/O	Crystal input.
2	XO	Analog I/O	Crystal output.
3	VREF	Analog Output	VREF output. Should be decoupled by a 1uF cap.
4	MICIN	Analog Input	Microphone signal input.
5	VCM	Analog Output	Common-mode Reference. Should be decoupled by a 10uF cap.
6	BAT_IN	Analog Input	Battery meter input.
7	CH	Analog Input	Channel adjustment signal input.
8	SDA/LOW_BAT	Digital I/O	Function1: Serial data I/O. Function2: Low voltage indicator output. Low active.
9	SCL	Digital I/O	Serial clock output.
10	DVDD	Power	Digital power supply.
11	CHIP_EN	Digital Input	Chip enable pin. 0 means power off. 1means power on.
12	MUTE	Digital Input	Mute signal input. High active.
13	AVSS	Ground	Analog ground.
14	OUTP	Analog Output	RF positive output.
15	OUTN	Analog Output	RF negative output.
16	AVSS	Ground	Analog ground.
17	AVDD	Power	Analog power supply.
18	VREF	Analog Output	VREF output. Should be decoupled by a 1uF cap.
19	AVSS	Ground	Analog ground.
20	INDN	Analog IO	Inductor connection for VCO.
21	INDP	Analog IO	Inductor connection for VCO.
22	AVSS	Ground	Analog ground.
23	AVSS	Ground	Analog ground.
24	AVDD	Power	Analog power supply.

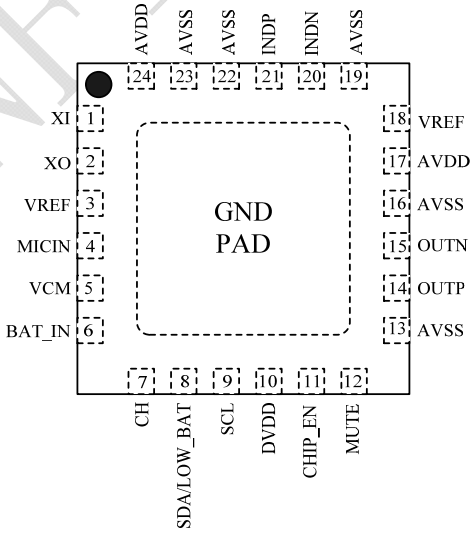


Figure 1: KT0603 Pin assignment (Top view)

3. Function Description

3.1. Overview

KT0603 offers a true single-chip, UHF-band wireless-microphone transmitter solution by minimizing the external components and offering the compatibility with state-of-art receiver solutions. It integrates a low-noise microphone pre-amplifier, a high fidelity audio frontend together with patent pending compandor technology to provide an audio dynamic range as high as 100dB. The fully integrated PLL modulates compressed audio signal to carrier frequency directly. The excellent PLL with ultra low level phase noise and spur emissions, reduces interference of other stations and ensure that more transmitters can operate simultaneously. A pilot signal of 32.768KHz could also be added to transmitted signal concurrently, which makes KT0603 compatible with current squelch technique used by high-end receivers.

3.2. Power-up

KT0603 enters normal operation mode about 100ms after power-supply is added to AVDD and DVDD pins and the working clock is stable and the CHIP_EN pin is pulled up to DVDD.

3.3. Crystal

KT0603 supports 24MHz/24.576MHz crystal to providing the working clock of the chip.

3.4. Microphone Interface

KT0603 integrates a low-noise microphone interface as shown in Figure 2. The audio signal from microphone enters KT0603 through the pin MICIN. An AC-coupling cap Cc is needed in series of MICIN when the DC bias of microphone does not equal the internal VCM, about 0.9V. The value of the coupling cap should be chosen properly to guarantee a good enough frequency response at the low end of audio band. A decoupling cap with the same value should be placed outside VCM pin. The sensitivity of microphone can be adjusted within a wide range by setting register MIC_SENS.

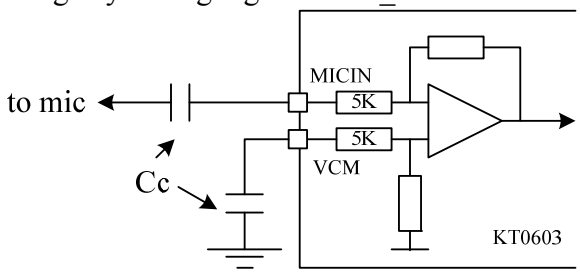


Figure 2: Audio Interface

3.5. Compandor

KT0603 compresses audio signal by a patent pending compandor circuit, which guarantees perfectly consistent performance compared with discrete solutions, whose performance is determined by the variant values of off-chip capacitors and resistors. The dynamic of audio signal is compressed by compandor at a precise 2 to 1 ratio. The time-constant of rectifier is set by register COMP_TC<2:0>. Setting COMP_DIS to 1 will disable the compandor.

3.6. Pre-emphasis

KT0603 supports 75us of pre-emphasis time constant. Pre-emphasis can be disabled by register PRE_DIS. The sequence of pre-emphasis and compandor is determined by register PRE_FIRST.

3.7. Mute

KT0603 could be mute by MUTE pin is pulled up to DVDD. An example of mute circuit is shown in Figure 3. When register MUTE_PILOT_EN is set to 1, pilot will be disabled when the MUTE pin is pulled up.

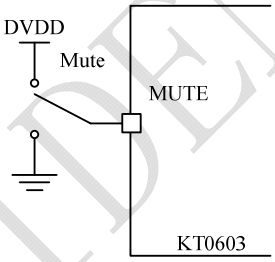


Figure 3: Mute Interface

3.8. Pilot generator

KT0603 provides a feature of adding a pilot to the transmitted audio signal to be compatible with the squelch algorithm widely used by high-end receivers. The pilot can be enabled by setting register PILOT_EN to 1 and the frequency deviation of the pilot is determined by register PILOT_FDEV<1:0>.

3.9. Channel selection

KT0603 supports a unique Potentiometer-Mode whose application circuit is shown in Figure 4.
The potentiometer is implemented by a variable resistor with the center tap connected to the chip. KT0603 measures the ratio of two parts of the variable resistor and maps the result to the real control channel. KT0603 can be configured 16 carrier frequencies by register CHAN_REGA_x<15:0> and CHAN_REGB_x<15:0>.

If the center tap of the variable resistor is located in one of 16 areas, the tuned channel could be determined by register CHAN_REGA_x<15:0> and CHAN_REGB_x<15:0>.

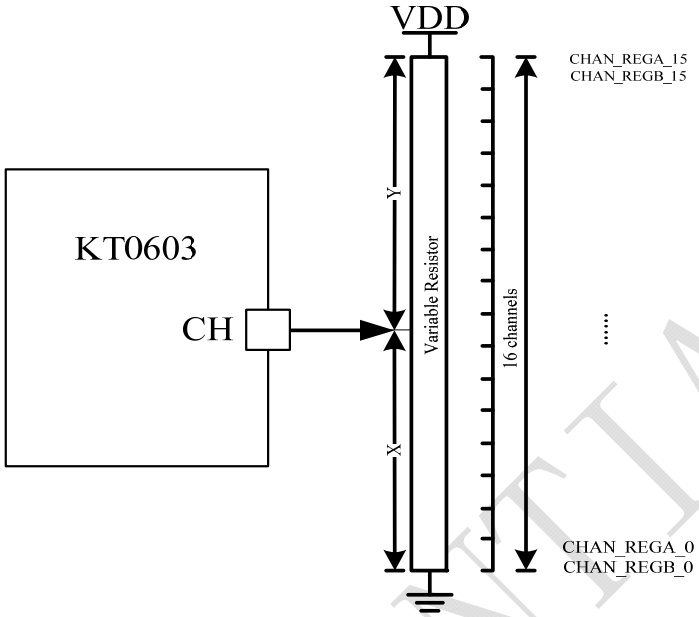


Figure 4: CH pin connection in potentiometer-mode

KT0603 supports UHF 470MHz~960MHz operating frequency range. An off-chip inductor, connected to pins INDN and INDP, determines the center frequency of band specified by manufacturer. The actual carrier frequency can be configured by CH pin within the range of ±24MHz from center frequency after the inductor is fixed. To guarantee noise performance, high-Q multi-layer chip inductor is recommended.
The actual transmitted carrier frequency is configured by register CHAN_REGA_x<15:0> and CHAN_REGB_x<15:0>, whose values could be obtained from the configuration software provided by KT Micro. Once CH pin is changed by a different value from the previous one, the PLL starts to lock to the new carrier frequency.
For more information about off-chip inductor and channel configuration, please refer to application notes.

3.10. Transmission Power

The transmission power can be adjusted by register PA_GAIN<3:0> in 3dB steps.
The PA of KT0603 outputs signal through two differential pins, OUTP and OUTN. To transfer RF power via a mono-pole antenna, a LC balun should be added to convert differential ports to a single-ended port. If the antenna is dipole type, the balun could be eliminated. For more information about LC balun and impedance matching circuits, please refer to application notes.

3.11.Low Battery Indicator

KT0603 integrates a low-battery indicator, which is enabled by register BATT_EN and LOWBAT_EN. When the voltage of BAT_IN is below the threshold of comparator, which is set by register LOWBAT_TH<7:0>, the SDA/LOW_BAT pin will pull down to 0, otherwise SDA/LOW_BAT pin will remain open-drain output. An example of interface circuit for batter meter is shown in Figure 5.

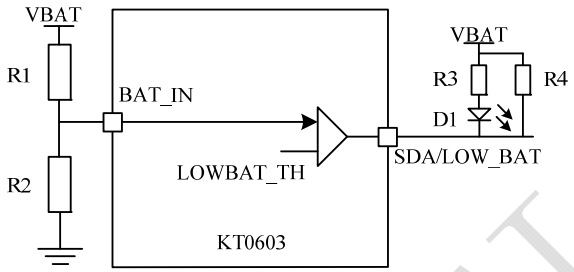


Figure 5: Battery Meter Interface

3.12.Chip Configuration

An I2C master interface is integrated in KT0603 and can be used to initialize and operate the chip together with an external EEPROM (e.g. 24C02). The initialization information is written into the EEPROM beforehand. When powered on, KT0603 will readout all the data stored in the EEPROM and write them into internal register bank. The mapping relationship of the register bit between KT0603 internal register bank and 24C02 can be found in Table 5. The effective device address for EEPROM is from 000(A2:A0) to 110.

Table 5: Register Bits Mapping Relationship between 24C02 and KT0603

24C02		**KT0603**	
address	bits	address	bits
0x00	D7:D0	0x00	D15:D8
0x01	D7:D0		D7:D0
0x02	D7:D0	0x01	D15:D8
0x03	D7:D0		D7:D0
…	…	…	…
…	…		…
0xFE	D7:D0	0x7F	D15:D8
0xFF	D7:D0		D7:D0

3.13.Register Bank

Table 6: Configuration Registers Overview

Address	Register	Description
0x03	SYS_CFG	System Configuration Register
0x18	MUTE_CFG	Mute Configuration Register
0x19	LOWBAT_CFG	Low Battery Indicator Configuration Register
0x1C	AUDIO_CFG	Audio Configuration Register
0x1F	PILOT_CFG	Pilot Configuration Register
0x24	GPIO_CFG	GPIO Configuration Register
0x2B	DSP_CFG	DSP Configuration Register
0x40	CHAN_REGA_0	Channel 0 Configuration Register A
0x41	CHAN_REGB_0	Channel 0 Configuration Register B
0x42	CHAN_REGA_1	Channel 1 Configuration Register A
0x43	CHAN_REGB_1	Channel 1 Configuration Register B
0x44	CHAN_REGA_2	Channel 2 Configuration Register A
0x45	CHAN_REGB_2	Channel 2 Configuration Register B
0x46	CHAN_REGA_3	Channel 3 Configuration Register A
0x47	CHAN_REGB_3	Channel 3 Configuration Register B
0x48	CHAN_REGA_4	Channel 4 Configuration Register A
0x49	CHAN_REGB_4	Channel 4 Configuration Register B
0x4A	CHAN_REGA_5	Channel 5 Configuration Register A
0x4B	CHAN_REGB_5	Channel 5 Configuration Register B
0x4C	CHAN_REGA_6	Channel 6 Configuration Register A
0x4D	CHAN_REGB_6	Channel 6 Configuration Register B
0x4E	CHAN_REGA_7	Channel 7 Configuration Register A
0x4F	CHAN_REGB_7	Channel 7 Configuration Register B
0x50	CHAN_REGA_8	Channel 8 Configuration Register A
0x51	CHAN_REGB_8	Channel 8 Configuration Register B
0x52	CHAN_REGA_9	Channel 9 Configuration Register A
0x53	CHAN_REGB_9	Channel 9 Configuration Register B
0x54	CHAN_REGA_10	Channel 10 Configuration Register A
0x55	CHAN_REGB_10	Channel 10 Configuration Register B
0x56	CHAN_REGA_11	Channel 11 Configuration Register A
0x57	CHAN_REGB_11	Channel 11 Configuration Register B
0x58	CHAN_REGA_12	Channel 12 Configuration Register A
0x59	CHAN_REGB_12	Channel 12 Configuration Register B
0x5A	CHAN_REGA_13	Channel 13 Configuration Register A
0x5B	CHAN_REGB_13	Channel 13 Configuration Register B
0x5C	CHAN_REGA_14	Channel 14 Configuration Register A
0x5D	CHAN_REGB_14	Channel 14 Configuration Register B
0x5E	CHAN_REGA_15	Channel 15 Configuration Register A
0x5F	CHAN_REGB_15	Channel 15 Configuration Register B

3.13.1. SYS_CFG (Address 0x03)

Bit	Symbol	Default	Functional Description
15:5	Reserved	0000_0000_000	**Reserved.**
4:1	PA_GAIN<3:0>	0_000	**Output Power Control.** 0000: Minimum power …… 1100: Maximum power 1101: Reserved …… 1111: Reserved
0	PA_SEL	0	**PA Power control selection Must be set to 1 after power-on.** 0: PA is un-controlled. 1: PA is controlled by PA_GAIN<3:0>.

3.13.2. MUTE_CFG (Address 0x18)

Bit	Symbol	Default	Functional Description
15:12	Reserved	0000	**Reserved.**
11	MUTE_PILOT_EN	0	**Pilot Disable Control** 0: Do not disable pilot. 1: Disable pilot when mute is enabled.
10	MUTE_PIN_EN	1	**Mute Enable Input.** 0: Disable. 1: Enable.
9:0	Reserved	00_0000_0000	**Reserved.**

3.13.3. LOWBAT_CFG (Address 0x19)

Bit	Symbol	Default	Functional Description
15:9	Reserved	0000 000	**Reserved.**
8	LOWBAT_EN	0	**Low Battery Indicator Enable.** 0: Low Battery Indicator is disabled. 1: Low Battery Indicator is enabled. SDA pin will output 0 when battery voltage is below LOWBAT_TH.
7	Reserved	0	**Reserved.**
6:0	LOWBAT_TH<6:0>	000 0000	**Low Battery Indicator Threshold.** 000 0000: 0/128 * 1.2V 000 0001: 1/128 * 1.2V …… 111 1111: 127/128 * 1.2V

3.13.4. AUDIO_CFG (Address 0x1C)

Bit	Symbol	Default	Functional Description
15:10	Reserved	0000_00	**Reserved.**
9	PRE_DIS	0	**Pre-Emphasis Disable.** 0: Enable pre-emphasis 1: Disable pre-emphasis
8:5	MIC_SENS<3:0>	0000	**Microphone Sensitivity Adjust.** 0000: 0dB 0001: 4dB 0010: 7dB 0011: 10dB 0100: 12dB 0101: 16dB 0110: 19dB 0111: 22dB 1000: 24dB 1001: 28dB 1010: 31dB 1011: 34dB 1100: 36dB 1101: 40dB 1110: 43dB1111: 46dB
4	COMP_DIS	0	**Compandor Disable.** 0: Enable compressor 1: Disable compressor
3:1	COMP_TC<2:0>	000	**Time-Constant of Compandor Rectifier.** 000: 6ms 001: 12ms 010: 24ms 011: 48ms 100: 93ms 101: 199ms 110: 398ms 111: 796ms
0	Reserved	0	**Reserved.**

3.13.5. PILOT_CFG (Address 0x1F)

Bit	Symbol	Default	Functional Description
15	PILOT_EN	1	**Pilot Enable.** 0: Disable pilot 1: Enable pilot
14:9	Reserved	000_000	**Reserved.**

8:7	PILOT_FDEV<1:0>	0_0	**Frequency Deviation of Pilot.** 00: 2.5KHz 01: 5KHz 10: 7.5KHz 11: 10KHz
6:0	Reserved	000_0000	**Reserved.**

3.13.6. GPIO_CFG (Address 0x24)

Bit	Symbol	Default	Functional Description
15:13	Reserved	001	**Reserved.**
12	BATT_EN	0	**Battery Meter Enable** 0: Disable battery meter 1: Enable battery meter
11:0	Reserved	0000_0000_0000	**Reserved.**

3.13.7. DSP_CFG (Address 0x2B)

Bit	Symbol	Default	Functional Description
15:1	Reserved	0000_0000_0000_000	**Reserved.**
0	PRE_FIRST	1	**Sequence of pre-emphasis and compandor.** 0: Compandor→pre-emphasis 1: Pre-emphasis→compandor

3.13.8. CHAN_REGA_0 (Address 0x40)

Bit	Symbol	Default	Functional Description
15:0	CHAN_REGA_0<15:0>	0x0000	**Channel Configuration Reg A for Channel 0.** Calculated by Config-Gen Software.

3.13.9. CHAN_REGB_0 (Address 0x41)

Bit	Symbol	Default	Functional Description
15:0	CHAN_REGB_0<15:0>	0x0000	**Channel Configuration Reg B for Channel 0.** Calculated by Config-Gen Software.

3.13.10. CHAN_REGA_1 (Address 0x42)

Bit	Symbol	Default	Functional Description
15:0	CHAN_REGA_1<15:0>	0x0000	**Channel Configuration Reg A for Channel 1.** Calculated by Config-Gen Software..

3.13.11. CHAN_REGB_1 (Address 0x43)

Bit	Symbol	Default	Functional Description
15:0	CHAN_REGB_1<15:0>	0x0000	**Channel Configuration Reg B for Channel 1.** Calculated by Config-Gen Software.

3.13.12. CHAN_REGA_2 (Address 0x44)

Bit	Symbol	Default	Functional Description
15:0	CHAN_REGA_2<15:0>	0x0000	**Channel Configuration Reg A for Channel 2.** Calculated by Config-Gen Software.

3.13.13. CHAN_REGB_2 (Address 0x45)

Bit	Symbol	Default	Functional Description
15:0	CHAN_REGB_2<15:0>	0x0000	**Channel Configuration Reg B for Channel 2.** Calculated by Config-Gen Software.

3.13.14. CHAN_REGA_3 (Address 0x46)

Bit	Symbol	Default	Functional Description
15:0	CHAN_REGA_3<15:0>	0x0000	**Channel Configuration Reg A for Channel 3.** Calculated by Config-Gen Software.

3.13.15. CHAN_REGB_3 (Address 0x47)

Bit	Symbol	Default	Functional Description
15:0	CHAN_REGB_3<15:0>	0x0000	**Channel Configuration Reg B for Channel 3.**

			Calculated by Config-Gen Software.

3.13.16. CHAN_REGA_4 (Address 0x48)

Bit	Symbol	Default	Functional Description
15:0	CHAN_REGA_4<15:0>	0x0000	**Channel Configuration Reg A for Channel 4.** Calculated by Config-Gen Software.

3.13.17. CHAN_REGB_4 (Address 0x49)

Bit	Symbol	Default	Functional Description
15:0	CHAN_REGB_4<15:0>	0x0000	**Channel Configuration Reg B for Channel 4.** Calculated by Config-Gen Software.

3.13.18. CHAN_REGA_5 (Address 0x4A)

Bit	Symbol	Default	Functional Description
15:0	CHAN_REGA_5<15:0>	0x0000	**Channel Configuration Reg A for Channel 5.** Calculated by Config-Gen Software.

3.13.19. CHAN_REGB_5 (Address 0x4B)

Bit	Symbol	Default	Functional Description
15:0	CHAN_REGB_5<15:0>	0x0000	**Channel Configuration Reg B for Channel 5.** Calculated by Config-Gen Software.

3.13.20. CHAN_REGA_6 (Address 0x4C)

Bit	Symbol	Default	Functional Description
15:0	CHAN_REGA_6<15:0>	0x0000	**Channel Configuration Reg A for Channel 6.** Calculated by Config-Gen Software.

3.13.21. CHAN_REGB_6 (Address 0x4D)

Bit	Symbol	Default	Functional Description
15:0	CHAN_REGB_6<15:0>	0x0000	**Channel Configuration Reg B for Channel 6.** Calculated by Config-Gen Software.

3.13.22. CHAN_REGA_7 (Address 0x4E)

Bit	Symbol	Default	Functional Description
15:0	CHAN_REGA_7<15:0>	0x0000	**Channel Configuration Reg A for Channel 7.** Calculated by Config-Gen Software.

3.13.23. CHAN_REGB_7 (Address 0x4F)

Bit	Symbol	Default	Functional Description
15:0	CHAN_REGB_7<15:0>	0x0000	**Channel Configuration Reg B for Channel 7.** Calculated by Config-Gen Software.

3.13.24. CHAN_REGA_8 (Address 0x50)

Bit	Symbol	Default	Functional Description
15:0	CHAN_REGA_8<15:0>	0x0000	**Channel Configuration Reg A for Channel 8.** Calculated by Config-Gen Software.

3.13.25. CHAN_REGB_8 (Address 0x51)

Bit	Symbol	Default	Functional Description
15:0	CHAN_REGB_8<15:0>	0x0000	**Channel Configuration Reg B for Channel 8.** Calculated by Config-Gen Software.

3.13.26. CHAN_REGA_9 (Address 0x52)

Bit	Symbol	Default	Functional Description
15:0	CHAN_REGA_9<15:0>	0x0000	**Channel Configuration Reg A for Channel 9.**

			Calculated by Config-Gen Software.

3.13.27. CHAN_REGB_9 (Address 0x53)

Bit	Symbol	Default	Functional Description
15:0	CHAN_REGB_9<15:0>	0x0000	**Channel Configuration Reg B for Channel 9.** Calculated by Config-Gen Software.

3.13.28. CHAN_REGA_10 (Address 0x54)

Bit	Symbol	Default	Functional Description
15:0	CHAN_REGA_10<15:0>	0x0000	**Channel Configuration Reg A for Channel 10.** Calculated by Config-Gen Software.

3.13.29. CHAN_REGB_10 (Address 0x55)

Bit	Symbol	Default	Functional Description
15:0	CHAN_REGB_10<15:0>	0x0000	**Channel Configuration Reg B for Channel 10.** Calculated by Config-Gen Software.

3.13.30. CHAN_REGA_11 (Address 0x56)

Bit	Symbol	Default	Functional Description
15:0	CHAN_REGA_11<15:0>	0x0000	**Channel Configuration Reg A for Channel 11.** Calculated by Config-Gen Software.

3.13.31. CHAN_REGB_11 (Address 0x57)

Bit	Symbol	Default	Functional Description
15:0	CHAN_REGB_11<15:0>	0x0000	**Channel Configuration Reg B for Channel 11.** Calculated by Config-Gen Software.

3.13.32. CHAN_REGA_12 (Address 0x58)

Bit	Symbol	Default	Functional Description
15:0	CHAN_REGA_12<15:0>	0x0000	**Channel Configuration Reg A for Channel 12.** Calculated by Config-Gen Software.

3.13.33. CHAN_REGB_12 (Address 0x59)

Bit	Symbol	Default	Functional Description
15:0	CHAN_REGB_12<15:0>	0x0000	**Channel Configuration Reg B for Channel 12.** Calculated by Config-Gen Software.

3.13.34. CHAN_REGA_13 (Address 0x5A)

Bit	Symbol	Default	Functional Description
15:0	CHAN_REGA_13<15:0>	0x0000	**Channel Configuration Reg A for Channel 13** Calculated by Config-Gen Software.

3.13.35. CHAN_REGB_13 (Address 0x5B)

Bit	Symbol	Default	Functional Description
15:0	CHAN_REGB_13<15:0>	0x0000	**Channel Configuration Reg B for Channel 13.** Calculated by Config-Gen Software.

3.13.36. CHAN_REGA_14 (Address 0x5C)

Bit	Symbol	Default	Functional Description
15:0	CHAN_REGA_14<15:0>	0x0000	**Channel Configuration Reg A for Channel 14.** Calculated by Config-Gen Software.

3.13.37. CHAN_REGB_14 (Address 0x5D)

Bit	Symbol	Default	Functional Description
15:0	CHAN_REGB_14<15:0>	0x0000	**Channel Configuration Reg B for Channel 14.**

			Calculated by Config-Gen Software.

3.13.38. CHAN_REGA_15 (Address 0x5E)

Bit	Symbol	Default	Functional Description
15:0	CHAN_REGA_15<15:0>	0x0000	**Channel Configuration Reg A for Channel 15.** Calculated by Config-Gen Software.

3.13.39. CHAN_REGB_15 (Address 0x5F)

Bit	Symbol	Default	Functional Description
15:0	CHAN_REGB_15<15:0>	0x0000	**Channel Configuration Reg B for Channel 15.** Calculated by Config-Gen Software

4. Typical Application Circuit

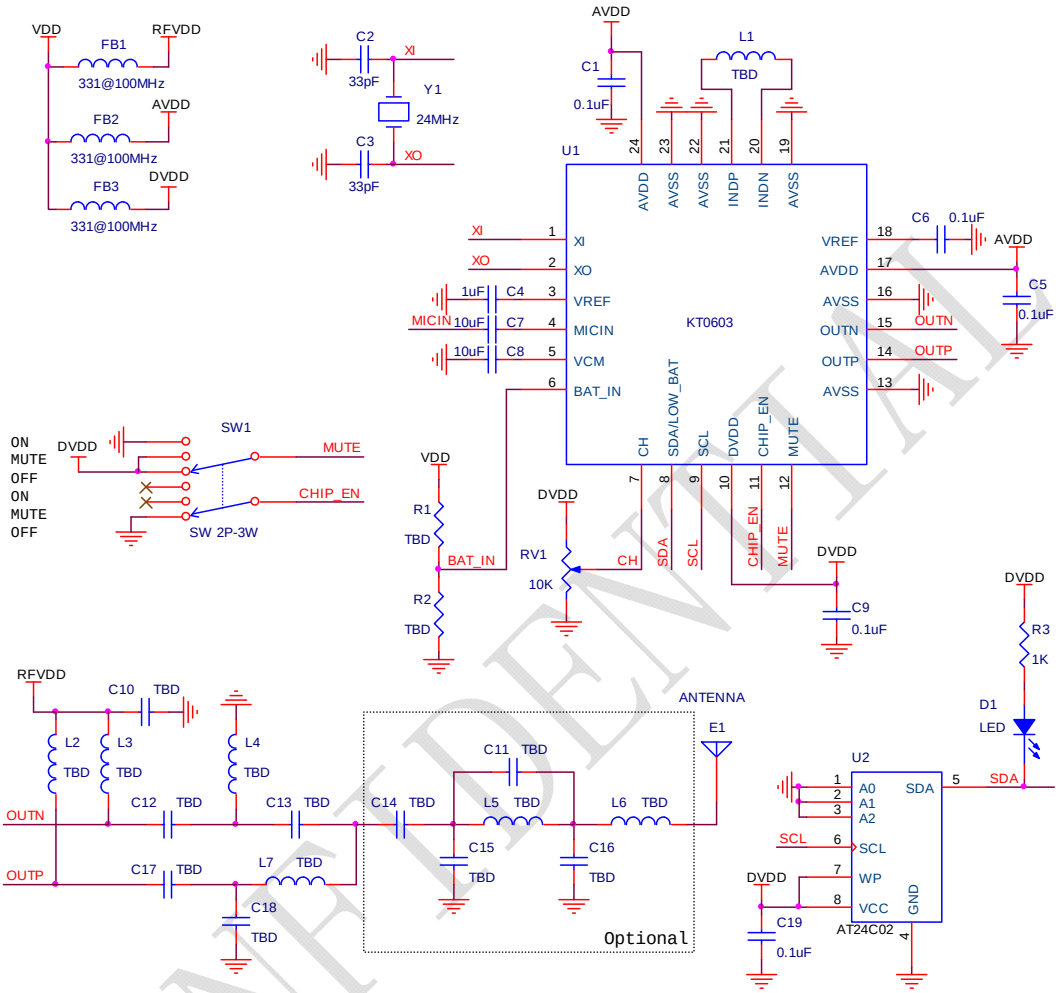
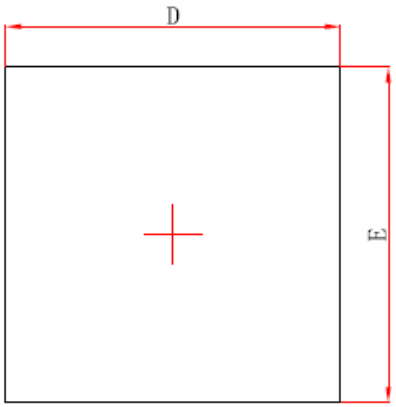


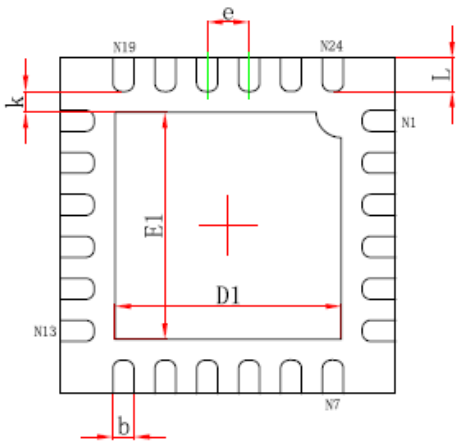
Figure 6: Typical application circuits

Components	Description	Value	Suppliers
C1,C5,C9,C19	Supply decoupling capacitor	0.1uF	
C2,C3	Crystal load capacitor	33pF	
C4	Decoupling capacitor	1uF	
C6	Decoupling capacitor	0.1uF	
C10	Decoupling capacitor	TBD	
C7,C8	Decoupling capacitor	10uF	
C11	Capacitor	TBD	
C12,C14,C17	Capacitor	TBD	
C13,C18	Capacitor	TBD	
C15	Capacitor	TBD	
C16	Capacitor	TBD	
D1	LED		
E1	Antenna		
FB1,FB2,FB3	Ferrite bead	331@100MHz	
L1	Inductance	TBD	Murata LQG series
L2,L3	Inductance	TBD	Murata LQG series
L4,L7	Inductance	TBD	Murata LQG series
L5,L6	Inductance	TBD	Murata LQG series
R1,R2	Resistor	TBD	
R3	Resistor	1K	
RV1	Variable resistor	10K	
SW1	Switch		
U1	KT0603		
U2	AT24C02		
Y1	Crystal	24MHz	

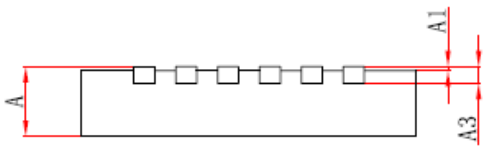
5. Package Outline



Top View



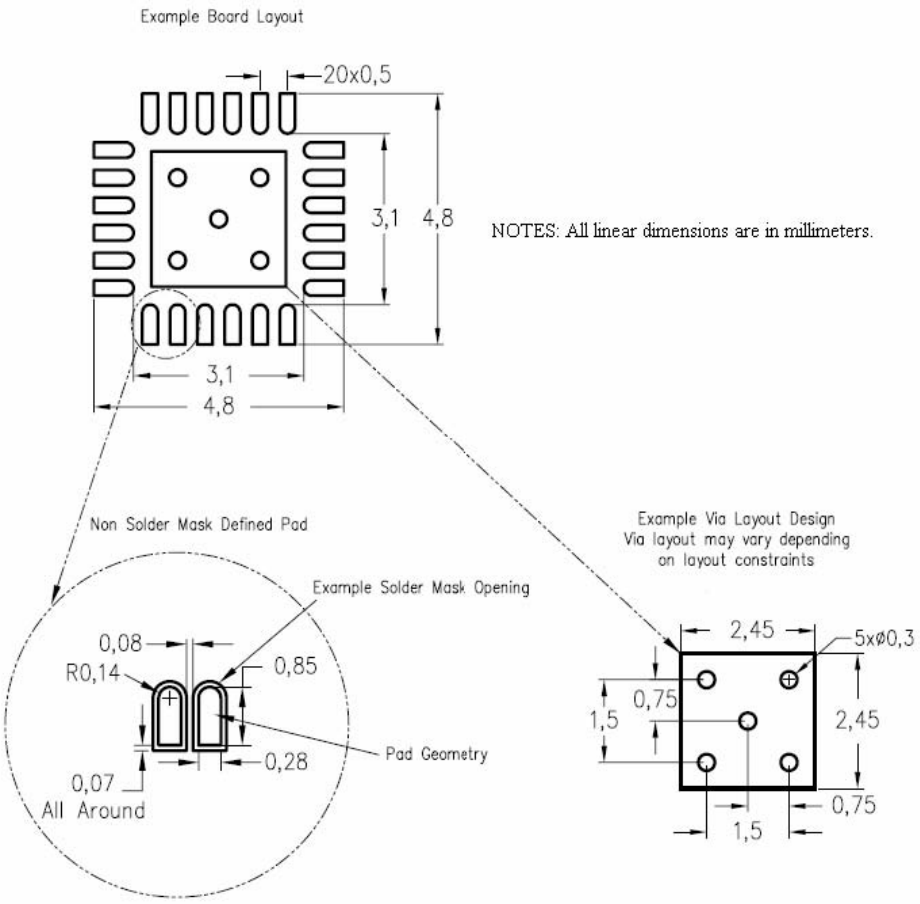
Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	3.900	4.100	0.154	0.161
E	3.900	4.100	0.154	0.161
D1	2.600	2.800	0.102	0.110
E1	2.600	2.800	0.102	0.110
k	0.200MIN.		0.008MIN.	
b	0.180	0.300	0.007	0.012
e	0.500TYP.		0.020TYP.	
L	0.300	0.500	0.012	0.020

6. PCB Land Pattern



7. Recommended Reflow Profile

The solder reflow profile should follow the paste manufacturer recommendation and the general JEDEC/IPC standard J-STD-20 guidelines. SnAgCu eutectic solder paste with melting temperature of 217℃ commonly used for lead-free solder reflow application. Figure 7 shows the range of temperature profiles of the J-STD-20 specification. The profile parameters and component peak temperature guidelines are listed in Table 7. Note all specified temperatures in Table 7 refer to the temperatures measured on the top surface of the package.

It is very important to control the peak reflow temperature below the maximum temperatures specified in Table 7 to prevent thermal damage to the package.

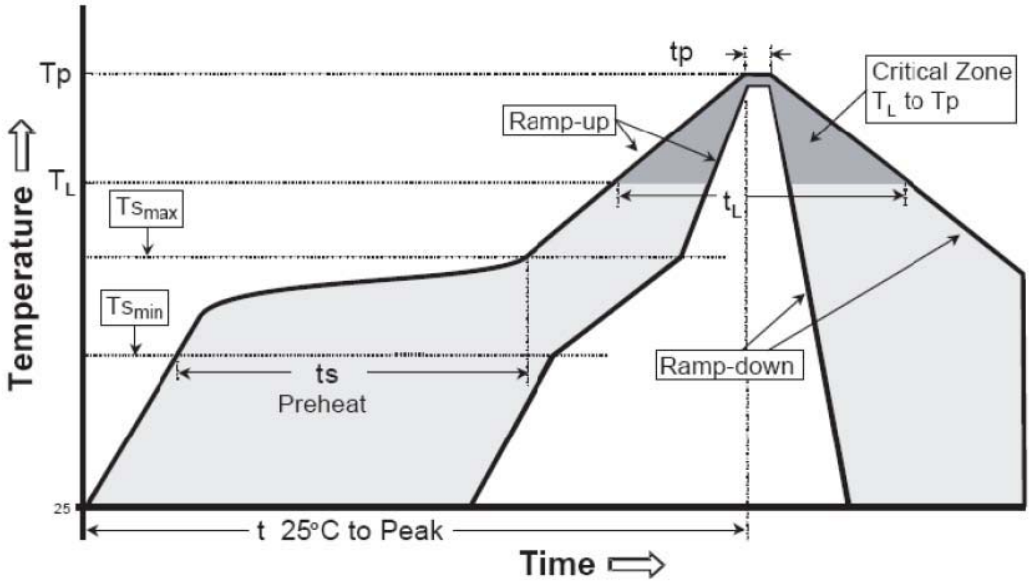


Figure 7: Typical reflow profile

Table 7: Reflow profile parameters

Profile Parameter	**Pb-FREE**
Average Ramp-Up Rate (TsMAX to Tp)	3℃/second maximum
Preheat: -Temperature Min (TsMIN) -Temperature Max (TsMAX) -Time (tsMIN to tsMAX)	 +150℃ +200℃ 60 to 180 seconds
Time maintained above: -Temperature (TL) -Time (tL)	 +217℃ 60 to 150 seconds
-Peak/Classification Temperature (Tp)	+260℃
Time within +5℃ of Actual Peak Temperature (tp)	20 to 40 seconds
Ramp-Down Rate	+6℃/second maximum
Time +25℃ to Peak Temperature	8 minutes maximum

8. Order Information

Part number	Description	Package
KT0603	Monolithic Digital UHF-band Transmitter	QFN24, Pb free

9. Revision History

V1. 0 Official Releases.
V1. 1 Modified register bank, application circuit and table 3.

10. Contact Information

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