Monolithic Digital UHF-band Receiver Wireless-Mic-on-a-Chip™

KT0616M

▪ Features

Fully integration
- **Low noise RF front end**
- **High fidelity digital audio processing**
- **Ultra Low noise LO synthesizer**

Worldwide full band support
- **UHF: 470MHz~960MHz**

Professional Grade Performance:
- **Low sensitivity: <-108dBm @12dB SINAD**
- **Audio Dynamic Range ≥ 106 dB**
- **Flat audio response: 20Hz~18KHz**
- **Low Distortion: <0.5%**

Ultra-Low Power Consumption:
- **< 100 mA operation current**
- **< 10 μA standby current**

Advanced Features:
- **Digital Auxiliary Channel**
- **Configurable Audio Harmonic Generator**
- **Configurable feedback noise cancellation**
- **Configurable bass boost and treble boost**
- **Configurable Audio Volume**
- **Configurable Automatic Mute Function**
- **Automatic Frequency Correction**
- **Built-in 75us de-emphasis**
- **Built-in Expandor**

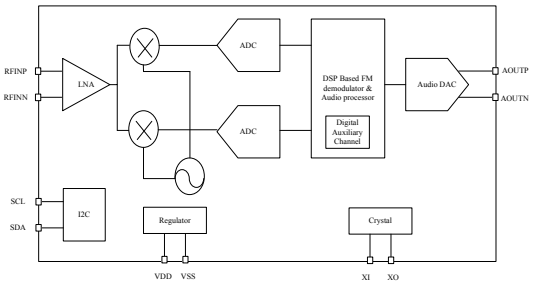
Small Form Factor:
- **QFN24 package**

Simple Interface:
- **Single power supply (2.7V- 3.6V)**
- **2-wire I²C slave interface**

Pb-free and RoHS Compliant

▪ Applications

Wireless Microphone, DVD player, Blue ray player, Set-top Box, Portable Device, Wireless Speaker



KT0616M System Diagram

▪ Description

The KT0616M is the UHF band chip of our full suite of the revolutionary wireless microphone chips, KT06xx, which replace hundreds of discrete components in a wireless microphone system while keeping the high standard of sound quality and functionality.

The KT0616M is a UHF band receiver that includes low noise amplifier, mixer, de-emphasis, expander, LO synthesizer and audio DAC. It is designed to process the modulated FM signal in UHF band and demodulate it into audio signal.

The KT0616M only requires a single low-voltage supply thanks to a built-in regulator. For an audio transmission system built with a KT0616M, no external tuning is required, which makes design-in effort minimum. And the KT0616M support digital auxiliary channel function.

The KT0616M is configured as an I²C slave and programmed through the industry standard 2-wire MCU interface. It is packaged in generic 24-pin QFN.

Rev.1.1

Beijing KT Micro, Ltd.
BeiWu New Technology Park, Building #4, 23 BeiWuCun Road,Haidian District, Beijing, China.
Tel: +86-10-88891955 http://www.ktmicro.com.cn
Fax: +86-10-88891977

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1. Electrical Specification

Table 1: Operation Condition

Parameter	Symbol	Operating Condition	Min	Typ	Max	Units
Analog Power Supply	AVDD	Relative to GND	2.7		3.6	V
Digital Power Supply	DVDD		2.7		3.6	V
Ambient Temperature	T_A		-30	25	70	℃
Electrostatic discharge maximum to MIL-Standard 883 C method 3015	Vmax				2000	V

Table 2: DC Characteristics

Parameter	Symbol	Test/Operating Condition	Min	Typ	Max	Units
Current Consumption	I_{VDD}		-	100	-	mA
Standby Current	I_{APD}			5	10	μA

Table 3: FM Receiver Characteristics

(Unless otherwise noted Ta = -30~70℃, AVDD= 2.7V to 3.6V)

Parameter	Symbol	Test/Operating Condition	Min	Typ	Max	Units
RF Frequency Range	F_{tx}		470		960	MHz
Sensitivity	Sen	SINAD=12		-108		dBm
Audio Dynamic Range[1,2,3]	DR	A-weighted		106		dB
Total Harmonic Distortion[1,2,3]	THD	Maximum Volume	-	0.3	0.5	%
Audio Output Swing	V_{out}		-		0.5	V_{RMS}
Audio Driving Capability	R_L			1		KΩ
Audio Frequency Response	F_{out}	Within 3dB	20	-	18K	Hz
Channel Step Resolution	STEP		-	25		KHz
Maximum Frequency Deviation					75	KHz
De-emphasis Time Constant	T_{pre}	PHTCNST = 1	-	75	-	μs
Crystal	CLK	Input clock		24/ 24.576		MHz
2-wire I^2C Clock	SCL			50		KHz

Notes:
1. FMOD=1KHz
2. △F=50KHz
3. V_{EMF}=1mV, Frequency=470MHz~960MHz

2. Pin List

Table 4: Pin list

Pin Index	Name	I/O Type	Function
1	XI	Analog I/O	Crystal input.
2	XO1	Analog I/O	1st Crystal output.
3	AVDD	Power	Analog power supply.
4	AOUTP	Analog Output	Audio positive output.
5	AOUTN	Analog Output	Audio negative output.
6	INT	Digital IO	Interrupt signal output.
7	N.C.	N.C.	No Connection.
8	SDA	Digital I/O	Serial data.
9	SCL	Digital I/O	Serial clock.
10	DVDD	Power	Digital power supply.
11	DVSS	Ground	Digital ground.
12	N.C.	N.C.	No Connection.
13	RFVSS	Ground	RF ground.
14	RFINP	Analog Input	RF positive input.
15	RFINN	Analog Input	RF negative input.
16	RFVSS	Ground	RF ground.
17	RFVDD	Power	Analog power supply.
18	AVDD	Power	Analog power supply.
19	VREF	Analog Output	VREF output. Should be decoupled by a 0.1uF cap.
20	AVSS	Ground	Analog ground.
21	INDP	Analog I/O	VCO inductor.
22	INDN	Analog I/O	VCO inductor.
23	AVSS	Ground	Analog ground.
24	XO2	Analog I/O	2nd Crystal output.

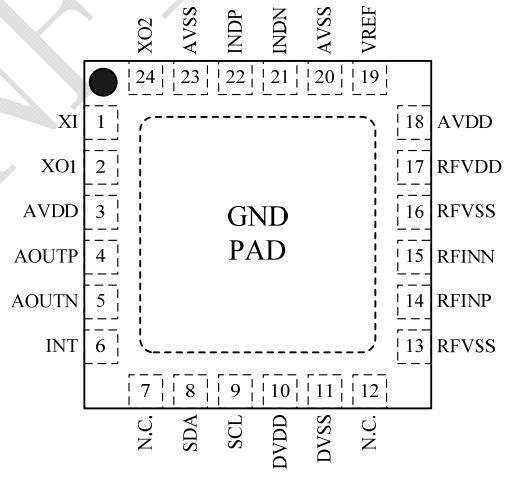


Figure 1: KT0616M Pin assignment (Top view)

3. Function Description

3.1. Overview

KT0616M offers a true single-chip, UHF-band wireless receiver solution by minimizing the external components and offering the compatibility with state-of-art transmitter solutions. It integrates a low-noise amplifier, mixers, LO synthesizer, FM demodulator, expandor and audio amplifier to provide RF sensitivity as low as -93dBm @80dB SNR and an audio dynamic range as high as 106dB. The excellent LO synthesizer with ultra low level phase noise ensures the high quality of the audio signal. A patented digital auxiliary channel is added in this chip to deal with the communication between the transmitter side and the receiver side. MCU can configure KT0616M through a simple I2C interface.

3.2. Power up and standby

KT0616M will enter normal operation mode within 50ms after power-supply is added to the power pins and the working clock is stable. To enter the standby mode, MCU should write STDBY to 1. Setting register STDBY back to 0 will wake up KT0616M to normal operation mode.

3.3. Crystal

KT0616M supports 24MHz/24.576MHz crystal to providing the working clock of the chip. The register XTAL_SEL is used to select crystal between 24MHz and 24.576MHz. When a 24MHz crystal is used, the register XTAL_SEL should be set to 0.

3.4. Expandor

KT0616M expands audio signal by a patent pending expandor circuit, which guarantees perfectly consistent performance compared with discrete solutions, whose performance is determined by the variant values of off-chip capacitors and resistors. The dynamic of audio signal is expanded by a precise 1 to 2 ratio. The time-constant of rectifier is set by register EXP_TC<2:0>. Setting EXP_DIS to 1 will disable the expandor.

3.5. Digital auxiliary channel

In order to cooperate with KT Micro's transmitter chip, digital auxiliary channel feature is also added in KT0616M to receive and demodulate the transmitted digital auxiliary information by KT060X series chip. This feature can be enabled AUXDATA_EN bits.
There are two application modes for digital auxiliary channel function:
In sequential mode, the received data of the digital auxiliary channel can be readout sequentially from register AUX_DATAA<7:0>, AUX_DATAB<7:0>, AUX_DATAC<7:0> and AUX_DATAD<7:0>.
In burst mode, the received data can be readout from BURST_DATA<15:0>.

An effective algorithm for the digital auxiliary channel will be provided by KT Micro. For more information, please refer to the application note.

3.6. Channel selection

KT0616M supports UHF 470MHz~960MHz operating frequency range. An off-chip inductor, connected to pins INDN and INDP, determines the center frequency of band specified by manufacturer. The actual channel frequency can be configured by user within the range of ±24MHz from center frequency once the inductor is fixed. To guarantee noise performance, high-Q multi-layer chip inductor is recommended if the inductor value exceeds 1nH. Otherwise, routing the inductance by PCB trace is recommended.

The actual received channel frequency is configured by register CHAN_REGA<15:0> and CHAN_REGB<15:0>, whose values could be obtained from the configuration software provided by KT Micro. Once CHAN_REGA or CHAN_REGB is written by a different value from the previous one, the internal LO synthesizer starts to lock to the new channel frequency. Within 50ms, the register PLL_READY will go high, indicating the PLL is locked.

For more information about off-chip inductor and channel configuration, please refer to application notes.

3.7. BASS, TREBLE and Harmonic Generator

KT0616M provides bass boost and treble boost feature to realize simple audio equalization. The gain of the bass boost and treble boost can be adjusted through BASS_BOOST<1:0> and TREBLE_BOOST<1:0> register bits.

In order to make the timbre more euphonious, KT0616M provides an on chip harmonic generator to add more even order harmonic in the audio signal. Register bits THD_POWER<1:0> is used to adjusted the power of the added harmonic.

3.8. Feedback noise cancellation

The squeal noise is very terrible in audio system and in order to eliminate this noise, a feedback noise cancellation algorithm is integrated in KT0616M. To enable this feature, SQUEAL_DIS bits should be clear to 0. For more information about the usage of squeal eliminator, please refer to the application note.

3.9. I2C interface

The serial interface (I2C mode) is used to read and write the device registers, the external controller can directly read and write a register without going through any other registers first. There is also an internal address counter that automatically moves the pointer forward after a read/write operation so that the external controller can continuously read/write desired number of chip registers starting from any of address. The MSB of a register data is transferred first.

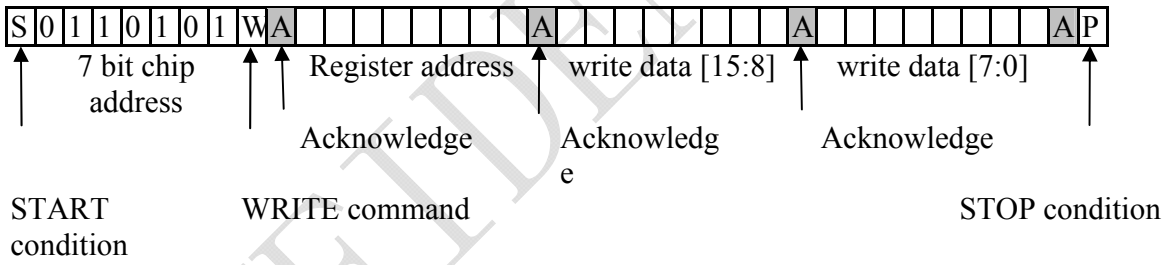
I2C bus mode uses SCL and SDA to transfer data. The device always drives data to SDA at the falling edge of SCL and captures data from SDA at the rising edge of SCL. The device acknowledges the external controller by driving SDA low at the falling edge of SCL. Data transfer always begins with START condition and ends with STOP condition. The external controller can read/write one 16-bits data at the specified address or read/write desired number of registers data continuously from the specified address till when STOP condition is occurred.

For write operations, external controller shall send command & data in the following sequence: START condition -> 7 bit chip address and Write command (“0”) -> 8 bit register address n -> write data n [15:8] -> write data n [7:0] -> write data n+1 [15:8] -> write data n+1 [7:0] -> …… -> STOP condition.

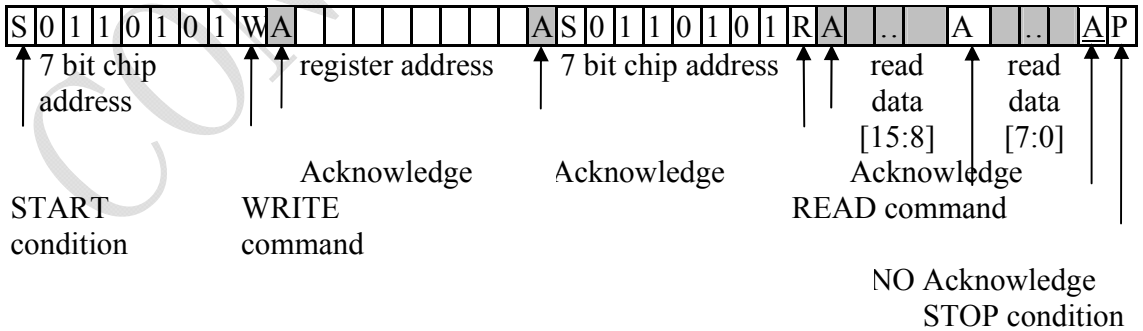
For read operations, external controller shall send command & data in the following sequence: START condition -> 7 bit chip address and Write command (“0”) -> 8 bit register address n -> 7 bit chip address and Read command (“1”) , then device will send read data n [15:8] -> read data n [7:0] -> read data n+1 [15:8] -> read data n+1 [7:0] -> …… till STOP condition.

Table 5: I2C Interface Protocol

RANDOM REGISTER WRITE PROCEDURE



RANDOM REGISTER READ PROCEDURE



Note: The data bits in gray color are sent by KT0616M

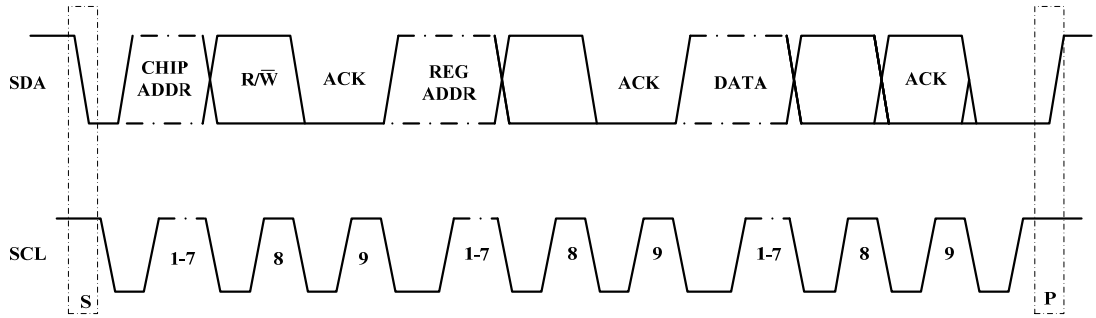


Figure 2: I2C interface timing diagram

3.10.Register Map

3.10.1. CHIP_ID (Address 0x01)

Bit	Name	Access	Default	Functional Description
15:0	KT Mark	R	0x4B54	**ASCII form of string "KT".**

3.10.2. BURST_DATA (Address 0x02)

Bit	Name	Access	Default	Functional Description
15:0	BURST_DATA <15:0>	RW	0x0000	**Data of the digital auxiliary channel in burst mode.**

3.10.3. AUX_DATAA (Address 0x03)

Bit	Name	Access	Default	Functional Description
15:0	AUX_DATAA<15:0>	RW	0x0000	**1st data of the digital auxiliary channel in sequence mode.**

3.10.4. AUX_DATAB (Address 0x04)

Bit	Name	Access	Default	Functional Description
15:0	AUX_DATAB<15:0>	RW	0x0000	**2nd data of the digital auxiliary channel in sequence mode.**

3.10.5. AUX_DATAC (Address 0x05)

Bit	Name	Access	Default	Functional Description
15:0	AUX_DATAC<15:0>	RW	0x0000	**3rd data of the digital auxiliary channel in sequence mode.**

3.10.6. AUX_DATAD (Address 0x06)

Bit	Name	Access	Default	Functional Description
15:0	AUX_DATAD<15:0>	RW	0x0000	**4th data of the digital auxiliary channel in sequence mode.**

3.10.7. SYSCFG (Address 0x07)

Bit	Name	Access	Default	Functional Description

15	STDBY	RW	0	**Standby mode enable.** 0: Normal work mode 1: Standby
14:9	Reserved	RW	000_000	**Reserved.**
8:6	Reserved	RW	0_00	**Reserved.**
5	XTAL_SEL	RW	0	**Crystal select.** 0: f=24M (1st) 1: f=24.576M (2nd)
4	Reserved	RW	1	**Reserved.**
3:0	Reserved	R	1000	**Reserved.**

3.10.8. CHAN_REGA (Address 0x0B)

Bit	Name	Access	Default	Functional Description
15:0	CHAN_REGA<15:0>	RW	0x0000	**Channel selection register A.**

3.10.9. CHAN_REGB (Address 0x0C)

Bit	Name	Access	Default	Functional Description
15:0	CHAN_REGB<15:0>	RW	0x0000	**Channel selection register B.**

3.10.10. PLL_STATUS (Address 0x10)

Bit	Name	Access	Default	Functional Description
15:12	Reserved	R	0000	**Reserved.**
11	PLL_READY	R	0	**PLL Status indicator.**0: Not ready 1: Ready
10:0	Reserved	RW	001_0111_0110	**Reserved.**

3.10.11. INT_CONFIG (Address 0x18)

Bit	Name	Access	Default	Functional Description
15	INT_EN	RW	0	**Interrupt enable control.** 0: No interrupt signal 1: Interrupt signal will output from INT pin
14	INT_LVL	RW	0	**Interrupt level selection.** 0: Low level interrupt 1: High level interrupt
13:6	Reserved	RW	11_1111_10	**Reserved.**
5	SQEAL_INT_EN	RW	0	**Squeal monitor interrupt enable.** 0: Disable 1: Enable
4	AUTOMUTE_INT_EN	RW	0	**Automute interrupt enable.** 0: Disable 1: Enable

3	PKGSYNC_INT_EN	RW	0	**Package synchronization interrupt enable.** 0: Disable 1: Enable
2	PILOT_INT_EN	RW	0	**Pilot detector interrupt enable.** 0: Disable 1: Enable
1	Reserved	RW	0	**Reserved.**
0	BURSTDATA_INT_EN	RW	0	**Burst mode data interrupt enable.** 0: Disable 1: Enable

3.10.12. INT_STATUS (Address 0x19)

Bit	Name	Access	Default	Functional Description
15:14	reserved	R	00	**Reserved.**
13	SQUEAL_STATUS	RW	0	**Indicator of the squeal detector.** 0: Squeal frequency is not detected. 1: Squeal frequency is detected.
12	MUTE_STATUS	R	0	**Status of the automute FSM.** 0: Mute is disable 1: Mute is enable
11	PKGSYNC_STATUS	RW	0	**Synchronization status of the auxiliary digital channel.** 0: Loss of synchronization 1: Synchronization
10	PILOT_STATUS	RW	0	**Indicator of the pilot carrier detector.** 0: No carrier frequency is detected. 1: Carrier frequency is detected.
9	STC_STATUS	RW	0	**Tune complete indicator.** 0: Tune FSM is still running 1: Tune complete
8:6	Reserved	R	00	**Reserved.**
5	SQUEAL_INT	RW	0	**If interrupt is triggered by squeal frequency detector, this bit will be set to 1 internally.**
4	AUTOMUTE_INT	RW	0	**If interrupt is triggered by automute detector, this bit will be set to 1 internally.**
3	PKGSYNC_INT	RW	0	**If interrupt is triggered by package synchronization block, this bit will be set to 1 internally.**
2	PILOT_INT	RW	0	**If interrupt is triggered by pilot frequency detector, this bit will be set to 1 internally.**
1	STC_INT	RW	0	**If interrupt is triggered by STC FSM, this bit will be set to 1 internally.**
0	BURSTDATA_INT	RW	0	**If interrupt is triggered by burst data detector, this bit will be set to 1 internally.**

3.10.13. VOLUME (Address 0x1A)

Bit	Name	Access	Default	Functional Description
15:8	Reserved	RW	00000000	**Reserved.**
7	AUTOMUTE_DIS	RW	1	**Automatic mute disable.** 0:Enable 1:Disable
6:5	Reserved	RW	0	**Reserved.**
4:0	VOLUME<4:0>	RW	0	**Volume control.** 0 : Mute 1 : -60dB …… 30:-4dB 31:-2dB

3.10.14. DSP_CONFIGA (Address 0x1D)

Bit	Name	Access	Default	Functional Description
15	Reserved	RW	0	**Reserved.**
14:12	AU_GAIN<2:0>	RW	000	**Configurable audio gain.** 000: 0dB 001: 3dB 010: 6dB 011: 9dB 100: 12dB 101: -4dB 110: -2.5dB 111: Reserved
11:8	Reserved	RW	0000	**Reserved.**
7	AFC_EN	RW	0	**Enable AFC.** 1: Enable 0: Disable
6	Reserved	RW	0	**Reserved.**
5:4	AFC_RNG<1:0>	RW	00	**Control the maximum frequency error range AFC can adjust.** 00: ±20kHz 01: ±40kHz 10: ±60kHz 11: ±90kHz
3:0	Reserved	RW	0000	**Reserved.**

3.10.15. DSP_CONFIGB (Address 0x1F)

Bit	Name	Access	Default	Functional Description
15	EXP_DIS<2:0>	RW	000	**Expandor disable.** 1: Disable 0: Enable

14:12	EXP_TC<2:0>	RW	000	**Time-constant of expandor rectifier.** 000: 6ms 001: 12ms 010: 24ms 011: 48ms 100: 93ms 101: 199ms 110: 398ms 111: 796ms
11:10	THD_POWER<1:0>	RW	00	**Audio THD enhancement.** 00: Bypass, not add extra THD 01: -40dB 10: -45dB 11: -51dB
9:4	Reserved	RW	000000	**Reserved.**
3:2	TREBLE_BOOST<1:0>	RW	00	**Boost high frequency.** 00: Bypass 01: Boost 4.0dB 10: Boost 5.2dB 11: Boost 7.3dB
1:0	BASS_BOOST<1:0>	RW	00	**Boost frequency around 220Hz.** 00: Bypass 01: Boost 6.16dB 10: Boost 9.73dB 11: Boost 14.2dB

3.10.16. DSP_AUXCFG (Address 0x20)

Bit	Name	Access	Default	Functional Description
15	AUXDATA_EN	RW	0	**Aux enable signal.** 1: Enable 0: Disable
14:0	Reserved	R	0	**Reserved.**

3.10.17. SQUEAL_CONFIG (Address 0x24)

Bit	Name	Access	Default	Functional Description
15	SQUEAL_DIS	RW	1	**Squeal elimination disable signal.** 1:Disable 0:Enable
14:0	Reserved	RW	0	**Reserved.**

3.10.18. STATUSA (Address 0x38)

Bit	Name	Access	Default	Functional Description
15:8	Reserved	R	0	**Reserved.**
7:0	SNR<7:0>	R	0	**SNR output.**

3.10.19. STATUSB (Address 0x3B)

Bit	Name	Access	Default	Functional Description
15:8	Reserved	R	0	**Reserved.**
7:0	RSSI<7:0>	R	0	**RSSI estimation value.**

4. Typical Application Circuit

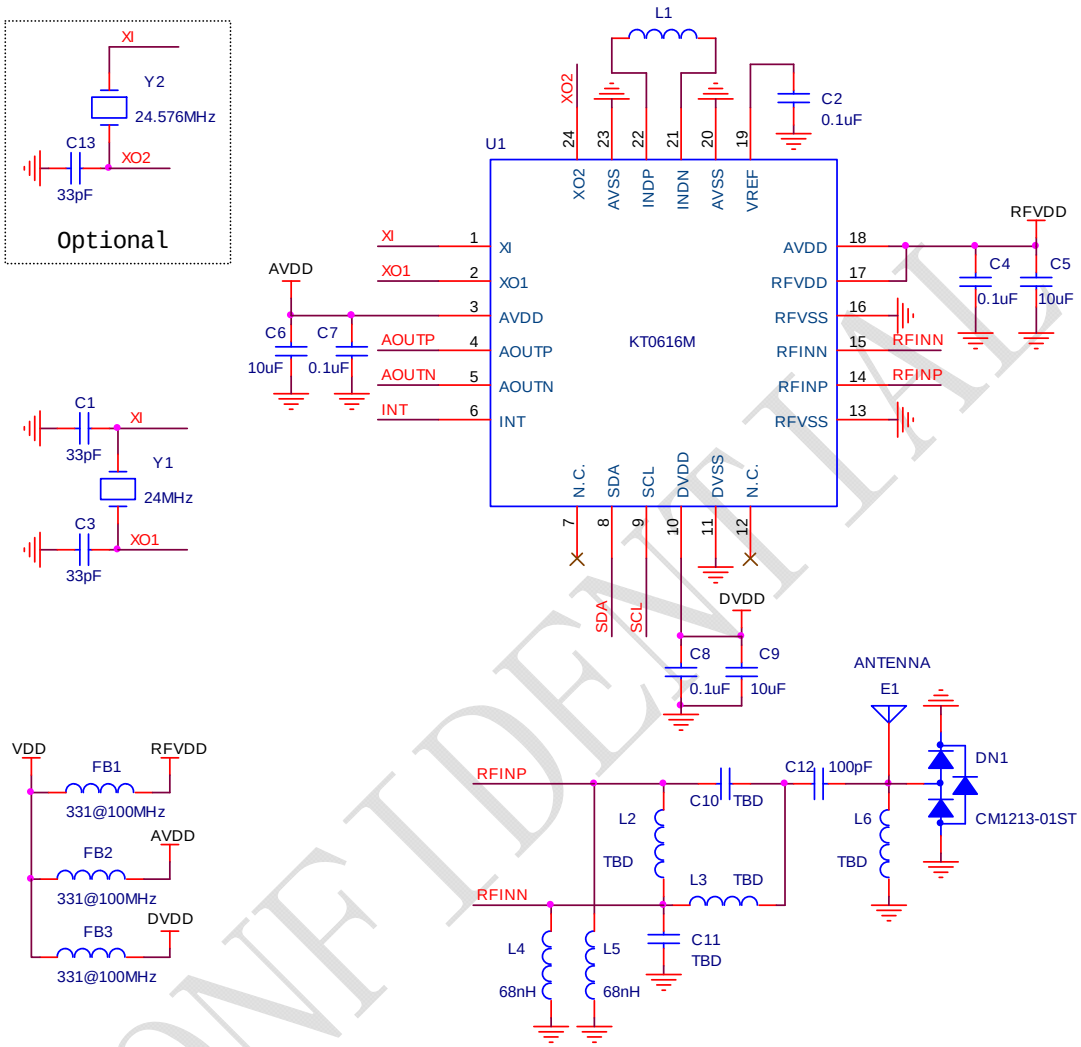
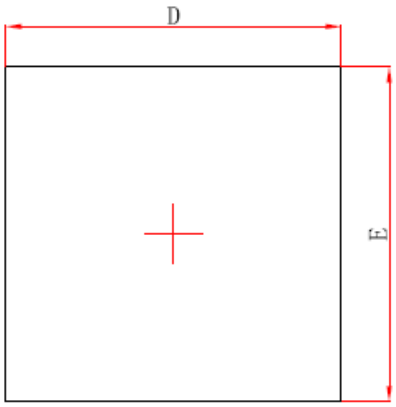


Figure 3: Typical application circuits

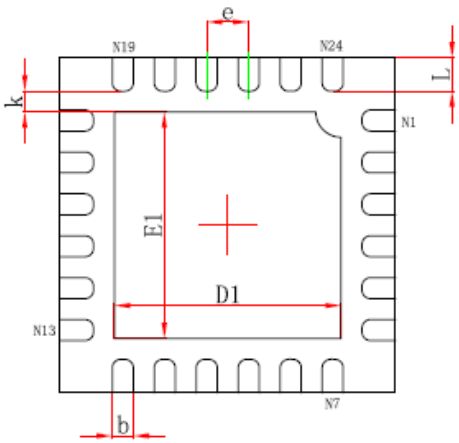
Components	Description	Value	Suppliers
C1,C3,C13	Crystal load capacitor	33pF	
C2,C4,C7,C8	Decoupling capacitor	0.1uF	
C5,C6,C9	Decoupling capacitor	10uF	
C10,C11	Capacitor	TBD	
C12	Decoupling capacitor	100pF	
DN1	Capacitor	CM1213-01ST	
E1	Antenna		
FB1, FB2, FB3	Ferrite bead	331@100MHz	
L1	Inductance	TBD	Murata LQG series
L2,L3,L6	Inductance	TBD	Murata LQG series
L4,L5	Inductance	68nH	Murata LQG series

U1	KT0616M		
Y1	Crystal	24MHz	
Y2	Crystal	24.576MHz	

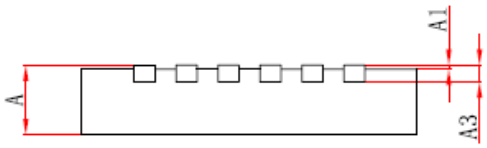
5. Package Outline



Top View



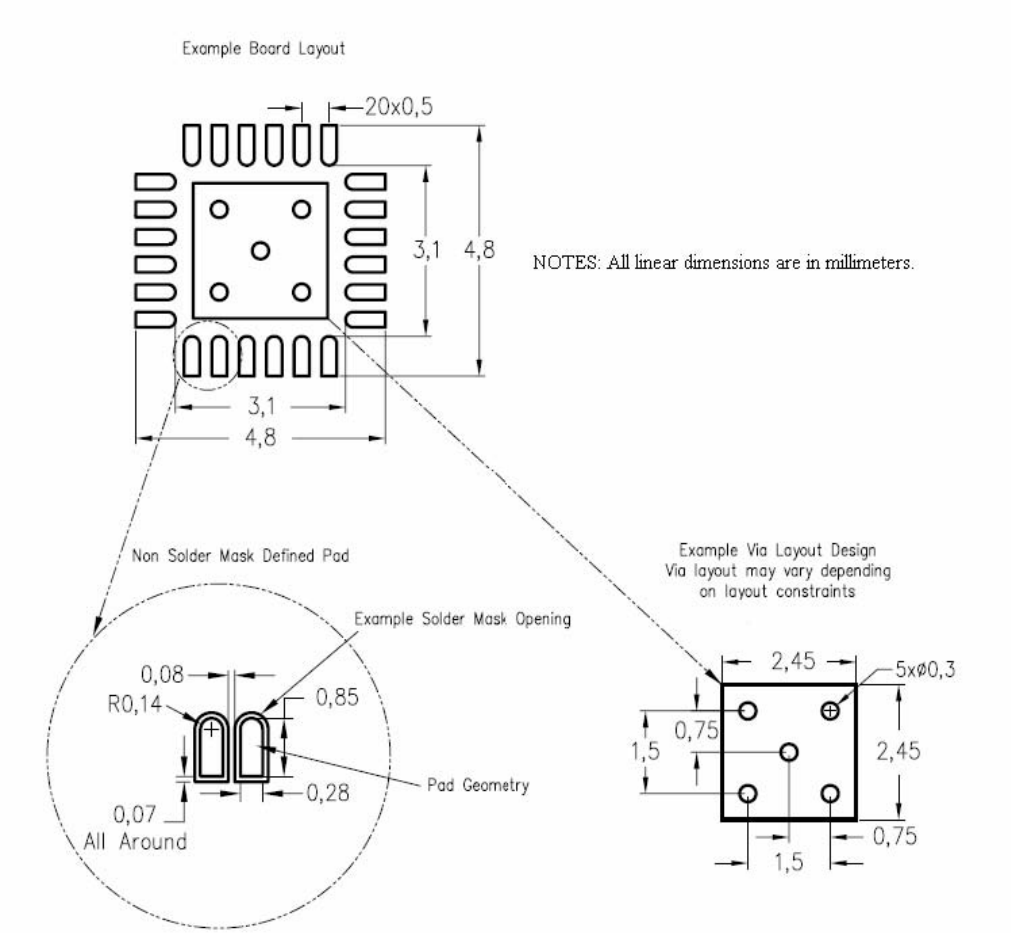
Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	3.900	4.100	0.154	0.161
E	3.900	4.100	0.154	0.161
D1	2.600	2.800	0.102	0.110
E1	2.600	2.800	0.102	0.110
k	0.200MIN.		0.008MIN.	
b	0.180	0.300	0.007	0.012
e	0.500TYP.		0.020TYP.	
L	0.300	0.500	0.012	0.020

6. PCB Land Pattern



7. Recommended Reflow Profile

The solder reflow profile should follow the paste manufacturer recommendation and the general JEDEC/IPC standard J-STD-20 guidelines. SnAgCu eutectic solder paste with melting temperature of 217℃ commonly used for lead-free solder reflow application. Figure 4 shows the range of temperature profiles of the J-STD-20 specification. The profile parameters and component peak temperature guidelines are listed in Table 6. Note all specified temperatures in Table 6 refer to the temperatures measured on the top surface of the package.

It is very important to control the peak reflow temperature below the maximum temperatures specified in Table 6 to prevent thermal damage to the package.

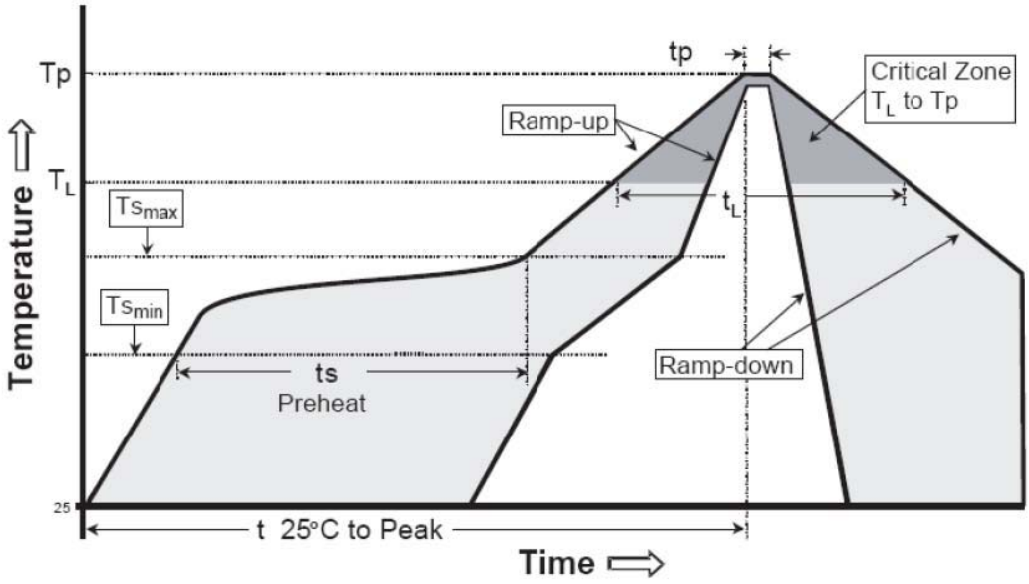


Figure 4: Typical reflow profile

Table 6: Reflow profile parameters

Profile Parameter	Pb-FREE
Average Ramp-Up Rate (TsMAX to Tp)	3℃/second maximum
Preheat: -Temperature Min (TsMIN) -Temperature Max (TsMAX) -Time (tsMIN to tsMAX)	 +150℃ +200℃ 60 to 180 seconds
Time maintained above: -Temperature (TL) -Time (tL)	 +217℃ 60 to 150 seconds
-Peak/Classification Temperature (Tp)	+260℃
Time within +5℃ of Actual Peak Temperature (tp)	20 to 40 seconds
Ramp-Down Rate	+6℃/second maximum
Time +25℃ to Peak Temperature	8 minutes maximum

8. Order Information

Part number	Description	Package
KT0616M	Monolithic Digital UHF-band Receiver	QFN24, Pb free

9. Revision History

V1. 0 Official Releases.
V1. 1 Modified Application Circuit.

10. Contact Information

Beijing KT Micro, Ltd.
BeiWu New Technology Park, Building #4, 23 BeiWuCun Road, Haidian District,
Beijing, China
Zip Code: 100195
Tel: +86-10-88891955
Fax: +86-10-88891977
Email: sales@ktmicro.com

Beijing KT Micro, Ltd. (US Office)
999 Corporate Drive, Suite 170
Ladera Ranch, CA 92694
USA
Tel: 949-713-4000
Fax: 949-713-4004
Email: sales@ktmicro.com