CHUKWUFUMNANYA OGBOGU

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RESEARCH INTERESTS

Low-power VLSI design, Computer Architecture, in-memory computing, Deep Learning Hardware accelerators.

EDUCATION

- **PhD. in Electrical Engineering & Computer Science** (4.0/4.0) Jan. 2021 - Present
  Washington State University. *Pullman, USA.*
  - Advisor: Prof. Partha Pande, co-advisor: Prof. Jana Doppa.
- **BSc. in Electronic and Electrical Engineering** Sep. 2014 - Dec. 2019
  Obafemi Awolowo University. *Ile-Ife, Nigeria.*
  - Dissertation: *A 0.55mW, 87dB Two-stage Low-Offset Operational Amplifier*, advised by Dr. Soji Ilori
  - Class rank: top 5%.

RESEARCH EXPERIENCE

Graduate Research Assistant Jan 2021 - Present
Washington State University – MARS lab *Pullman, USA*

- Working on hardware/software co-design of energy-efficient processing-in-memory architectures for accelerating Deep Learning and Graph Applications. (**Pytorch, Tensorflow, C++/CUDA**)
- Developing fault-tolerant schemes to enable reliable and high-performance neural network training on emerging non-memory systems. (**Python**)

Undergraduate Research Assistant Apr 2017 - Jun 2017
Obafemi Awolowo University *Ile-Ife, Nigeria*

- Implemented Schematic and Layout designs of basic CMOS Digital Logic Circuits. (**SPICE, CAD**)
- Performed Verification and Validation of Physical Layouts using Electric-VLSI Design Package

PUBLICATIONS

Journal Papers

- **C. Ogbogu**, A. Arka, L. Pfromm, B. Joardar, J. Doppa, K. Chakrabarty, P. Pande '*Accelerating Graph Neural Network Training on ReRAM-based PIM Architectures via Graph and Model Pruning*' in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, (Accepted!)
- **C. Ogbogu**, A. Arka, B. Joardar, J. Doppa, H. Li, K. Chakrabarty, P. Pande '*Accelerating Large-Scale Graph Neural Network Training on Crossbar Diet*' in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Nov. 2022 [Paper]

PROFESSIONAL EXPERIENCE

KPMG, Nigeria Jan 2020 - Aug 2020
Intern, Forensic Data Analyst *Lagos, Nigeria*

- I worked on fraud prediction models used in main-stream forensic audit procedures. (**Python**)
- Performed digital evidence recovery using EnCase and FTK software packages.

Total Exploration & Production Sep 2017 - Feb 2018
Intern, Electrical/Controls Engineer *Lagos, Nigeria*

- I was involved in installation of pipeline measurement and instrumentation equipment aboard oil and gas production vessel.
- Routine maintenance of electrical equipment aboard vessel.

OTHER PROJECTS

Clock Distribution in a SoC (Course project) (**Cadence Virtuoso**)
- Designed a H-tree Network-on-chip (NoC) topology on a $20mm \times 20mm$ die in 65nm tech node.
- Calculated the power dissipation and skew of the 2Ghz clock network in multiple clock domains.

GPU Acceleration of Kalman Filter [code] (**CUDA, PyCUDA**)
- Developed a framework that accelerates Kalman Filter Matrix operations on a GPU for Multiple Object tracking applications.
- Explored optimization techniques (coalescing memory accesses, avoiding memory bank conflicts etc) for SpMM of state transition matrices.
- Achieved 2× - 4× speed-up compared to its CPU implementation.

A 0.55mW, 87dB Two-stage Low-Offset Operational Amplifier (**SPICE, GLADE**)
Implemented design in 2.5 micron 2P2M CMOS technology (CNM 25).
- Designed schematic and physical layout of circuit using open-source layout and schematic editor (GLADE).
- Simulated and Optimized circuit for gain, area and quiescent power using SPICE-OPUS.
- Performed LVS and 3D parasitics extraction using Gemini and FastCap programs respectively

TECHNICAL STRENGTHS

Circuit Design & Analysis	Cadence Virtuoso, SPICE, Verilog.
Programming Languages and APIs	Python (Pytorch, Tensorflow), C/C++ (CUDA).
Others	Bash, LaTeX.

HONOURS AND AWARDS

- IEEE SSCS Conference Student travel grant award ($1000) — Dec 2018
- Murli T. Chellaram Foundation Scholarship — Aug 2017
- Dean's Honor roll First and Second year — Jan 2016
- Etisalat NG Merit Scholarship Award – value ($250) — Jan 2016
- MTN-NG Science and Technology Foundation Scholarship – cumm. value ($3,550) — Dec 2016
- Total EP National Merit Award Scholarship – cumm. value ($2,000) — Sep 2016

CONFERENCES AND TALKS

- CASES: International Conference on Compilers, Architectures, and Synthesis for Embedded Systems.
  Hybrid+Shanghai+Phoenix, AZ, Oct 2022.
- IEEE ESSCIRC/ESSDERC
  Krakow, Poland, Sep 2019.