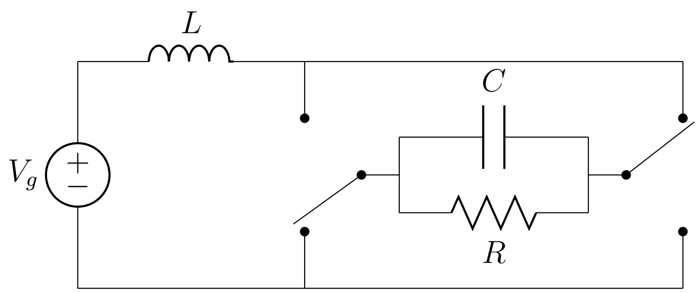
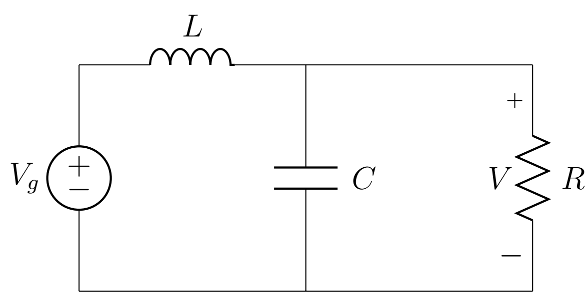
ECEN 4797 Fall 2014	Homework #2	Vince Coghlan

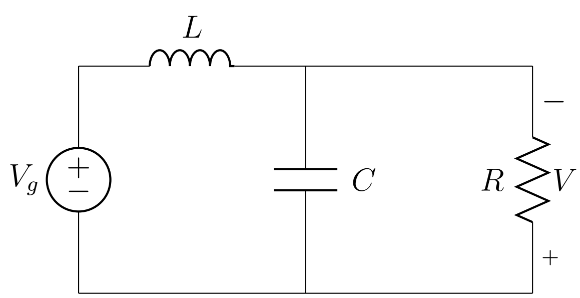
2.1: In the converter of Fig 3.31, the inductor has winding resistance R_L. All other losses can be ignored. The switches operate synchronously: each is in position 1 for $0 < t < DT_g$, and in position 2 for $DT_g < t < T_g$.



(a) Derive an expression for the nonideal voltage conversion ratio V/V_g.
In one state of the converter:



in the otehr state:



Using KVL:

$$V_L = V_g - i_L R_L - V \text{ and } V_L = V_g - i_L R_L + V$$

$$D(V_g - i_L R_L - V) + (1-D)(V_g - i_L R_L + V) = 0$$

$$DV_g - Di_L R_L - DV + V_g - i_L R_L + V - DV_g + Di_L R_L - DV = 0$$

$$-2DV + V_g - i_L R_L + V = 0$$

Using KCL:

$$i_C = i_L + \frac{V}{R} \text{ and } i_C = i_L - \frac{V}{R}$$

$$D(i_L - \frac{V}{R}) + (1-D)(i_L + \frac{V}{R}) = 0$$

$$\frac{-2DV}{R} + i_L + \frac{V}{R} = 0 \Rightarrow i_L = (2D-1)\frac{V}{R}$$

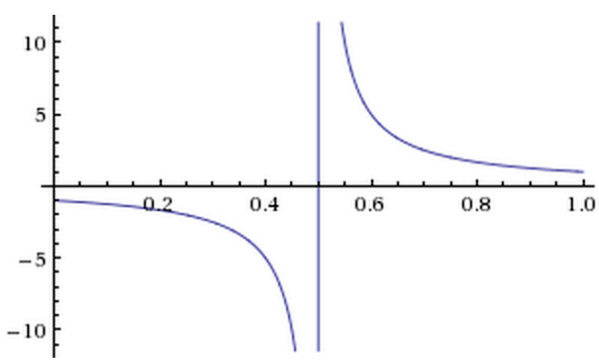
Two equations, two unknowns, we can plug and go:

$$-2DV + V_g - (2D-1)\frac{V}{R}R_L + V = 0$$

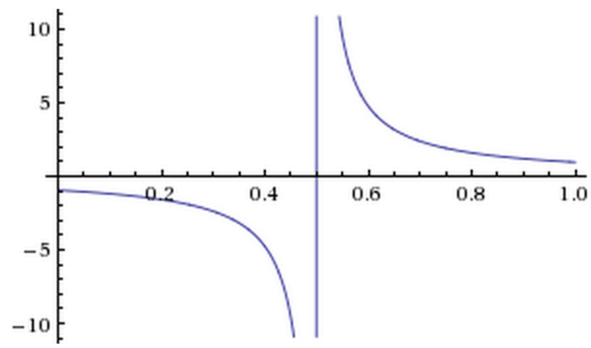
$$V_g = 2DV + (2D-1)\frac{VR_L}{R} - V$$

$$\frac{V}{V_g} = \frac{1}{2D + (2D-1)\frac{R_L}{R} - 1} = \frac{1}{(2D-1)(1+\frac{R_L}{R})}$$

(b) Plot your result of part (a) over the range $0 < D \leq 1$, for $R_L/R = 0.001$, amd 0.05.
For $\frac{R_L}{R} = 0.001$, we find:



For 0.05, we find:



(c) Derive an expression for the efficiency. Manipulate your expression into a form similar to Eq. (3.35)

Luckily for us, the same current is always flowing through L.

$$\eta = \frac{P_{in}}{P_{out}}$$

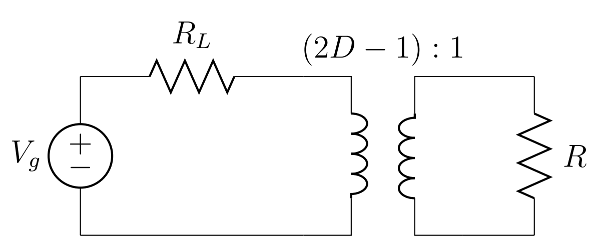
$$P_{in} = V_g \cdot I_L$$

$$P_{out} = V \cdot I_L$$

$$\eta = \frac{V_g}{V} = (2D - 1)(1 + \frac{R_L}{R})$$

It makes sense that at .5 duty cycle, no power would be transmitted, and the efficiency would be 0.

2.2: The inductor in the converter of Fig. 3.31 has winding resistance R_L. All other losses can be ignored. Derive an equivalent circuit model for this converter.



2.3: A 1.5V battery is used to power a 5V, 1A load. It has been decided to use a buck-boost converter in this application. A suitable transistor is found with an on-resistance of $35m\Omega$, and a Schottky diode is found with a forward drop of 0.5V. The on-resistance of the Schottky diode may be ignored. The power stage schematic is shown in Fig. 3.34.

(a) Derive an equivalent circuit that models the dc properties of this converter. Include the transistor and diode conduction losses, as well as the inductor copper loss, but ignore all other sources of loss. Your model should correctly describe the converter dc input port.
If we split up the circuit, we can do some analysis, using KVL:

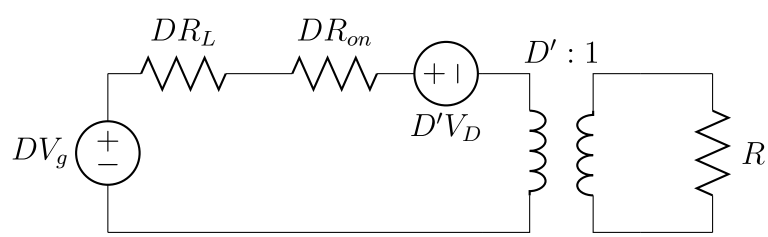
$$v_L = V_g - i_L R_L - i_L R_{on} \text{ and } v_L = V + V_D$$

$$D(V_g - i_L R_L - i_L R_{on}) + D'(V + V_D) = 0$$

using KCL:

$$i_c = \frac{V}{R} \text{ and } i_c = \frac{V}{R} - i_L$$

$$D(\frac{V}{R}) + D'(\frac{V}{R} - i_L) = 0$$



(b) It is desired that the converter operate with at least 70% efficiency under normal conditions (i.e., when the input voltage is 1.5 V and the output voltage is 5V at 1 A). How large can the inductor winding resistance be? At what duty cycle will the converter then operate? *Note:* there is an easy way and a not-so-easy way to analytically solve this part.
We know that the output power is $P_{out} = IV = 5W$. We can work backwards to account for power loss in every component in the circuit.

$$\eta = \frac{P_{out}}{P_{in}} = 0.7 = \frac{5}{P_{in}} \Rightarrow P_{in} = \frac{5}{0.7} \Rightarrow I_{in} = \frac{5/.7}{1.5}$$

$$\frac{5}{.7} = \frac{5/.7}{1.5}(0.035) + (\frac{5/.7}{1.5} - 1)R_L + (1 \cdot 0.5) + 5$$

$$R_L = 0.3924\Omega$$