Digital Integrated Circuits

#Homework 2 2024.03.16 (Due: 03.22, 13:20)

/* Using 32 nm CMOS devices with **VDD= 0.8 V**, Wmin=64 nm, Lmin=32nm with resolution of 1nm; there are three kinds of Vt: High Vt, medium Vt and low Vt CMOS*/

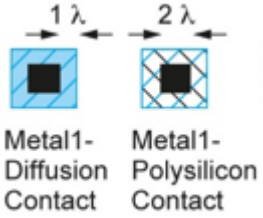
All the transistors use Low Vt

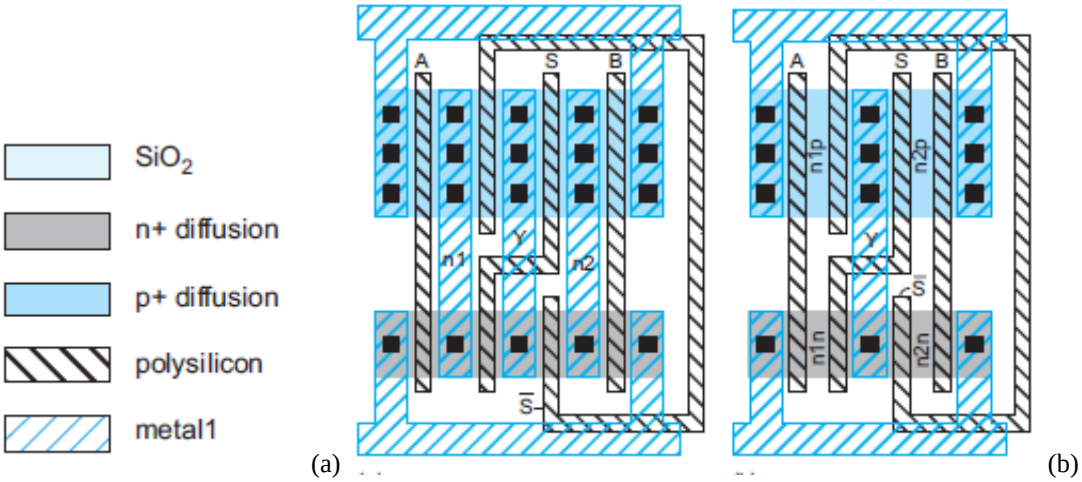
1. (40%)

a) (20%) Draw the circuit schmetic of the attached layout (a) and (b). The signal name of each node shall be marked at the schematic. Explain which circuit has higher speed.

b) (10%) Indicate the W/L ratio (X.Y) and AD/AS (in terms of λ) of each transistor.

c) (10%) Mark the design rules in this layout that determine the width of this layout.





2.Timing and power analysis (60%)

(a) (15%) Design a two inputs NAND logic gate (NAND2) as shown at Fig.9.8 such that it has the logic threshold of 0.45*VDD (when two inputs have the same voltage). Indicate the W/L of PMOS and NMOS and show the Spice simulation results of VTC.

(b) (10%) Run SPICE to get the output capacitances of the NAND2 and input capacitance of NAND2, leakage power dissipation when input and output are in 0/1 and 1/0 respectively (estimate reasonable AD, AS, PD, PS using the micro rule listed in the page 3-19 of the note with scale ratio 32/65)

(c) (25%) Do the timing and power analysis of a NAND2 (Fig.9.8) which has a fanout of two NAND2s. Input signal is a pulse waveform with duration of 2ns (with tr=0.4ns and tf=0.4ns defined as 0%-100%, duty=0.5). Run two cases by using SPICE (5ns) to get the timing (tdf and tdr) and power waveform: (i) A=1 and B changes from 0 to 1, (ii) B=1 and A=1changes from 0 to 1. Then list in table form with the tdf, tdr, average power and peak power of the NAND2.

(d) (10%) Discuss the behavior of two cases based on the SPICE simulation results.

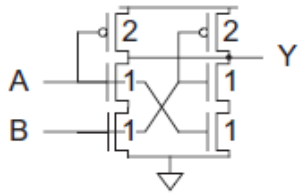


FIGURE 9.8 Perfectly symmetric 2-input NAND gate