Lec1 Introduction to HSPICE

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SPICE Overview

- SPICE

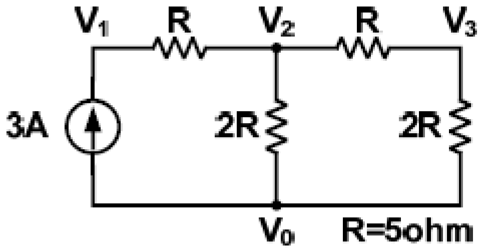
  Simulation Program with Integrated Circuit Emphasis

  - A transistor level simulation tool
  - Developed by University of California/Berkeley
  - In market—SBTSPICE, HSPICE, Spectre ,TSPICE, Pspice, Smartspice ...

SPICE Overview

- HSPICE Calculation

➢ Linear: Gaussian elimination method



$$\begin{pmatrix} 0.2 & 0 & -0.1 & -0.1 \\ 0 & 0.2 & -0.2 & 0 \\ -0.1 & -0.2 & 0.5 & -0.2 \\ 0 & 0 & -0.2 & 0.3 \end{pmatrix}\begin{pmatrix} V_0 \\ V_1 \\ V_2 \\ V_3 \end{pmatrix} = \begin{pmatrix} -3 \\ 3 \\ 0 \\ 0 \end{pmatrix}$$

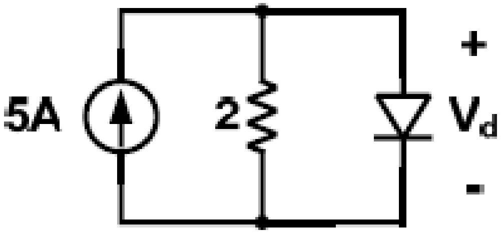
$$\begin{pmatrix} 0.2 & -0.2 & 0 \\ -0.2 & 0.5 & -0.2 \\ 0 & -0.2 & 0.3 \end{pmatrix}\begin{pmatrix} V_1 \\ V_2 \\ V_3 \end{pmatrix} = \begin{pmatrix} 3 \\ 0 \\ 0 \end{pmatrix}, V_0 \text{ is ground}$$

With Gaussian elimination

$$\begin{pmatrix} 0.2 & -0.2 & 0 \\ 0 & 0.3 & -0.2 \\ 0 & 0 & 0.25 \end{pmatrix}\begin{pmatrix} V_1 \\ V_2 \\ V_3 \end{pmatrix} = \begin{pmatrix} 3 \\ 3 \\ 3 \end{pmatrix}$$

Results: $V_1 = 33V$, $V_2 = 18V$, $V_3 = 12V$

➢ Nonlinear: Numerical analysis



$$I_d = 1pA \times \left[e^{(40 \times V_d)} - 1\right]$$

$$5 = \frac{V_d}{2} + Id$$

$$5 = \frac{V_d}{2} + 1pA \times \left[e^{(40 \times V_d)} - 1\right]$$

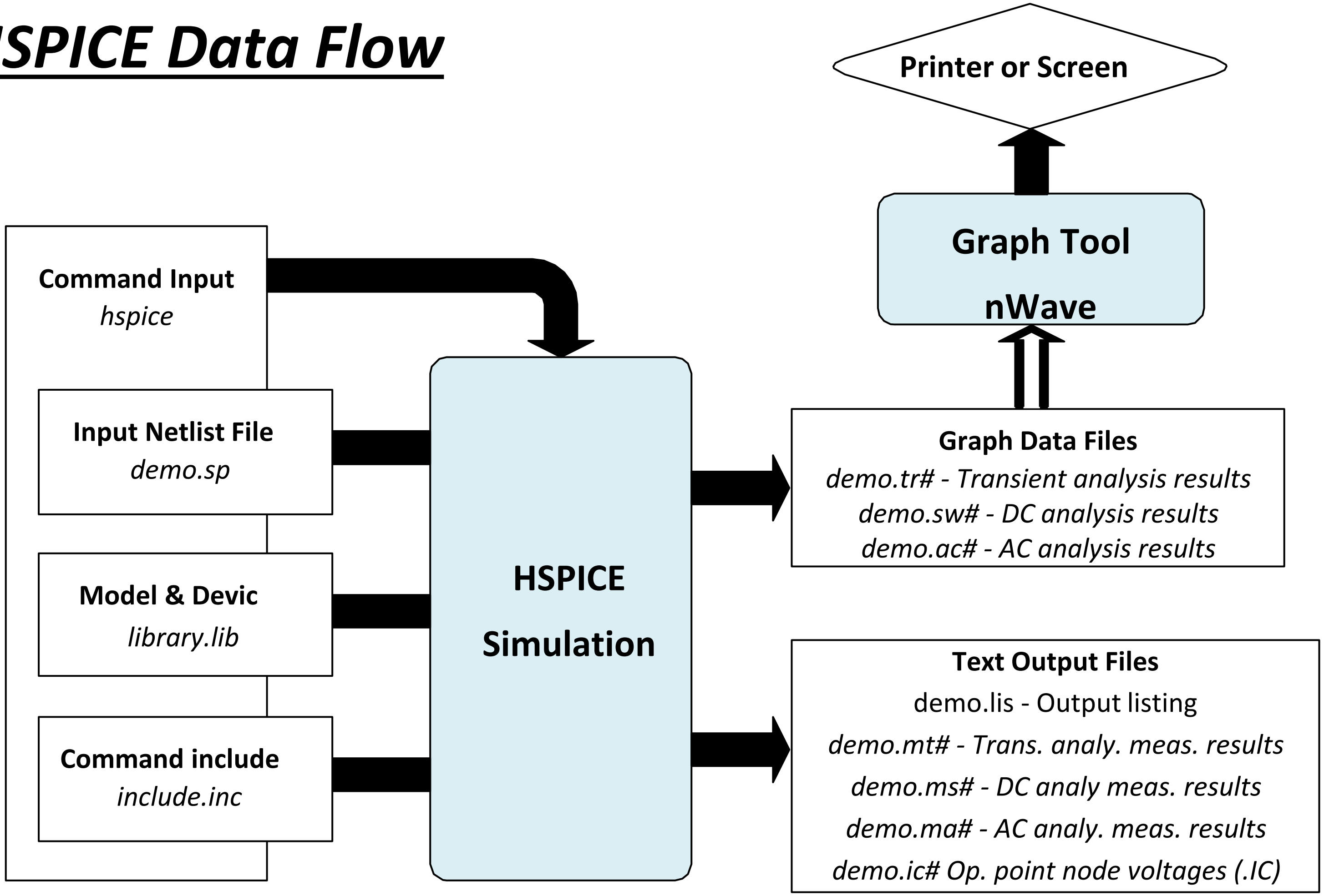
$$V_{d+1} = V_d - \frac{F(V_d)}{F'(V_d)}$$

Convergence criteria : Delta $V = (V_{d+1} - V_d) < 0.001$

Reference:chrome-extension://efaidnbmnnnibpcajpcglclefindmkaj/http://scholar.fju.edu.tw/%E8%AA%B2%E7%A8%8B%E5%A4%A7%E7%B6%B1/upload/013031/content/962/D-5013-02530-.pdf

SPICE Overview (Cont’d)

HSPICE Data Flow



Printer or Screen

Graph Tool

nWave

Command Input
hspice

Input Netlist File
demo.sp

Model & Devic
library.lib

Command include
include.inc

HSPICE

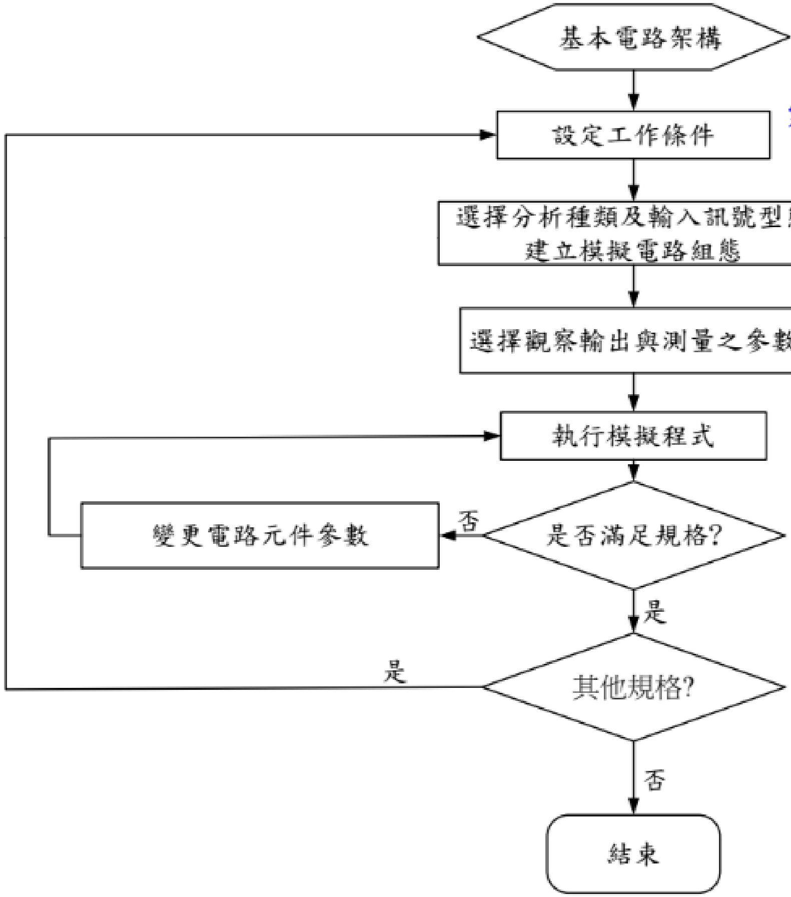
Simulation

Graph Data Files
demo.tr# - Transient analysis results
demo.sw# - DC analysis results
demo.ac# - AC analysis results

Text Output Files
demo.lis - Output listing
demo.mt# - Trans. analy. meas. results
demo.ms# - DC analy meas. results
demo.ma# - AC analy. meas. results
demo.ic# Op. point node voltages (.IC)

SPICE Overview (Cont’d)

Basic flow for SPICE



基本電路架構

設定工作條件

製程條件、工作電壓
、溫度、負載

選擇分析種類及輸入訊號型態
建立模擬電路組態

OP/DC/TRAN/AC

選擇觀察輸出與測量之參數

.probe/measurement

執行模擬程式

是否滿足規格?

否

變更電路元件參數

是

其他規格?

是

否

結束

Reference:chrome-extension://efaidnbmnnnibpcajpcglclefindmkaj/http://scholar.fju.edu.tw/%E8%AA%B2%E7%A8%8B%E5%A4%A7%E7%B6%B1/upload/013031/content/962/D-5013-02530-.pdf

SPICE

- Netlist Structure :

xxx.sp

Title Inverter

Ignored during simulation

Set-up

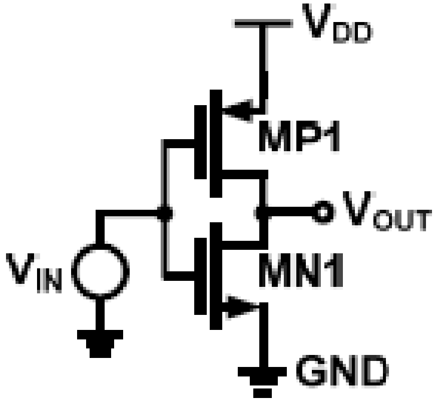
```
. options post
. param supply = 1.8v
. global vdd gnd
```

Sources

```
vin vin gnd 0v
```

Circuits

```
MP1 vout vin vdd vdd pch l=1u w=4u
MN1 vout vin gnd gnd nch l=1u w=1u
```



Analysis

```
.dc vin 0 1.8 0.01
. print v(5) i(r1)
. plot v(3) v(in)
  ...........
```

End file

```
. end
```

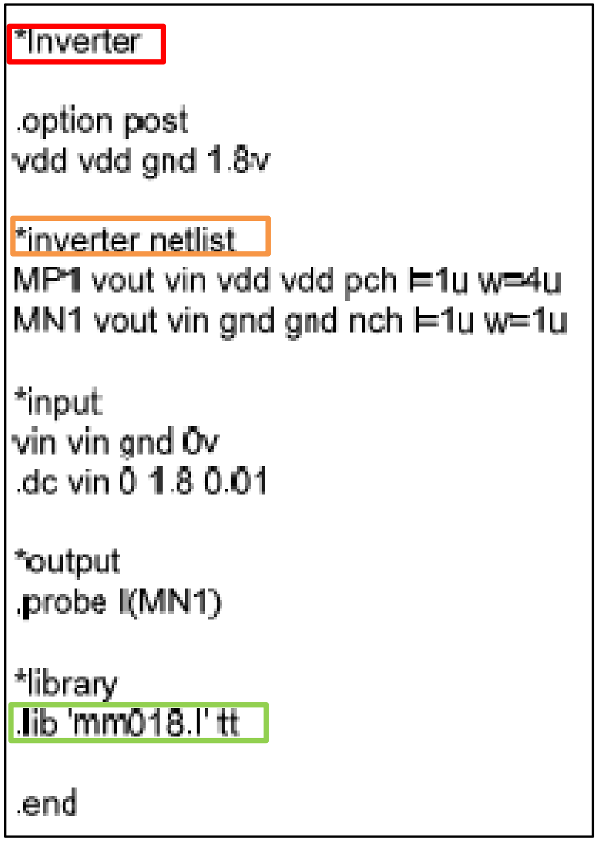
SPICE - Syntax

- TITLE
  - First line is input netlist file title (not executed)
  - up to 72 characters
- ‘*’ or ‘$’
  - Comments to describe circuit
- ‘+’ or ‘\’
  - Continued line

  Ex:

```
.MEAS  TRAN  Trise         TRIG   v(out)   VAL=‘0.1*Vmax’   RISE=2
+                          TARG   v(out)   VAL =‘0.9*Vmax’  RISE=2
```

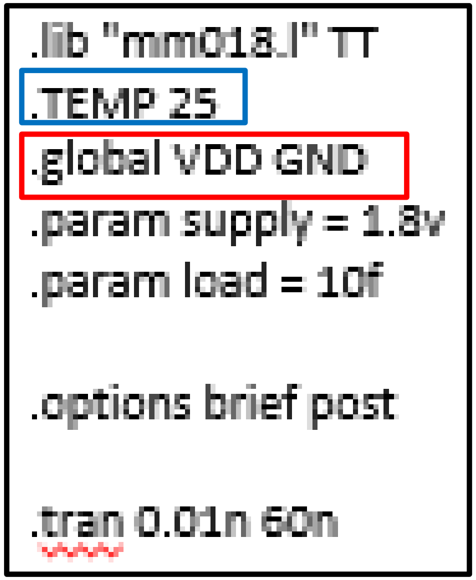
- .LIB/.INCLUDE
  - Call library or general include files
  - Syntax : ***.LIB ‘<filepath> filename’***



```
*Inverter

.option post
vdd vdd gnd 1.8v

*inverter netlist
MP1 vout vin vdd vdd pch l=1u w=4u
MN1 vout vin gnd gnd nch l=1u w=1u

*input
vin vin gnd 0v
.dc vin 0 1.8 0.01

*output
.probe I(MN1)

*library
.lib 'mm018.l' tt

.end
```

SPICE - Syntax

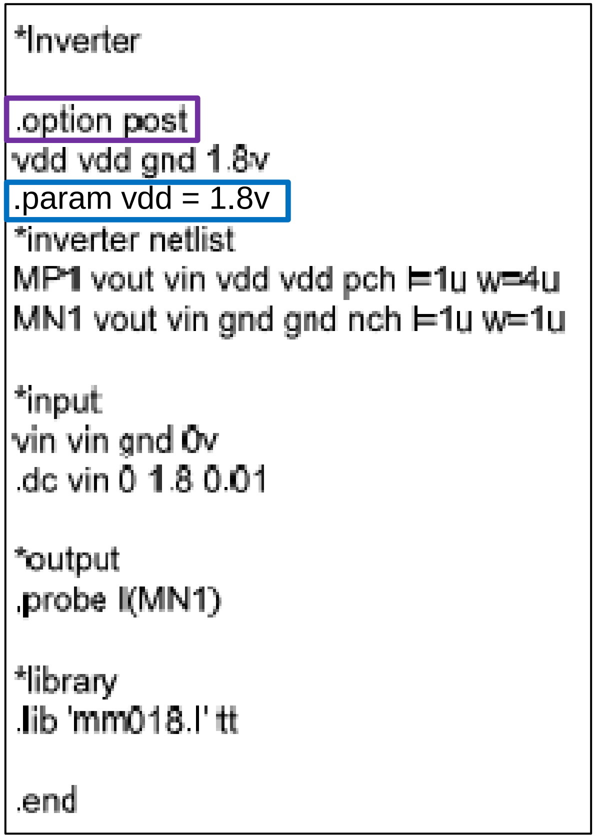
- .global
  - Globally assigns a node name
  - Syntax : ***.GLOBAL node1 node2 node3 …***
- .TEMP
  - Specifies the circuit temperature for an HSPICE simulation
  - Syntax : ***.TEMP t1***
- .END
  - Ending file



```
.lib "mm018.l" TT
.TEMP 25
.global VDD GND
.param supply = 1.8v
.param load = 10f

.options brief post

.tran 0.01n 60n
```

SPICE - Syntax

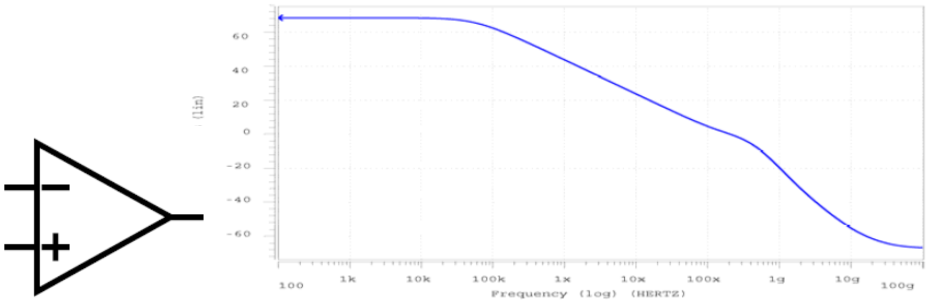
- .Options
  - Set conditions for simulation
  - Syntax : ***.OPTIONS opt1 <opt2 ...>***
  - .options post
    - the output file contains simulation output suitable for a waveform display tool
  - .options brief
    - Not to print very detail information
- .param
  - Defines parameters in HSPICE
  - Syntax: ***.PARAM <ParamName>=<Value>***



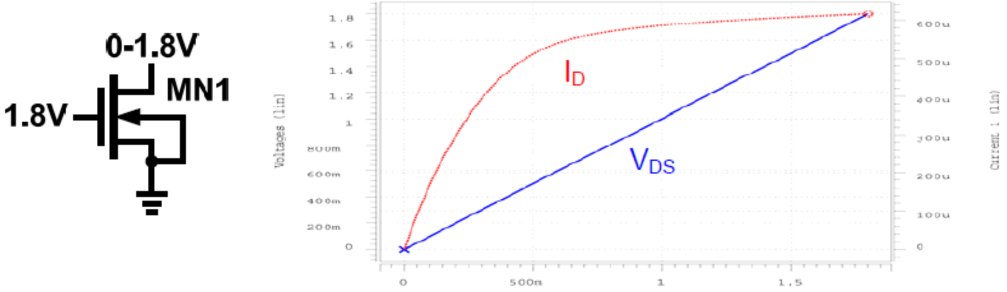
```
*Inverter

.option post
vdd vdd gnd 1.8v
.param vdd = 1.8v
*inverter netlist
MP1 vout vin vdd vdd pch l=1u w=4u
MN1 vout vin gnd gnd nch l=1u w=1u

*input
vin vin gnd 0v
.dc vin 0 1.8 0.01

*output
.probe I(MN1)

*library
.lib 'mm018.l' tt

.end
```

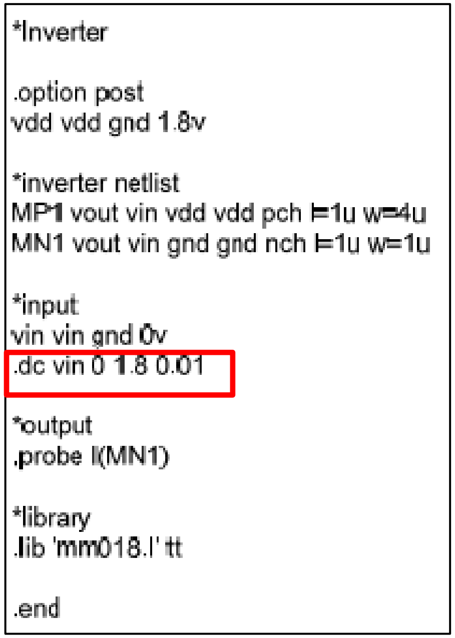
SPICE - Syntax

- Analysis
  - Statements to set sweep variables
    - .AC: Frequency response AC analysis



    - .DC: Steady-state DC analysis



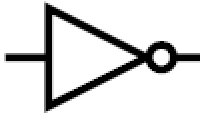


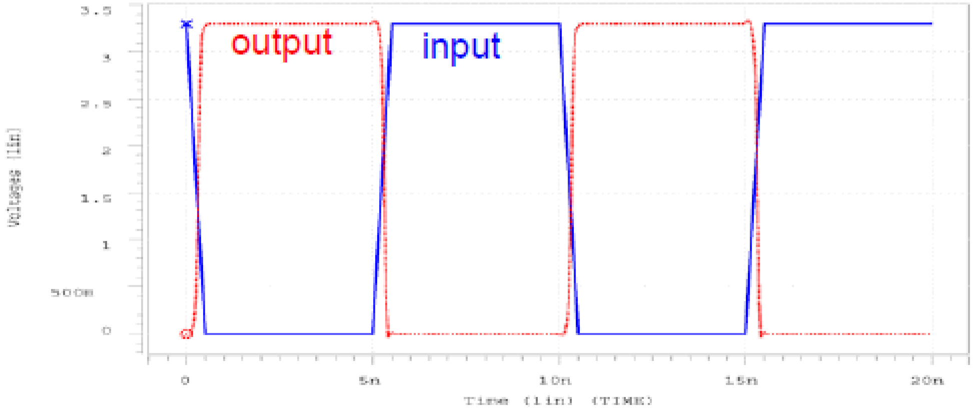
```
*Inverter

.option post
vdd vdd gnd 1.8v

*inverter netlist
MP1 vout vin vdd vdd pch l=1u w=4u
MN1 vout vin gnd gnd nch l=1u w=1u

*input
vin vin gnd 0v
.dc vin 0 1.8 0.01

*output
.probe I(MN1)

*library
.lib 'mm018.l' tt

.end
```

Reference:chrome-extension://efaidnbmnnnibpcajpcglclefindmkaj/http://scholar.fju.edu.tw/%E8%AA%B2%E7%A8%8B%E5%A4%A7%E7%B6%B1/upload/013031/content/962/D-5013-02530-.pdf

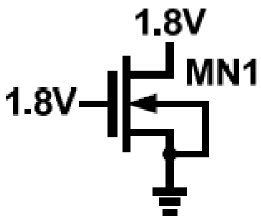
SPICE - Syntax

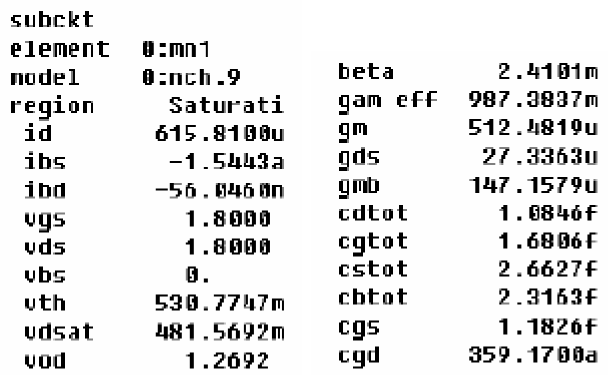
- .TRAN : Time transient analysis





- .OP: Operating point analysis





```
subckt
element  0:mn1
model    0:nch.9            beta      2.4101m
region     Saturati         gam eff  987.3837m
 id        615.8100u        gm       512.4819u
 ibs        -1.5443a        gds       27.3363u
 ibd       -56.0460n        gmb      147.1579u
 vgs         1.8000         cdtot      1.0846f
 vds         1.8000         cgtot      1.6806f
 vbs         0.             cstot      2.6627f
 vth       530.7747m        cbtot      2.3163f
 vdsat     481.5692m        cgs        1.1826f
 vod         1.2692         cgd      359.1700a
```

Reference:chrome-extension://efaidnbmnnnibpcajpcglclefindmkaj/http://scholar.fju.edu.tw/%E8%AA%B2%E7%A8%8B%E5%A4%A7%E7%B6%B1/upload/013031/content/962/D-5013-02530-.pdf

SPICE - analysis

- DC analysis- syntax
  - ***.DC var1 start1 stop1 incr1 < var2 start2 stop2 incr2 >***
  - ***.DC var1 start1 stop1 incr1 < sweep var2 type incr2 start2 stop2 >***
- AC analysis- syntax
  - ***.AC type point fstart fstop***
  - ***.AC type point fstart fstop <sweep var2 start2 stop2 incr2 >***
- TRAN analysis- syntax
  - ***.TRAN tincr1 tstop1***
  - ***.TRAN tincr1 tstop1 <sweep tincr2 tstop2 ..... ><START=val>***

SPICE - Components

Instance & Elements Name

C	Capacitor
D	Diode
E, F, G, H	Dependent Sources
I	Current
J	JFET or MESFET
K	Mutual Inductor
L	Inductor
M	MOSFET
Q	BJT
R	Resistor
O, T, U	Transmission Line
V	Voltage Source
X	Subcircuit Call

Scale Factor

M	1e-3
U	1e-6
N	1e-9
P	1e-12
F	1e-15
K	1e3
Meg	1e6
G	1e9
T	1e12
DB	20log10

SPICE - Components

- R, C, …

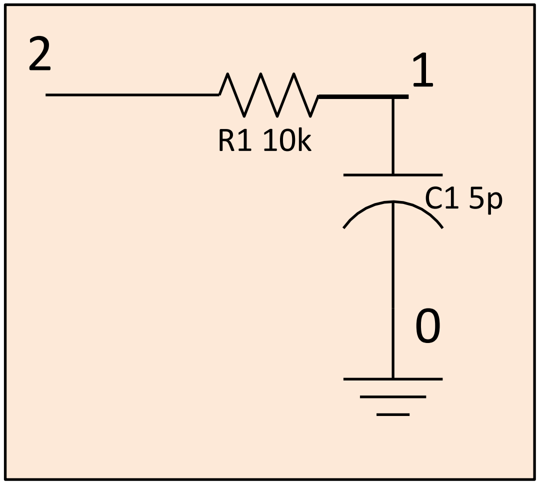
  Syntax :

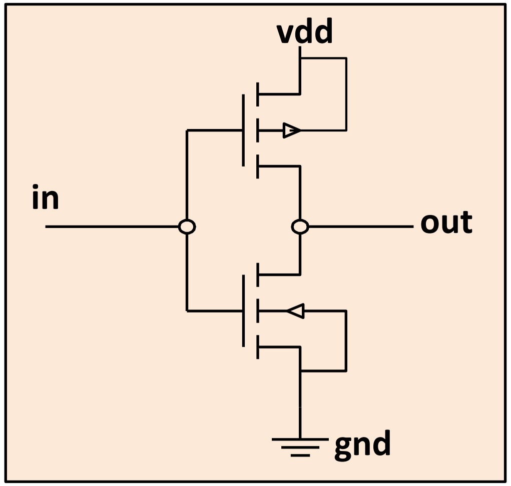
  Rxxx v+ v- scale

  Cxxx v+ v- scale

  e.g. C1 1 0 5p

  R1 2 1 10k





- Mxxx Drain Gate Source Body Model width length

  Mxxx d g s b modelname w=width l=length

  ex.

  M1 out in vdd vdd pch w=2.5u l=0.18u

  M2 out in gnd gnd nch w=2.5u l=0.18u

SPICE - Subcircuit

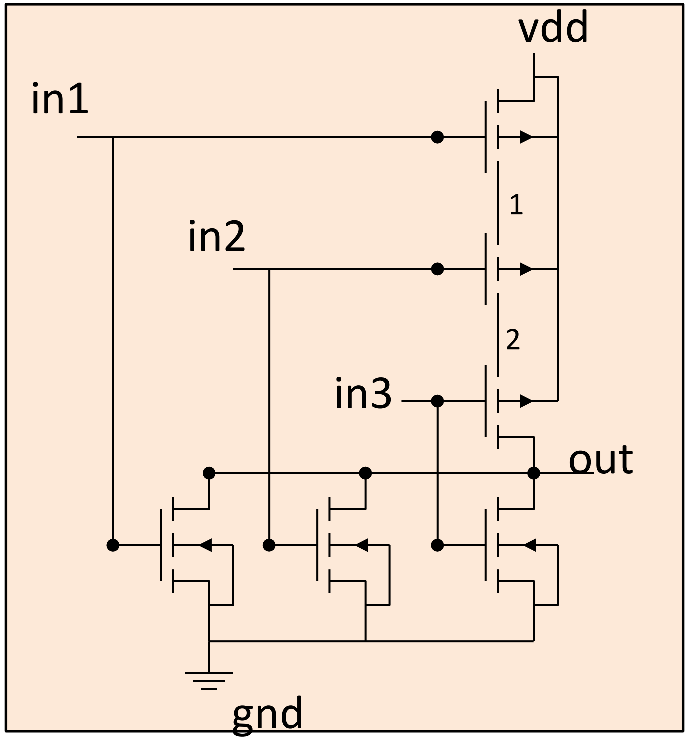
- .subckt subname n1<n2 n3 ……> <param=val>

  your subcircuit design

  .ends

  e.g.

```
 .subckt NOR3 in1 in2 in3 out
+ wp=0.18u lp=0.18u      wn=0.18u
ln=0.18u  mp1 1     in1 vdd vdd pch W=wp
L=lp
Mp2 2     in2 1       vdd pch W=wp L=lp
Mp3 out in3 2       vdd pch W=wp L=lp
Mn1 out in1 gnd gnd nch W=wn L=ln
Mn2 out in2 gnd gnd nch W=wn L=ln
Mn3 out in3 gnd gnd nch W=wn L=ln
.ends
```



- Call subcircuit

  Syntax: ***Xyyy n1 <n2 n3 ……> subname <param=val>***

SPICE - Independent Source Elements

Syntax

```
Vxxx   n+   n-   DC   AC= ac_mag, ac_phase
Iyyy   n+   n-   DC   AC= ac_mag, ac_phase
```

e.g.

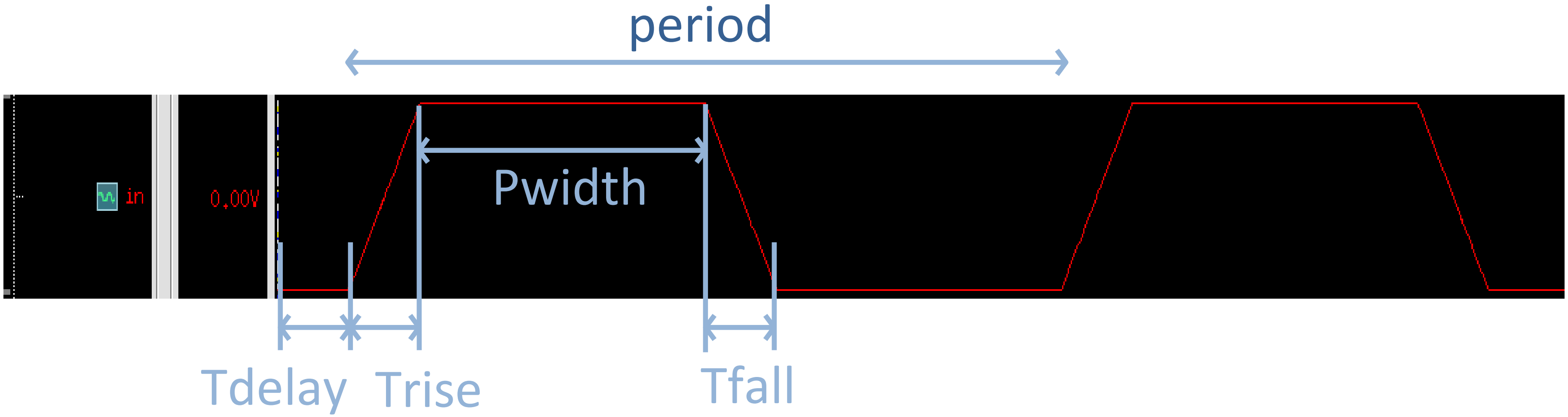
DC	*v1*	*1*	*0*	*DC=5v*
	v2	*2*	*0*	*5v*
	i3	*3*	*0*	*5mA*
AC	*v4*	*4*	*0*	*AC=10v, 90*
	v5	*5*	*0*	*AC=1v, 180*
MIX	*v6*	*6*	*0*	*5v AC=1v, 90*

SPICE - Transient Source

- PULSE

  Syntax: ***PULSE (V1 V2 <Tdelay Trise Tfall Pwidth Period>***

  e.g. Vin 1 0 PULSE (0v 1.8v 10ns 10ns 10ns 40ns 100ns)



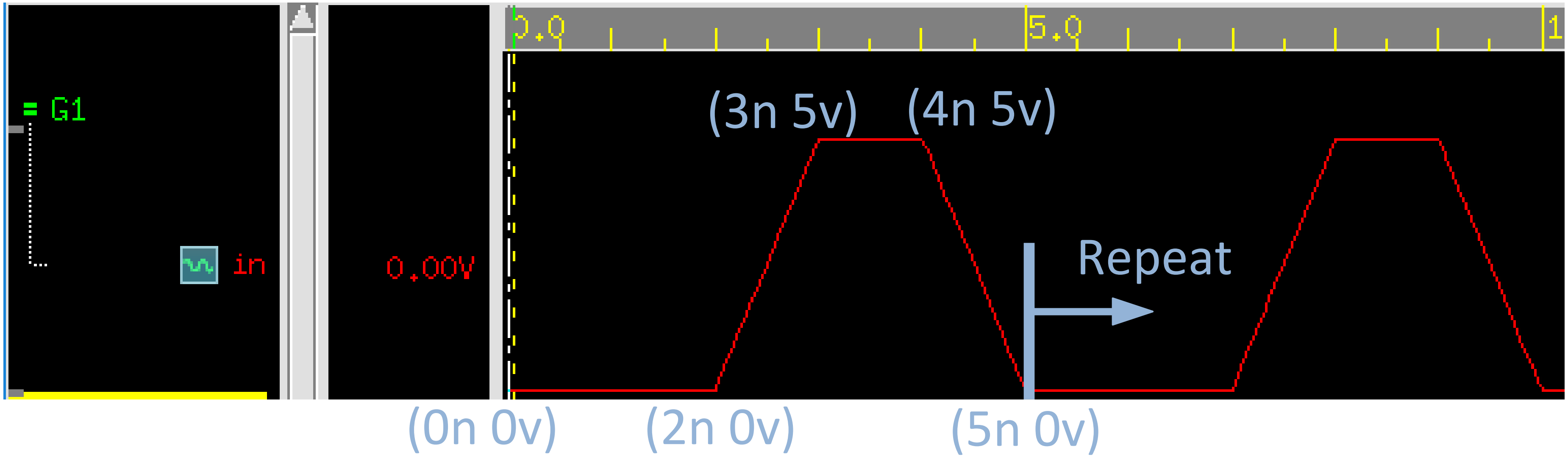
SPICE - Transient Source

- PWL

  Syntax: ***PWL (<t1 v1 t2 v2 ..> <R> <Tdelay>)***

  - *R = repeat_from_what_time
  - *TD = time_delay_before_PWL_start

  e.g. Vin 1 0 PWL (0n 0v, 2n 0v, 3n 5v, 4n 5v, 5n 0v,R 0)

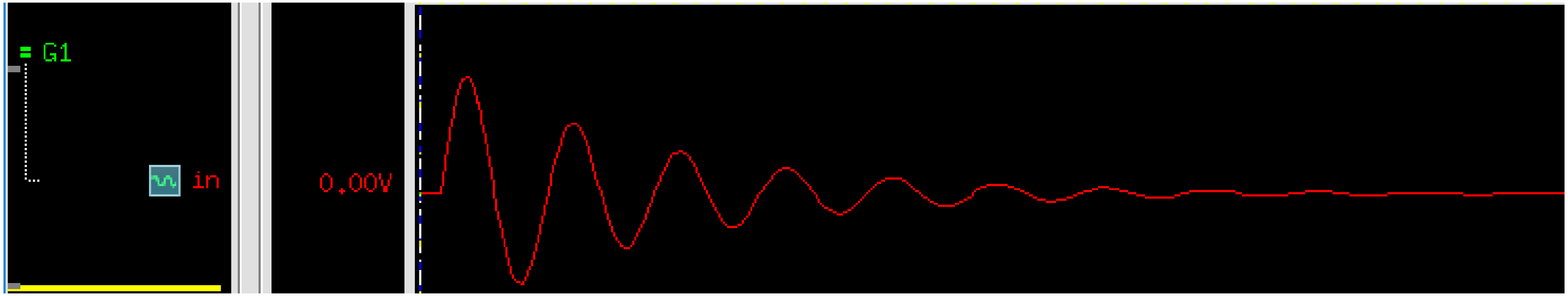


SPICE - Transient Source

- SIN

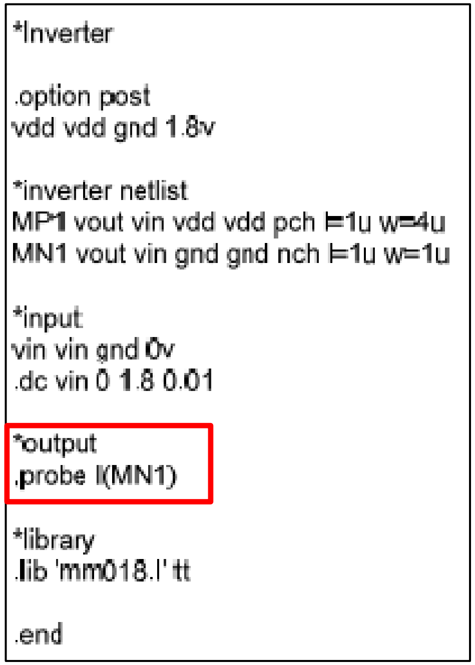
Syntax: ***SIN (Voffset Vacmag <Freq Tdelay Dfactor>)***

e.g. Vin 1 0 SIN (0 1 100Meg 2ns 5e7)



SPICE - Syntax

- OUTPUT
  - .MEASURE
    - Prints numeric results of measured specifications.
  - .PROBE
    - Saves output variables to interface and graph data files
    - Syntax: ***.PROBE antype ov1 <ov2 ...>***
  - .PRINT
    - Prints the values of specified output variables.
    - Syntax: ***.PRINT antype ov1 <ov2 ... ov32>***



```
*Inverter

.option post
vdd vdd gnd 1.8v

*inverter netlist
MP1 vout vin vdd vdd pch l=1u w=4u
MN1 vout vin gnd gnd nch l=1u w=1u

*input
vin vin gnd 0v
.dc vin 0 1.8 0.01

*output
.probe I(MN1)

*library
.lib 'mm018.l' tt

.end
```

- PLOT
  - Generates low-resolution (ASCII) plots in the output listing file
  - Syntax: ***.PLOT antype ov1 <(plo1,phi1)> <ov2> <(plo2,phi2)> ...>***

SPICE - Syntax

- .MEASURE Statement
  - Can include
    - Propagation Delay, Rise time, Fall time
    - Average, RMS, Peak-to-peak voltage, Min. & Max. voltage over a specified period
    - Equation, Derivative, Integral evaluation
  - Fundamental measurement mode
    - Rise, Fall, and Delay (TRIG-TARG)
      - Syntax: ***.MEASURE <DC | AC | TRAN> result TRIG ... TARG ...***
        + <GOAL=val> <MINVAL=val> <WEIGHT=val>
    - AVG, RMS, MIN, MAX, and Peak-to-Peak (FROM-TO)
      - Syntax: ***.MEASURE <TRAN > result func FROM=start TO=end***
    - FIND-WHEN
      - Syntax: ***.meas <DC | AC | TRAN> result FIND ov1 WHEN ov2=val***

SPICE - Syntax

- .ALTER Statement :
  - Reruns an HSPICE simulation using different parameters and data.
  - Can’t include :
    - .PRINT, .PLOT, .GRAPH or any other I/O statements
  - Can be included in only one :
    - All analysis statements (.DC, .AC, .TRAN, .FOUR, .DISTO, .PZ, and so on)
  - Can include :
    - Element Statement (except source elements)
    - .DATA, .LIB, .INCLUDE, .MODEL Statements
    - .IC, .NODESET Statements
    - .OP, .PARAM, .TEMP, .TRAN, .DC, .AC Statements
  - Syntax: ***.ALTER <title_string>***

SPICE – output file of analysis

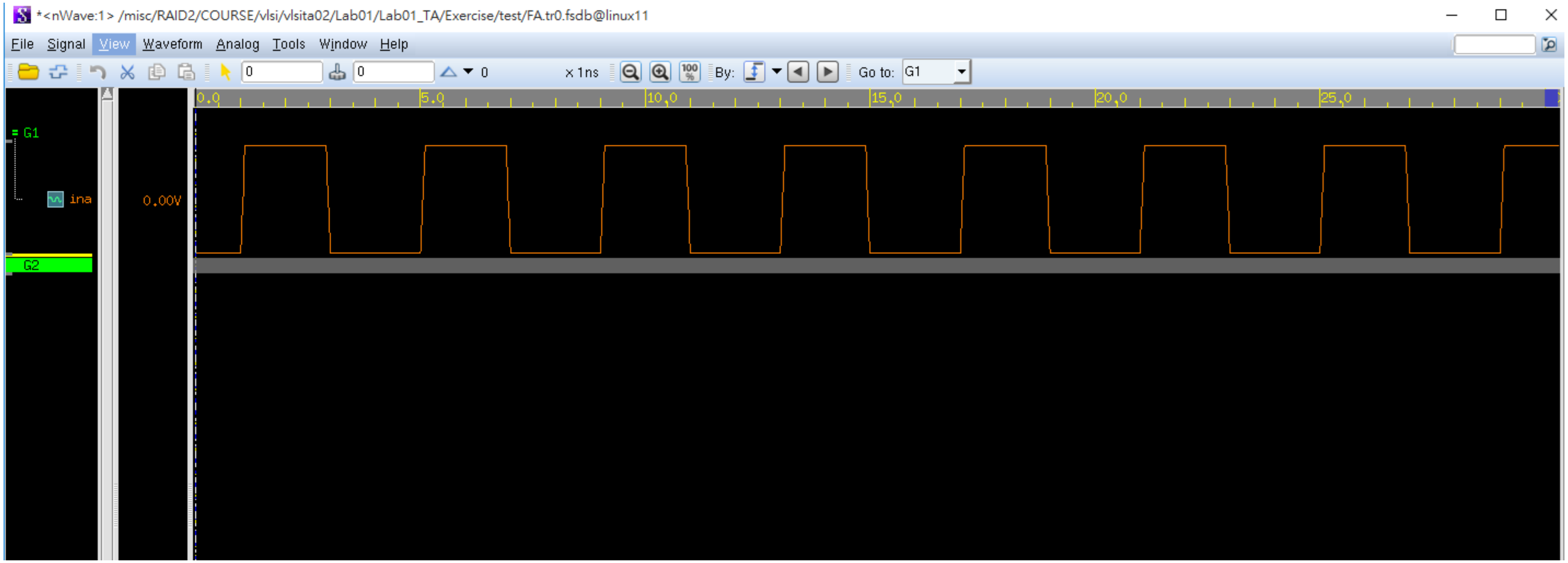
Output file type	extensi
Output list	.lis
DC analysis result	.sw#
DC analysis measurement result	.ms#
AC analysis result	.ac#
AC analysis measurement result	.ma#
TRAN analysis result	.tr#
TRAN analysis measurement result	.mt#
Subcircuit cross-listing	.pa#
Initial condition	.ic

SPICE - Graphic Tool

Window:

```
unix% hspice buffer.sp
unix% nWave &
```

buffer.tr0 =>buffer.tr0.fsdb => waveform
buffer.mt0 => measured result

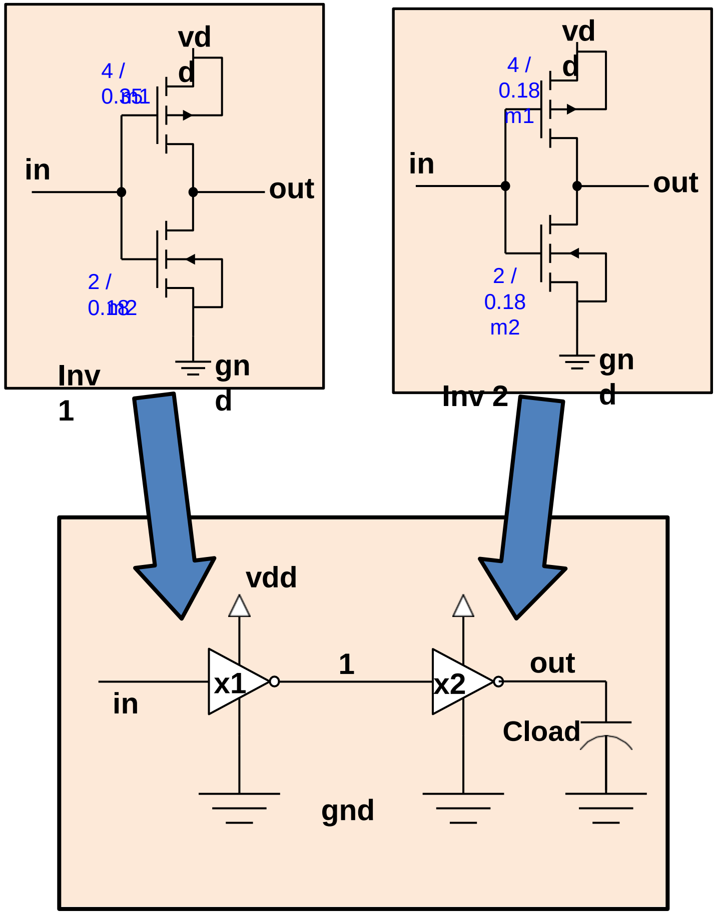


*<nWave:1> /misc/RAID2/COURSE/vlsi/vlsita02/Lab01/Lab01_TA/Exercise/test/FA.tr0.fsdb@linux11

SPICE - Example

- Example – 0.18μm Buffer

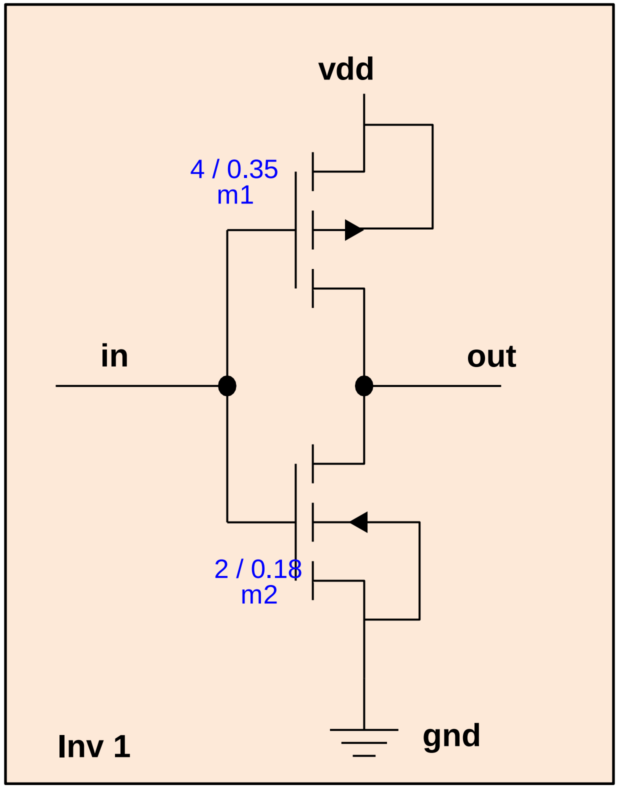
```
**** VLSI Lab01: HSPICE ****
**** example: buffer ****
**** Author: Xin-Ru Lee ****

.lib "mm018.l" TT
.TEMP 25
.global VDD GND
.param supply = 1.8v
.param load = 10f

.options brief post

.tran 0.01n 60n

.meas tran Imax max I(vd1) from=0.1ns to=60ns
.meas Pmax param='abs(Imax)*supply'
.meas tran tprop trig v(in) val='supply/2' rise=1
+targ v(out) val='supply/2' rise=1
.meas tran tr trig v(out) val='supply*0.1' rise=1
+targ v(out) val='supply*0.9' rise=1
.meas tran tf trig v(out) val='supply*0.9' fall=1
+targ v(out) val='supply*0.1' fall=1

Vd1 VDD GND supply
Vd in GND pulse(0 supply 1ns 0.1ns 0.1ns 1.9ns 4ns)

X1 in 1 inv
X2 1 out inv
Cload out GND load
```



SPICE - Example

- Example – 0.18µm Buffer

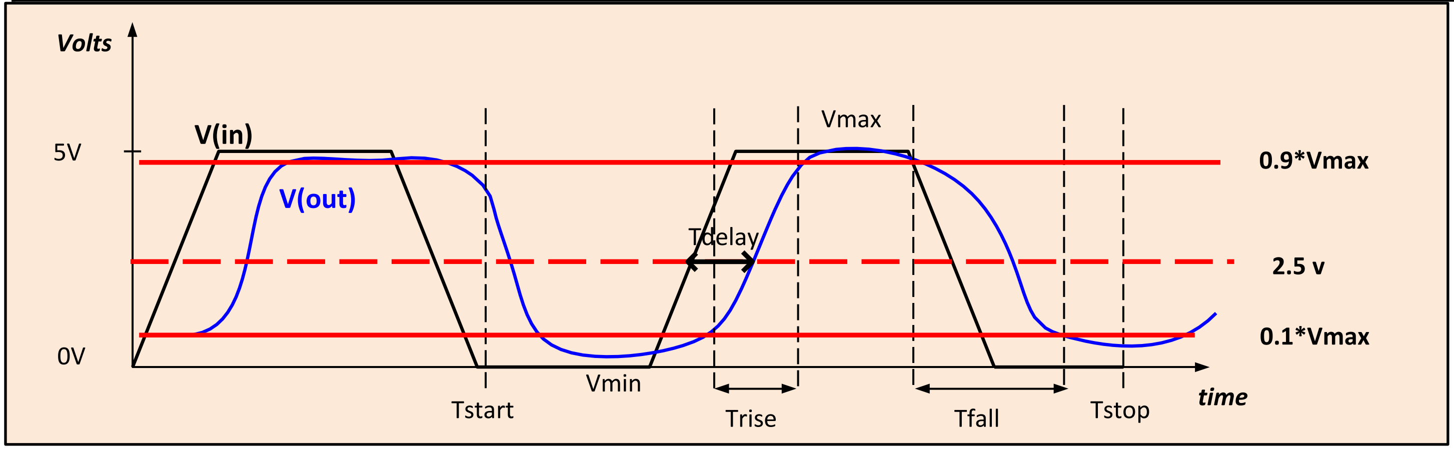
```
.subckt inv in out

*vdd vdd 0 1.8v

mp out in VDD VDD pch l=0.18u w=wx
mn out in GND GND nch l=0.18u w=wx

.ends inv

.param wx=2.5u

.alter
.param wx=1.25u

.alter
.param wx=0.625u


.end
```



SPICE - Example

- Example of MEASURE Statement:

```
.MEAS   TRAN    Vmax            MAX v(out) FROM=Tstart  TO=Tstop
.MEAS   TRAN    Vmin            MIN v(out) FROM=Tstart TO=Tstop
.MEAS   Power   param='I*V'
.MEAS   TRAN    Trise           TRIG     v(out)     VAL='0.1*Vmax'     RISE=2
+                               TARG     v(out)     VAL ='0.9*Vmax'    RISE=2
.MEAS   TRAN    Tfall           TRIG     v(out)     VAL='0.9*Vmax'     FALL=2
+                               TARG     v(out)     VAL ='0.1*Vmax'    FALL=2
.MEAS   TRAN    Tdelay          TRIG     v(in)      VAL=0.5            RISE=2
+                               TARG     v(out)     VAL=0.5            RISE=2
```



SPICE - Example

- Example of ALTER contains PARAM:

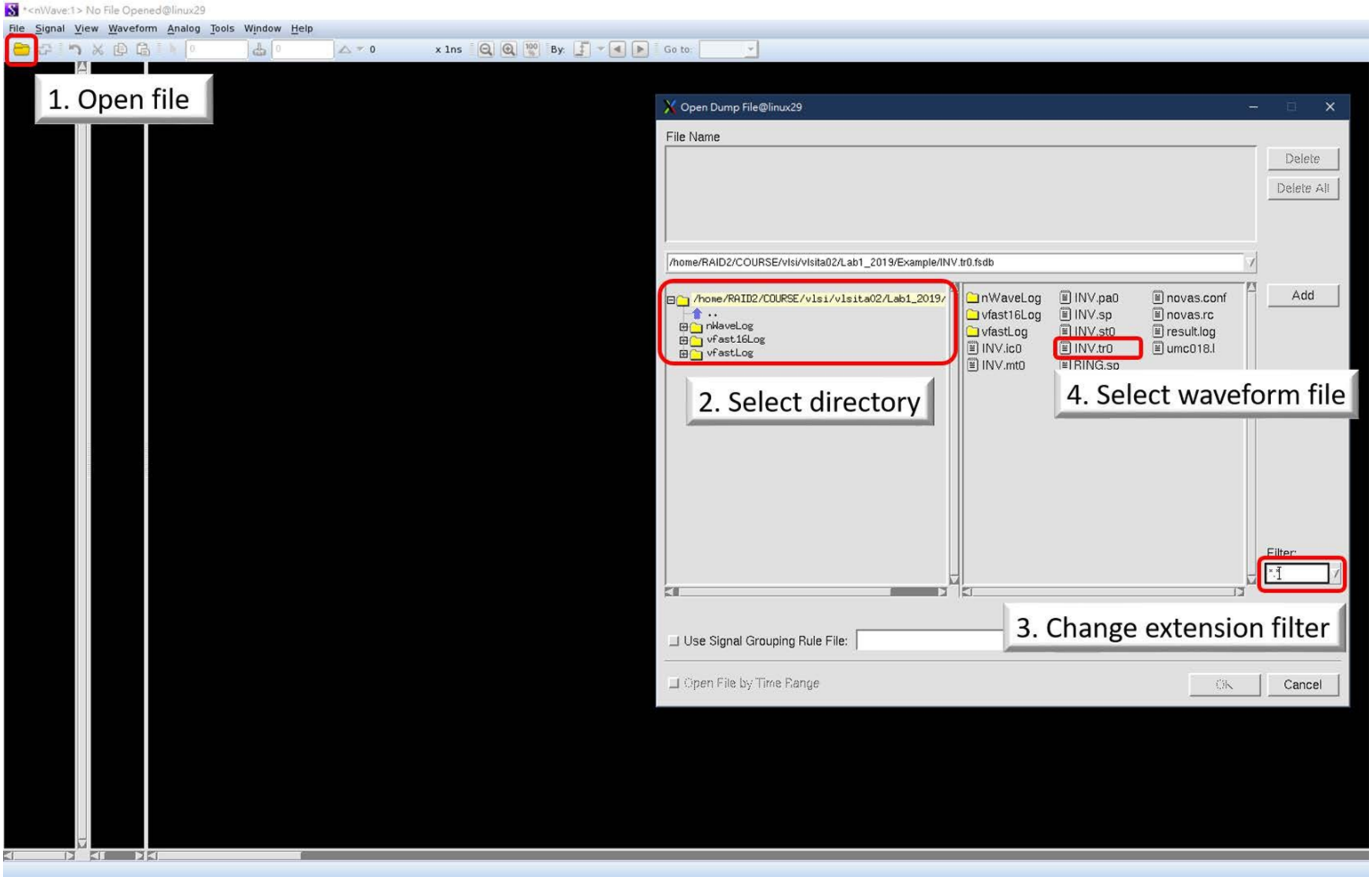
```
Example of ALTER contains PARAM
.OPTION LIST NODE POST
.TRAN 200P 20N
.PRINT TRAN V(IN) V(OUT)
M1 OUT IN VCC VCC PCH L=1U W=Wx
M2 OUT IN 0 0 NCH L=1U W=Wx
VCC VCC 0 5
VIN IN 0 0 PULSE .2 4.8 2N 1N 1N  5N 20N
CLOAD OUT 0 Cx
.MODEL PCH PMOS LEVEL=1
.MODEL NCH NMOS LEVEL=1
.PARAM Wx=20U Cx=.75p
```

```
.ALTER
.PARAM Wx=20U Cx=.50p
.ALTER
.PARAM Wx=20U Cx=.25p
.ALTER
.PARAM Wx=20U Cx=.10p
.ALTER
.PARAM Wx=10U Cx=.10p
.ALTER
.PARAM Wx=5U Cx=.10p

.END
```

Instruction (workstation)

- Compile spice file
  - First link to workstation (ex : mobaXterm, putty)
  - Move to the corresponding directory
  - Type “***hspice filename.sp***”
  - If you want to see the log file after compiling hspice file,
    Type “***hspice filename.sp >! file.txt*** ”
- Show the waveform
  - Type “***nWave &***”
  - Type “***wv &***”

Waveform (nWave)



1. Open file

2. Select directory

3. Change extension filter

4. Select waveform file

/home/RAID2/COURSE/vlsi/vlsita02/Lab1_2019/Example/INV.tr0.fsdb

/home/RAID2/COURSE/vlsi/vlsita02/Lab1_2019/
- ..
- nWaveLog
- vfast16Log
- vfastLog

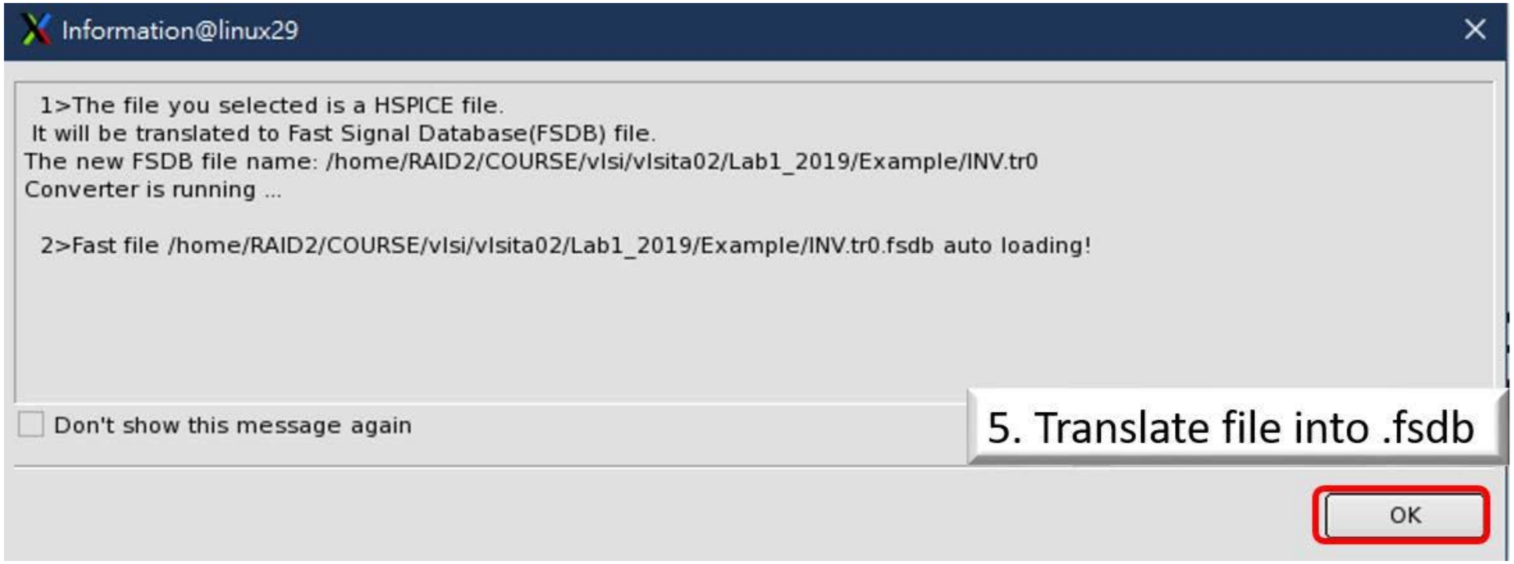
nWaveLog	INV.pa0	novas.conf
vfast16Log	INV.sp	novas.rc
vfastLog	INV.st0	result.log
INV.ic0	INV.tr0	umc018.l
INV.mt0	RING.sp	

Filter: *.I

□ Use Signal Grouping Rule File:

□ Open File by Time Range

Waveform (nWave)

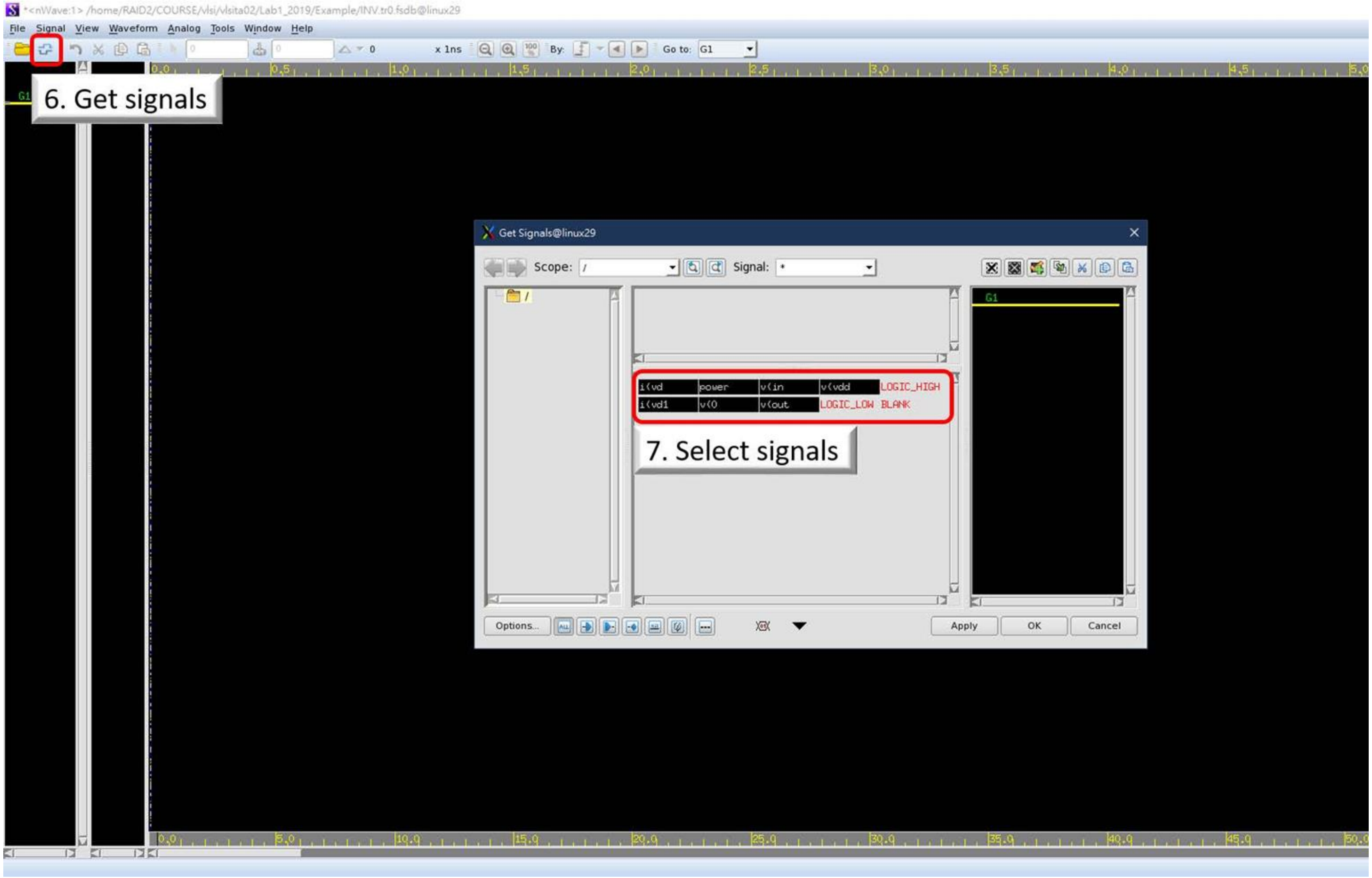


```
 1>The file you selected is a HSPICE file.
 It will be translated to Fast Signal Database(FSDB) file.
The new FSDB file name: /home/RAID2/COURSE/vlsi/vlsita02/Lab1_2019/Example/INV.tr0
Converter is running ...

 2>Fast file /home/RAID2/COURSE/vlsi/vlsita02/Lab1_2019/Example/INV.tr0.fsdb auto loading!
```

□ Don't show this message again

5. Translate file into .fsdb

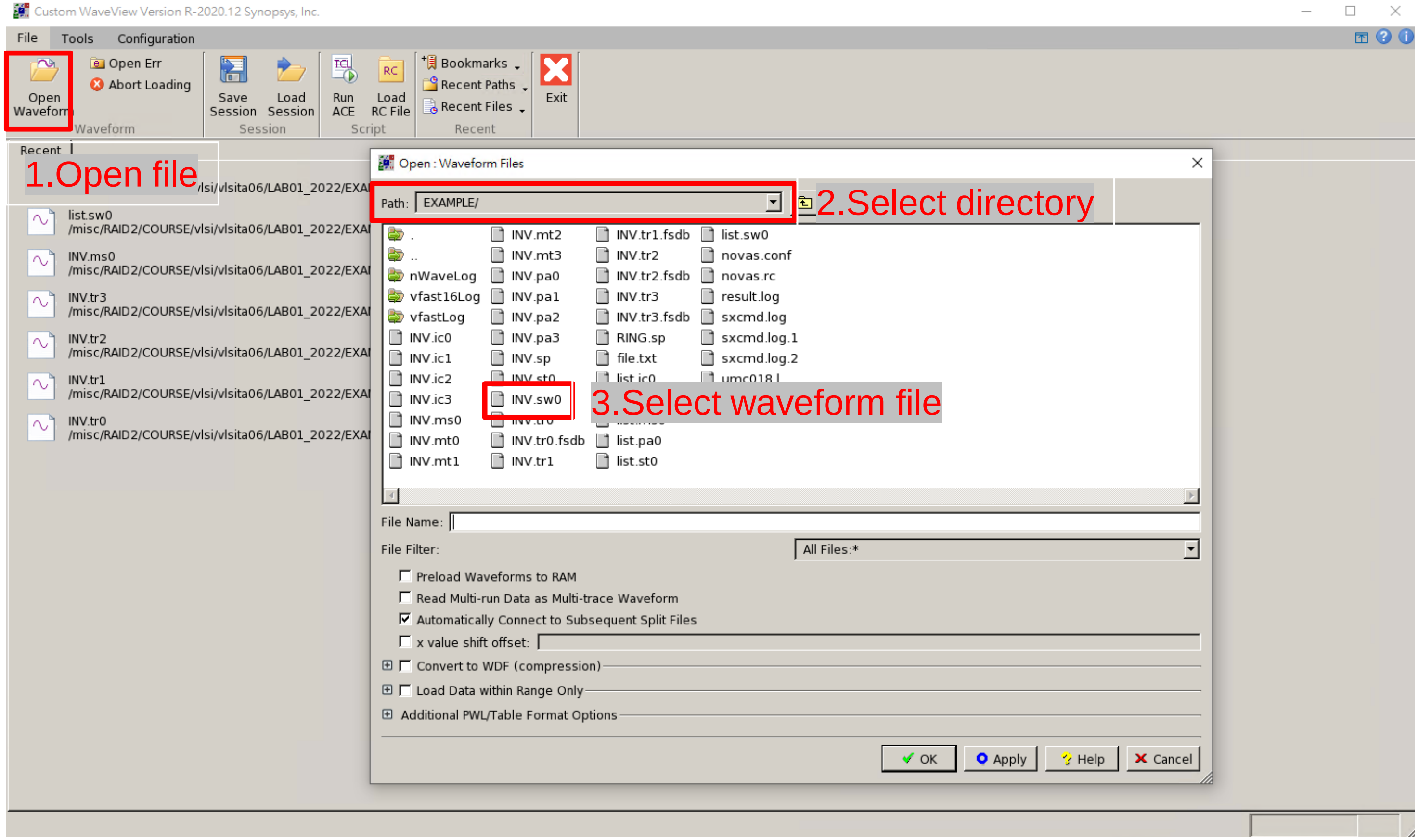
Waveform (nWave)



6. Get signals

7. Select signals

Waveform (waveview)



1.Open file

2.Select directory

3.Select waveform file

```
.../vlsi/vlsita06/LAB01_2022/EXA
list.sw0
/misc/RAID2/COURSE/vlsi/vlsita06/LAB01_2022/EXA
INV.ms0
/misc/RAID2/COURSE/vlsi/vlsita06/LAB01_2022/EXA
INV.tr3
/misc/RAID2/COURSE/vlsi/vlsita06/LAB01_2022/EXA
INV.tr2
/misc/RAID2/COURSE/vlsi/vlsita06/LAB01_2022/EXA
INV.tr1
/misc/RAID2/COURSE/vlsi/vlsita06/LAB01_2022/EXA
INV.tr0
/misc/RAID2/COURSE/vlsi/vlsita06/LAB01_2022/EXA
```

Path: EXAMPLE/

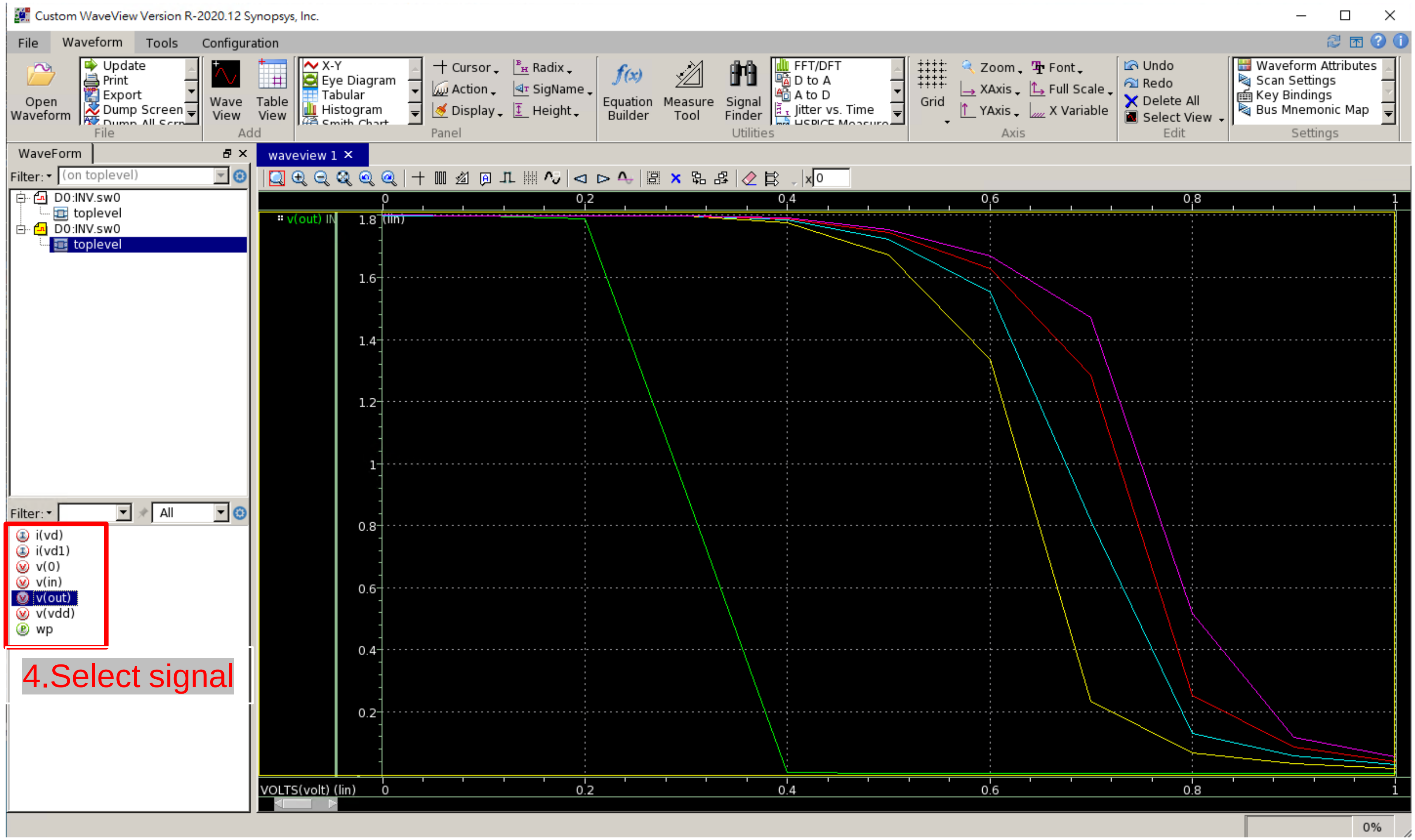
```
.             INV.mt2       INV.tr1.fsdb   list.sw0
..            INV.mt3       INV.tr2        novas.conf
nWaveLog      INV.pa0       INV.tr2.fsdb   novas.rc
vfast16Log    INV.pa1       INV.tr3        result.log
vfastLog      INV.pa2       INV.tr3.fsdb   sxcmd.log
INV.ic0       INV.pa3       RING.sp        sxcmd.log.1
INV.ic1       INV.sp        file.txt       sxcmd.log.2
INV.ic2       INV.st0       list.ic0       umc018.l
INV.ic3       INV.sw0       list.ms0
INV.ms0       INV.tr0       list.mt0
INV.mt0       INV.tr0.fsdb  list.pa0
INV.mt1       INV.tr1       list.st0
```

File Name:

File Filter: All Files:*

- ☐ Preload Waveforms to RAM
- ☐ Read Multi-run Data as Multi-trace Waveform
- ☑ Automatically Connect to Subsequent Split Files
- ☐ x value shift offset:
- ⊞ ☐ Convert to WDF (compression)
- ⊞ ☐ Load Data within Range Only
- ⊞ Additional PWL/Table Format Options

Waveform (waveview)



4.Select signal