Digital Integrated Circuits

#Home Work 6 2024.05.12 (Due:05.22 13:20)

Reference to the class note: B5-*Array and Recoded Multiplier*

Design a 14-bit unsigned multiplier P=X×Y by using modified Radix-4 Booth multipliers. **The goal is to have minimum critical path delay time with the least gate count.**

(1) Show your block diagram as shown in Fig.1 below (example for the case of 8-bit; Booth decoder and Multiplicand scale corresponding to Booth Encoder and Booth selector of Fig.10.80). For each block, you shall show its logic design diagram. Indicate the critical path. Explain your design concepts (30).

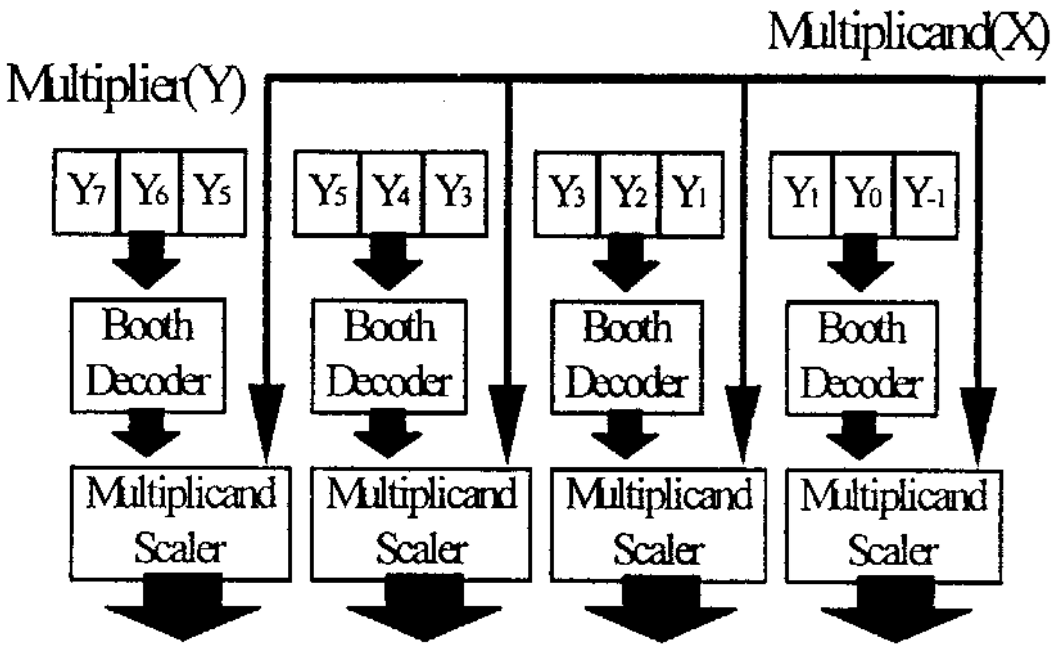

Fig.1

(2) Shown the Radix Booth-4 encoded partial products with simplified sign extension like that shown in Fig.10.82 of B5_Array and Recoded Multuplier. Draw another diagram with the dots or S that replace p_{ij} where i is the ith row and j is the bit location . (20)

(3) Design the partial products with array multiplier as that shown in Fig.5.2. Draw the block diagram in terms of FA and HA and p_{ij} as inputs. Show the critical path and indicate the delay time in terms of number of HA and FA. For area, show the number of FA and HA used. Explain your design concepts. (25)

(4) Design the partial products with Dadda method shown in Fig.5.19. To fairly compare with array multiplier, Carry-ripple adder is used in the last stage of CPA. Show the critical path and indicate the delay time in terms of number of HA and FA. For area, show the number of FA and HA used. Explain your design concepts (25)