Digital Integrated Circuits

#Homework 3
04.10 (Due: 04.17, 15:30)

/* Using 7 nm CMOS FiFFT devices with VDD= 0.8 V, FF process corner and medium Vt CMOS process*/
/*Rise time and fall time of input signals and clock are 0.02ns (0V-0.8V)*/

1. MOS and Inverter (30%)
   a) Run SPICE to draw the I-V DC curves (like the one in **Fig.2.7 of page A2-2 with Vgs of 0.8, 0.6, 0.35)** for PMOS and NMOS with Fin n=1. **In table form**, mark Ids_max (Vgs=Vds= Vdd). Discuss the results.
   b) Keep a unit size inverter with NMOS n=1and choose the n of PMOS for n=1 and 2 to show the logic threshold voltage. Run SPICE to verify your results by showing simulated waveforms.
2. Ring oscillator (20%)
   According to the results of 1(b), design a 3-stage inverter-based ring oscillator with unit size inverter with berter logic threshold voltage. Set the initial voltage of each node so that it can oscillate. Show **in table form**, the SPICE simulation results of oscillation frequency and power consumption.
3. (50%) Design a static D register as shown in Fig.1 with propose size of NMOS and PMOS to have better tsetup, tpcq, tpdq and thold time. The loading of Q and Q-have 4 unit size inverters as loading. Both D and CLK has rise time and fall time of 0.1ns (0V-0.8V).
   a) Explain your sizing principle of each MOS to have least tsetup, tpcq, tpdq and thold time for register 1 and 0. (explain that by changing which transistors would affect each timing respectively)
   b) Run SPICE to verify your results and list the results (size of each transistor and four kinds of timing) in table form for part (a).

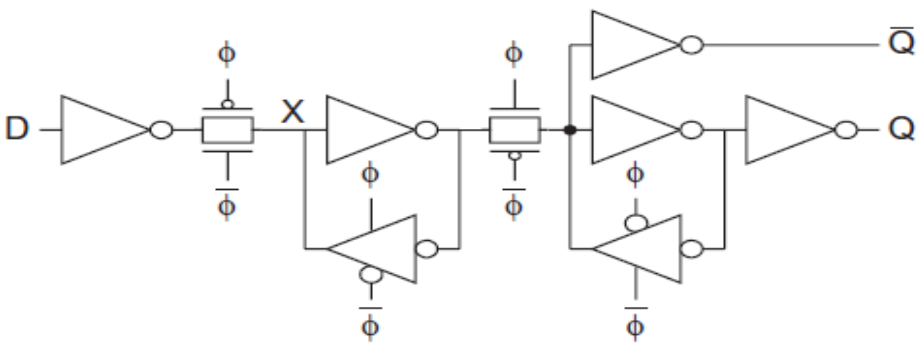

Fig.1