Digital Integrated Circuits

#Home work 1 2024.03.06 (Due:03.13 15:30; in the class)

/* Using 32 nm CMOS devices with VDD= 0.9 V, Wmin=64 nm, Lmin=32nm with resolution of 1nm; there are three kinds of Vt: High Vt, medium Vt and low Vt CMOS*/

(1) MOS and Inverter with medium threshold voltages (30%)

a) Run SPICE to draw the I-V DC curves for PMOS and NMOS with minimum feature size.

b) Keep L equal Lmim, design the W of each transitor (**in table form**) using medium Vt such that the logic threshold of inverter is at 0.5 VDD. Discuss your design procedures and the way you choose your MOS dimensions.

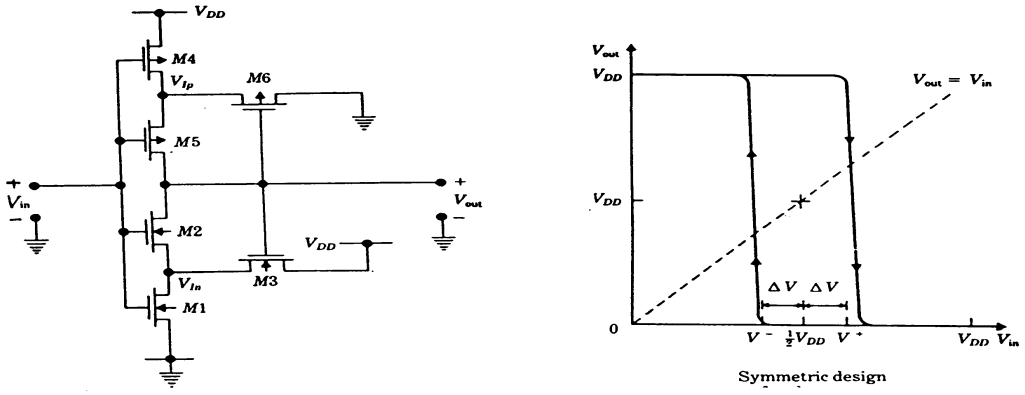
c) Run SPICE to verify your results

(2) Design a CMOS schmitt trigger shown at Fig.1 (b) such that V^+ = 0.54-0.57 V and V^- = 0.36~0.33 V with CT=VDD(70%)

a) Discuss the difference between Fig.1 (a) and (b). Give the W/L of each device (**in table form**) of Fig.1 (b) with CT= VDD and discuss your design procedures to determine the size of each transistor using medium Vt. (30%)

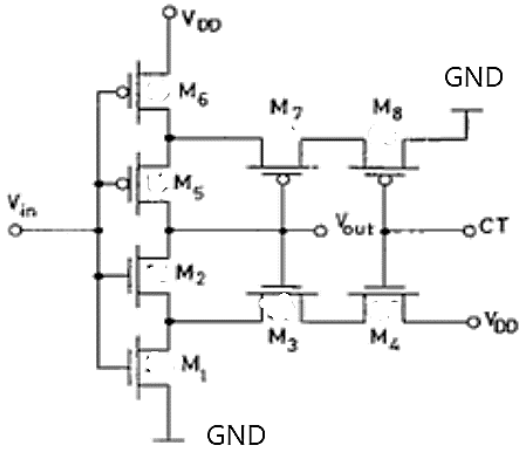
b) Run SPICE to verify your results. Your report must have the figures of VTC and Isc vs Vin (20%)

c) CT is changed to 0.8 VDD and use the same size in a). Repeat b) to have figures to indicate the new V^- and V^+(20%)



Circuit diagram Symmetric design

(a)



(b) Schmitt trigger with controllable hysteresis

Fig.1 Schmitt Trigger circuit