Digital Integrated Circuits

#Home work 4 2024.04.26(Due: 05.03, 13:20)

/* Using 7 nm CMOS FiFFT devices with VDD= 0.8 V, FF process corner and medium Vt CMOS process*/ /*Rise time and fall time of input signals and clock are 0.02ns (0V-0.8V)*/

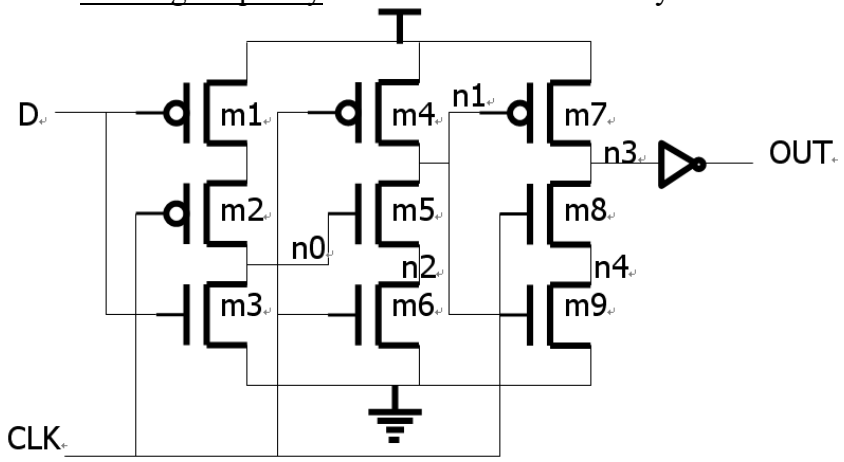
1. A 4-bit ripple adder as ahown at Fig.1 is designed with Fully Complementary Static Logic Gate for FA. Input signals are A[3:0], B[3:0] and Cin which are provided by a unit size inverter. Outputs are Sum[3:0] with loading of 5 unit size inverters connected in parallelism (FO5). You shall provide SPICE simulation results of timing and power waveforms.

(1) Try your best to design the fastest adder. First, show your block diagrams in terms of the 1-bit Full-Adder(FA). Second, show the circuit schematic of each block. Use logic effort concepts (you do not have to write down the procedure) to design transistor widths. **Describe your design concept.** (40%)

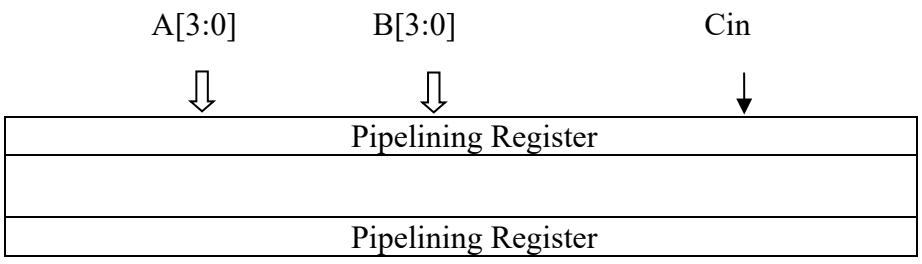
(2) Based on the design of (1), run SPICE to find the the propagation delay time (with pattern from 000011110 to 000011111 (A[3:0]@B[3:0]@Cin). Determine the maximum propagation of a clock with the delay time estimated by SPICE. (20%)

(3) Run SPICE to get the average, peak and leakage power dissipation and energy/bit, respectively of this adder with loading (FO4) when working at the maximum working frequency. (20%)

(4) Add one pipelining stage using the designed D register into the 4-bit ripple adder as shown at Fig.1(b). Run SPICE to find the the propagation delay time (with pattern from 000011110 to 000011111 (A[3:0]@B[3:0]@Cin) between pipelining stages to determine the maximum working frequency of the clock with the delay time estimated by SPICE. (20%)



(a)



(b)

Fig.1 (a) TSPC register (b) pipeline design of 4 bit adder.

(When running SPICE simulation in (3), use the follwing input patterns)

Average and peak power	Leakage power
A[3:0] is from 0000 to 1111	A[3:0] is 0000
B[3:0] is from 1111 to 0000	B[3:0] is 1111
Cin is 0/1 by turns	Cin is 0

/*You should provide the SPICE input description, timing and power waveforms*/