Digital Integrated Circuits

#Home Work 7 2024.05.29 (Due:2023.06.05, 15:30)

Consider the circuit in Fig.7. Modules A and B have a delay of 19 ns and 30.5 ns at 0.9V (Vdd) with switching of 20 pF and 30 pF respectively. All the buses in Fig.7 are 16 bits. One register has a 0.5 ns clock-to-Q delay and switches 0.05 pF. The clock rate of Fig.7 is thus 1/(50 ns) and the power dissipation is P0. The power dissipation can be estimated by $P= C \bullet Vdd^2 \bullet F$ and the delay with respect to Vdd can be approximated by k/(Vdd-Vt) with Vt equals 0.3 V. k is a constant and is different for A and B. You can use the information of delay time, Vdd and Vt to calculate k.

(a) Adding a pipeline register between A and B allows for reduction of the supply voltage (A and B can use different Vdd) while maintaining throughput with power dissipation of P1. Show the block diagram. Explain the operation and calculate the power reduction ratio, P1/P0 (30%)

(b) Assume that a 2-to-1 multiplexer has a delay of 0.4 ns at 0.9 V and switches 0.05 pF. Try parallel version with two copies (using two A and B modules) while maintaining date rate (P2). Show the block diagram, explain the operation and calculate power reduction ratio, P2/P0. (30%)

(c) Try to combine (a) and (b) to design a parallel-pipeline version while maintaining data rate (p3). Show the block diagram, explain the operation and calculate power reduction ratio, P3/P0 (40%)

Fig.7