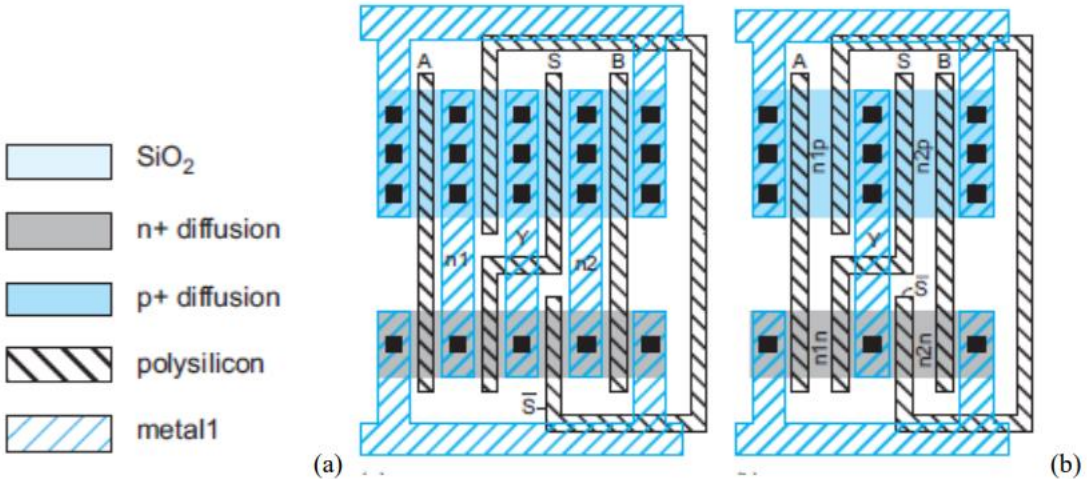
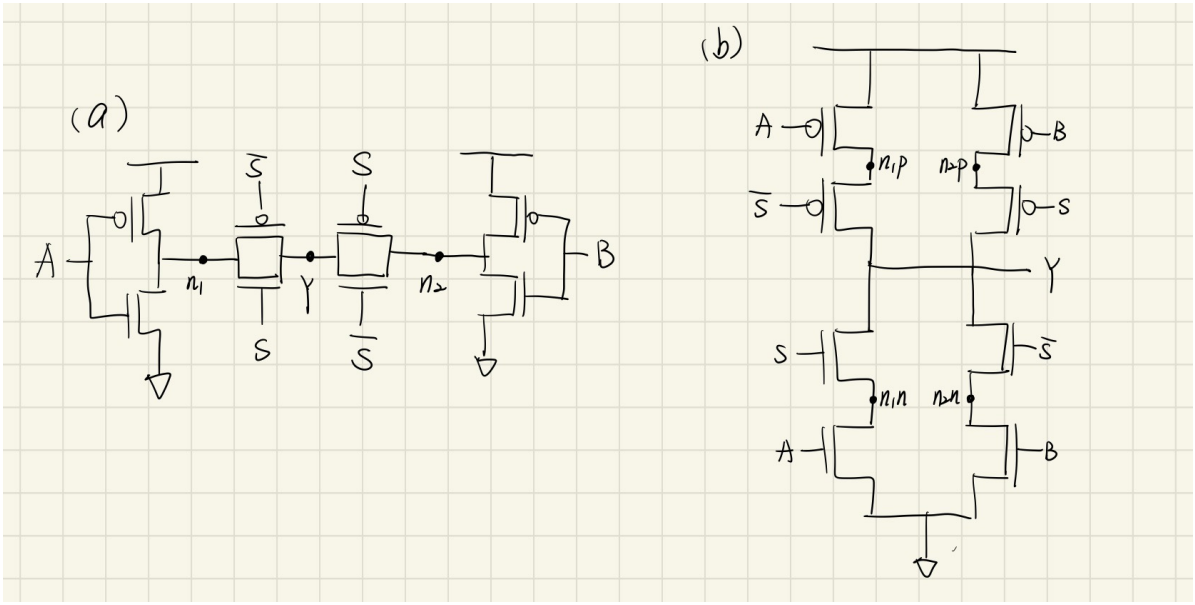
DIC HW2 0811562 何祁恩

1. (40%)

a) (20%) Draw the circuit schmetic of the attached layout (a) and (b). The signal name of each node shall be marked at the schematic. Explain which circuit has higher speed.

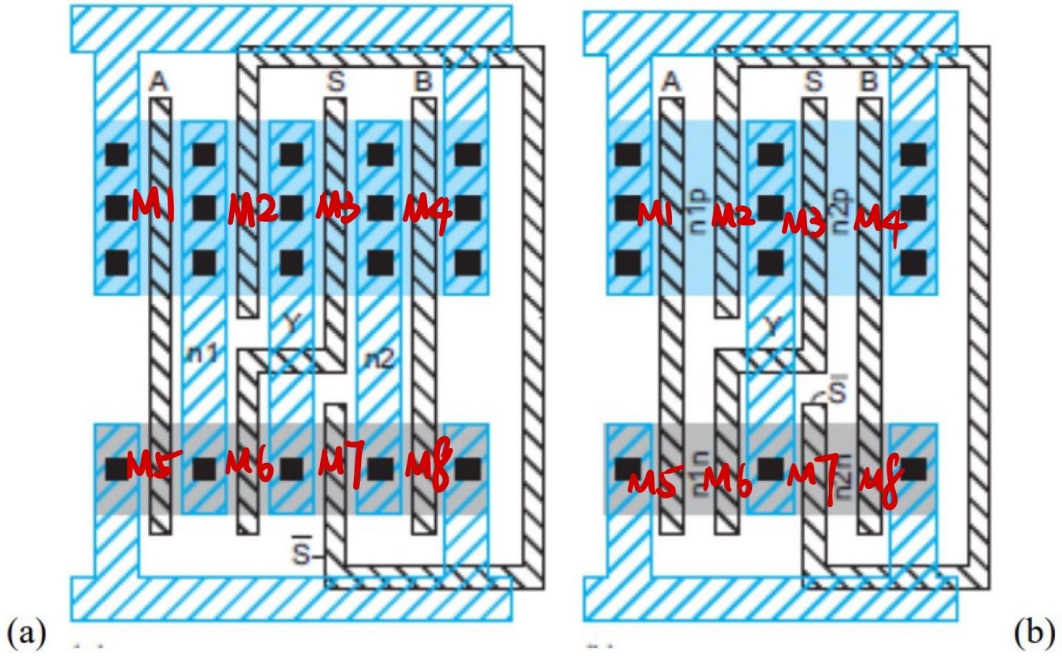




兩個 layout 的差別在於，(a)的部分將(b)可以成對出現的開關 TXG 電路拉出來放在一起。為了要分析這兩個電路誰比較快，我們可以很快地使用等效電阻的方式來快速得到答案。假設 PMOS 及 NMOS 的的等效電阻為 R。我們可以很快地得知(a)電路的 pull up/down 電阻為 $(R \| R)+R=\frac{3}{2}R$ ，而右邊的(b)電路的 pull up/down 電阻為 $R+R=2R$ ，因此可以推測左邊的(a)電路較為快速。

b) (10%) Indicate the W/L ratio (X.Y) and AD/AS (in terms of λ) of each transistor.

為了識別每顆 MOS，因此先幫每個 MOS 進行編號，再來進行分析:



1. 計算W_p, W_n

$$\text{已知/假設:}\begin{cases} Metal\_Diffusion\_Contact = 1\lambda \\ W_{Contact} = 2\lambda \\ Spacing_{Contact2Contact} = 3\lambda \\ Spacing_{Contact2Poly} = 2\lambda \\ Spacing_{Poly2Poly} = 3\lambda \end{cases}$$

$$W_p = 2\cdot Metal\_Diffusion\_Contact + 3\cdot W_{Contact} + 2\cdot Spacing_{Contact2Contact} = 14\lambda$$
$$W_n = 2\cdot Metal\_Diffusion\_Contact + W_{Contact} = 4\lambda$$
$$\Rightarrow \begin{cases} W_p = 14\lambda \\ W_n = 4\lambda \end{cases}$$

2. 計算 Source drain 長度

主要分成兩種 case 來做計算，是在 layout 邊緣的 source/drain 或者是在中間的。

$$\begin{cases} L_{edge} = 2\cdot Metal\_Diffusion\_Contact + W_{Contact} + Spacing_{Contact2Poly} = 5\lambda \\ L_{internal} = 2\cdot Spacing_{Contact2Poly} + W_{Contact} = 6\lambda \end{cases}$$

此外。針對(b)layout 中串聯部分因為沒有打 Contact，因此:

$$L_{Serial} = Spacing_{Poly2Poly} = 3\lambda$$

3.

Layout (a) W/L ratio

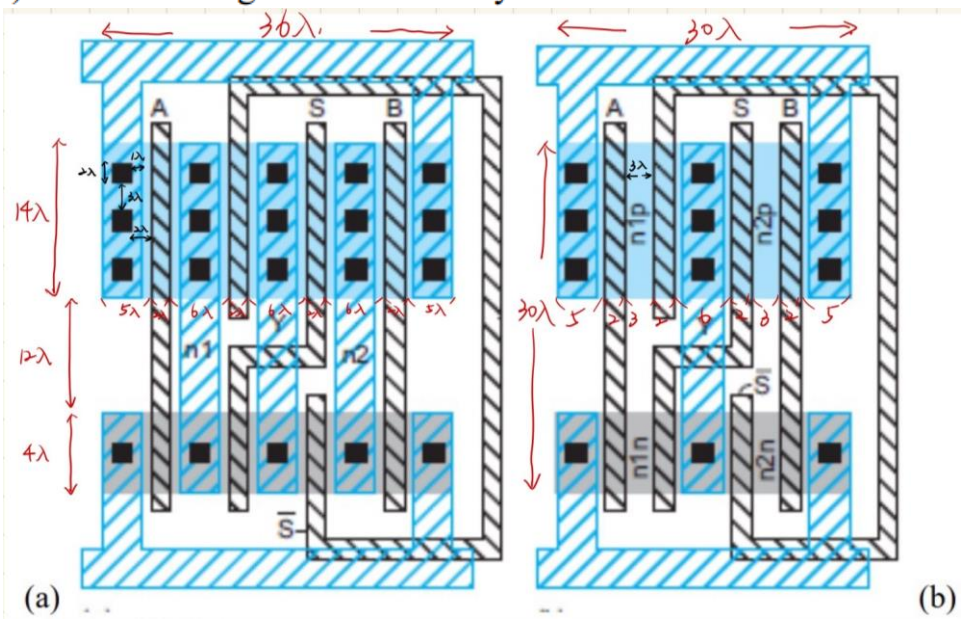
Note: for TXG [left diffusion/right diffusion: Drain/Source]

MOSFET	W/L	AD	AS
M1	$14\lambda / 2\lambda$	$14\lambda \cdot 6\lambda = 84\lambda^2$	$14\lambda \cdot 5\lambda = 70\lambda^2$
M2	$14\lambda / 2\lambda$	$14\lambda \cdot 6\lambda = 84\lambda^2$	$14\lambda \cdot 6\lambda = 84\lambda^2$
M3	$14\lambda / 2\lambda$	$14\lambda \cdot 6\lambda = 84\lambda^2$	$14\lambda \cdot 6\lambda = 84\lambda^2$
M4	$14\lambda / 2\lambda$	$14\lambda \cdot 6\lambda = 84\lambda^2$	$14\lambda \cdot 5\lambda = 70\lambda^2$
M5	$4\lambda / 2\lambda$	$4\lambda \cdot 6\lambda = 24\lambda^2$	$4\lambda \cdot 5\lambda = 20\lambda^2$
M6	$4\lambda / 2\lambda$	$4\lambda \cdot 6\lambda = 24\lambda^2$	$4\lambda \cdot 6\lambda = 24\lambda^2$
M7	$4\lambda / 2\lambda$	$4\lambda \cdot 6\lambda = 24\lambda^2$	$4\lambda \cdot 6\lambda = 24\lambda^2$
M8	$4\lambda / 2\lambda$	$4\lambda \cdot 6\lambda = 24\lambda^2$	$4\lambda \cdot 5\lambda = 20\lambda^2$

Layout (b) W/L ratio

MOSFET	W/L	AD	AS
M1	$14\lambda / 2\lambda$	$14\lambda \cdot 3\lambda = 42\lambda^2$	$14\lambda \cdot 5\lambda = 70\lambda^2$
M2	$14\lambda / 2\lambda$	$14\lambda \cdot 3\lambda = 42\lambda^2$	$14\lambda \cdot 6\lambda = 84\lambda^2$
M3	$14\lambda / 2\lambda$	$14\lambda \cdot 6\lambda = 84\lambda^2$	$14\lambda \cdot 3\lambda = 42\lambda^2$
M4	$14\lambda / 2\lambda$	$14\lambda \cdot 3\lambda = 42\lambda^2$	$14\lambda \cdot 5\lambda = 70\lambda^2$
M5	$4\lambda / 2\lambda$	$4\lambda \cdot 3\lambda = 12\lambda^2$	$4\lambda \cdot 5\lambda = 20\lambda^2$
M6	$4\lambda / 2\lambda$	$4\lambda \cdot 3\lambda = 12\lambda^2$	$4\lambda \cdot 6\lambda = 24\lambda^2$
M7	$4\lambda / 2\lambda$	$4\lambda \cdot 6\lambda = 24\lambda^2$	$4\lambda \cdot 3\lambda = 12\lambda^2$
M8	$4\lambda / 2\lambda$	$4\lambda \cdot 3\lambda = 12\lambda^2$	$4\lambda \cdot 5\lambda = 20\lambda^2$

c) (10%) Mark the design rules in this layout that determine the width of this layout.



使用到的 design rule 有: (包含假設及參考講義)

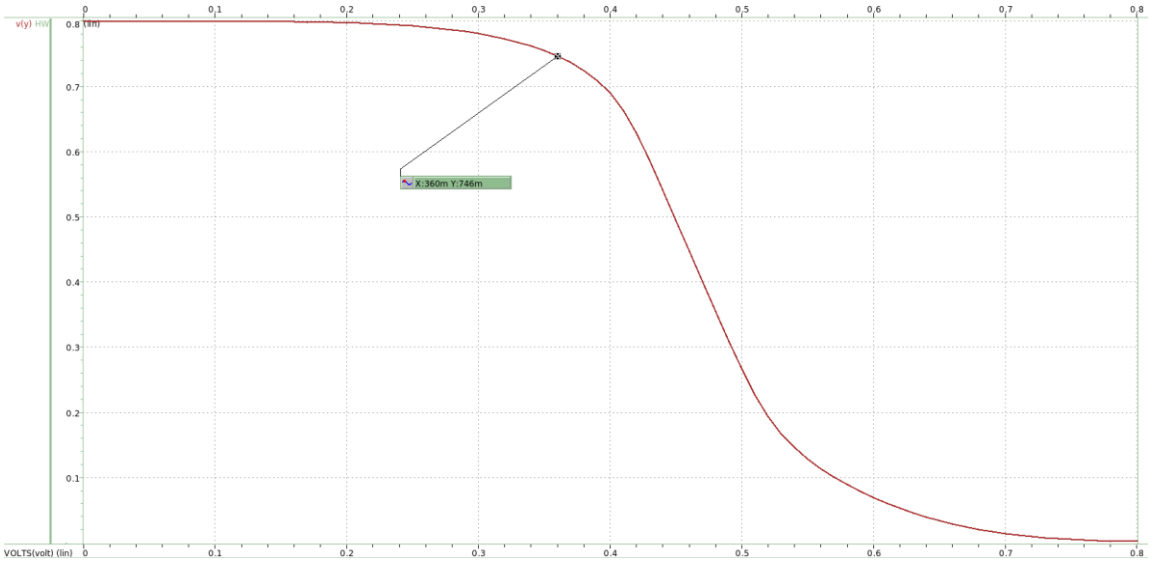
$$\begin{cases} Metal\_Diffusion\_Contact = 1\lambda \\ W_{Contact} = 2\lambda \\ Spacing_{Contact2Contact} = 3\lambda \\ Spacing_{Contact2Poly} = 2\lambda \\ Spacing_{Poly2Poly} = 3\lambda \\ Spacing_{Diff2Diff} = 12\lambda \end{cases}$$

因此可以得知(a) layout 的面積為 $36\lambda \cdot 30\lambda = 1080\lambda^2$，而(b)layout 的面積為 $30\lambda \cdot 30\lambda = 900\lambda^2$，雖然(a)layout 速度較快，但是面積較大。因此也可以透過這題了解到沒有最好的 design，只有最適合的 design。在面積與速度間的取捨，也是一門學問!

2.Timing and power analysis (60%)

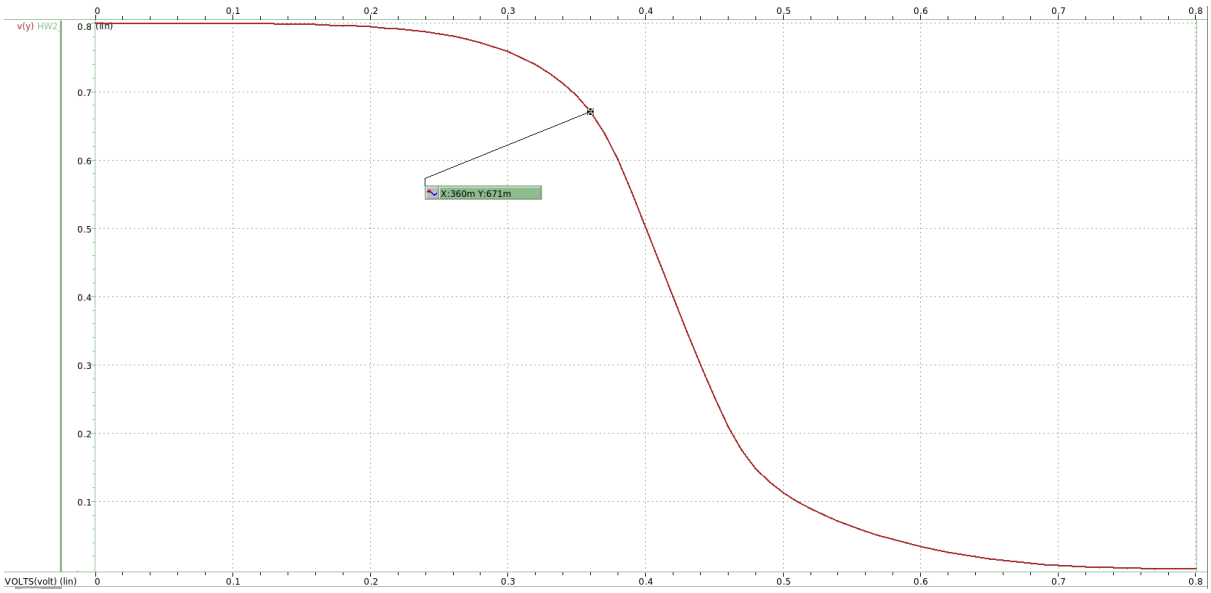
(a) (15%) Design a two inputs NAND logic gate (NAND2) as shown at Fig.9.8 such that it has the logic threshold of 0.45*VDD (when two inputs have the same voltage). Indicate the W/L of PMOS and NMOS and show the Spice simulation results of VTC.

$$\frac{W_p}{W_n} = \frac{128n}{64n}, L_p = L_n = 32n$$



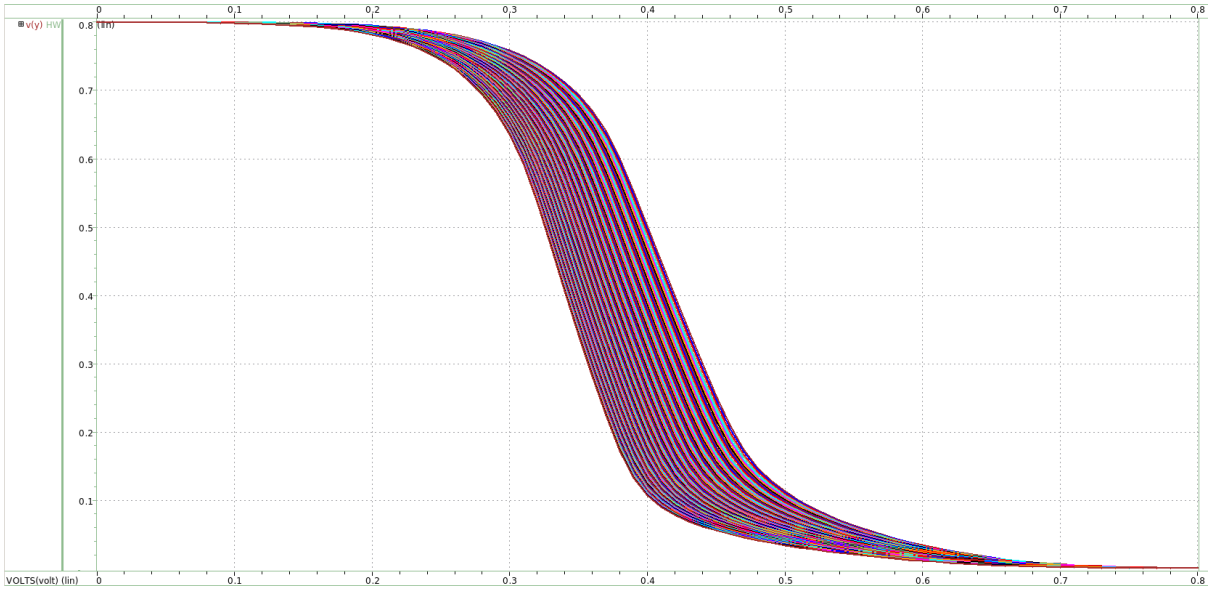
按照之前的經驗，將 PMOS 的寬度調為兩倍大，結果發現 PMOS 強度大於 NMOS，因此我便將 PMOS 也先調整成 64nm 觀察看看。

$$\frac{W_p}{W_n}=\frac{64n}{64n}, L_p = L_n = 32n$$

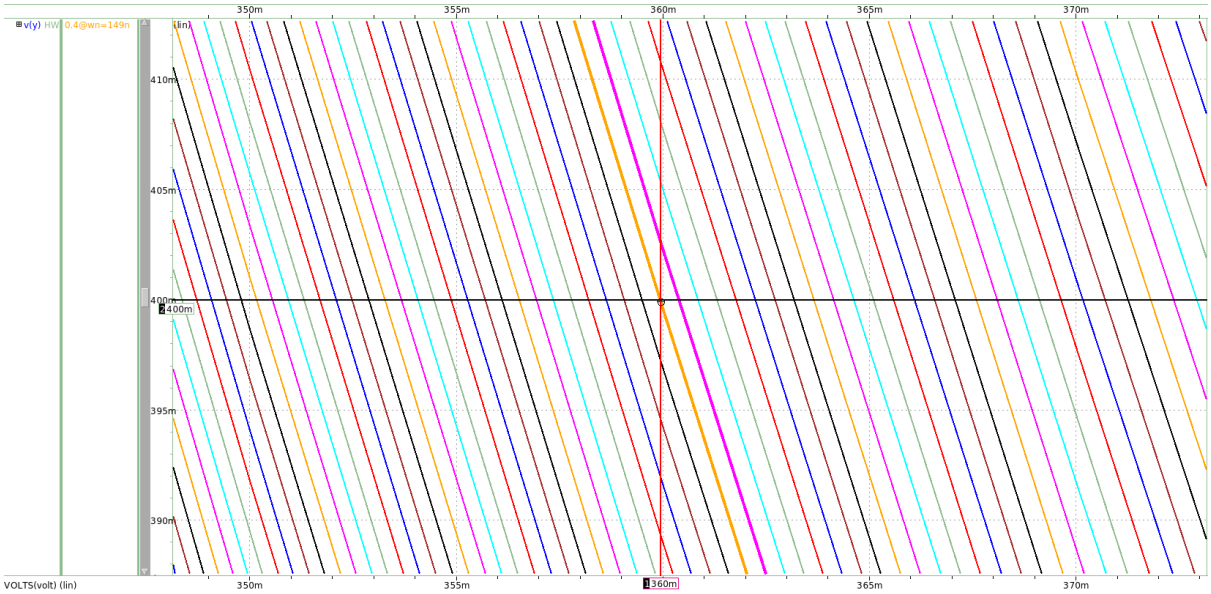


發現就算W_p已經不能再小了，PMOS 的強度仍然比較強，因此我們可以試看看透過增大W_n加強 NMOS 的強度。因為不知道W_n要大到什麼樣的層度，因此使用 SWEEP W_n來找到相對應的W_n。

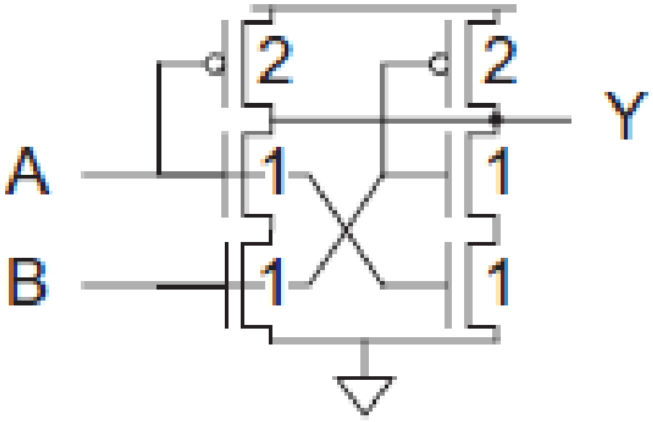
$$\frac{W_p}{W_n}=\frac{64nm}{64\sim 200nm}, L_p = L_n = 32nm$$



$\frac{W_p}{W_n} = \frac{64nm}{64 \sim 200nm}, L_p = L_n = 32nm$ Zoom In



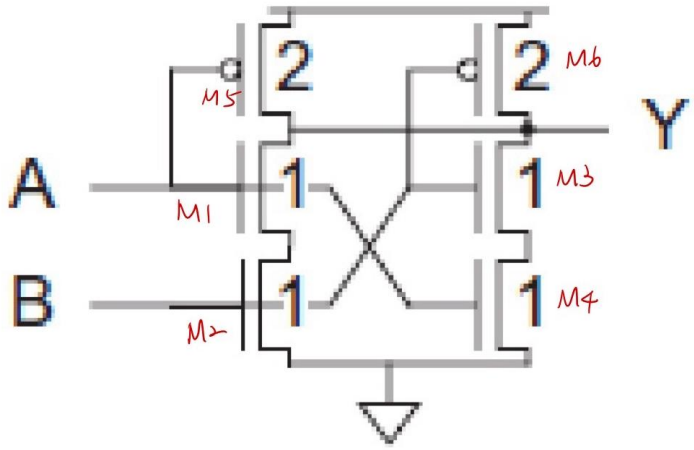
當 input signal 為 $0.45V_{DD} = 0.45 \cdot 0.8 = 0.36V$ 時，output 為 $0.5V_{DD} = 0.5 \cdot 0.8 = 0.4V$ 的情況在 $W_n = 149nm$ 符合 spec。用表格的方式來整理這題的 W/L:



MOSFET Type	$\frac{W}{L}$
PMOS	$\frac{W}{L} = \frac{64nm}{32nm}$
NMOS	$\frac{W}{L} = \frac{149nm}{32nm}$

(b) (10%) Run SPICE to get the output capacitances of the NAND2 and input capacitance of NAND2, leakage power dissipation when input and output are in 0/1 and 1/0 respectively (estimate reasonable AD, AS, PD, PS using the micro rule listed in the page 3-19 of the note with scale ratio 32/65)

一樣，先來幫 MOS 編號:



來計算 source/drain 的長度:

由 Design Rule:

Contact (to poly or active)	5.1, 6.1	Width (exact)	0.08
	5.2b, 6.2b	Overlap by poly or active	0.01
	5.3, 6.3	Spacing to contact	0.10
	5.4	Spacing to gate	0.07

$$L_{Drain,Source} = \left(W_{Contact} + 2 \cdot Spacing_{Contact2Poly}\right) \cdot \frac{32}{65} = \left(0.08\mu m + 2 \cdot 0.07\mu m\right) \cdot \frac{32}{65} \approx 0.108\mu m = 108nm$$

因此可以透過:

$$\begin{cases} AD = W \cdot L_{Drain} \\ AS = W \cdot L_{Source} \\ PD = 2 \cdot \left(W + L_{Drain}\right) \\ PS = 2 \cdot \left(W + L_{Source}\right) \end{cases}$$

求出每顆 MOS 的參數，使 spice simulation 與 layout 的結果更為接近

MOSFET	AD nm^2	AS nm^2	PD nm	PS nm
M1(N)	16092	16092	514	514
M2(N)	16092	16092	514	514
M3(N)	16092	16092	514	514
M4(N)	16092	16092	514	514
M5(P)	6912	6912	344	344
M6(P)	6912	6912	344	344

[Note: 與同學討論過後其實關於 share diffusion layout 的 drain 與 source 的長度是否要取一半而有不同意見，我認為就算是 share diffusion，對於每個 MOS，應該仍要有完整的 source drain 來跑 simulation。]

接著，套用以上參數來跑模擬:
使用.alter 跑兩種 case 後，在 lis 檔案裡可以查看模擬出來的電容為:

I/O:0/1

```
   nodal  capacitance table

   node    =    cap      node    =    cap      node    =    cap

+0:a       = 560.0006a 0:n1      = 580.5332a 0:n2      = 580.5332a
+0:vdd     =   1.0625f 0:vss     =   2.4966f 0:y       = 955.3566a
```

I/O:1/0

```
   node    =    cap      node    =    cap      node    =    cap

+0:a       = 828.2633a 0:n1      = 699.8649a 0:n2      = 699.8649a
+0:vdd     = 988.4253a 0:vss     =   2.6507f 0:y       =   1.1077f
```

In Table Form:

I/O	Output Capacitance	Input Capacitance
0/1	955.3566a	560.0006a
1/0	1.1077f	828.2633a

而至於 leakage power，則是在固定輸入為 0/1 後，量測 vdd 的電流，一樣使用.alter 觀察兩種 case，而後在 lis 找到模擬數據:

I/O:0/1

```
subckt
element  0:va       0:vvdd     0:vvss
 volts      0.       800.0000m    0.
 current   78.0391p  -35.1933n   35.1153n
 power      0.        28.1547n    0.
```

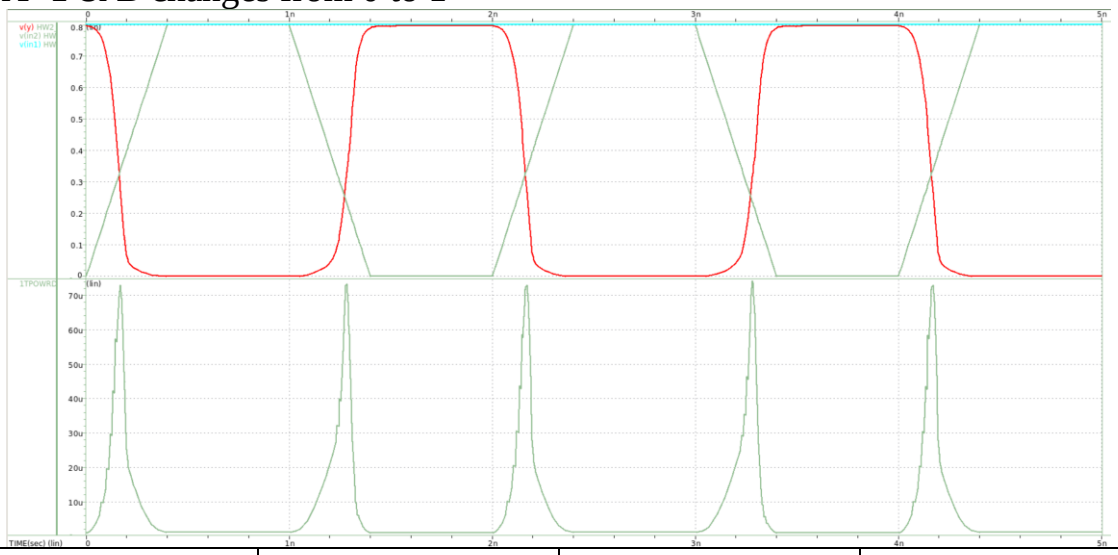
I/O:1/0

```
subckt
element  0:va       0:vvdd     0:vvss
 volts    800.0000m  800.0000m    0.
 current -437.1304p -224.8531n  225.2903n
 power    349.7044p  179.8825n    0.
```

I/O	Leakage Power watt
0/1	28.1547n
1/0	179.8825n

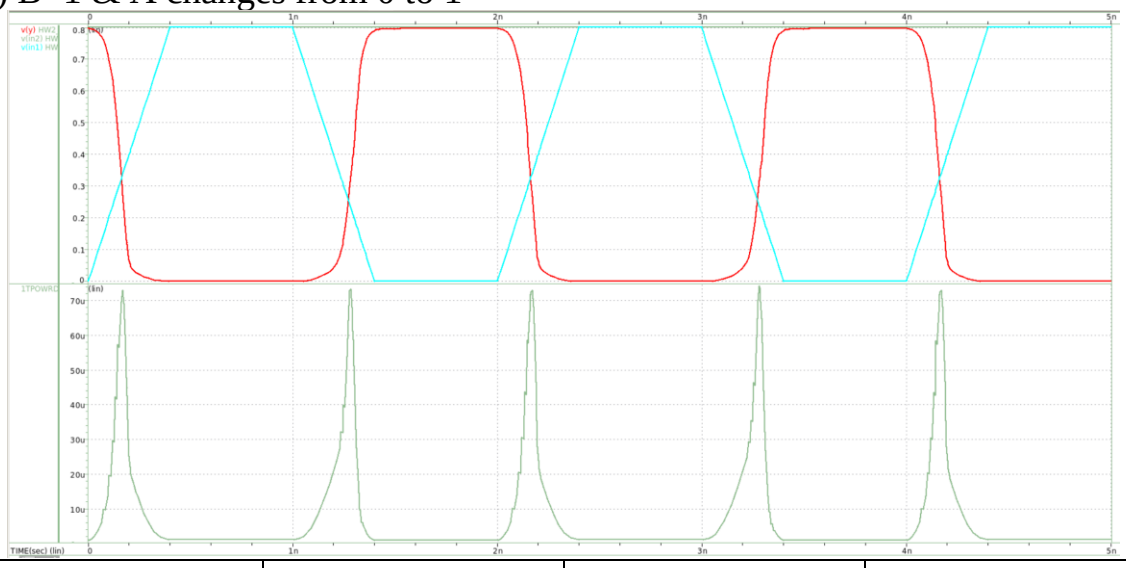
(c) (25%) Do the timing and power analysis of a NAND2 (Fig.9.8) which has a fanout of two NAND2s. Input signal is a pulse waveform with duration of 2ns (with tr=0.4ns and tf=0.4ns defined as 0%-100%, duty=0.5). Run two cases by using SPICE (5ns) to get the timing (tdf and tdr) and power waveform: (i) A=1 and B changes from 0 to 1, (ii) B=1 and A=1changes from 0 to 1. Then list in table form with the tdf, tdr, average power and peak power of the NAND2.

(i) A=1 & B changes from 0 to 1



tdf	tdr	Average power	Peak power
75,4ps	-25.72ps	7.371e-06w	7.404e-05w

(ii) B=1 & A changes from 0 to 1

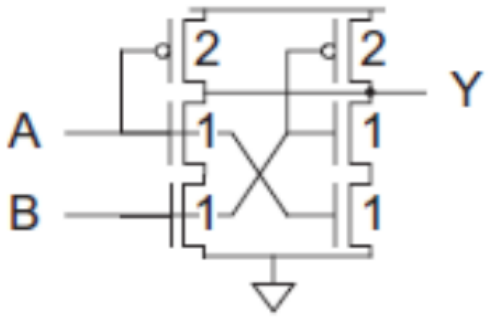


tdf	tdr	Average power	Peak power
75.4ps	-25.72ps	7.371e-06	7.404e-05

Note that the data are from measurement result with alter.

值得注意的是對於 tdr，我設計的電路會使得 input 還沒下降至 0.45VDD，output 就已經上升至 0.5VDD 了，因此會是負的!

(d) (10%) Discuss the behavior of two cases based on the SPICE simulation results.



如同這個電路的名稱一樣，Symmetric 2-input NAND gate，對於兩個 input 的設計是非常對稱的， 因此可以從 2c 的 spice 的量測結果發現，不管動哪個訊號，量測出來的 timing 及功耗皆為相同。不過如果再多考慮到 layout 實際上的 topology，我認為還是會有些微的不同，因為不可能擺放得非常對稱，及 metal 的走線也可能導致一些 delay 上的誤差。

心得反饋:

這次的作業算是越做越好玩，從一開始設計電路調整參數，在沒有標準答案的 solution space 裡面找尋一組可以 meet spec 的解。而後去跑考慮 AS AD PS PD 的 hspice simulation，這些都是過去沒有過的體驗。經過這次作業，也大致上對 spice 各種量測及使用方法有更進一步的了解!