

# Chapter 1

## Basic Elements

### 1.1 Inverter

The inverter is easy to verify. It has only one input.

I want to compare the result of using different models.

- v1: Use Hspice sampled data model  $Mn Mp$
- v2: Use interpolated polynomial model  $Mn Mp$
- v3: Use one interpolated polynomial model  $Minv$
- v4: Use brockett from NAND circuit
- v5: Use first order model  $Mn Mp$

The reachable space are shown in figure 1.1 1.3 1.5, 1.7. The brockett annulus<sup>1</sup> are shown in figure 1.2 1.4 1.6, 1.8. The results are almost the same.

### 1.2 NAND circuit

The NAND circuit is shown in figure 1.9.

#### 1.2.1 First Try

The first try use Mnp and Mn2 model, with no extra constraint on  $y_n$  variables.

The brockett annulus of stage 11 is shown in figure 1.10. The error is too large in the brockett annulus.

Figure 1.15, 1.16, 1.17, 1.18 and figure 1.19 1.20 1.21 1.22 shows the value of  $y$  and  $y_n$  when  $x_1$  is high. Figure 1.23, 1.24, 1.25, 1.26 and figure 1.27 1.28 1.29 1.30 shows the value of  $y$  and  $y_n$  when  $x_2$  is high. When  $x_1$  or  $x_2$  is high, the NAND circuit is similar with an inverter. However, compared with the reachable space of inverter as shown in figure 1.14, the lower bound of  $y$  drops too fast.

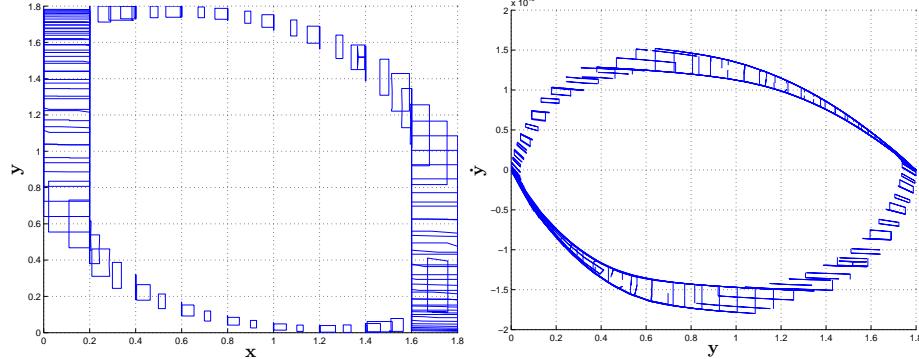


Figure 1.1: The reachable space of inverter, v1  
Figure 1.2: The brockett annulus of inverter, v1

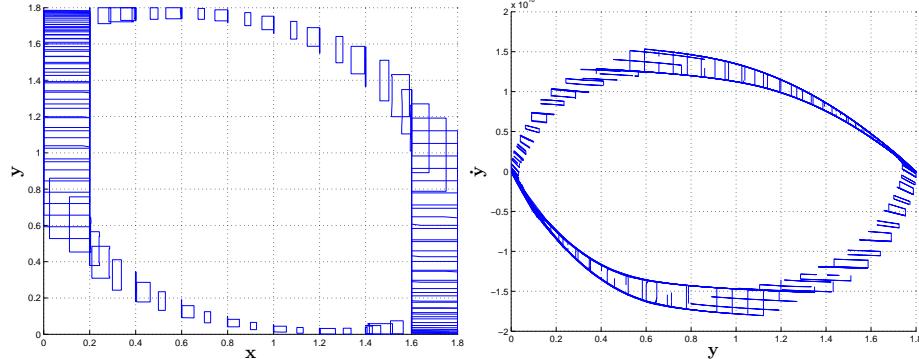


Figure 1.3: The reachable space of inverter, v2  
Figure 1.4: The brockett annulus of inverter, v2

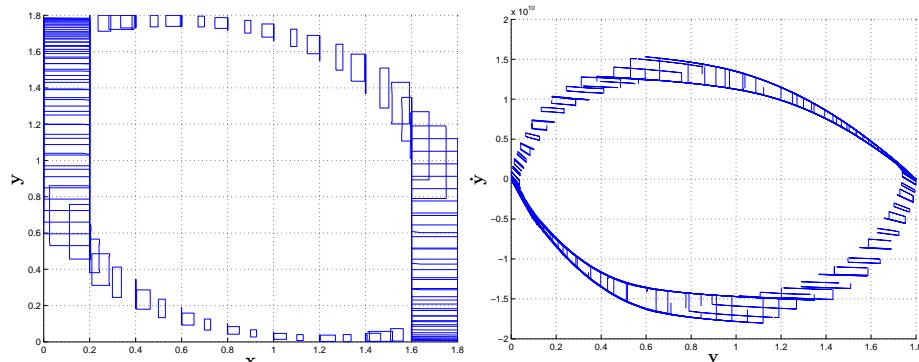


Figure 1.5: The reachable space of inverter, v3  
Figure 1.6: The brockett annulus of inverter, v3

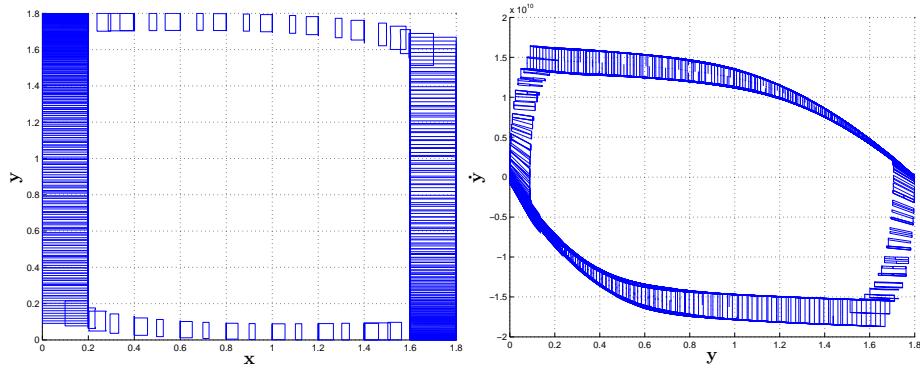


Figure 1.7: The reachable space of in-  
Figure 1.8: The brockett annulus of in-  
verter, v5

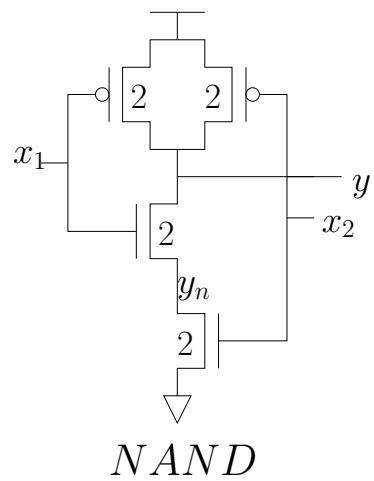


Figure 1.9: The NANA circuit

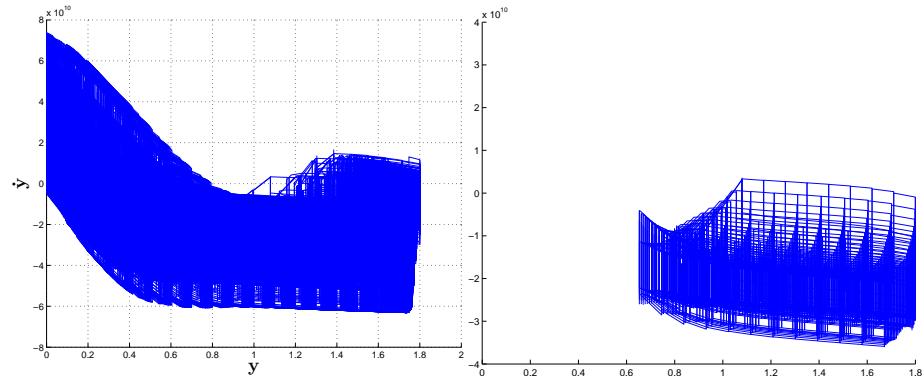


Figure 1.10: The brockett annulus of version 1, stage 11.

Figure 1.11: The brockett annulus of version 1, state  $\langle 9, 6 \rangle$

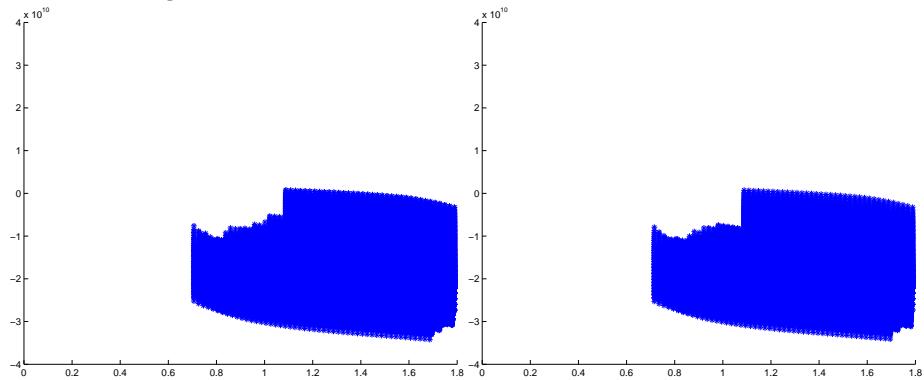


Figure 1.12: The brockett annulus of state  $\langle 9, 6 \rangle$ , sampling, Mn Mp model.

Figure 1.13: The brockett annulus of state  $\langle 9, 6 \rangle$ , sampling, Mnp model.

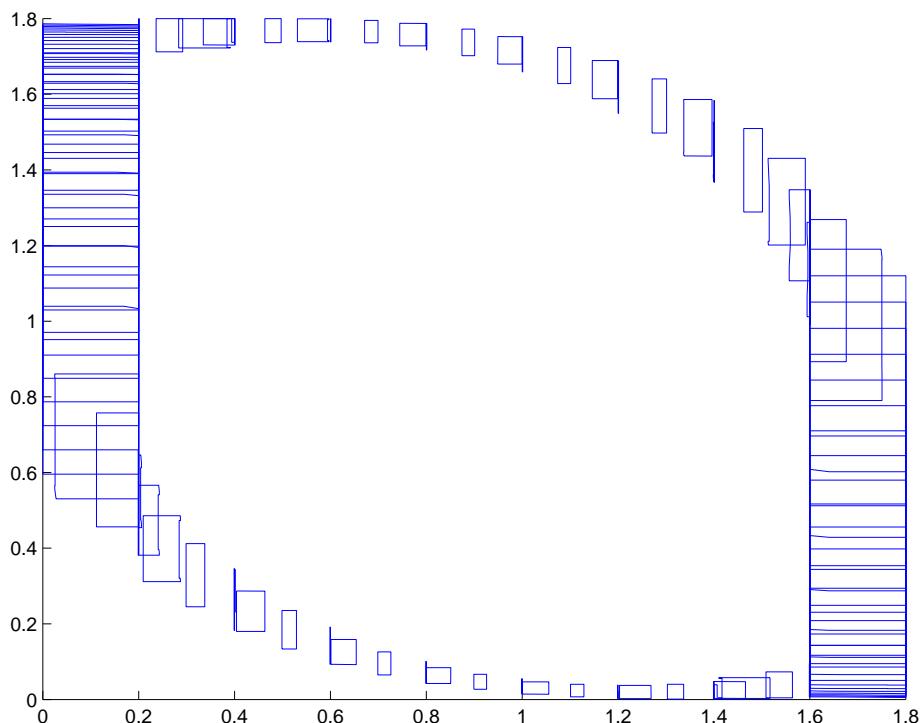


Figure 1.14: The reachable space of inverter

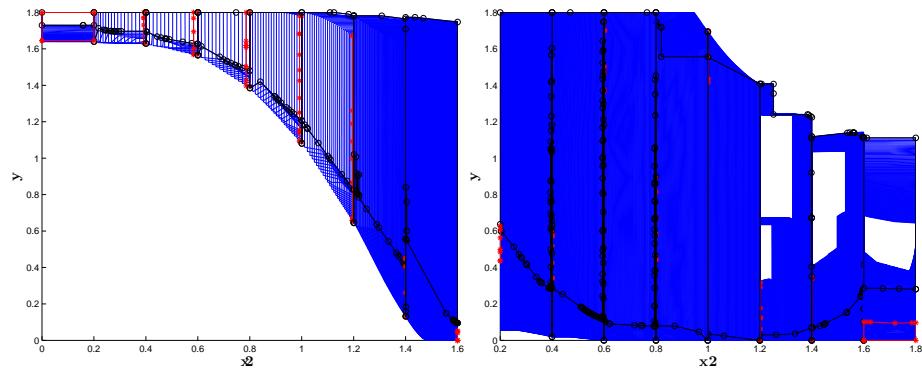


Figure 1.15: The  $y$  value when  $x_1$  is high, version 1, stage 11.

Figure 1.16: The  $y$  value when  $x_1$  is high, version 1, stage 12.

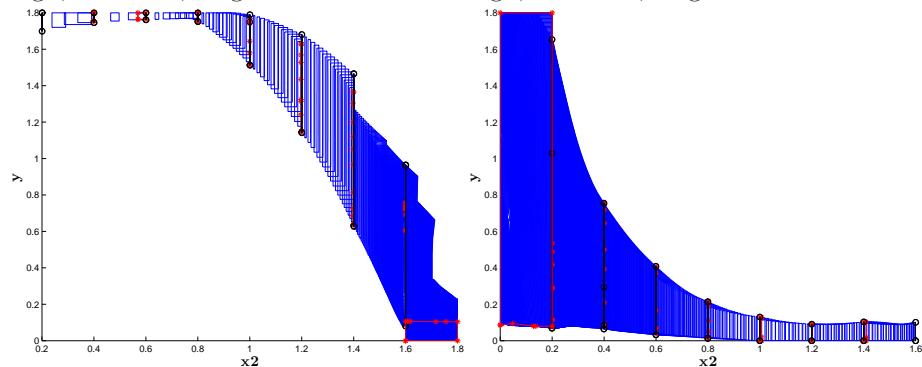


Figure 1.17: The  $y$  value when  $x_1$  is high, version 1, stage 13.

Figure 1.18: The  $y$  value when  $x_1$  is high, version 1, stage 14.

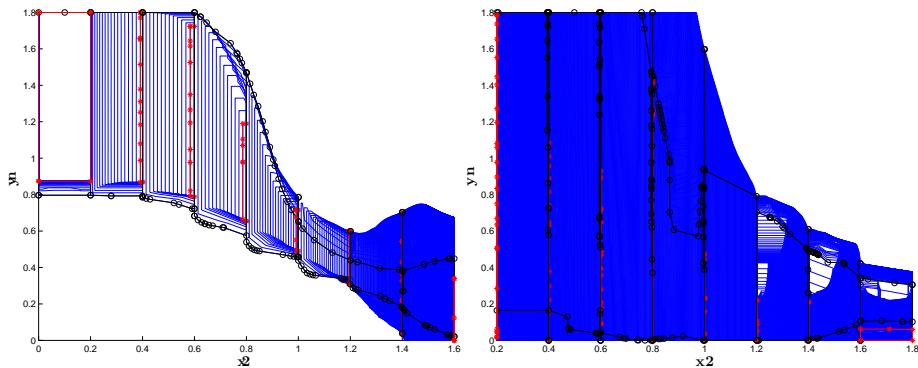


Figure 1.19: The  $y_n$  value when  $x_1$  is high, version 1, stage 11.

Figure 1.20: The  $y_n$  value when  $x_1$  is high, version 1, stage 12.

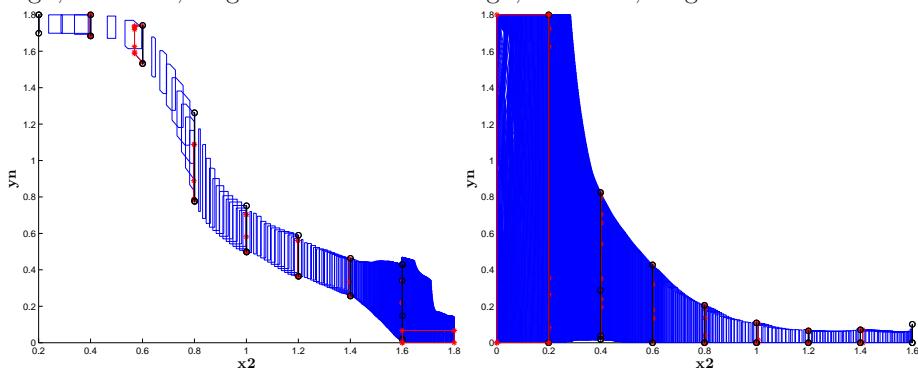


Figure 1.21: The  $y_n$  value when  $x_1$  is high, version 1, stage 13.

Figure 1.22: The  $y_n$  value when  $x_1$  is high, version 1, stage 14.

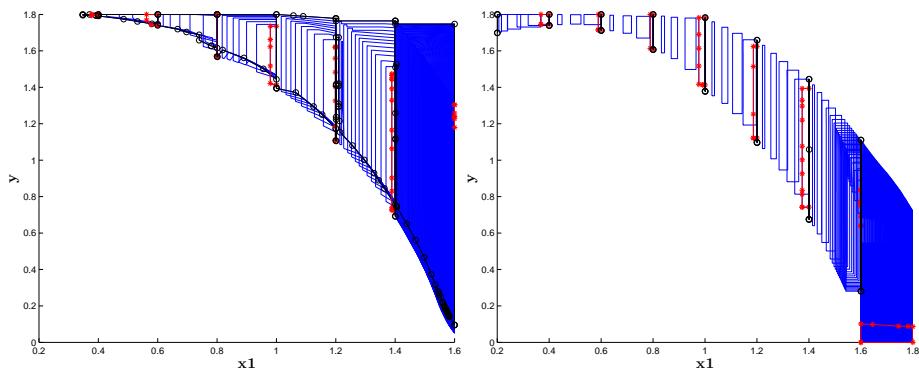


Figure 1.23: The  $y$  value when  $x_2$  is high, version 1, stage 11.

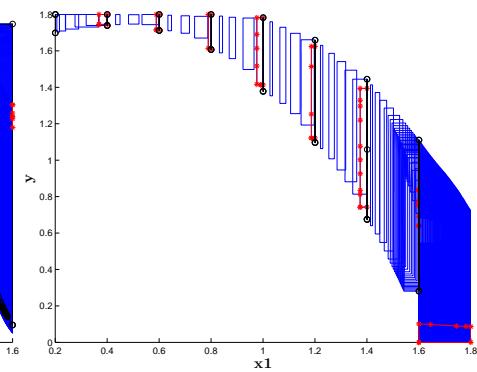


Figure 1.24: The  $y$  value when  $x_2$  is high, version 1, stage 12.

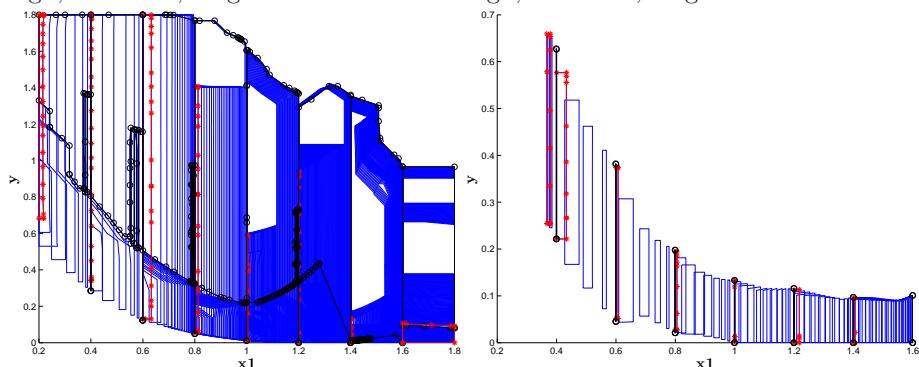


Figure 1.25: The  $y$  value when  $x_2$  is high, version 1, stage 13.

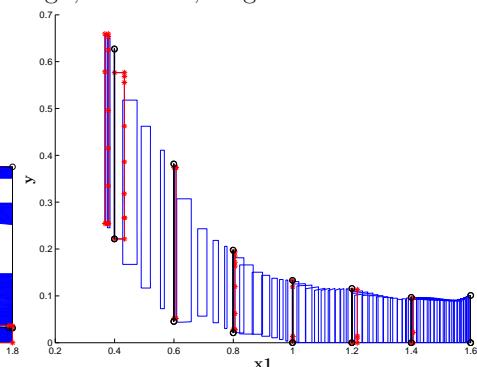
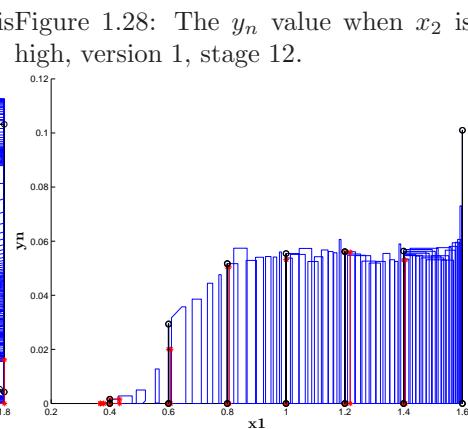
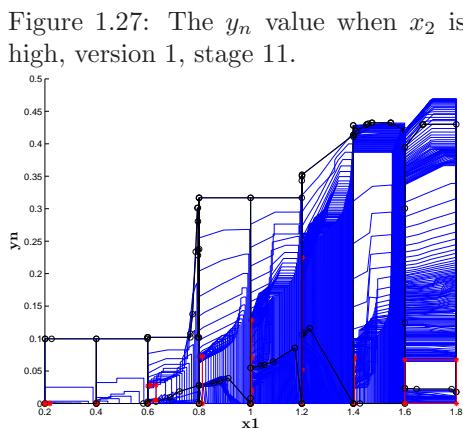
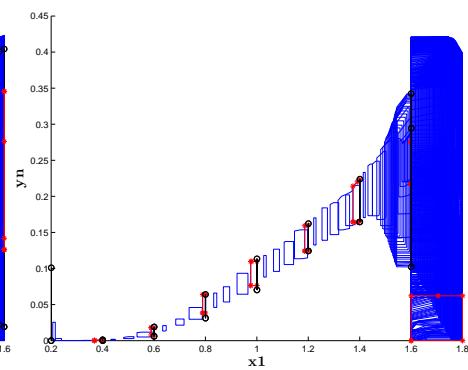
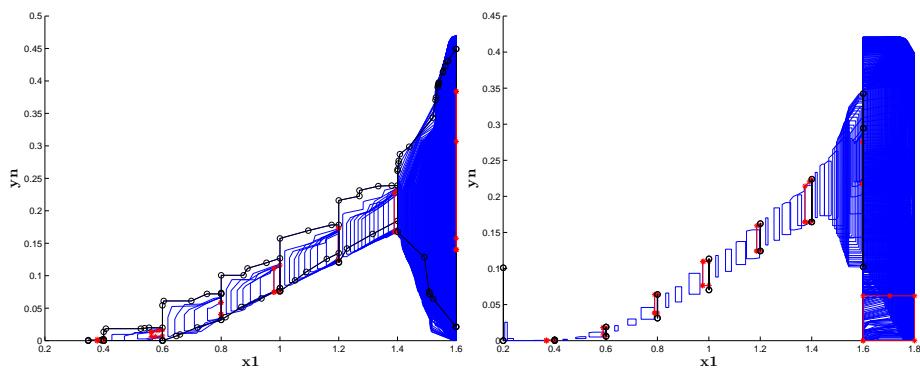


Figure 1.26: The  $y$  value when  $x_2$  is high, version 1, stage 14.



First, I worked on the  $\langle 9, 6 \rangle$  state, the brockett is shown in figure 1.11. I tried other methods which compute the derivative at some discrete points. However, the result is similar as shown in figure 1.12, 1.13, which shown the computation error is small.

The result from *AND* circuit is similar. The brockett of stage 11 is shown in figure 1.32. And figure 1.31 shows the difference of the output inverter and the signal inverter as shown in figure 1.14.

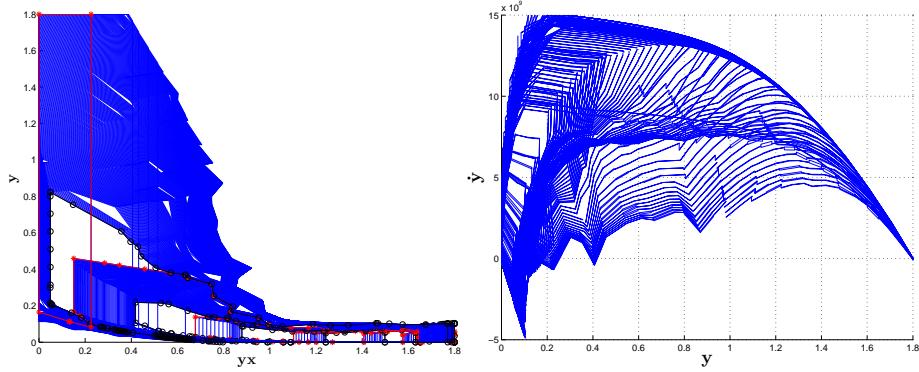


Figure 1.31: Inverter of AND circuit

Figure 1.32: Brockett of AND circuit

### 1.2.2 Simulation

I want to see the simulation result and find out where the approximation is.

The brockett annulus of  $y$  signal is shown in figure 1.33, and figure 1.34 shows an example.

The reachable space when  $x_1 = [1.6, 18]$  is shown in figure 1.35 and the reachabel space when  $x_2 = [1.6, 1.8]$  is shown in figure 1.36.

### 1.2.3 Second Try

I add the constraint that  $y_n \leq 1.45, y_n \leq y$  and also  $\langle y, y_n \rangle$  plane. And want to see if there are any difference.

#### Stable Stage

I try to compute the reachable space when  $x_1 = [1.6, 1.8]$  and  $x_2 = [0.0, 0.2]$  (stage 18) with the initial value  $y = y_n = [0.0, 1.8]$  as an example to find why  $y, y_n$  are always in the range of  $[0.0, 1.8]$  in the first version as shown in figure 1.18 and figure 1.22.

I tried four methods

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<sup>1</sup>We use hspice simulated model to compute the brockett annulus.

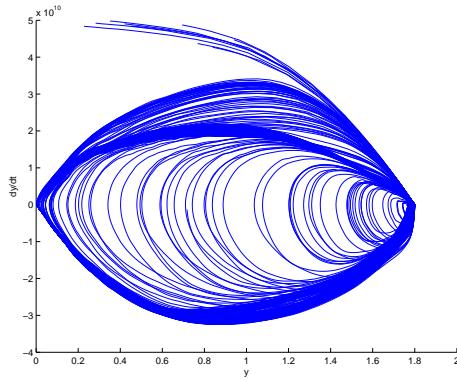


Figure 1.33: The brockett annulus of  $y$  signal from simulation

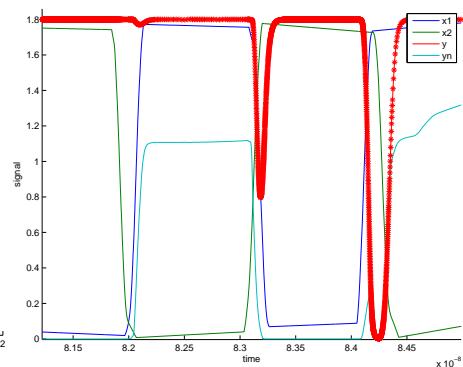


Figure 1.34: An example of  $y$  signal that violates the brockett annulus

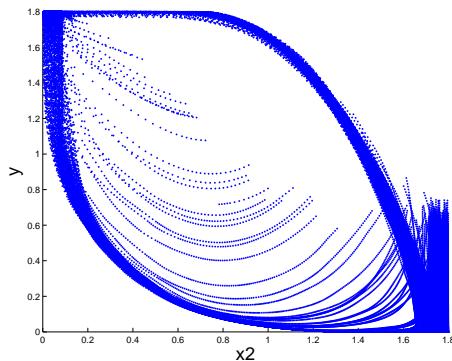


Figure 1.35: Reachable space when  $x_1$  is high from simulation

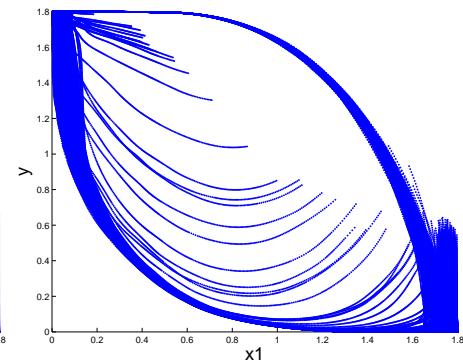


Figure 1.36: Reachable space when  $x_2$  is high from simulation

**v1:** same with the first version. With only  $\langle x_1, y \rangle, \langle x_2, y \rangle, \langle x_1, y_n \rangle, \langle x_2, y_n \rangle$  slice and  $x_1, x_2, y, y_n \in [0, 1.8]$  constraints

**v2.1:** add  $\langle y, y_n \rangle$  slice

**v2.2:** add  $y_n \in [0, 1.45], y_n \leq y$  constraints

**v2:** add both slice and constraints

The bounding box of proejctagon is shown in table 1.1.

var	v1	v2	v2.1	v2.2
$x_1$	[1.6,1.8]	[1.6,1.8]	[1.6,1.8]	[1.6,1.8]
$x_2$	[0.0,0.2]	[0.0,0.2]	[0.0,0.2]	[0.0,0.2]
$y$	[0.07,1.8]	[1.64,1.8]	[1.63,1.8]	[1.64,1.8]
$y_n$	[0.0,1.45]	[0.87,1.45]	[0.87,1.56]	[0.88,1.45]
steps	400(v1)/1200(v11)	400	400	600
time	50ps/165ps	500ps	440ps	250ps

Table 1.1: The bounding box of stable region

And the  $\langle y, y_n \rangle$  plot is shown in figure 1.37 for v2, figure 1.38 for v2.1 and figure 1.39 for v2.2. With the extra slice, We can see that COHO can find the

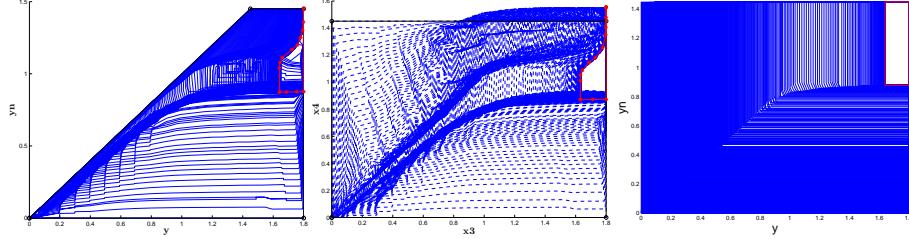


Figure 1.37: The  $\langle y, y_n \rangle$  plot of v2, stage 18.      Figure 1.38: The  $\langle y, y_n \rangle$  plot of v2.1, stage 18.      Figure 1.39: The  $\langle y, y_n \rangle$  plot of v2.2, stage 18.

similar invariant as  $y_n \leq y$  automatically.

Without the  $\langle y, y_n \rangle$  slice,  $y$  rises to high very slowly. For example, for the face  $y = 0.2$ , there is large current from VDD, however, on the other hand, there is relative large current from  $y$  to  $y_n$  when  $y_n = 0$ . When I measure the current for pmos and nmos, I find the current throw the pmos is about  $-0.0024$  and for the nmos is  $0.0025$ . Thus, the DC operation point of  $y$  is around 0.2 when both nmos and pmos with same size are fully conducted. When working on slices with  $y_n$ ,  $y_n$  should not stay as 0 (but smaller than 0.2). However, the linearization error should be large because the interval of  $y$  is large as shown in figure 1.40. Even with the linearization error,  $\dot{y}_n$  should still be clear positive.

But we should avoid the case that the range of current of a device is huge. And the bloat amount for  $y_n$  is about 0.1, although it is not quite large, it can change the current  $\dot{y}_n$  significantly. (use inner bloat amount?) Thus, the reachable space can not shrink any more (or very slowly).

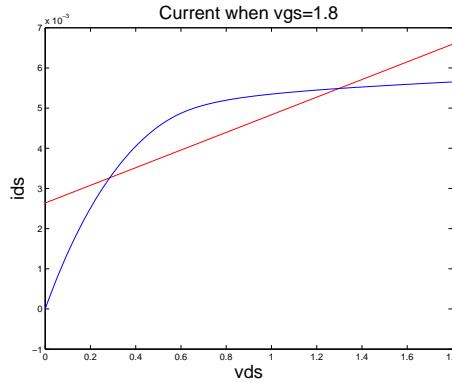


Figure 1.40: Large linearization error for  $y_n$  face because interval of  $y$  is large.

### Transition Stage

After running stable region, I run other stages. The result is better, especially the stage 12. However, it does not satisfies a brockett annulus shown in figure 1.41 as expected .

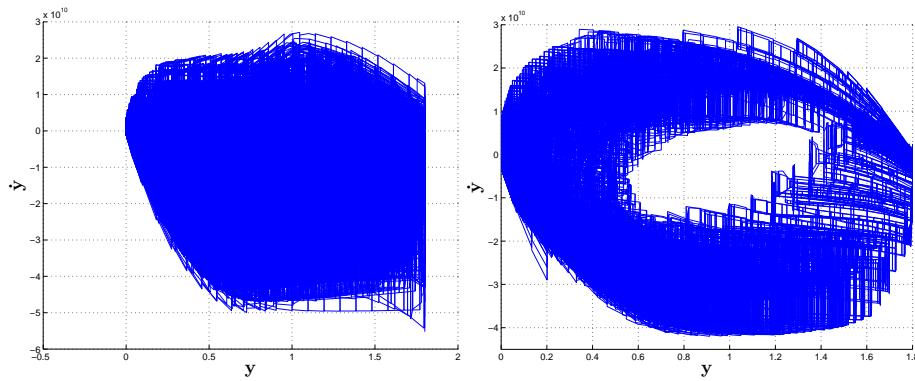


Figure 1.41: The brockett annulus of v2

Figure 1.42: The brockett annulus of v3

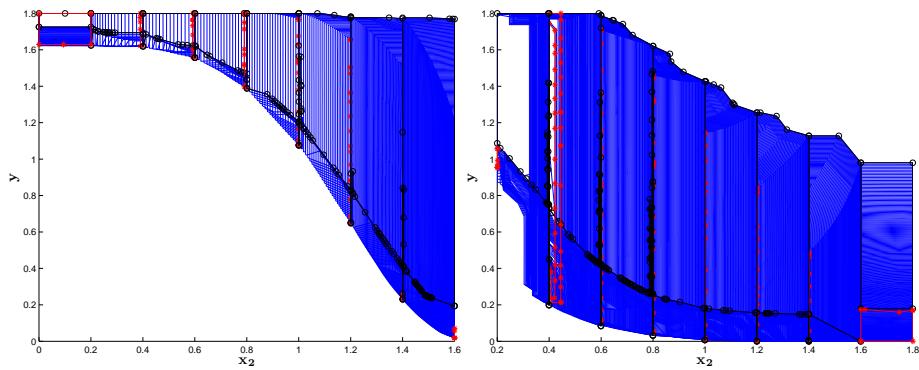


Figure 1.43: The  $y$  value when  $x_1$  is high, version 2, stage 11.

Figure 1.44: The  $y$  value when  $x_1$  is high, version 2, stage 12.

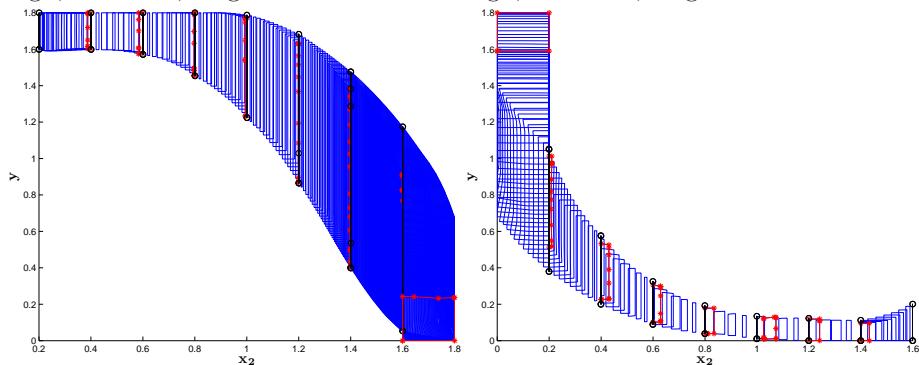


Figure 1.45: The  $y$  value when  $x_1$  is high, version 2, stage 13.

Figure 1.46: The  $y$  value when  $x_1$  is high, version 2, stage 14.

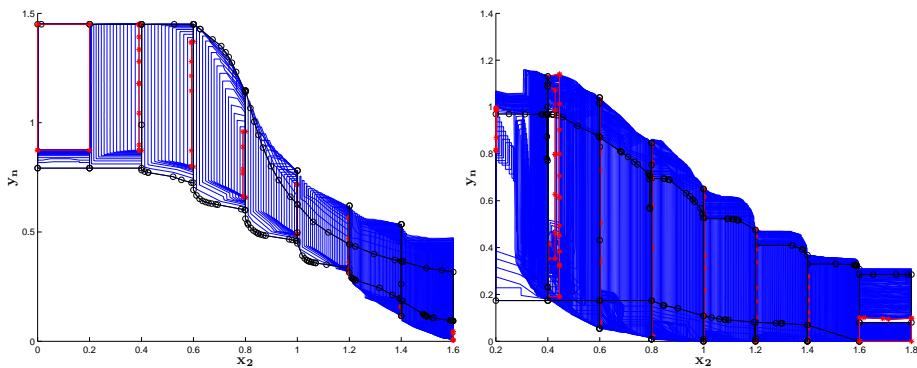


Figure 1.47: The  $y_n$  value when  $x_1$  is high, version 2, stage 11.

Figure 1.48: The  $y_n$  value when  $x_1$  is high, version 2, stage 12.

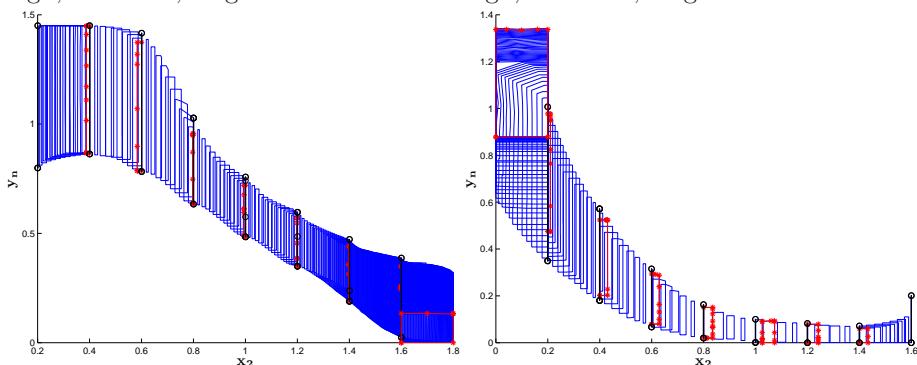


Figure 1.49: The  $y_n$  value when  $x_1$  is high, version 2, stage 13.

Figure 1.50: The  $y_n$  value when  $x_1$  is high, version 2, stage 14.

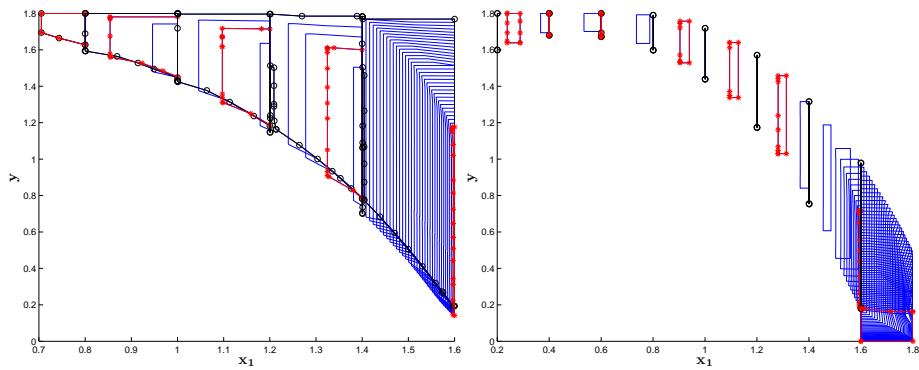


Figure 1.51: The  $y$  value when  $x_2$  is high, version 2, stage 11.

Figure 1.52: The  $y$  value when  $x_2$  is high, version 2, stage 12.

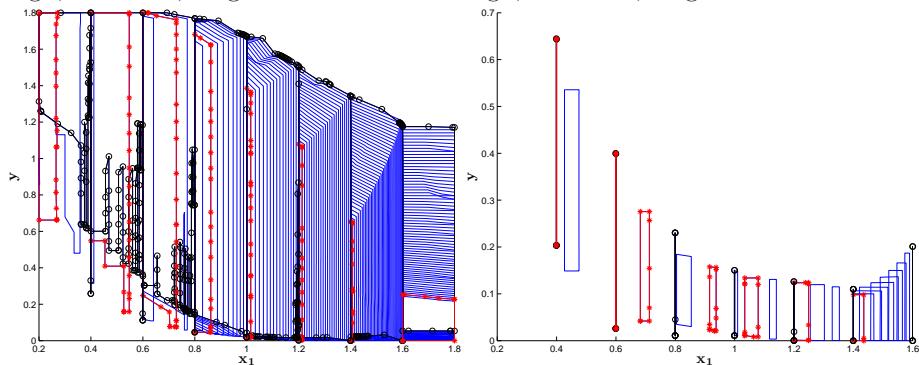


Figure 1.53: The  $y$  value when  $x_2$  is high, version 2, stage 13.

Figure 1.54: The  $y$  value when  $x_2$  is high, version 2, stage 14.

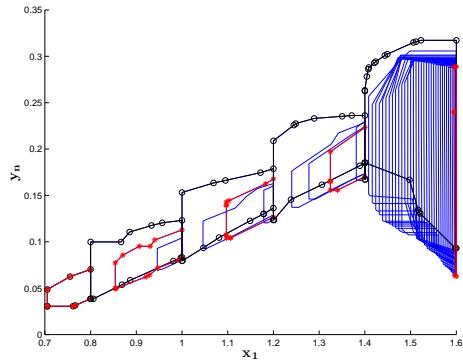


Figure 1.55: The  $y_n$  value when  $x_2$  is high, version 2, stage 11.

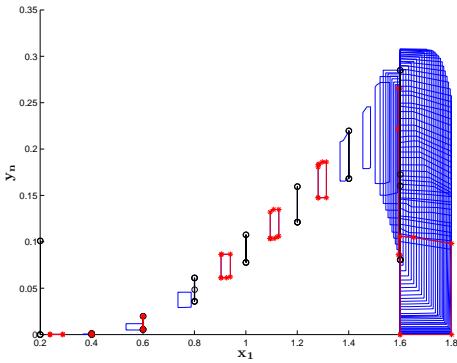


Figure 1.56: The  $y_n$  value when  $x_2$  is high, version 2, stage 12.

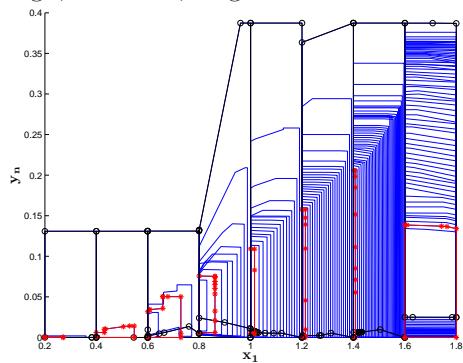


Figure 1.57: The  $y_n$  value when  $x_2$  is high, version 2, stage 13.

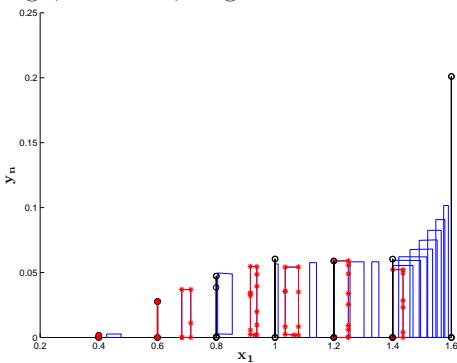


Figure 1.58: The  $y_n$  value when  $x_2$  is high, version 2, stage 14.

### 1.2.4 Third Try

Because we know that the output of NAND circuit does not satisfies an brockett annulus. Thus, we add the constraint that the input can not change at the same time.

We also add the error to the model because we find an error the voltage does not satisfies the constraint  $x \geq 0$  because of interpolation error.

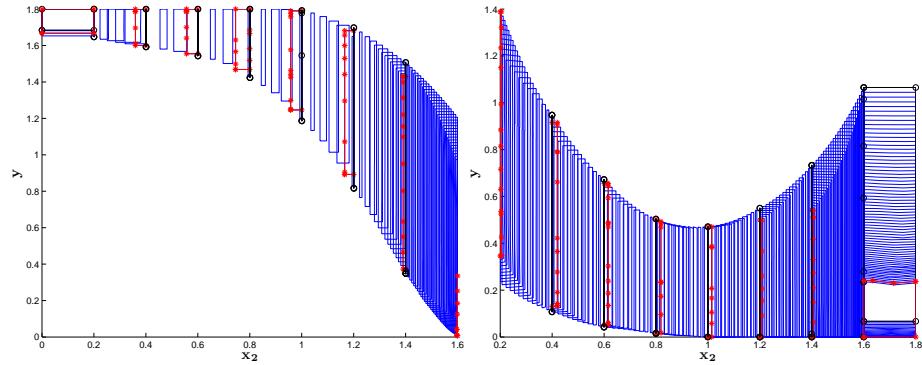


Figure 1.59: The  $y$  value when  $x_1$  is high, version 2, stage 11.

Figure 1.60: The  $y$  value when  $x_1$  is high, version 2, stage 12.

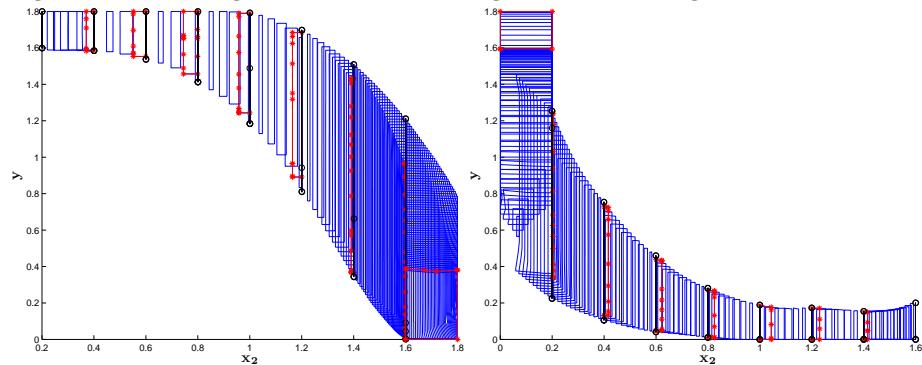


Figure 1.61: The  $y$  value when  $x_1$  is high, version 2, stage 13.

Figure 1.62: The  $y$  value when  $x_1$  is high, version 2, stage 14.

## 1.3 AND

### 1.3.1 Use result from NAND

The result is shown in figure 1.75.

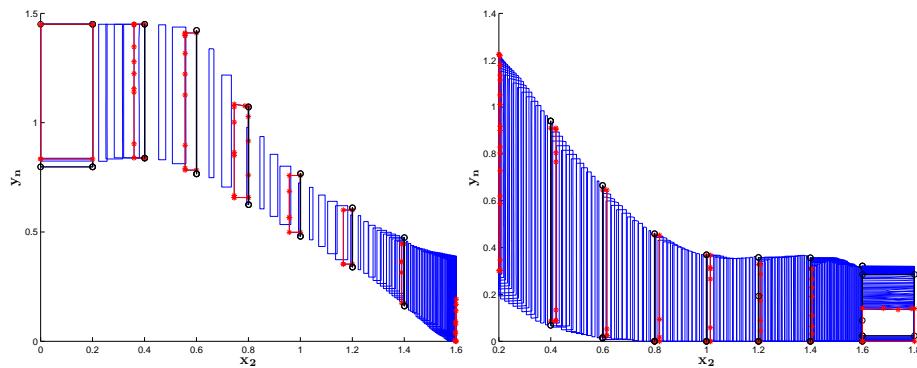


Figure 1.63: The  $y_n$  value when  $x_1$  is high, version 2, stage 11.

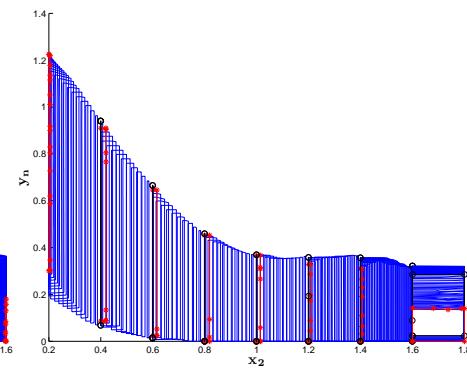


Figure 1.64: The  $y_n$  value when  $x_1$  is high, version 2, stage 12.

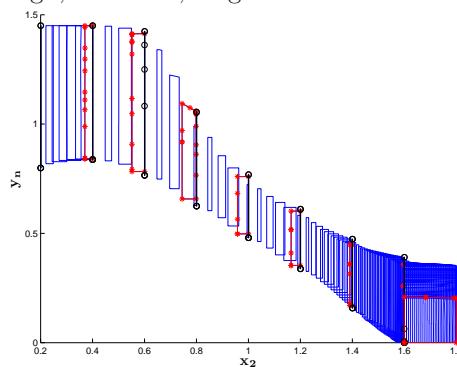


Figure 1.65: The  $y_n$  value when  $x_1$  is high, version 2, stage 13.

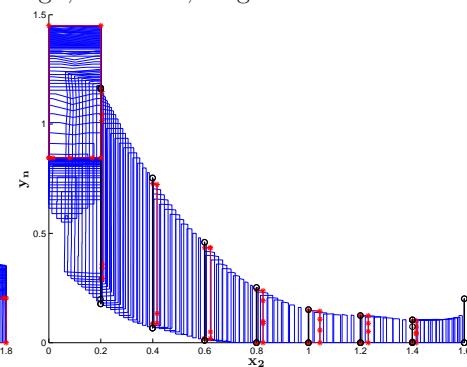


Figure 1.66: The  $y_n$  value when  $x_1$  is high, version 2, stage 14.

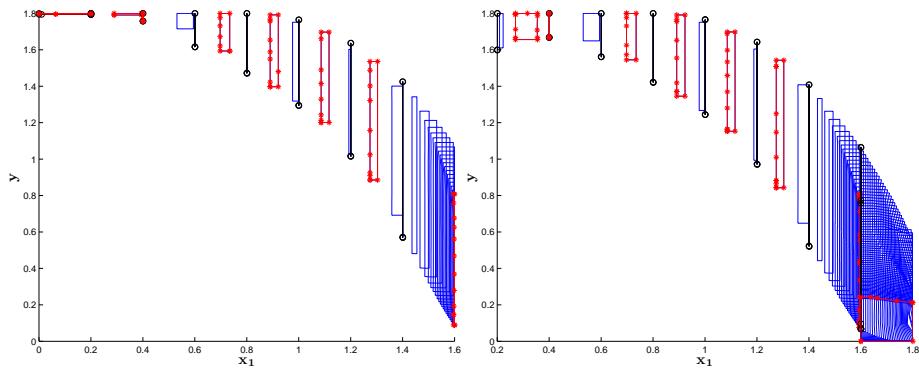


Figure 1.67: The  $y$  value when  $x_2$  is high, version 2, stage 11.

Figure 1.68: The  $y$  value when  $x_2$  is high, version 2, stage 12.

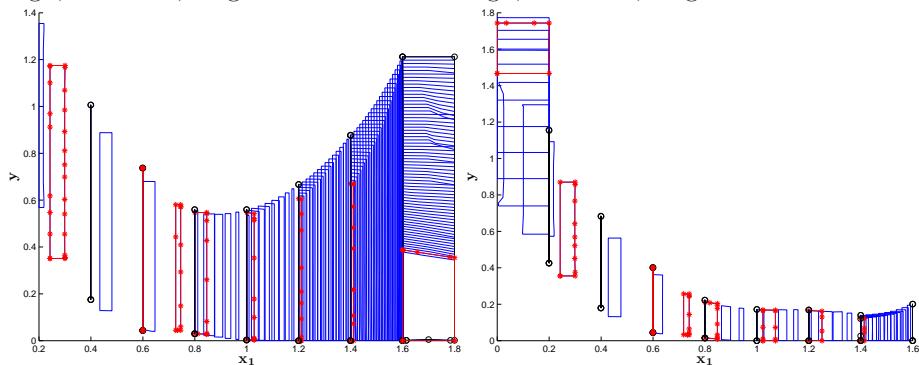


Figure 1.69: The  $y$  value when  $x_2$  is high, version 2, stage 13.

Figure 1.70: The  $y$  value when  $x_2$  is high, version 2, stage 14.

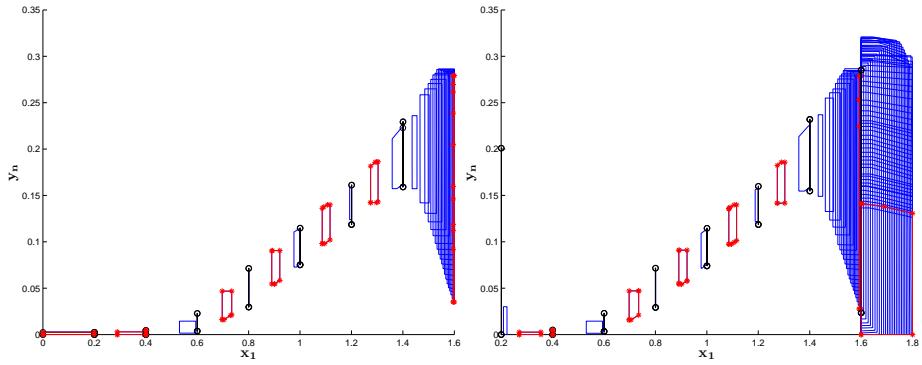


Figure 1.71: The  $y_n$  value when  $x_2$  is high, version 2, stage 11.

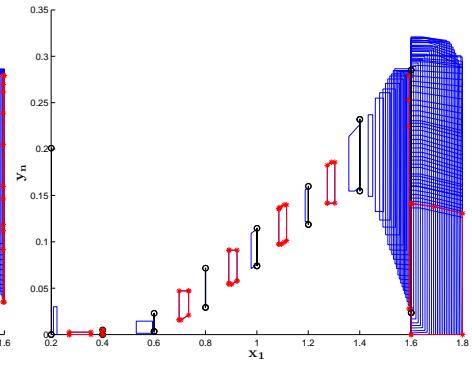


Figure 1.72: The  $y_n$  value when  $x_2$  is high, version 2, stage 12.

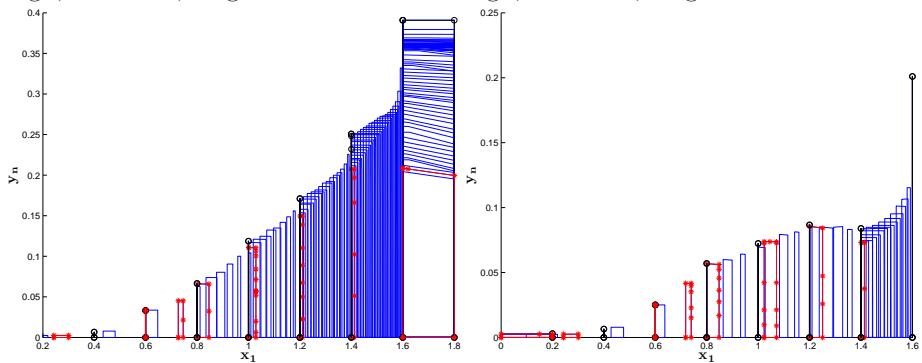


Figure 1.73: The  $y_n$  value when  $x_2$  is high, version 2, stage 13.

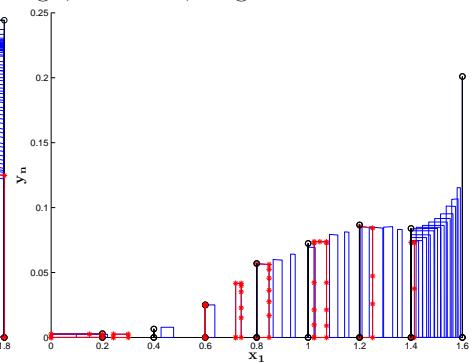


Figure 1.74: The  $y_n$  value when  $x_2$  is high, version 2, stage 14.

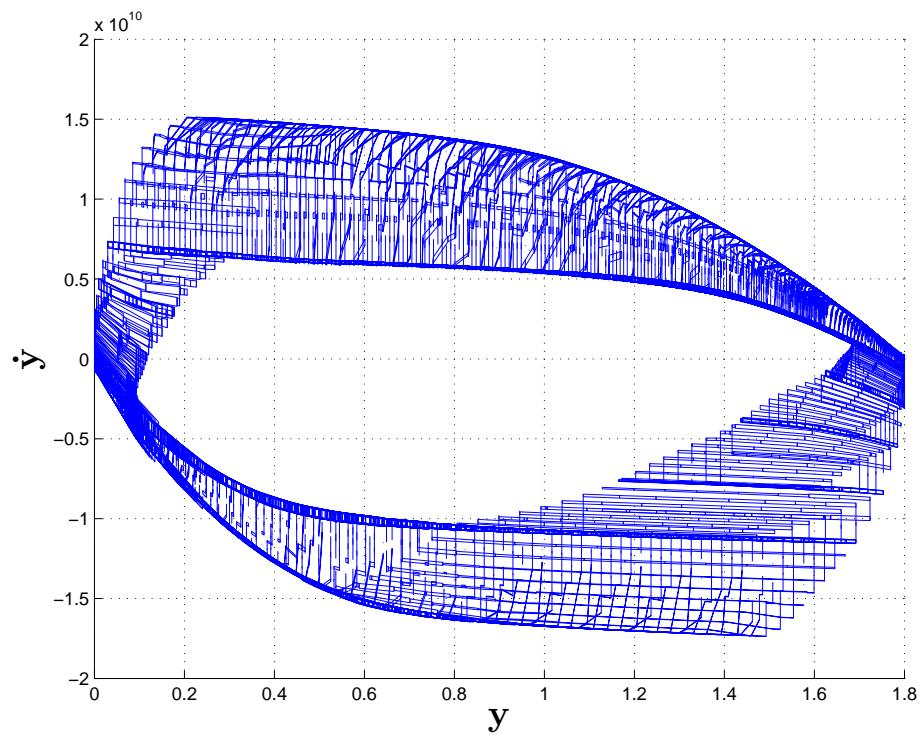


Figure 1.75: The brockett annulus of AND using NAND result

### 1.3.2 Verify it directly

However, the output does not satisfies a brockett annulus. The problem is that the input of inverter  $y_x$  does not satisfies the minimum stable time requirement of the brockett annulus. For example, as shown in figure 1.76, at beginning,  $x_1$  is low and  $x_2$  is high; then  $x_1$  starts to rise and  $y_x$  starts to fall and its final voltage depends on how long  $x_1, x_2$  stay as high. Then  $x_1$  can start to fall and  $y_x$  rises up again. Therefore,  $y_x$  may fall to a middle value and then comes back to high, which make the  $y_x$  does not satisfies a brockett annulus, thus  $y$  also does not satisfies a brockett annulus. Therefore, brockett annulus is really too strictly to describe a signal.

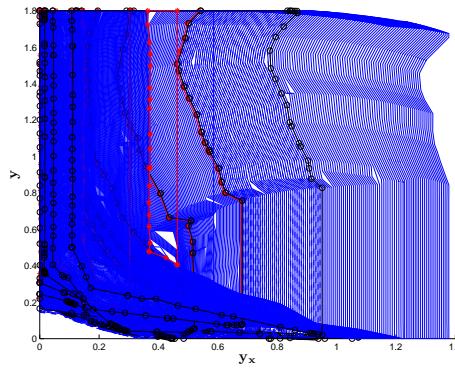


Figure 1.76: The reachable space of stage 12

## 1.4 NOR gate

We use the same computation order with passgate latch circuit. However, there is no forbidden states anymore.

The rising delay from when  $a$  starts to fall ( $b$  low) to when  $y$  is clear high (greater than 1.6) is greater than 238ps (about 284ps), from when  $b$  starts to fall( $a$  low) to when  $y$  is clear high is greater than 232ps (about 285ps). The rising delay from when both  $a$  and  $b$  are low (smaller than 0.2) to when  $y$  is clear high is 187ps.

The falling delay from when  $a$  starts to rise( $b$  low) to when  $y$  is clear low(smaller than 0.2) is 167ps. The delay from when  $b$  starts to rise ( $a$  low) to when  $y$  is clear low is greater than 154ps. The delay from when both  $a$  and  $b$  are clear high to when  $y$  is clear low is 26ps.

The delay is large, because we use large brockett annulus (2-6e10).

The initial and final faces are (in the order of a b i y)

face	initial	result
------	---------	--------

clk(1,1)	0.2 0.0 0.0 1.7	0.2 0.2 1.8 1.8		0.2 0.0 1.7652 1.7388	0.2 0.2 1.8 1.8
data(1,1)	0.0 0.2 0.0 1.7	0.2 0.2 1.8 1.8		0.0 0.2 1.7652 1.7388	0.2 0.2 1.8 1.8
clk(1,9)	0.2 1.6 0.0 0.0	0.2 1.8 1.8 0.1		0.2 1.6 1.7986 0.0	0.2 1.8 1.8 0.0007
data(1,9)	0.0 1.6 0.0 0.0	0.2 1.6 1.8 0.1		0.0 1.6 1.7986 0.0	0.2 1.6 1.8 0.0007
clk(9,1)	1.6 0.0 0.0 0.0	1.6 1.8 1.8 0.1		1.6 0.0 0.0 0.0	1.6 0.2 0.8303 0.0649
data(9,1)	1.6 0.2 0.0 0.0	1.8 0.2 1.8 0.1		1.6 0.2 0.0 0.0	1.8 0.2 0.8303 0.0649
clk(9,9)	1.6 1.6 0.0 0.0	1.6 1.8 1.8 0.1		1.6 1.6 1.373 0.0	1.6 1.8 1.8 0.004
data(9,9)	1.6 1.6 0.0 0.0	1.8 1.6 1.8 0.1		1.6 1.6 1.373 0.0	1.8 1.6 1.8 0.004

## 1.5 C-element

The circuit to verify is shown as in Figure 1.77. The c-element is used in the

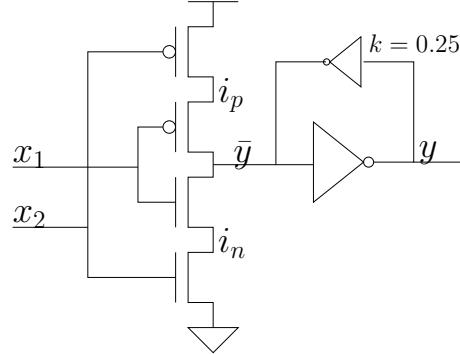


Figure 1.77: The c-element circuit

Micro-Pipeline, where the input requirement is

$$(\square x_1 \cup y) \wedge (\square \neg x_1 \cup \neg y) \wedge (\square x_2 \cup y) \wedge (\square \neg x_2 \cup \neg y).$$

Using Brockett annulus, this specification requires that  $x_1(x_2)$  can not go to  $B_2$  unless  $y \in B_1$  and  $x_1(x_2)$  can not go to  $B_4$  unless  $y \in B_3$ . The specification to verify is that the output  $y$  also satisfies a Brockett annulus.

The brockett annulus of the output is shown in Figure 1.78 and the reachable space is shown in Figure 1.79 and Figure 1.80.

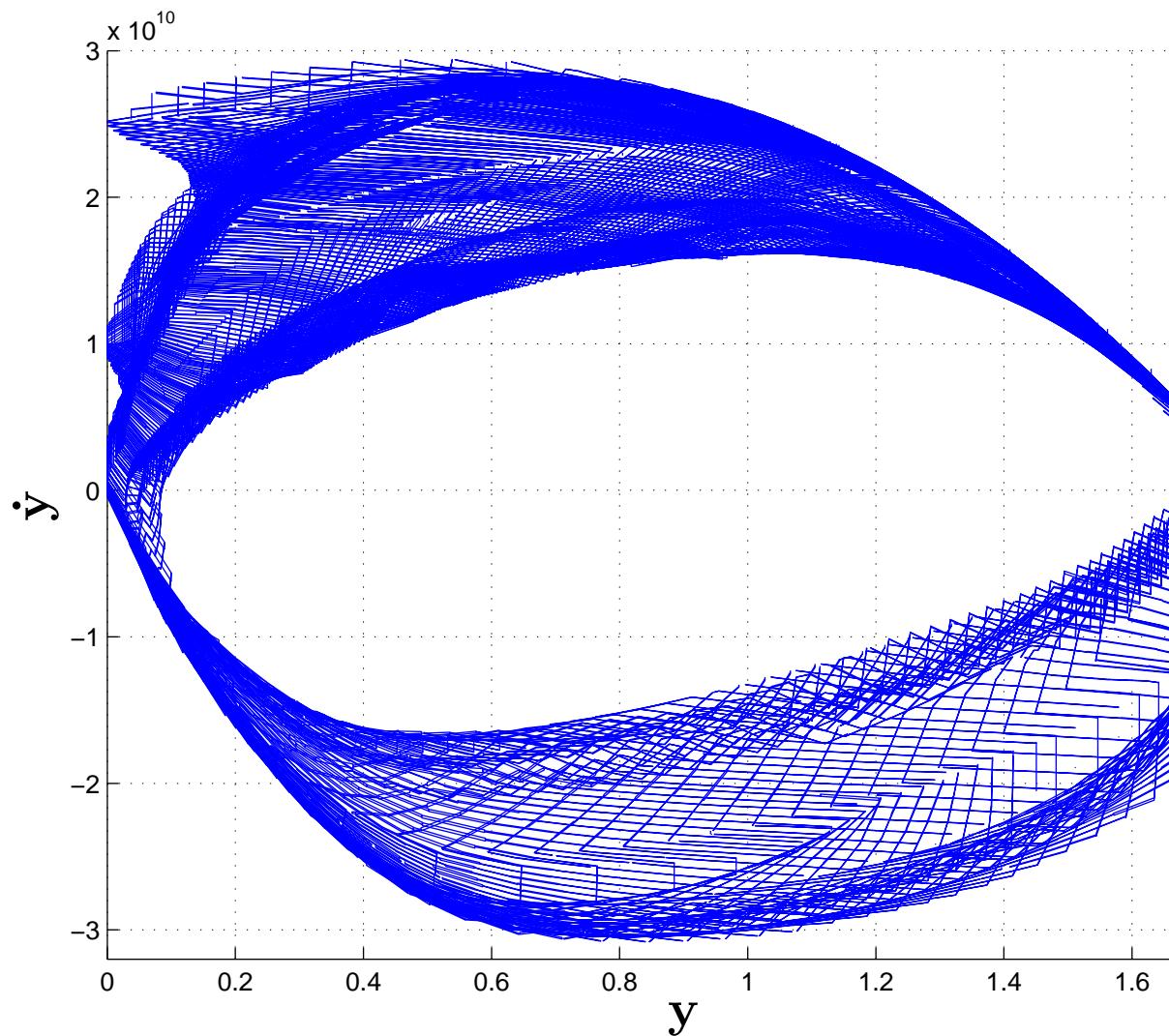
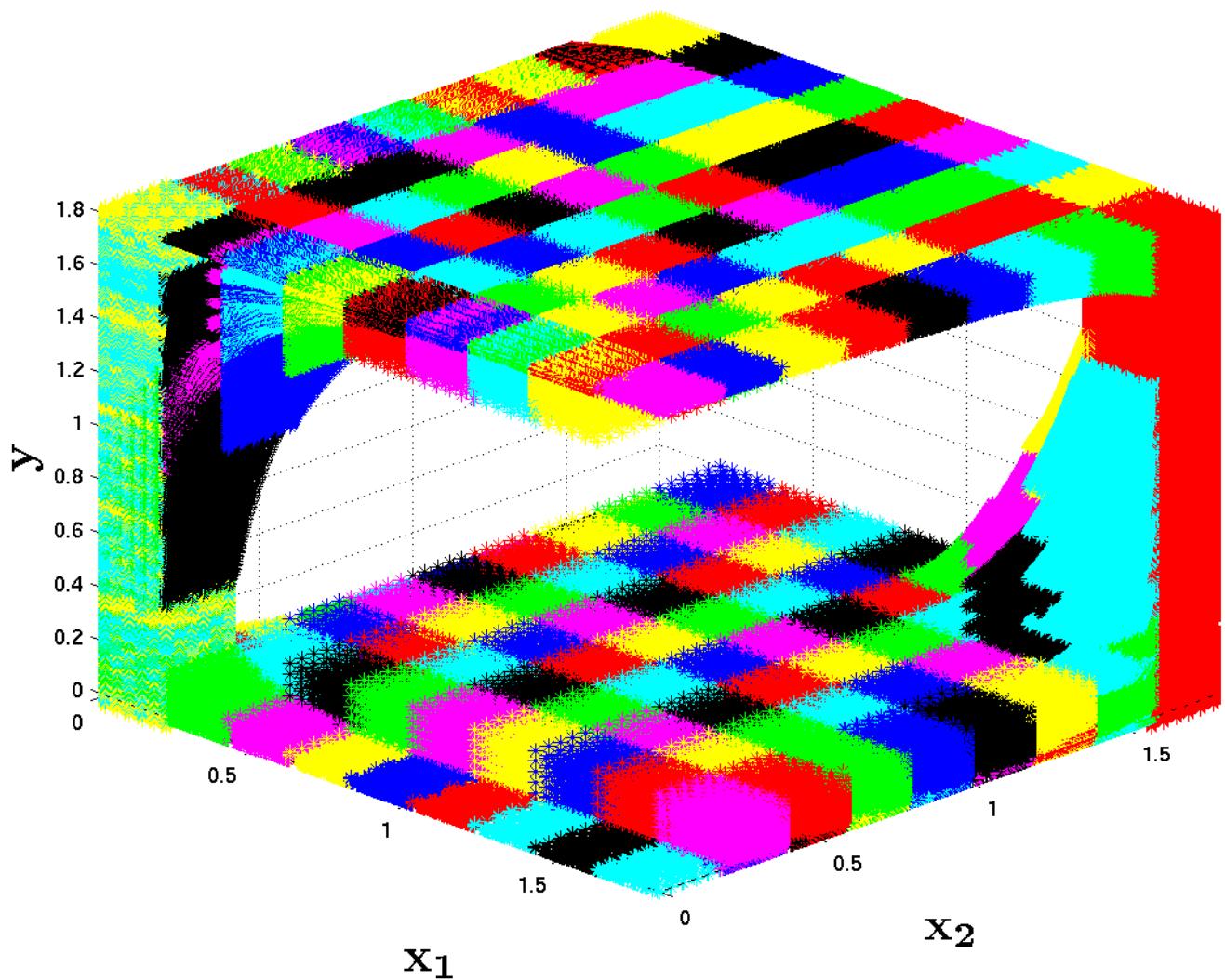


Figure 1.78: The Brockett annulus

Figure 1.79: The Reachable Space of  $y$

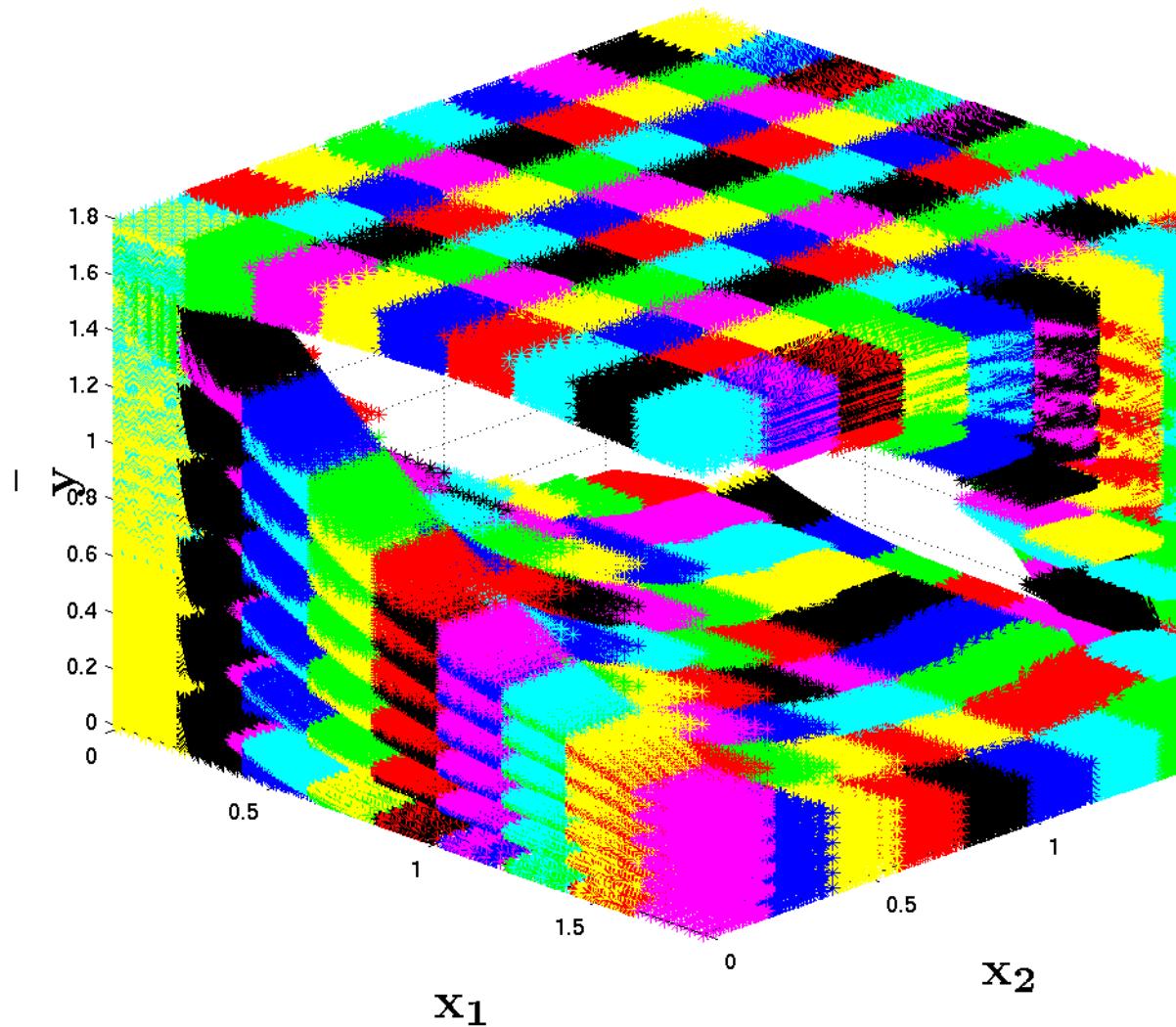


Figure 1.80: The Reachable Space of  $\bar{y}$