COMP2611 Fall 2018 Homework #1

Note:

1. **The due date is 5pm Monday, Oct 8.**
2. **Work out your solution either by typing or handwriting.**
3. **Take photos of the solution before submission.**
4. **Submit a hard copy to COMP2611 assignment collection box. The box is in a <u>big blue metal cabinet</u> located in the CSE lab area, in the corridor of lift 21 opposing the male-toilet close to lift 21. There are assignment collection boxes for other courses nearby, make sure you submit to the COMP2611 box.**

Question 1: Data representation (16 points)

a) Given the following **signed integer values**, write their corresponding 16-bit 2's complement representations and decimal values. (4 points)

I. **$E0B7_{(16)}$**:

2's complement =

Decimal =

II. **$146_{(10)}$**:

2's complement =

Hexadecimal =

b) Given the following **signed integer values**, write their corresponding 32-bit 2's complement representations and decimal values. (4 points)

I. **$F0D1_{(16)}$**:

2's complement =

Decimal =

II. **$-2450_{(10)}$**:

2's complement =

Hexadecimal =

c) Please give the IEEE754 single-precision representation of the following decimal number. Can the decimal number be represented precisely? If not, please find the nearest approximation of the number. Show your steps briefly. (4 points)

I. -313.3125

II. 0.095

d) What decimal values are represented by the following IEEE754 single-precision floating-point representations? Show your steps briefly. (4 points)

I. 0 1000 1011 11110000000000000000000

II. 1 1000 0001 00011000000000000000000

Question 2: Boolean algebra (8 points)

Simplify the following logic equations using the laws of Boolean algebra only. Briefly show your steps.

I. $A\overline{B}C + AB + A\overline{C} + AB\overline{C}$

II. $(AB(C + \overline{BD}) + \overline{AB})CD$

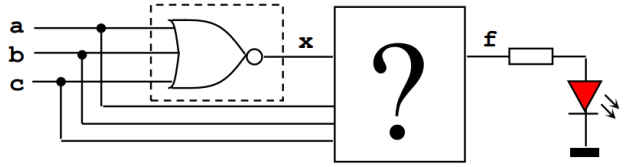
III. $B(A + \overline{C}) + A + A(\overline{A} + B)$

IV. $AB + \overline{A}C + \overline{B}C$

Question 3: Combinational Logic (14 points)

We want to design a circuit that verifies whether a 3-input NOR gate works properly or not. f ='1' (LED ON) if the NOR gate does NOT work properly.

Assumption: when the NOR gate does not work properly, it generates 1's instead of 0's and vice versa.



a) Construct the truth table for the circuit. (3 points)

Input				Output
a	**b**	**c**	**x**	**f**

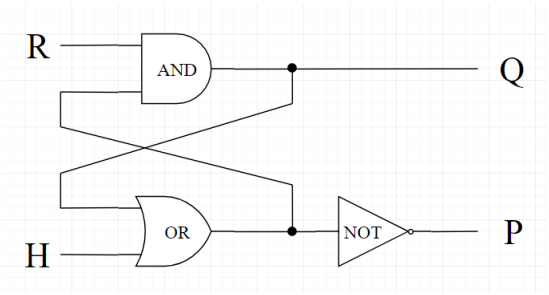
b) Derive the logic expression the corresponding logic function f (x, a, b, c), **in both Sum-of-Product** and **Product-of-Sum** format. (2 points)

c) Use K-map to simplify the SoP logic function. Write the logic function in simplest form. (5 points)

d) Implement the simplified logic function with OR gate(s) and XNOR gate(s) only.
A XNOR B = $AB + \overline{A}\,\overline{B}$.
Note: If you use other gates and your logic is correct, you will get 2 points. (4 points)

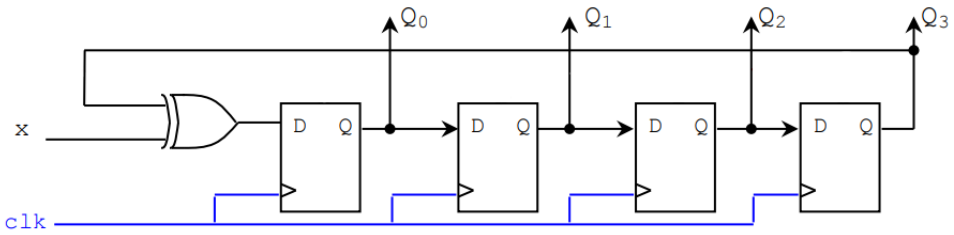
Question 4: Sequential Logic (12 points)

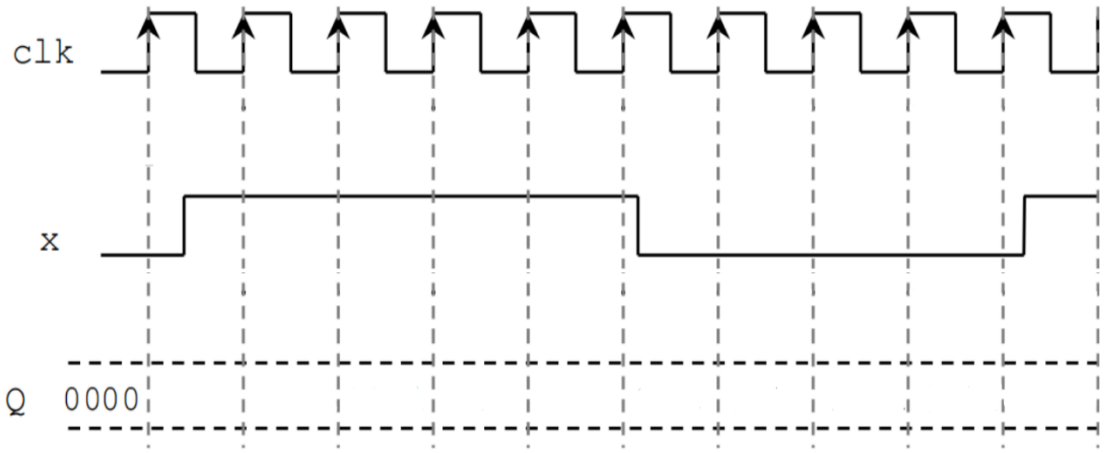
a) Fill the truth table of the given sequential circuit. Assume Q_t and Q_{t+1} are the value of output Q at clock cycle t and t+1, respectively. (4 points)



Input			Output	
R	H	Q_t	Q_{t+1}	P
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

b) The below circuit consists of an XOR gate and four rising edge-triggered D Flip-flops. Refer to the circuit and the timing diagram, write the value of Q (where $Q=Q_3Q_2Q_1Q_0$) for each clock-cycle in the timing diagram. Assume the initial Q value equals to "0000". Ignore any propagation delays. (8 points)





----------End----------