

# ***LCFC Confidential***


## ***RAVEN EX85 Rev0.1 Schematic***

***AMD Raven Ridge FP5 Processor with DDR4***

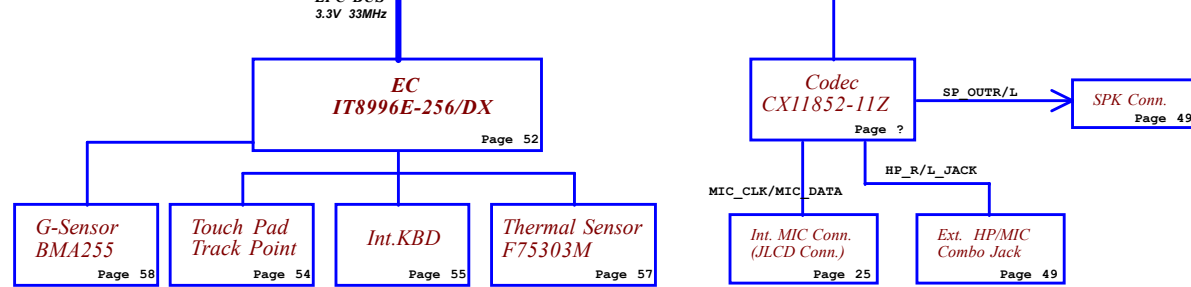
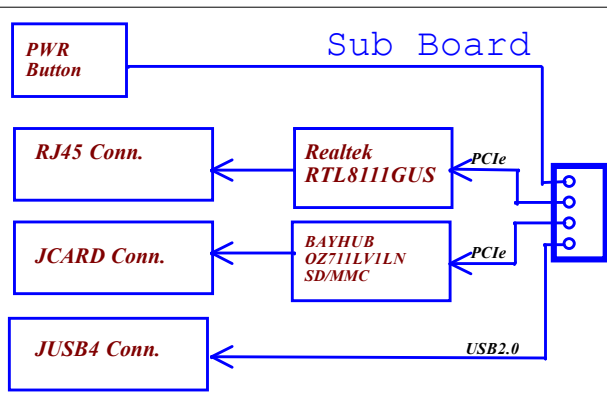
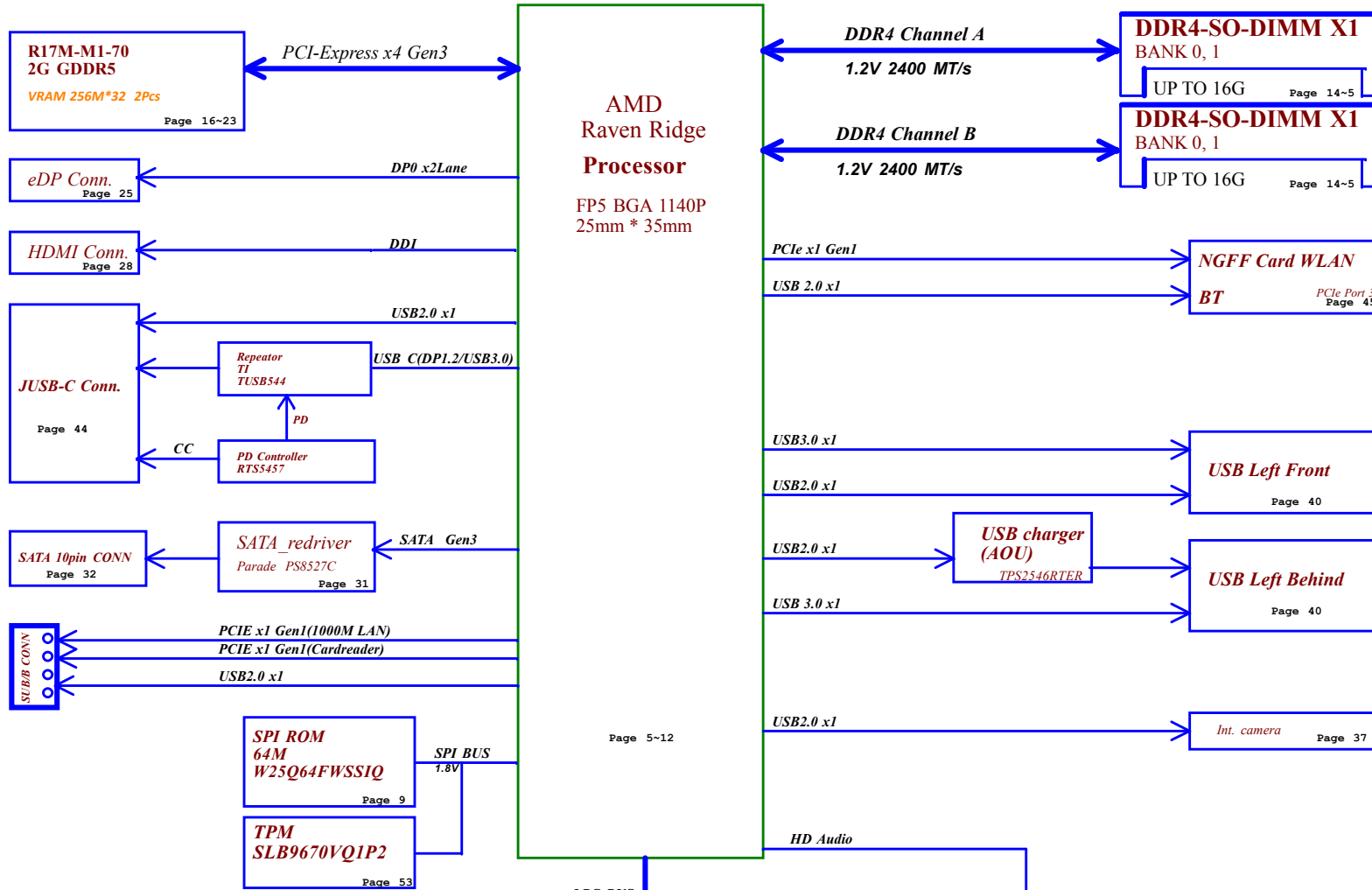
***R17M-M1-70 with DDR5 2GB***

***2017-3-30 Rev0.1***

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				<small>Rev</small> SDV	



# AMD Raven Ridge FP5



Voltage Rails ( O --> Means ON , X --> Means OFF )

Power Plane				+5VS +3VS +1.5VS +0.9VS_VDDP +0.6VS +VDDCR_SOC +VDDC_VDD +VGA_CORE +3.3VGS +1.8VGS +1.35VGS +0.95VGS
State	B9+	+3VALW  +5VALW  +1.8VALW +0.9VALW_VDDP	+1.2V   +2.5V	
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE	SIGNAL	SLP_A#	SLP_S3#		SLP_S5#	EC_ON	SUSP#
S0		HIGH	HIGH		HIGH	ON	ON
S3 (Suspend to RAM)		LOW	LOW		HIGH	ON	OFF
S4 (Suspend to Disk)		LOW	LOW		HIGH	ON	OFF
S5 (Soft OFF)		LOW	LOW		LOW	ON	OFF

USB2 Port

Port	Device
0	USBC
1	USB3 port1
2	USB3 port2
3	USB2 port1
4	USB(WLAN)
5	Int. Camera

USB3 Port

Port	Device
0	USB Type-C
1	USB3 port1
2	USB3 port2
3	X
4	X

PCIE Port

Port	Device
0	LAN
1	CardReader
2	WLAN
3	X
4	X
5	X
GFX0	GPU
GFX1	GPU
GFX2	GPU
GFX3	GPU

SATA Port

Port	Device
1	HDD
2	X

SMBUS Control Table


	SOURCE	Main VGA	BATT	SODIMM	WLAN WiMAX	Thermal Sensor	APU	CP Module	Charge	PD	G-Sensor	PMIC
EC_SMB_CK1 EC_SMB_DA1	IT8986F +3VL	X	V +3VL	X	X	X	X	X	V +3VL	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8986F +3VALW	X	X	X	X	X	X	X	X	V +3VALW	X	X
EC_SMB_CK3 EC_SMB_DA3	IT8986F +3VS	V +3VS_VGA	X	X	X	V +3VS	V +3VS	X	X	X	V +3VS	X
EC_SMB_CK4 EC_SMB_DA4	IT8986F +3VL	X	X	X	X	X	X	X	X	X	X	V

APU I2C

APU Port	Net	Device
I2C2_SCL/SDA	APU_SMB0CLK/SDA	DIMM1/DIMM2
I2C3_SCL/SDA	APU_SMB1_CLK/SDA	TOUCHPAD
SIC/SID	EC_SMB_CK3/DA3	Conn EC
USBC_I2C_SCL/SDA	EC_SMB_CK2/DA2	PD




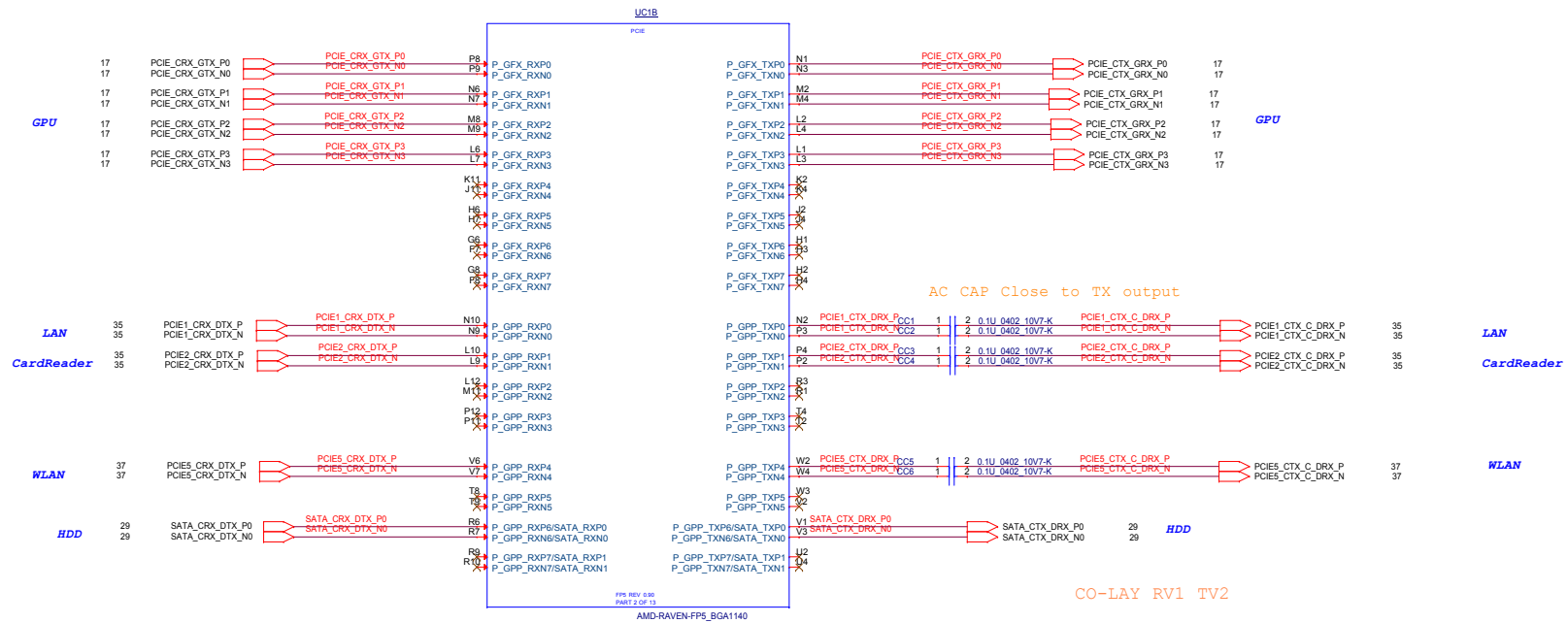
APPLY PCB PN

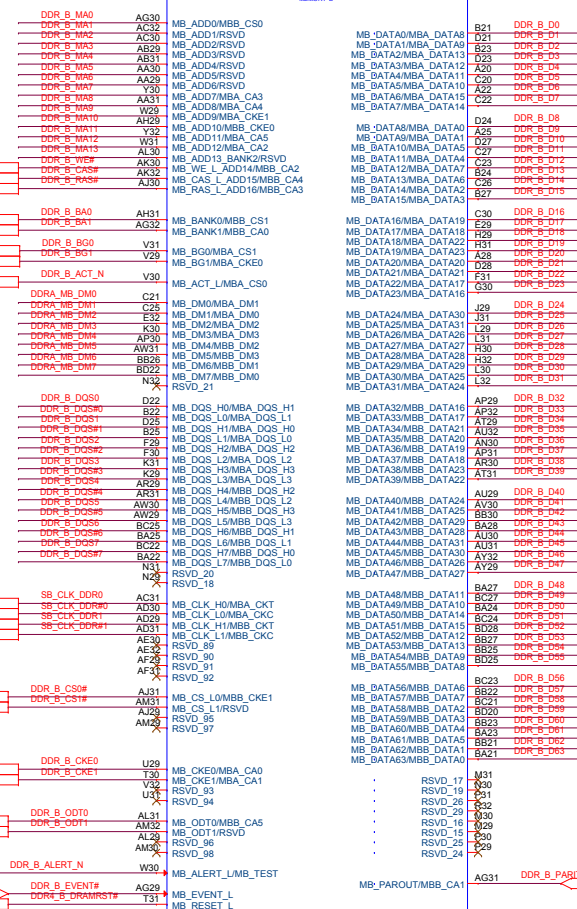
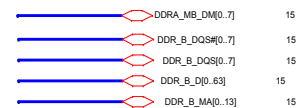
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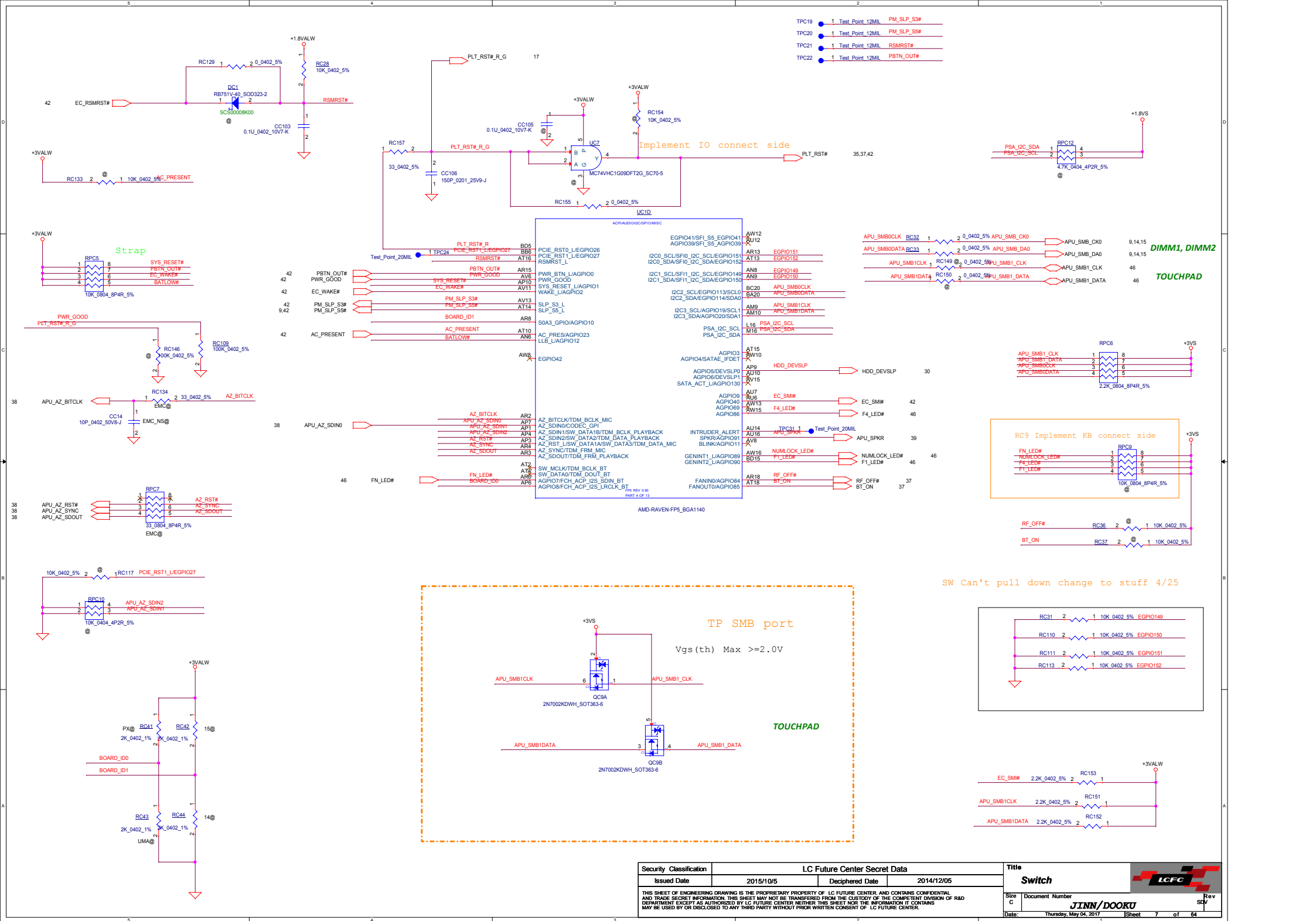
BOM Structure Table

BOM Structure	NOTE
HDT@	For HDT AMD debug port
LPC@	For LPC AMD debug port
PX@	For GPU function
X76@	GPU VRAM Setting
TPM@	Trusted Platform Module (TPM)
UMA@	UMA SKU ID
CD@	COST DOWN
EMC_NS@	EMC Reserves
ME@	ME Connector
RF@	For RF function
EMC@	For EMI function
RF_NS@	reserves RF component
RF_PXNS@	VGA reserves RF component
14@	14 inch
15@	15 inch

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- TPC19 1 Test\_Point\_12MIL PM\_SLP\_S3#
- TPC20 1 Test\_Point\_12MIL PM\_SLP\_S5#
- TPC21 1 Test\_Point\_12MIL RSMRST#
- TPC22 1 Test\_Point\_12MIL PBTN\_OUT#

DIMM1, DIMM2

TOUCHPAD

TP SMB port

Vgs(th) Max >=2.0V

TOUCHPAD

SW Can't pull down change to stuff 4/25

DP0-EDP

HDMI

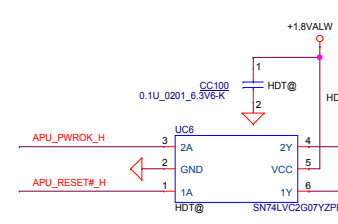
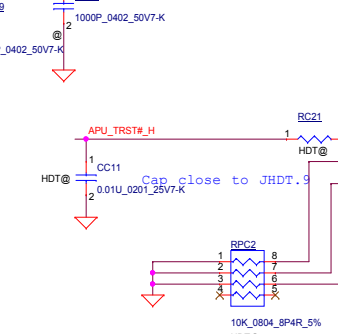
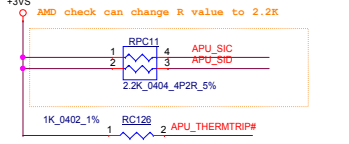
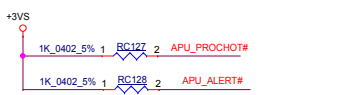
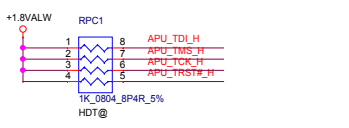
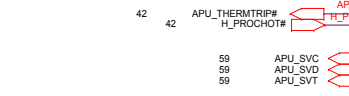
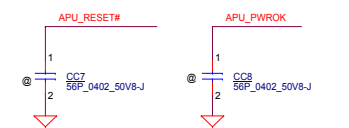
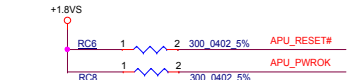
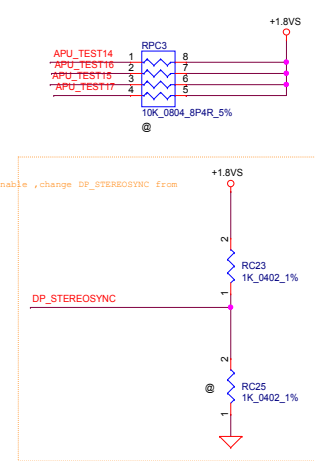
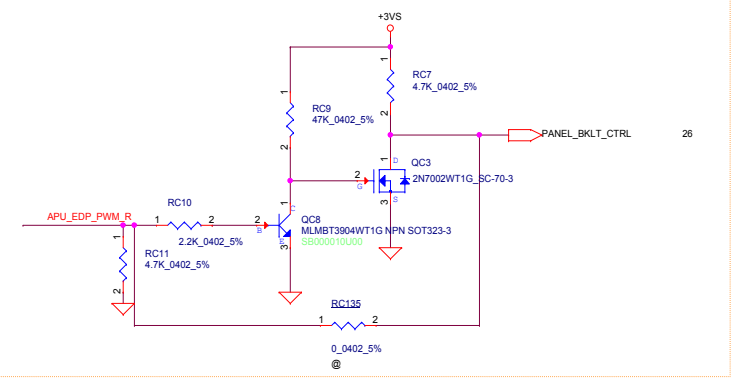
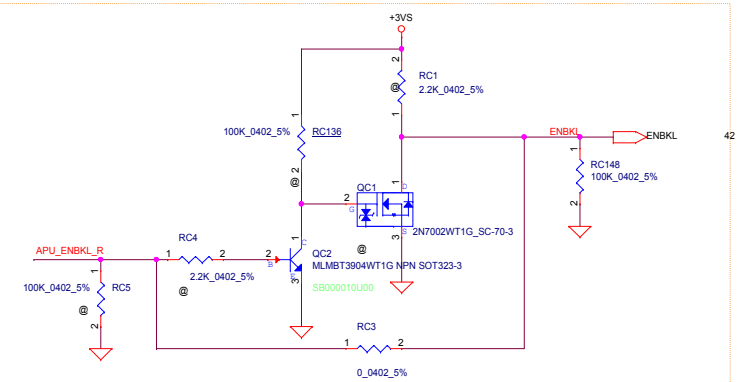
UC1C

DISPLAY/SV3/UTAG/TEST

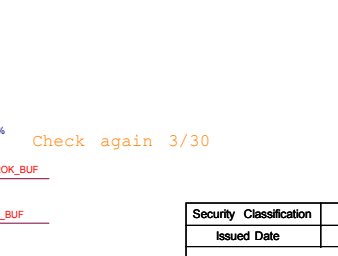
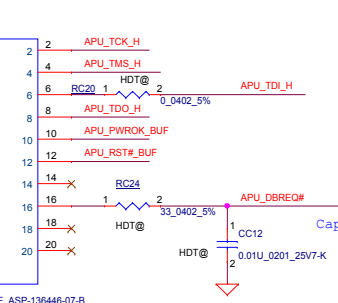
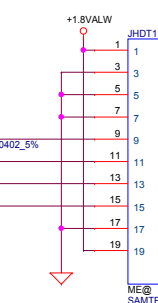
eDP

HDMI


Typec0



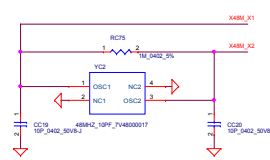
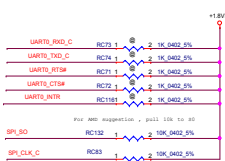
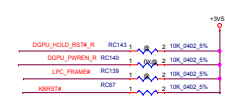
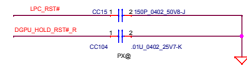
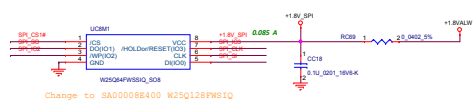
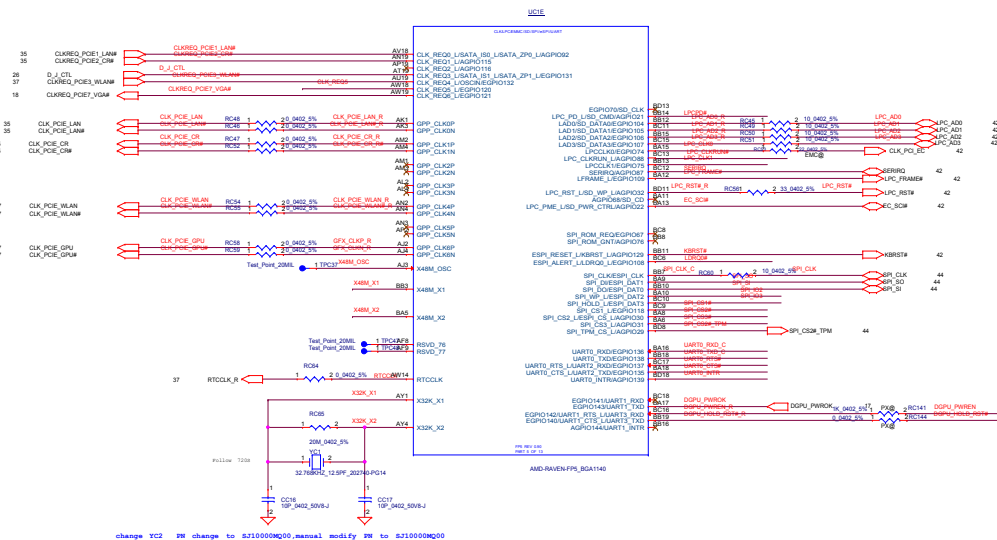
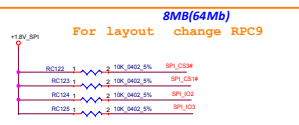
AMD-RAVEN-FP5\_BGA1140



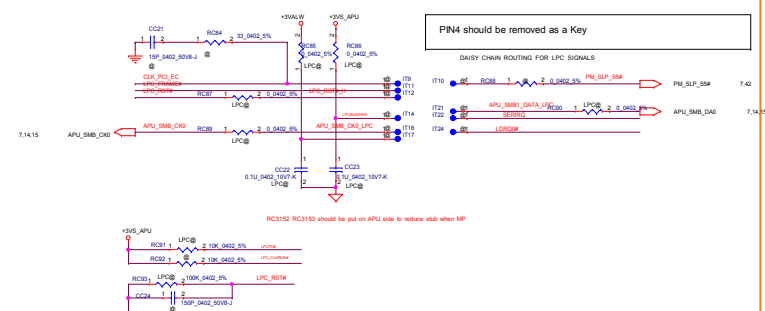
Check again 3/30

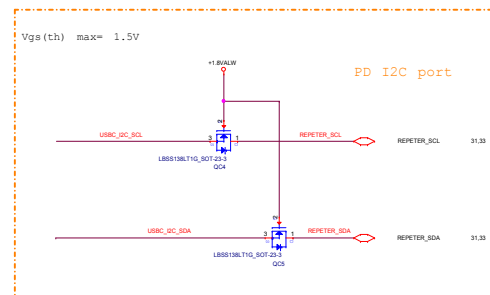
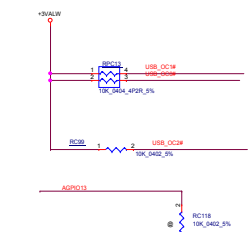
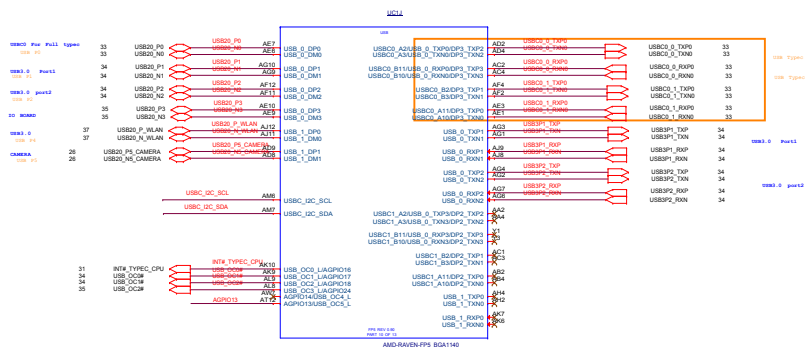
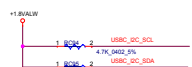
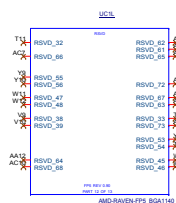
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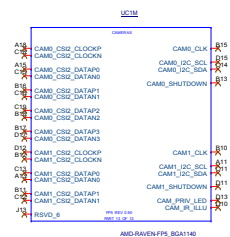



## LPC ROM EMULATOR HEADER



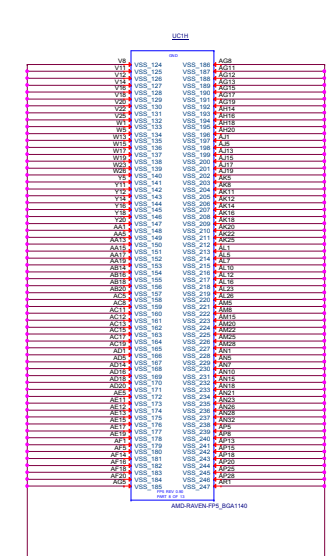
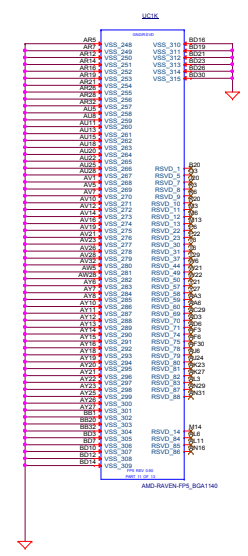
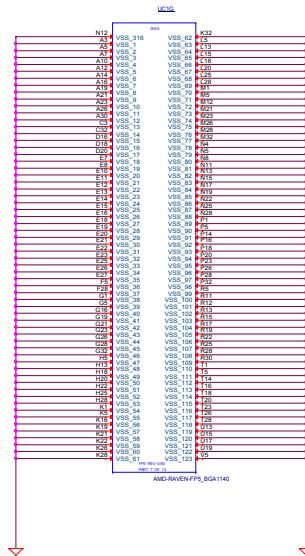


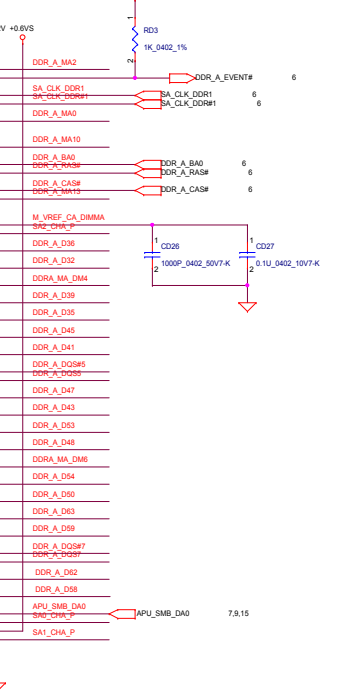
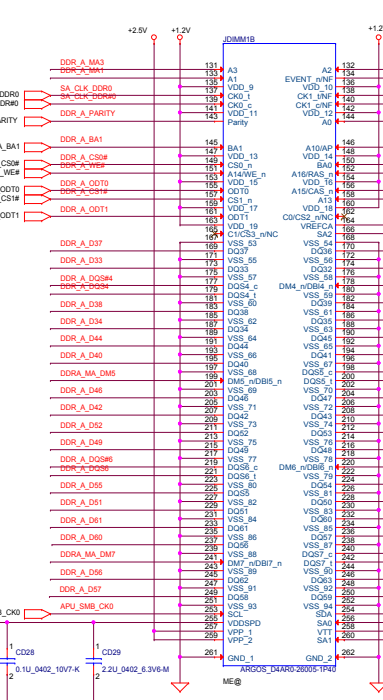
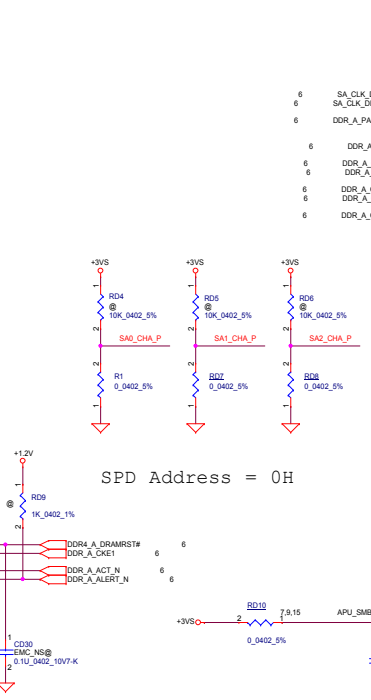
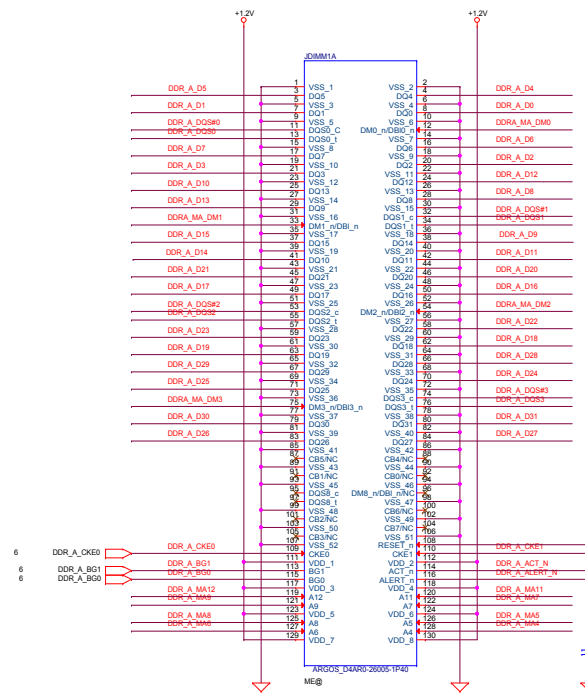
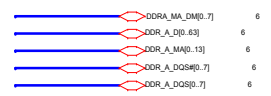
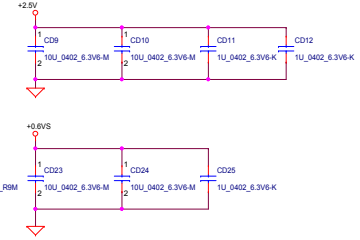
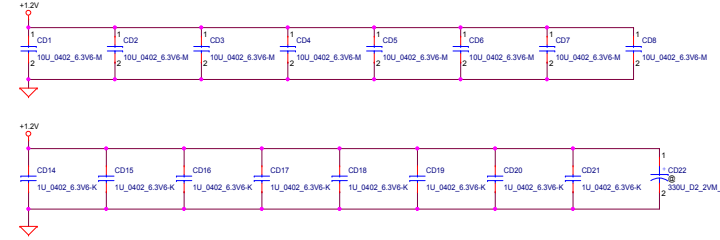
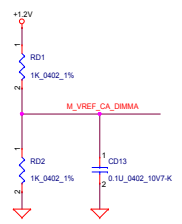
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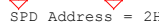
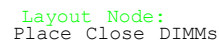
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SPD Address = 0H



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Power-Up/Down Sequence

"Topaz" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

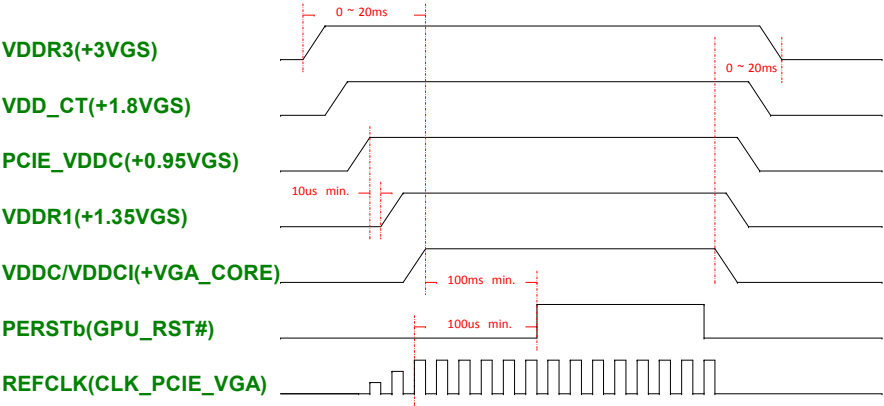
All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μ s.

It is recommended that the 3.3-V rail ramp up first.

The 3.3-V, 1.8-V, and 0.95-V rails must reach their ready state at least 10 μ s before VDDC, VDDCI, and VMEMIO start to ramp up.

The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as ≤ 50 mV/μ s)

For power down, reversing the ramp-up sequence is recommended.

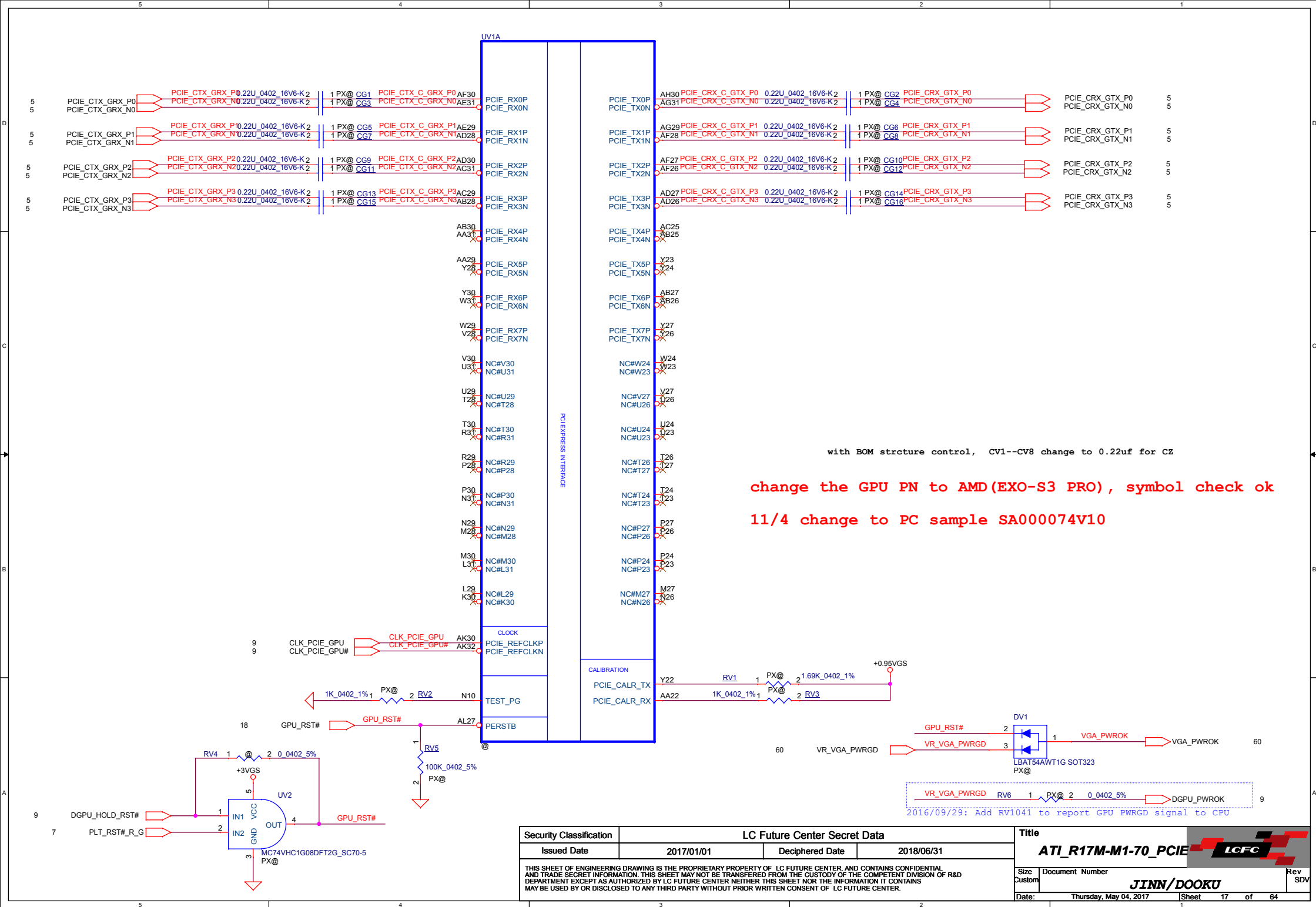


VRAM ID config

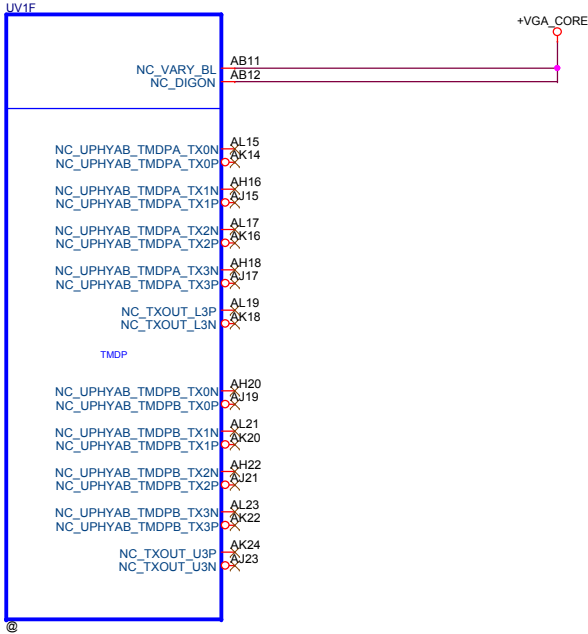
Memory Type		VRAM ID PS_3[3:1]	PU resistor RV63	PD resistor RV70
		100	4.53K	4.99K
		111	4.75K	NC
		110	3.4K	10K
8Gb GDDR5 512M x 32	Hynix H5GC8H24MJR-R0C 6.0Gbps@1.35V	000	NC	4.75K
	Micron MT51J256M32HF-70-A 6.0Gbps@1.35V	010	4.53K	2K
	Samsung K4G80325FB-HC28 6.0Gbps@1.35V	001	8.45K	2K

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Samsung K4G80325FB-HC28  
Micron MT51J256M32HF-70-A

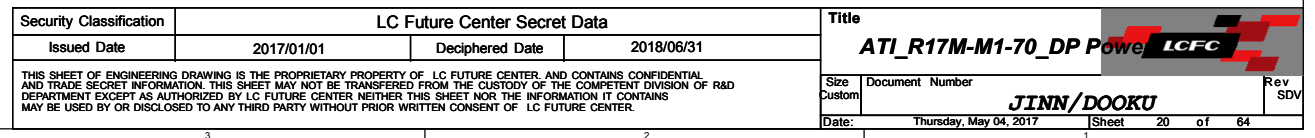




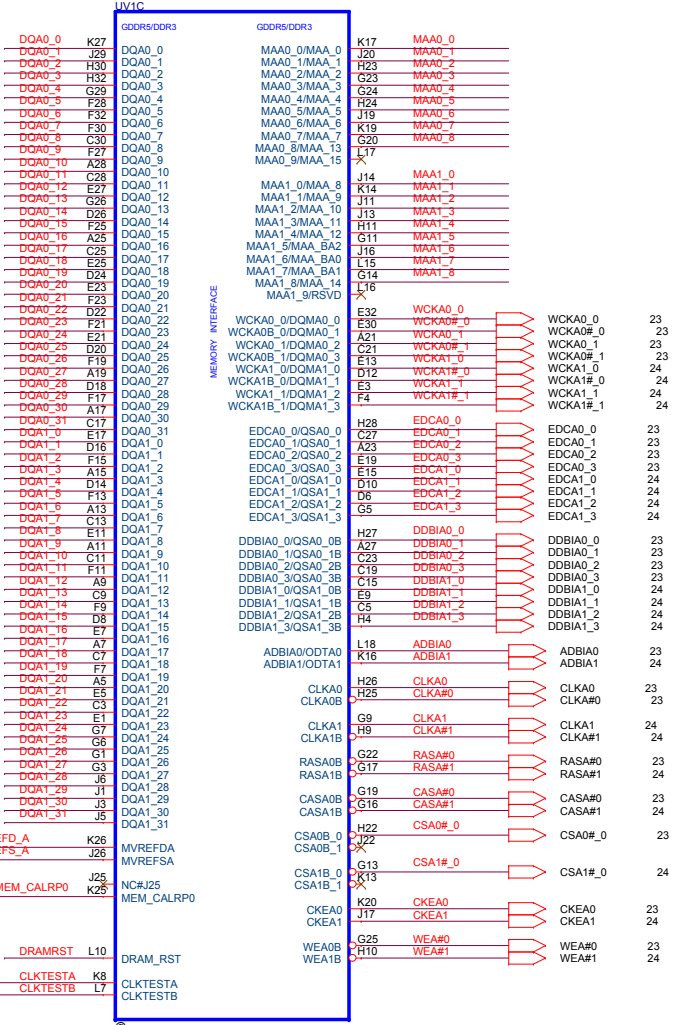
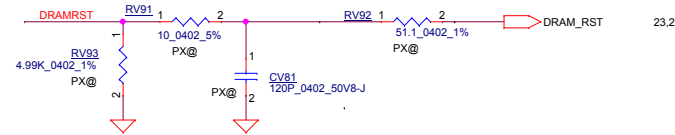
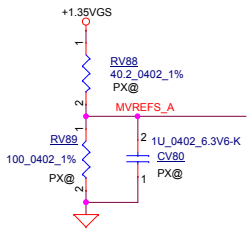
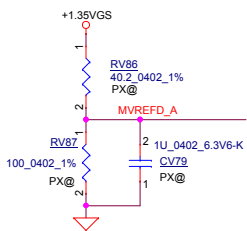
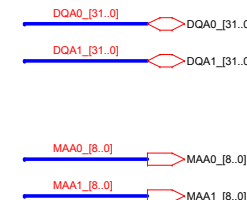





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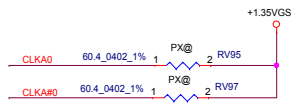
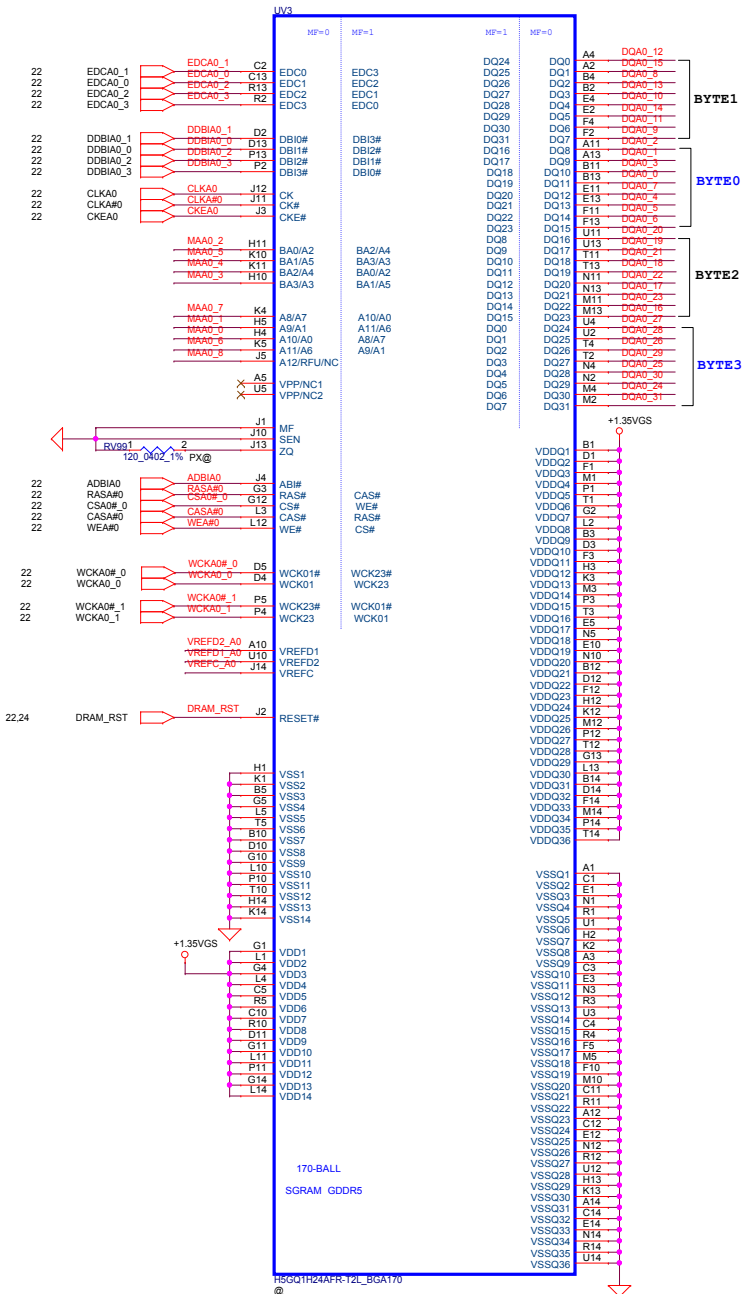
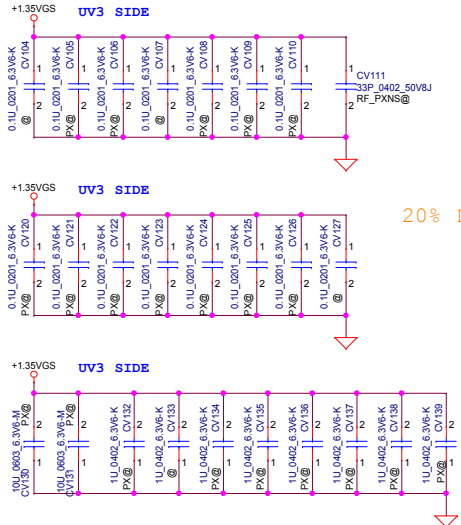
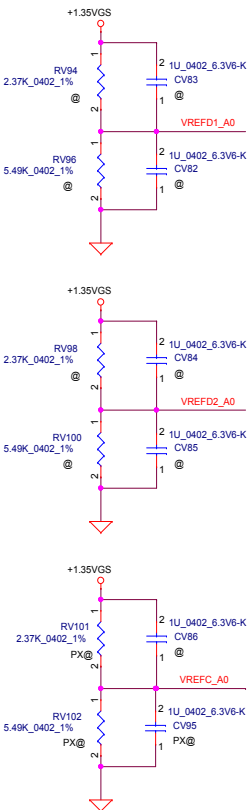


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Custom								SDV	
Date:		Thursday, May 04, 2017		Sheet		22		of 64	

Lower 32 bits



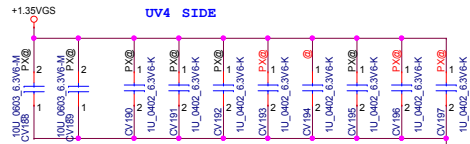
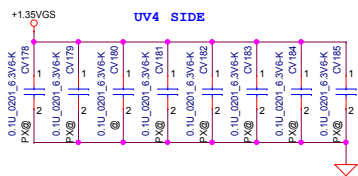
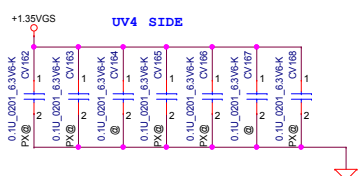
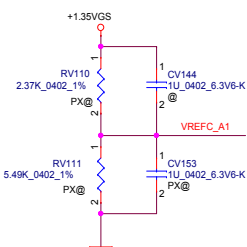
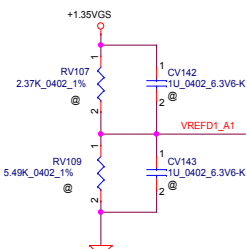
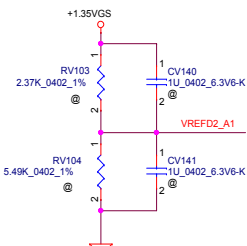
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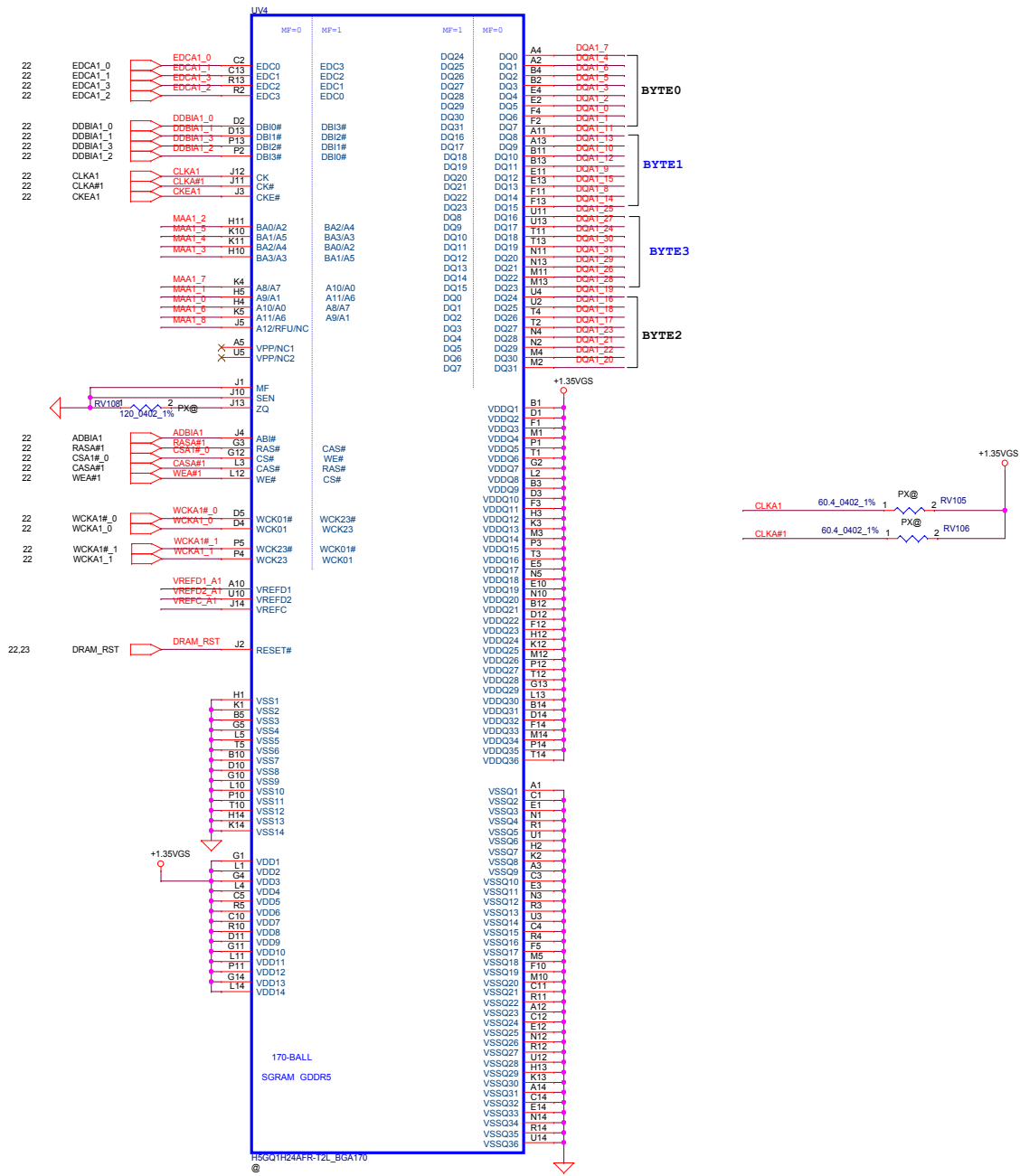
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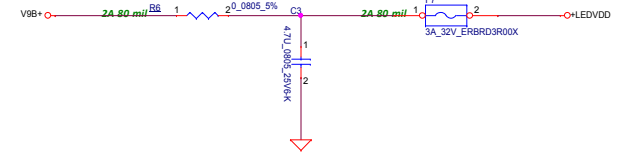
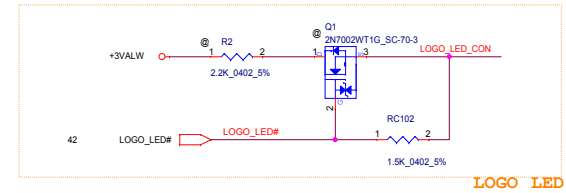
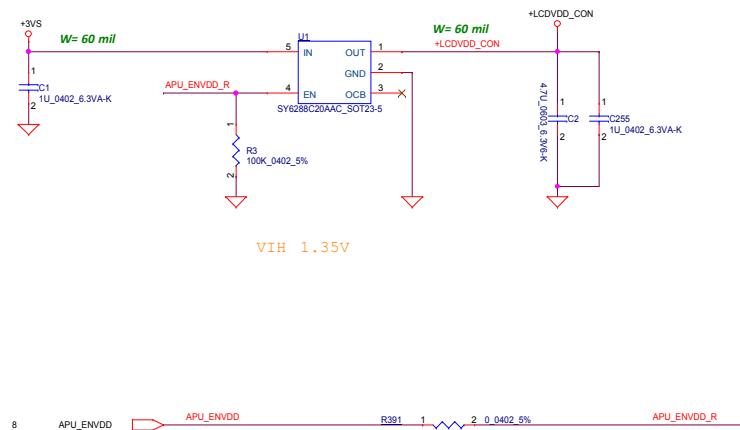
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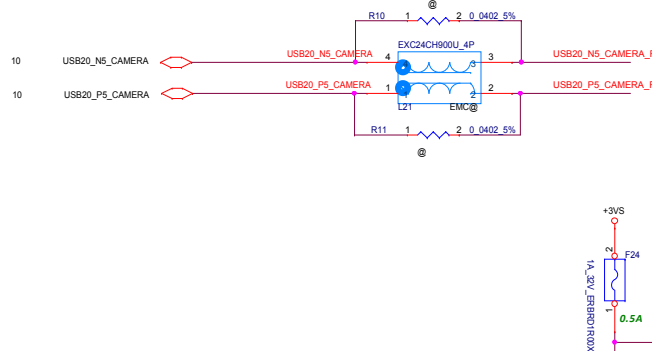
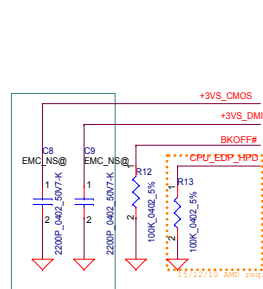
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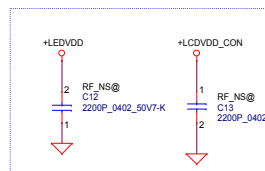
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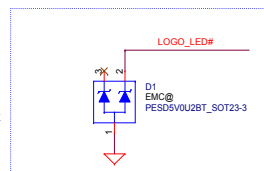
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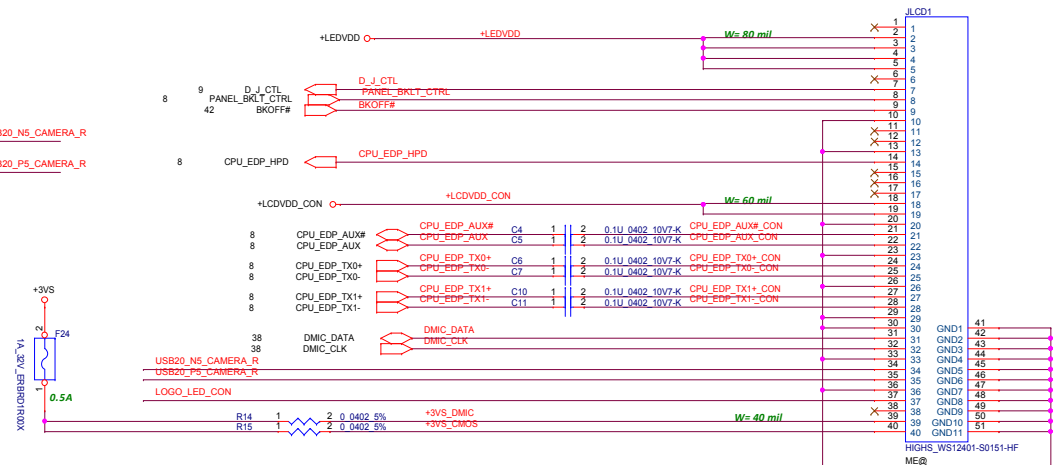
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*ESD request*

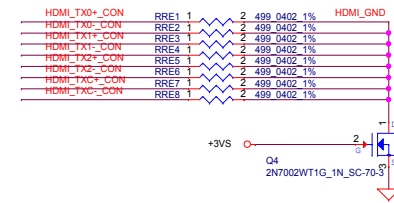
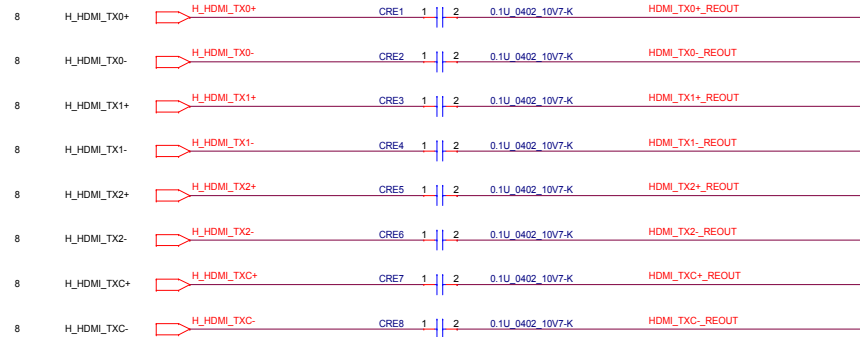
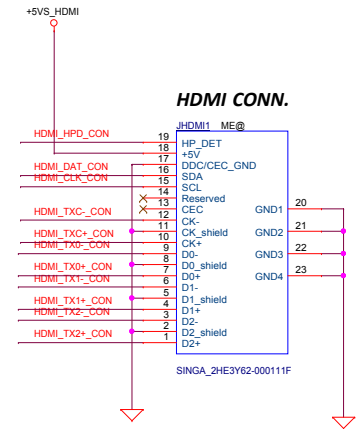
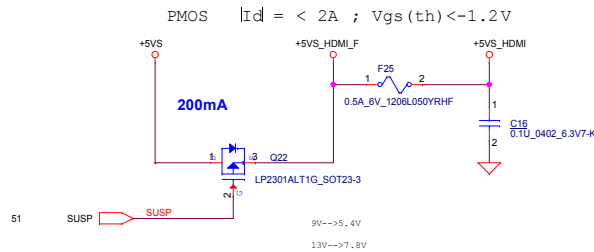
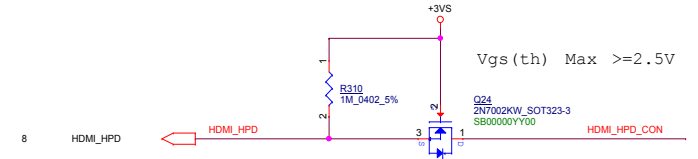
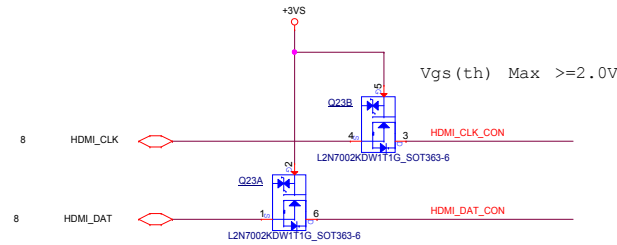
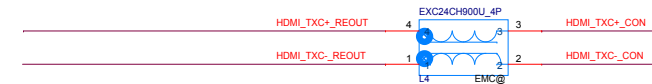
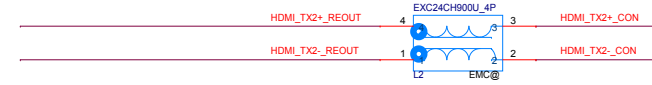
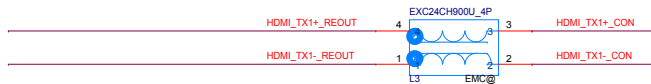
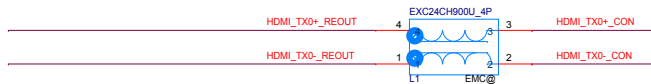
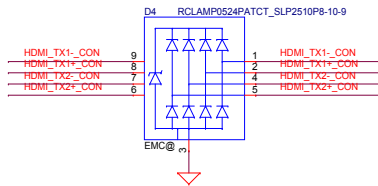
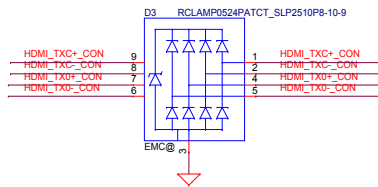
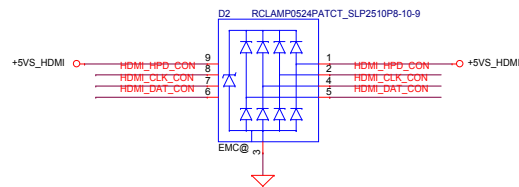
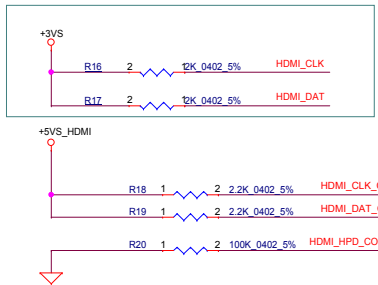


**eDP/CMOS/LOGO-LED CONN.**



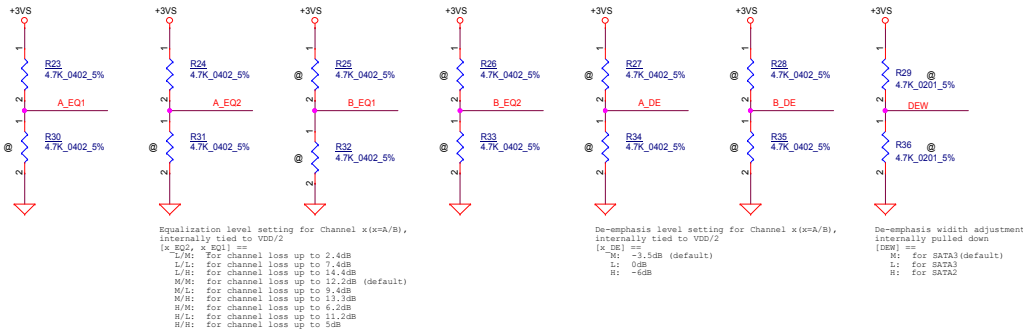
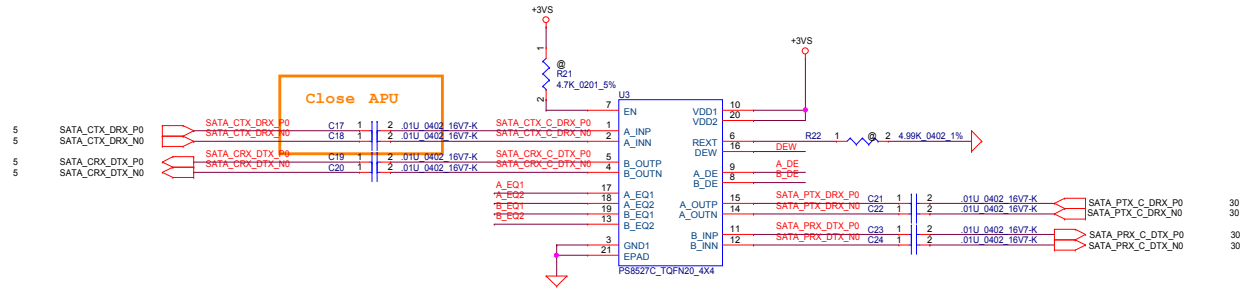
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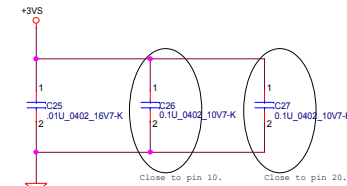


Need two gerbout about SATA redriver and no redriver 0324

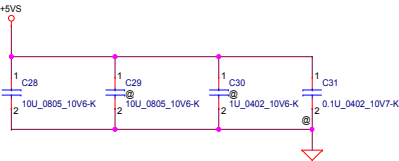
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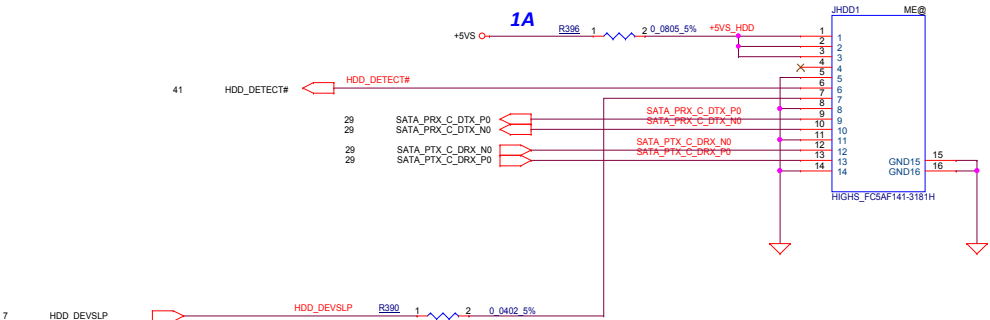
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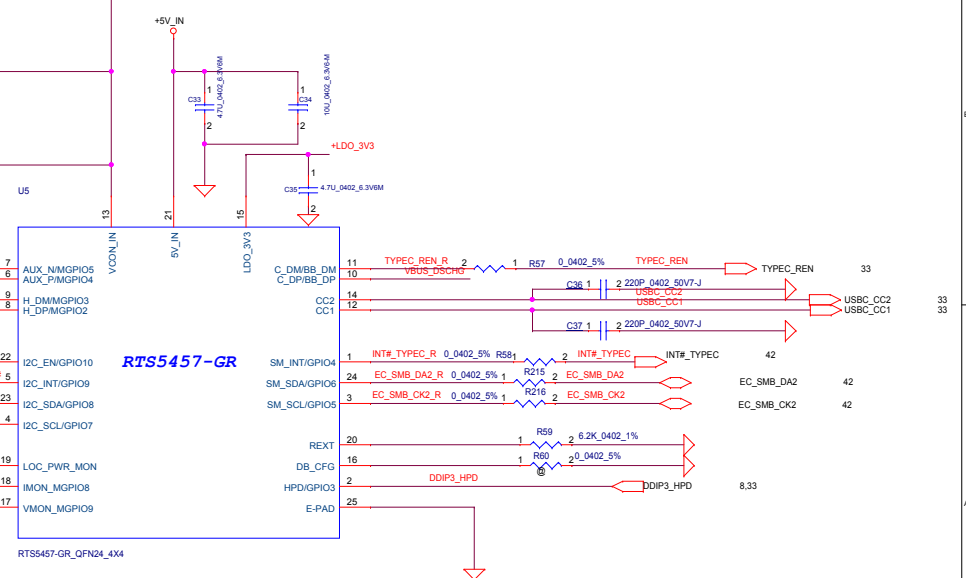
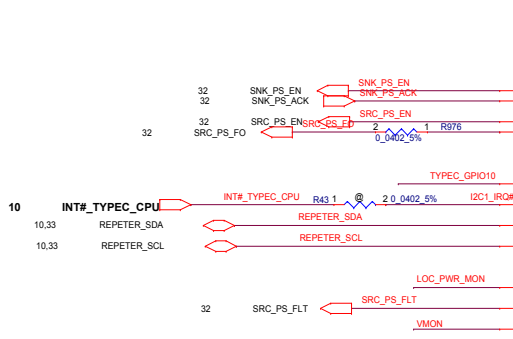
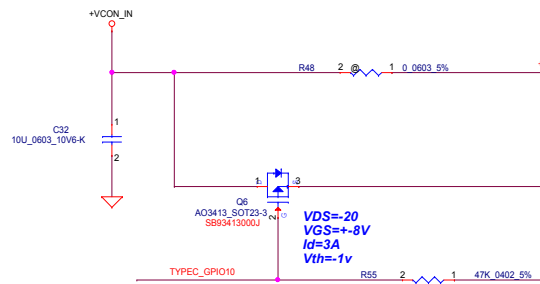
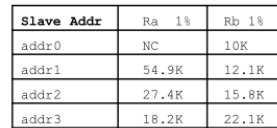


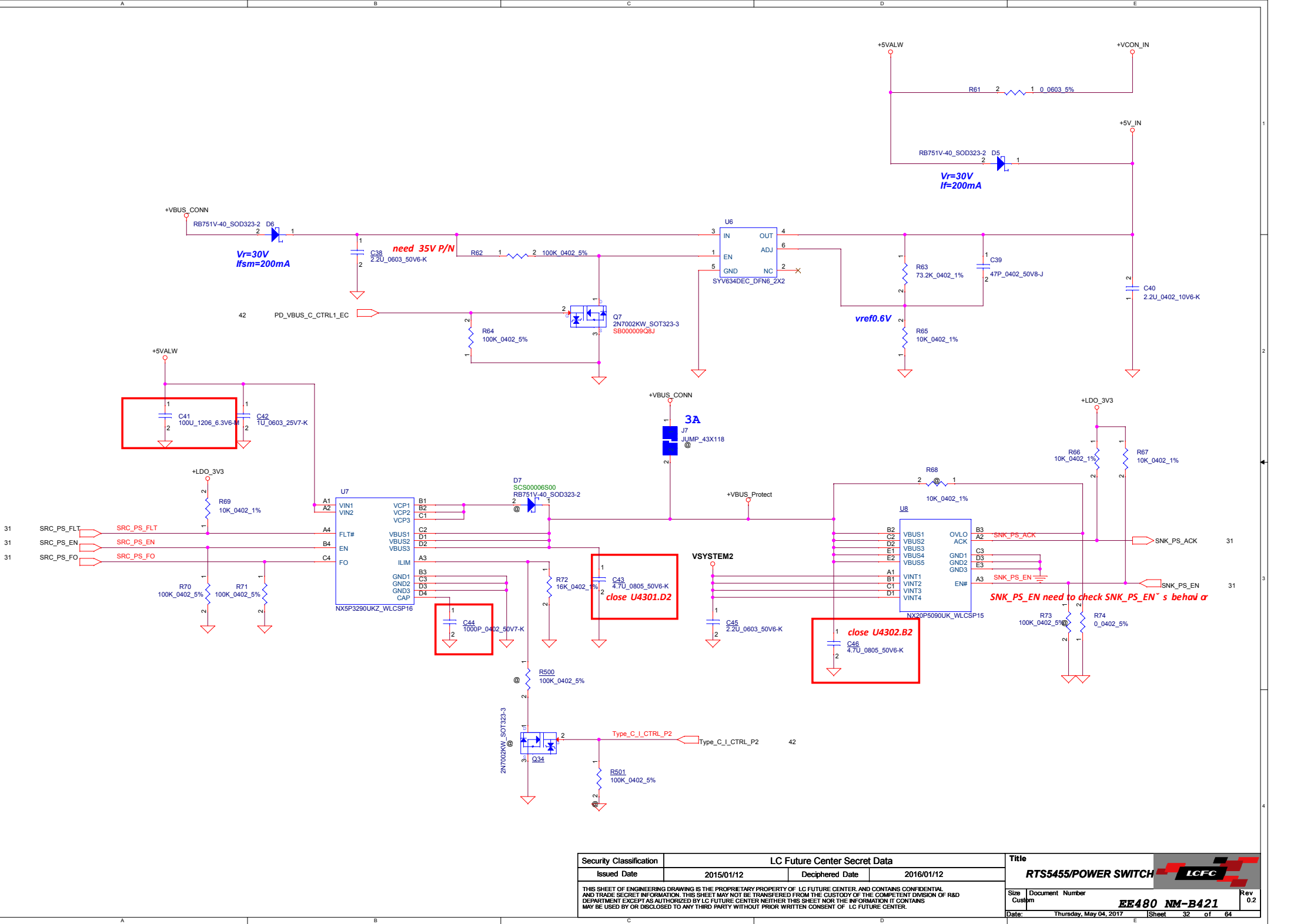
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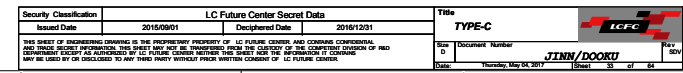
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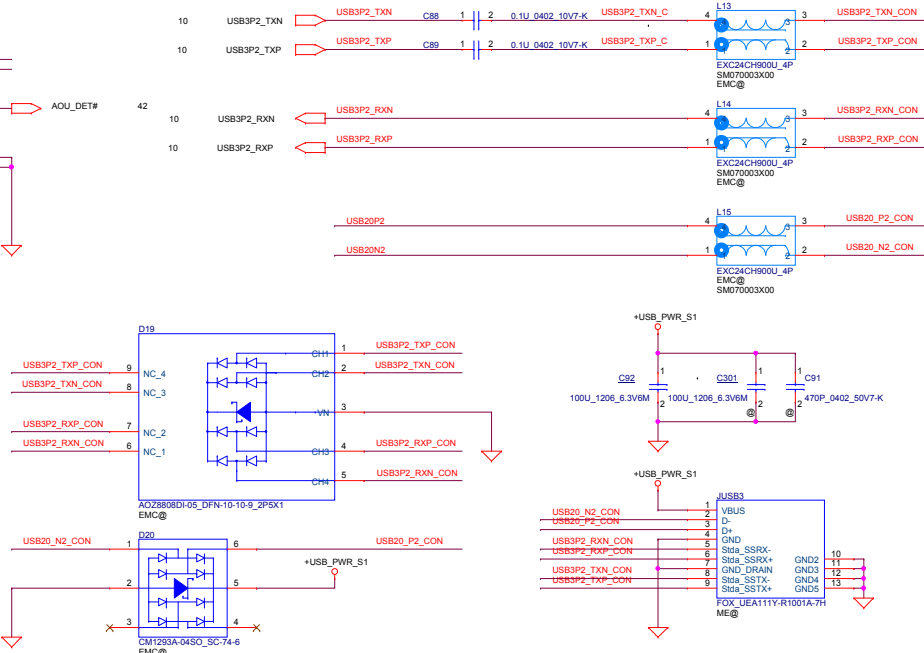
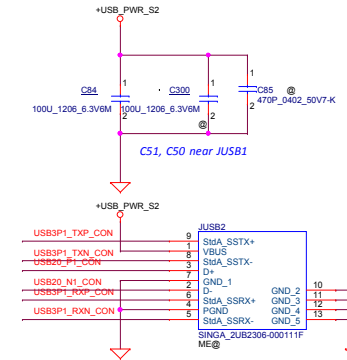








### On Board (LEFT-Back)

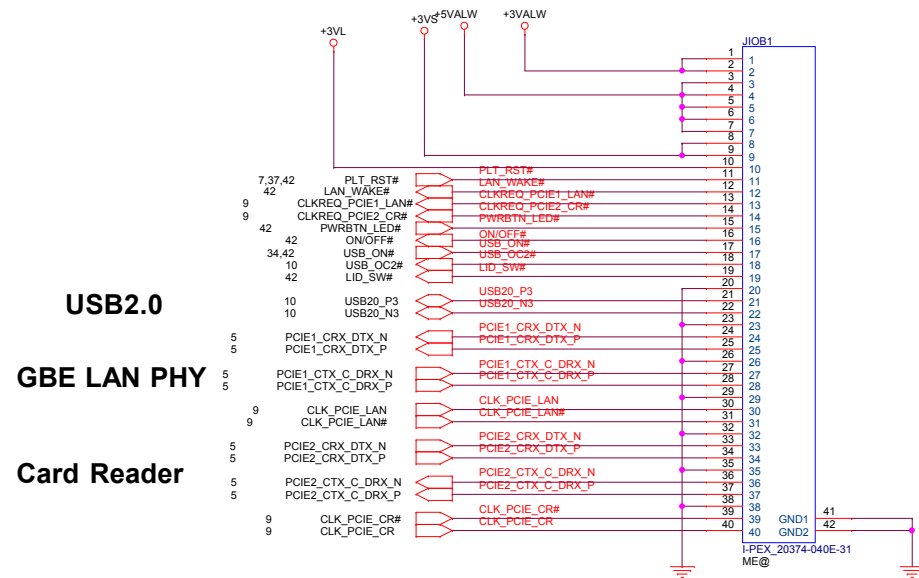



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## IO\_40\_Pin conn

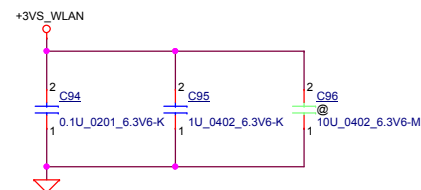
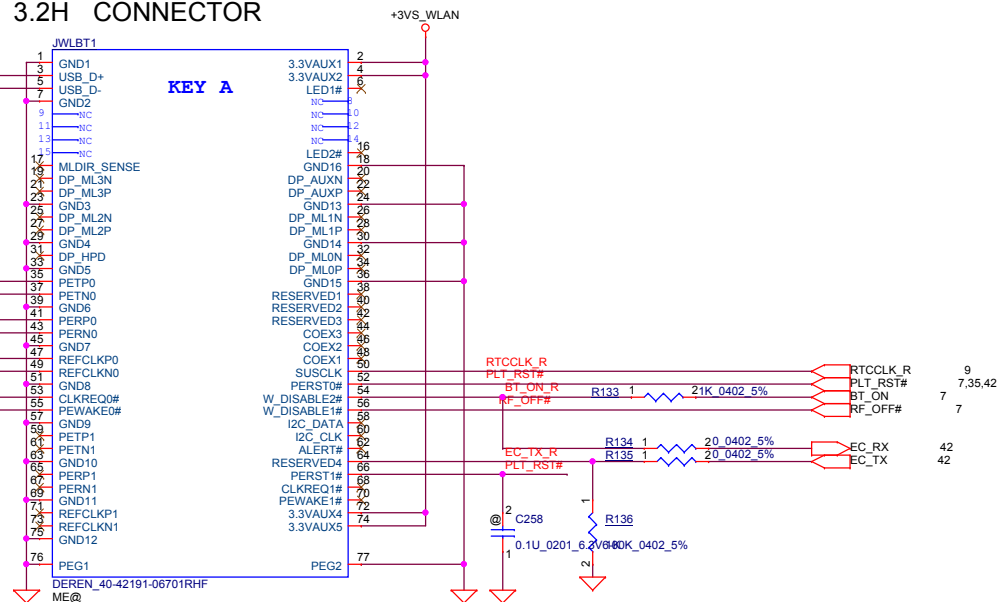



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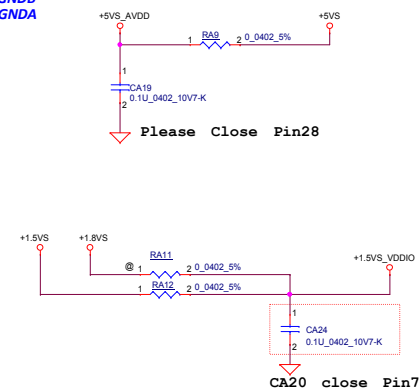
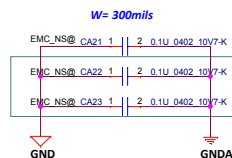
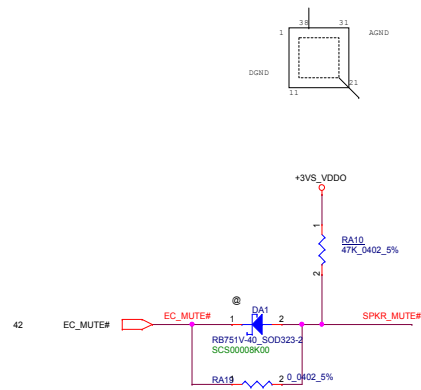
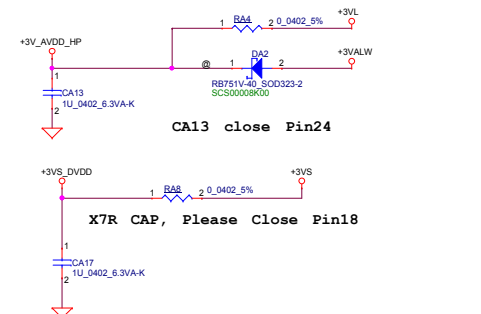
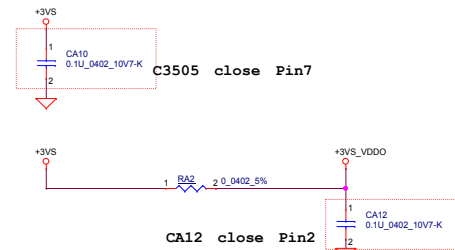


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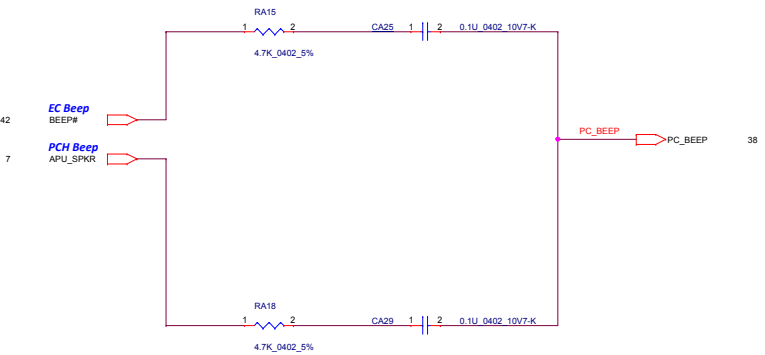
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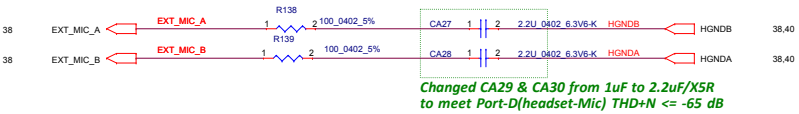
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PC BEEP

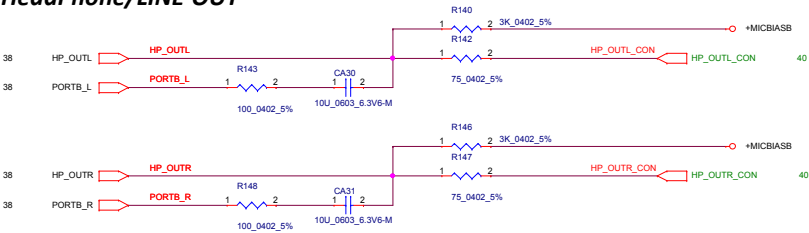


EXT. MIC/LINE IN Apple --> EXT\_MIC\_A, HGND B  
Nokia --> EXT\_MIC\_B, HGND A

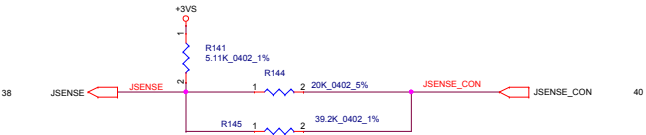


Changed CA29 & CA30 from 1uF to 2.2uF/X5R to meet Port-D(headset-Mic) THD+N <= -65 dB

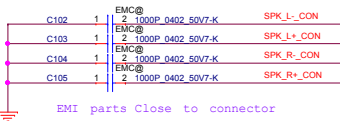
HeadPhone/LINE OUT



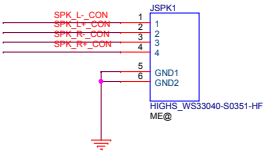
CA31, CA32 change to 4.7uF for Quality requirement



SPK CONN.

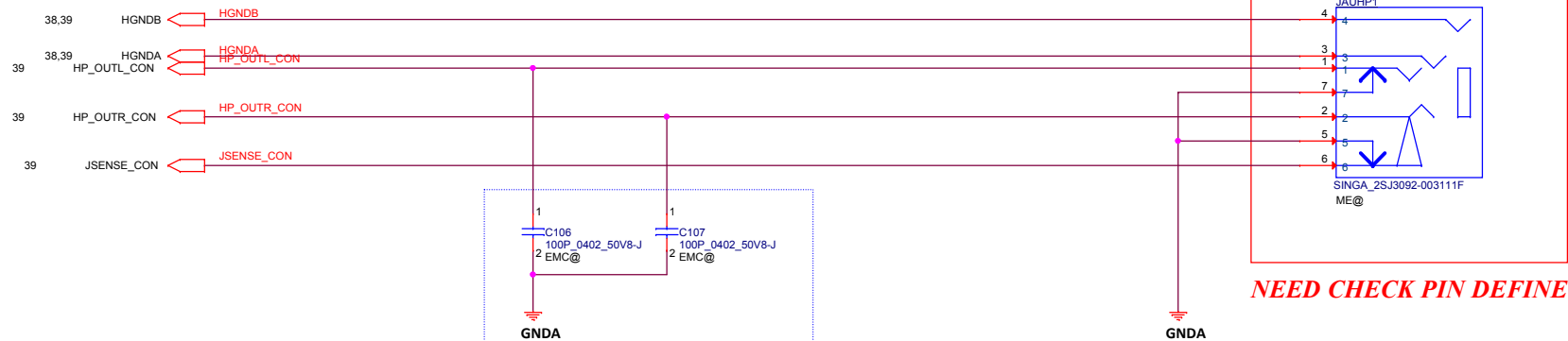


EMI parts Close to connector



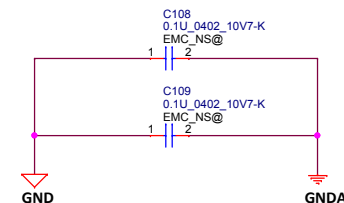
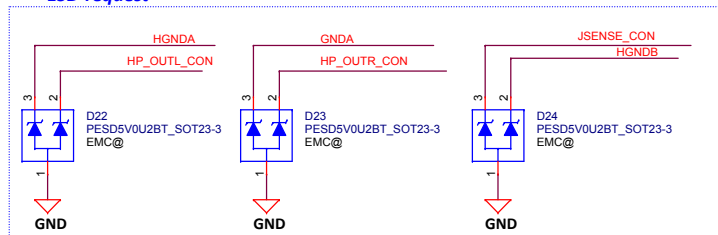
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Issued Date	2015/11/02	Deciphered Date	2015/8/10	AUDIO CONNECTOR
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				Document Number JINN/DOOKU
				Rev SDV
				Date: Thursday, May 14, 2017 Sheet 39 of 64






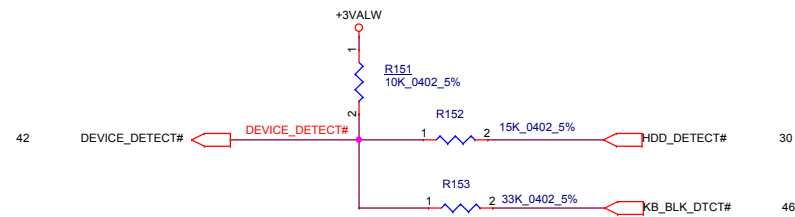
Vendor suggestion. Reserve for EMI.  
Close to JAUHP.

#### ESD request




Security Classification		LC Future Center Secret Data		Title					
Issued Date	2015/11/02	Deciphered Date	2015/8/10	AUDIO JACK SENSE					
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						Custom	JINN/DOOKU		SEV
						Date:	Thursday, May 04, 2017	Sheet	40 of 64

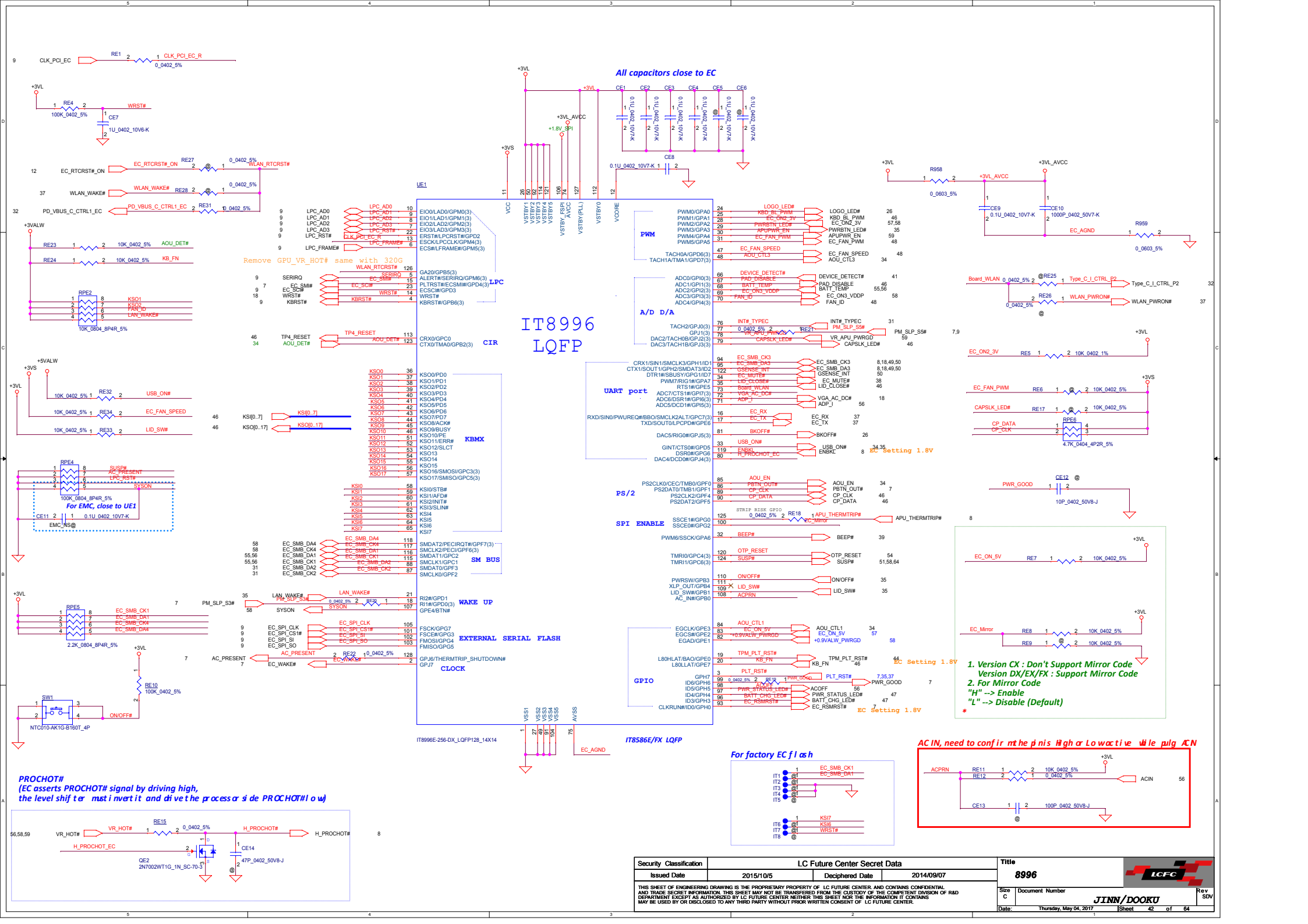




Add KB DETECT Ned check

Vcc	3.3V														
R409	10K +/- 1%														
DEVICE_DETECT1#	1.98V	1.675V	1.772V	2.759V	2.533V	3.3V	2.87V	0.26V	1.82V	2.27V	2.45V	2.00V	1.64V	1.558V	
HDD_DETECT#	V	V	V	X	X	X	X	V	V	X	X	X	V	V	
KB_BLK_DTCT#	X	V	X	X	V	X	X	V	X	V	X	V	X	V	
	X	X	V	V	X	X	X	V	X	X	V	V	V	X	
	X	X	X	X	X	X	V	X	V	V	V	V	V	V	

Security Classification	LC Future Center Secret Data			Title		
Issued Date	2015/11/02	Deciphered Date	2015/8/10	Device Detect# Table		
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				Custom	JINN/DOOKU	SEV
				Date:	Thursday, May 04, 2017	Sheet 41 of 64

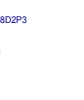
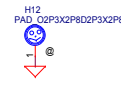


## Screw Hole

**CPU**



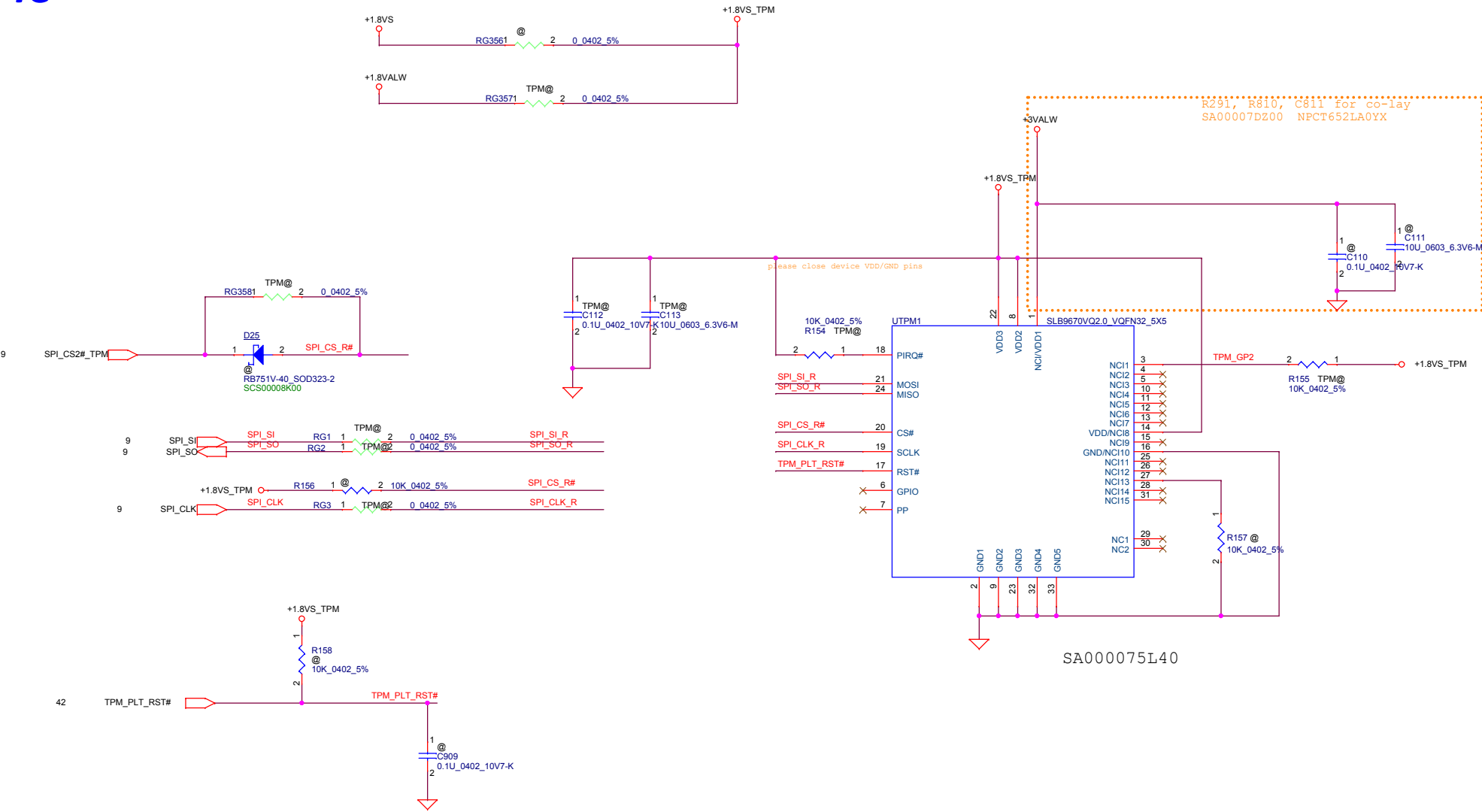
**WLNN**



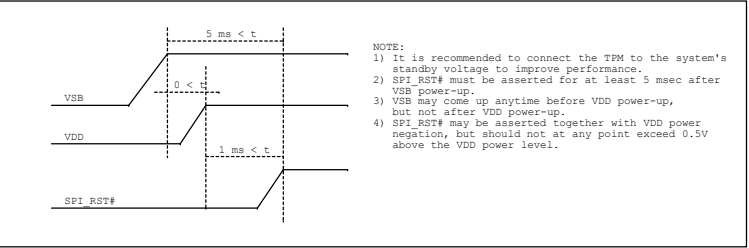
## PCB Federal Mark PAD



TPM IC

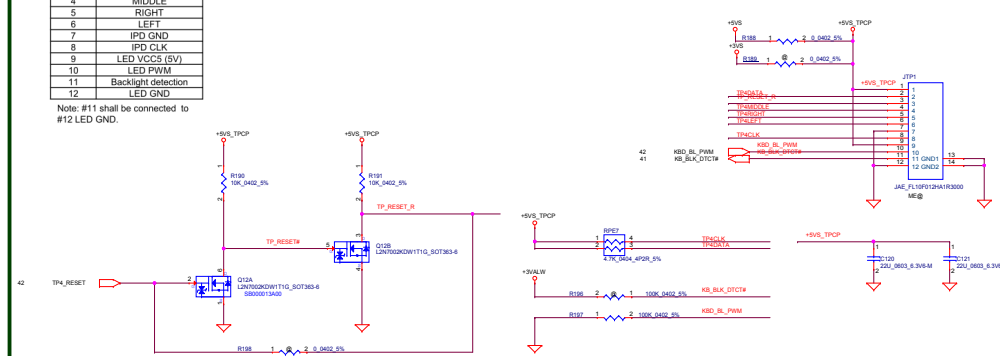
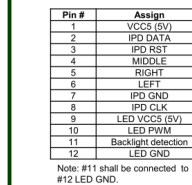
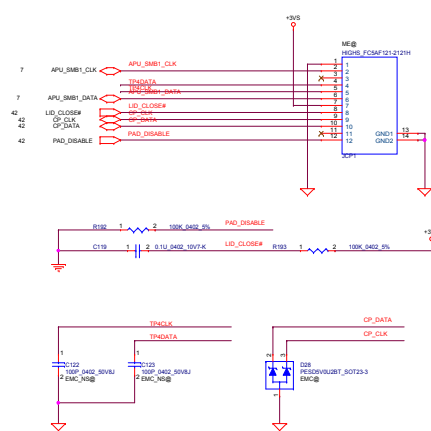
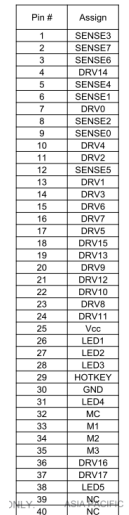
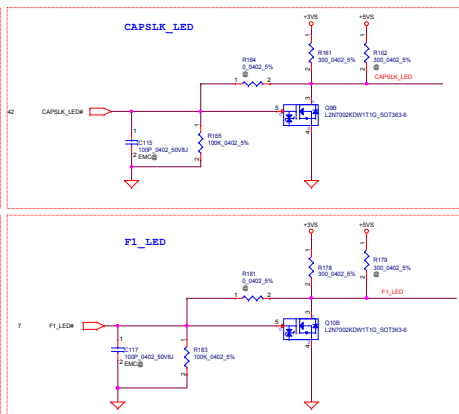


NOTE:  
Check timing sequence in SDV phase.

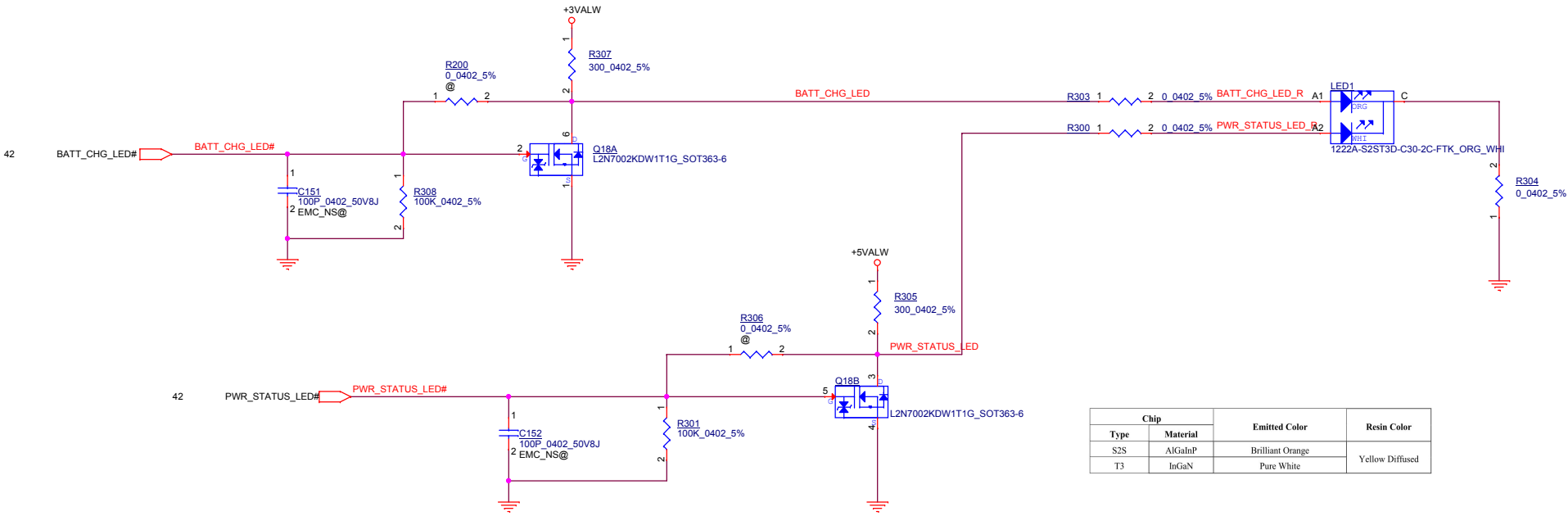


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				Date:	Thursday, May 04, 2017
				Sheet	44 of 64
				Rev	SDV





POWER ADAPTER Bi-COLOR (ORANGE/WHITE)



40mil

R201  
0\_0603\_5%

+5VS\_FAN

EC\_FAN\_PWM

EC\_FAN\_SPEED

FAN\_ID

JFAN1

GND2

GND1

5


4

3

2

1

HIGHS\_WS33050-S0351-HF  
ME@

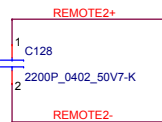
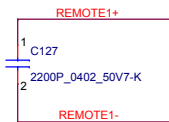
Security Classification		LC Future Center Secret Data		Title			
Issued Date	2015/11/02	Deciphered Date	2015/8/10	FAN CONNECTOR			
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Date: Thursday, May 04, 2017				Sheet	48	of 64	



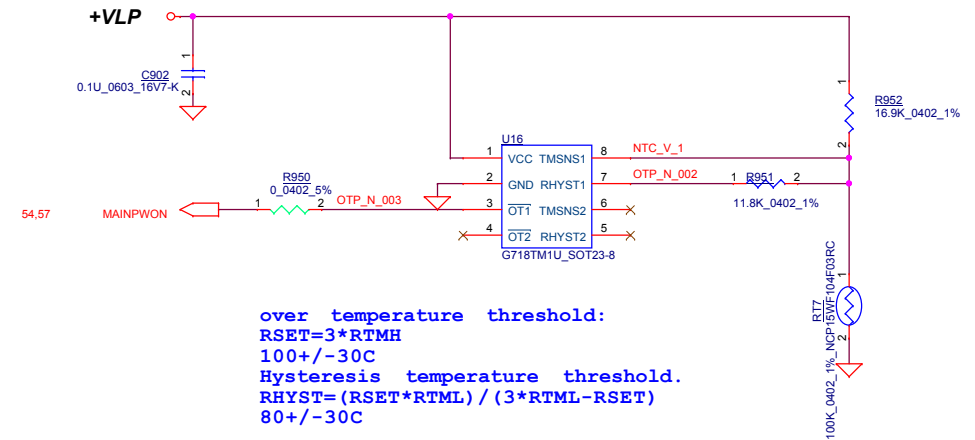
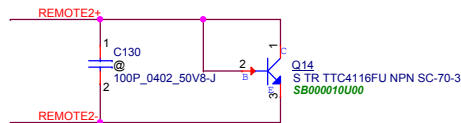
The diagram shows the F75303M\_MSOP10 package with the following connections:

- Pin 10 (SCL):** Connected to EC\_SMB\_CK3 (8,18,42,50).
- Pin 9 (SDA):** Connected to EC\_SMB\_DA3 (8,18,42,50).
- Pin 8 (ALERT#):** Not connected (marked with an X).
- Pin 7 (THERM#):** Connected to F75303M\_THERM# R202. The signal path includes a 1K resistor, a 0.404 resistor, and a 5% tolerance, connected to +3VS.
- Pin 6 (GND):** Connected to ground.


*Close to U1*

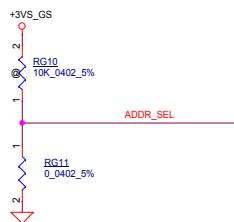
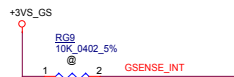
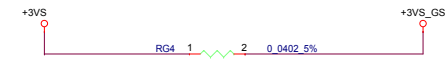


**Close JDIMM1&JDIMM2**



```
over temperature threshold:
RSET=3*RTMH
100+/-30C
Hysteresis temperature threshold.
RHYST=(RSET*RTML)/(3*RTML-RSET)
80+/-30C
```

Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/10/5	Deciphered Date	2016/10/31	<b>Thermal Sensor</b> 	
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				Custom	SDV
				<b>JINN/DOOKU</b>	
Date:		Thursday, May 04, 2017		ISheet	49 of 64



## APS G-Sensor

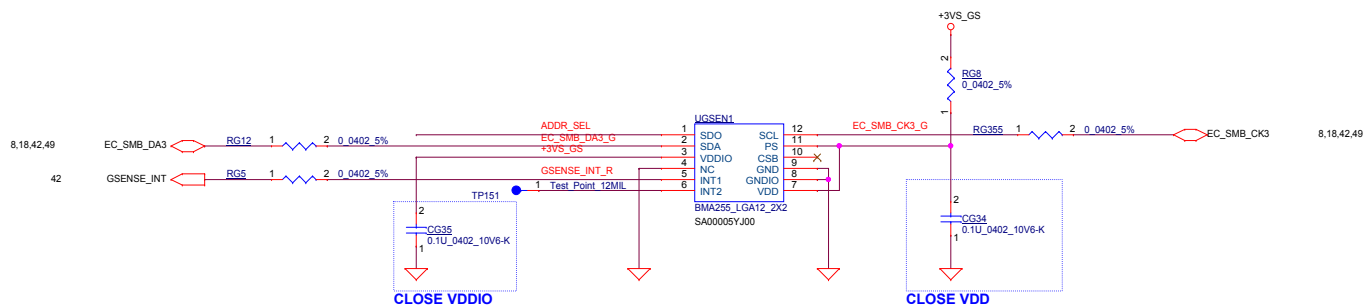
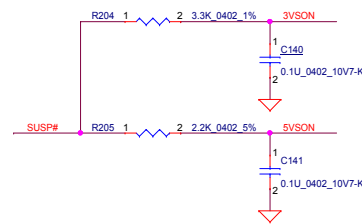


TABLE of G-Sensor (UG5701)		
Vendor	P/N	LCFC P/N
BOSCH	BMA255	SA00005YJ00
Kionix	KX022-1020	SA000081E00

TABLE

P/N	ADDR_SEL	Address
BMA255	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)
KX022-1020	H	3Eh (W) & 3Fh (R)
	L	3Ch (W) & 3Dh (R)

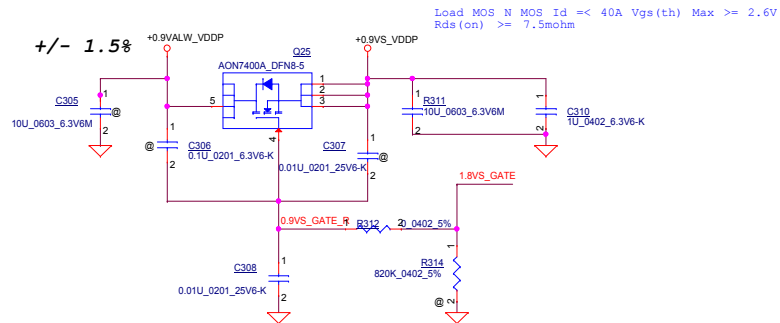


**VIN 5V and 3.3V (VBIAS=5V), I<sub>MAX</sub>(per channel)=6A, R<sub>ds</sub>=18mohm**

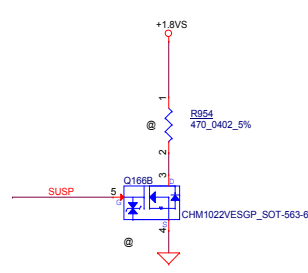
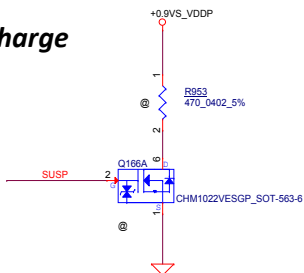
The schematic shows a 2-channel PMOS load switch IC (TPS22966) driving two LEDs. The IC is configured with VIN1 and VIN2 at 5V, and VBIAS at 3.3V. The load resistors are 1000Ω. The LEDs are connected to +3VS and +5VS rails. The schematic includes component values like C134, C139, C132, and C137, and pin numbers for the IC.


V9B+      9V--13V

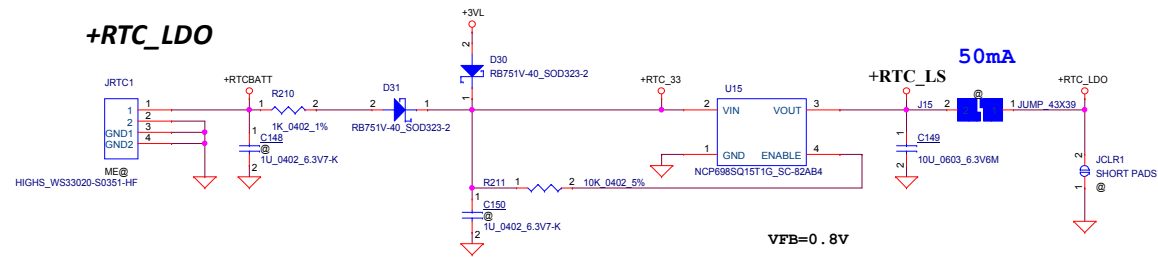
**AON7400**



$\pm 1.5\%$   
 +1.8V\_ALW  
 Q28  
 AON7400A\_DFN8-5  
 C311  
 10U\_0603\_6.3V6M  
 C312  
 0.10U\_0201\_6.3V6-K  
 C313  
 0.01U\_0201\_25V6-K  
 C314  
 10U\_0603\_6.3V6M  
 C315  
 10U\_0402\_6.3V6-K  
 C316  
 0.01U\_0201\_25V6-K  
 R318  
 2 0402 5%  
 R320  
 2 50K 0402 5%  
 R322  
 1M 0402 5%  
 Q29  
 2N7002KW\_SOT323-3  
 SUSP  
 V9B+

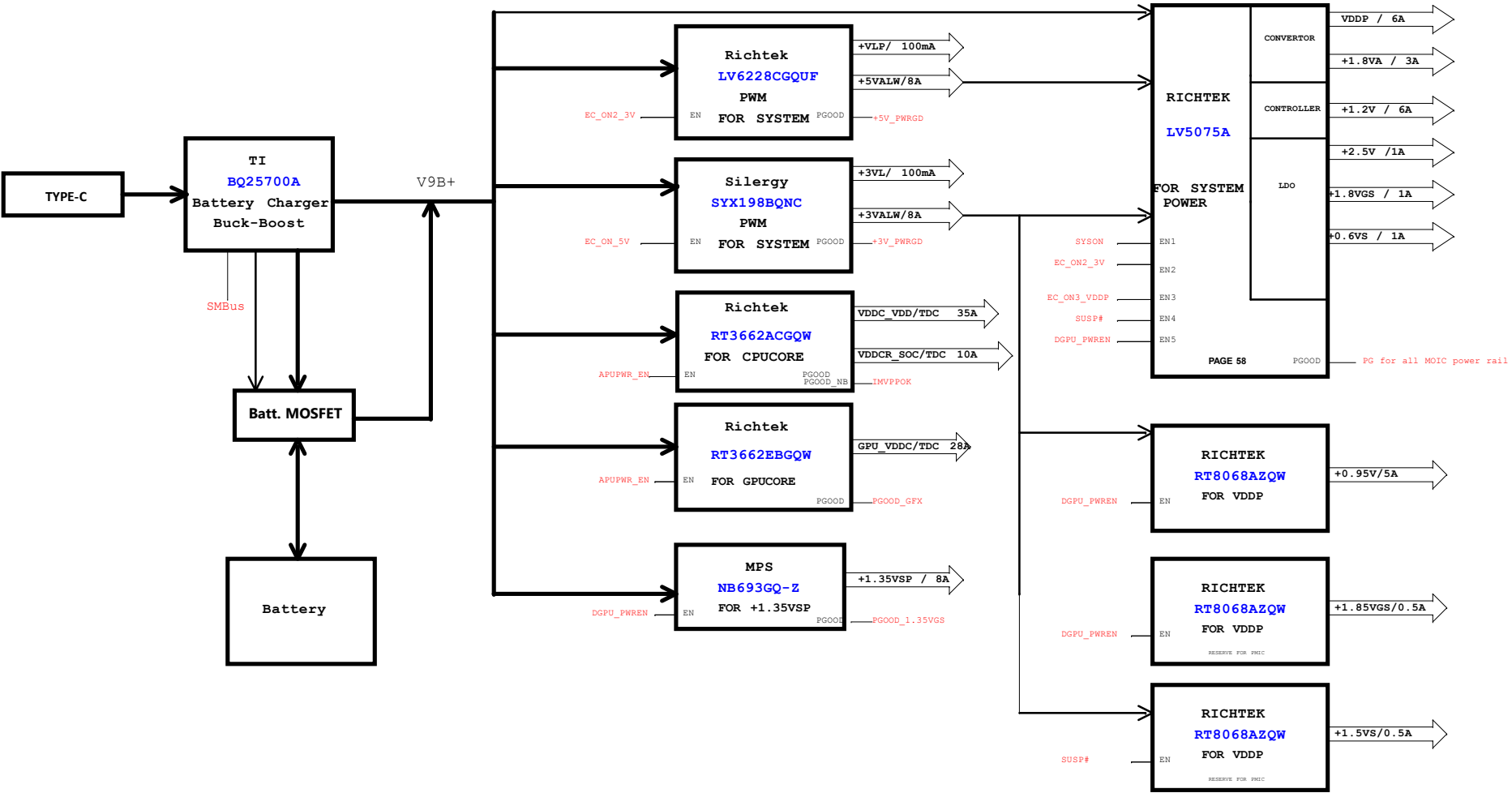


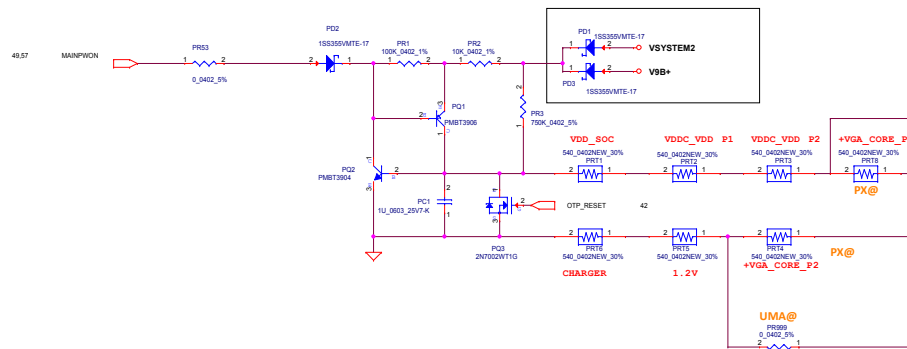
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Issued Date	2015/10/5	Deciphered Date	2016/10/31	3VS/5VS/1.1VS/VDDIO_RUN	
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				Size	
				Document Number	
				JINN/DOOKU	
				Date: Thursday, May 04, 2017	
				ISheet 51 of 64	
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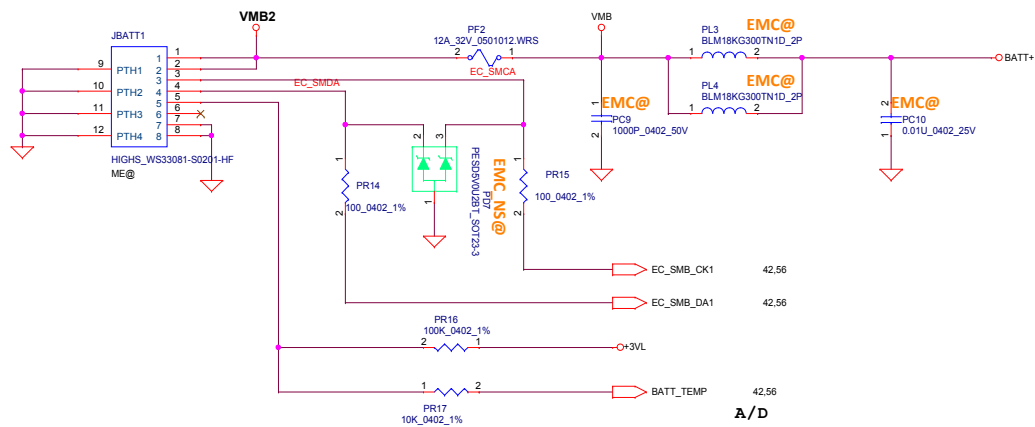


Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/10/5	Deciphered Date	2016/10/31	3VS/5VS/1.1VS/VDDIO_RUN	
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				Custom	SDV
				JINN/DOOKU	
				Date:	Thursday, May 04, 2017
				Sheet	52 of 64



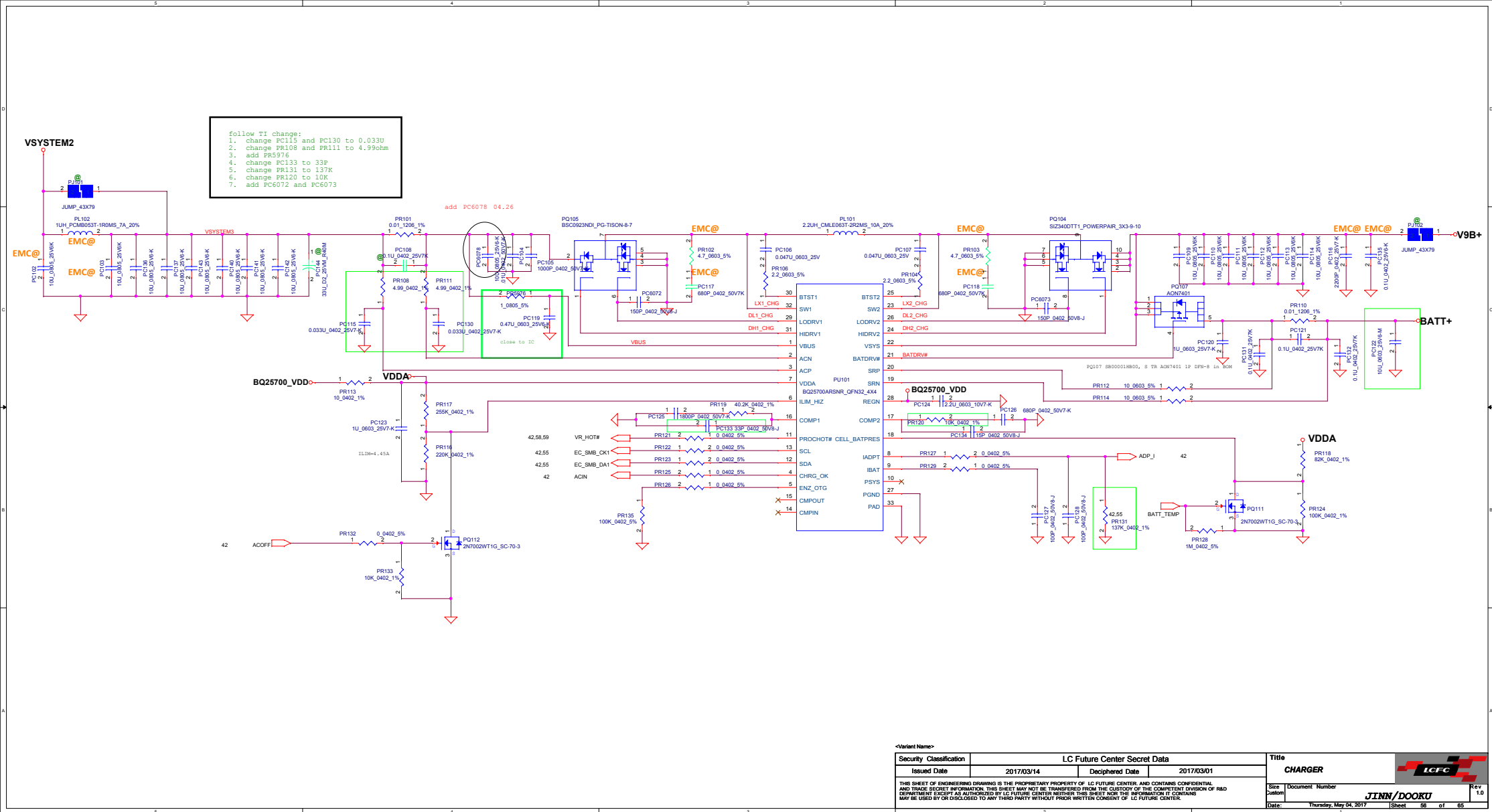




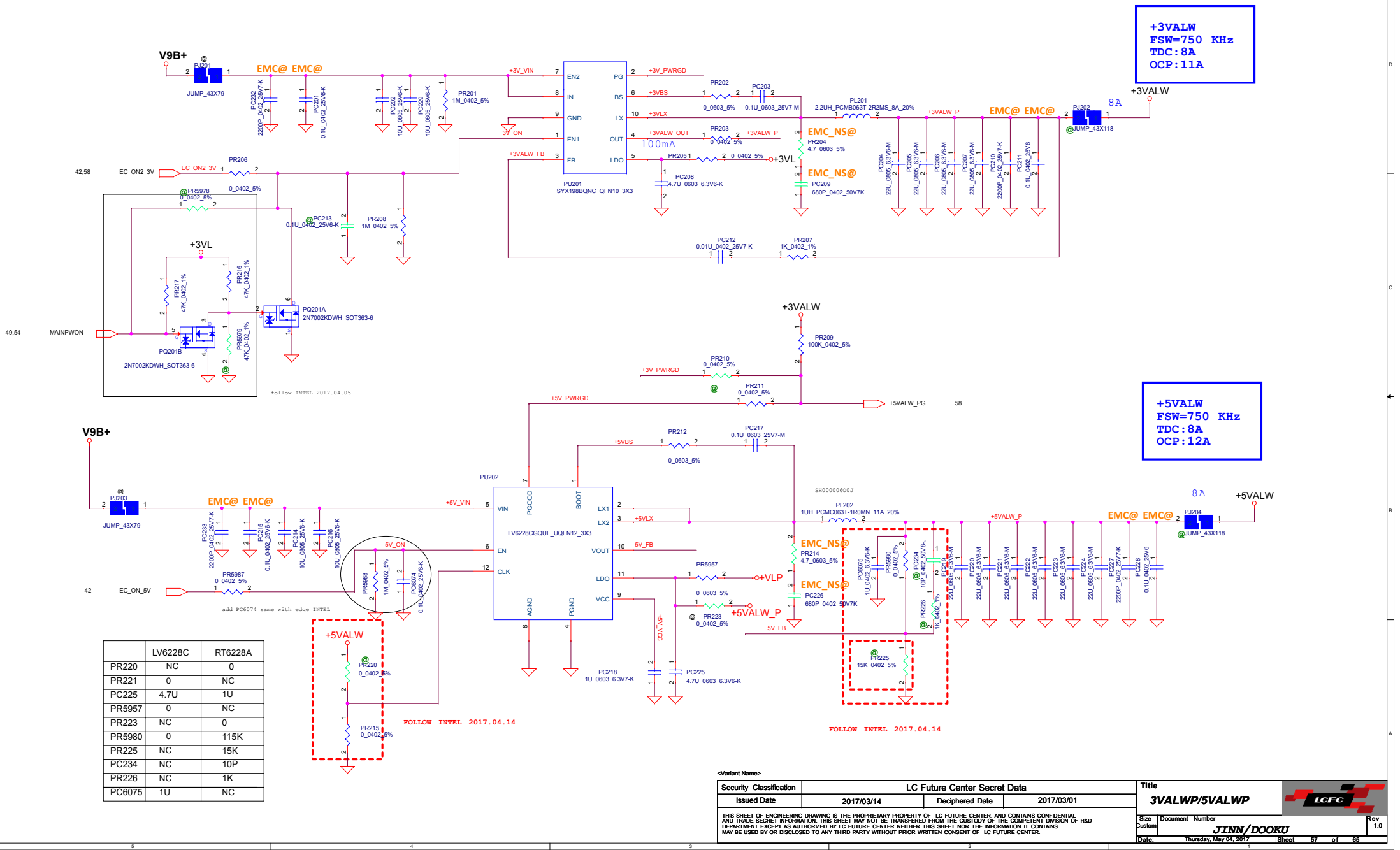


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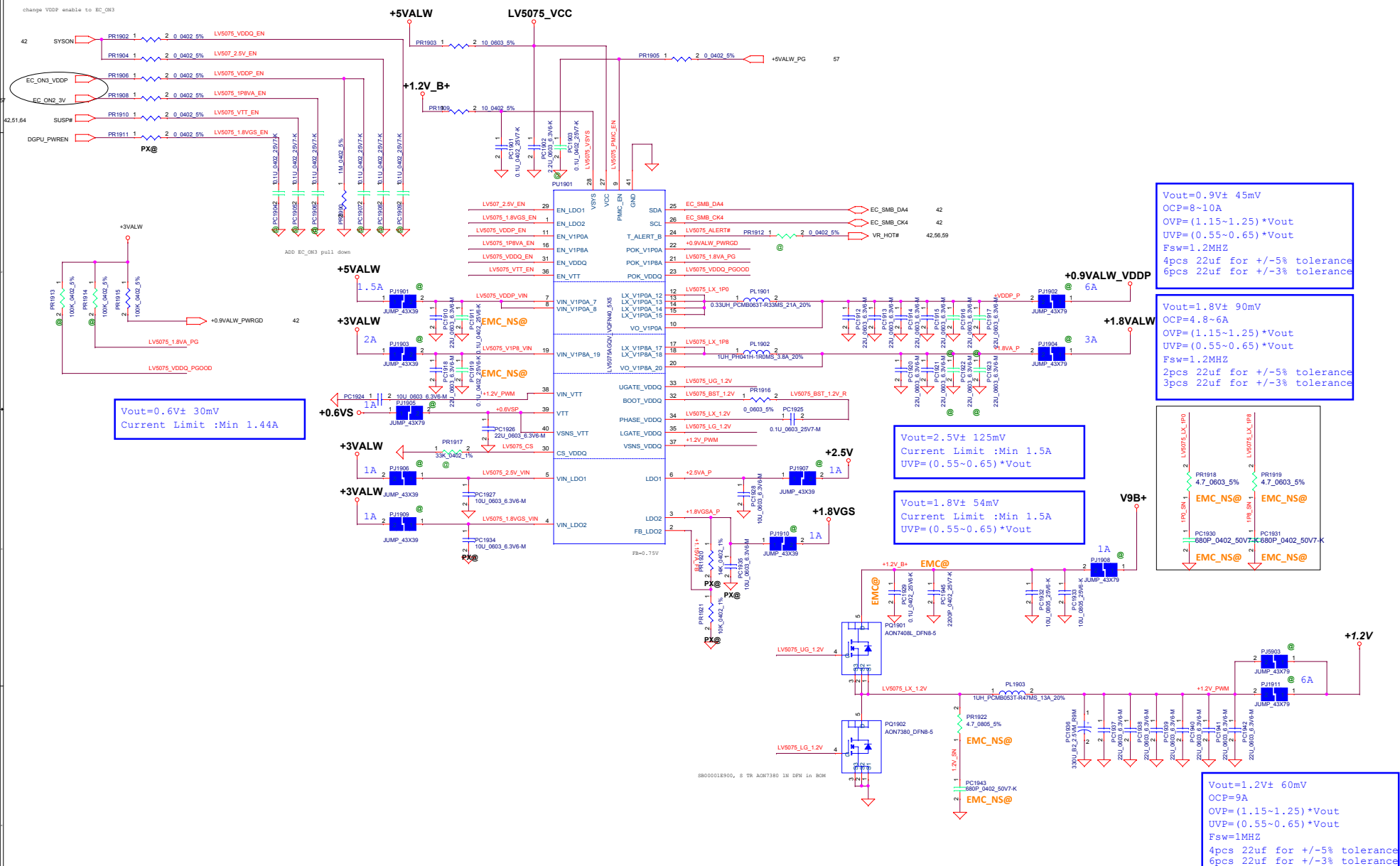
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Size Custom	Document Number	JINN/DOOKU		Rev 1.0
Date:	Thursday, May 04, 2017	Sheet	55 of 65	




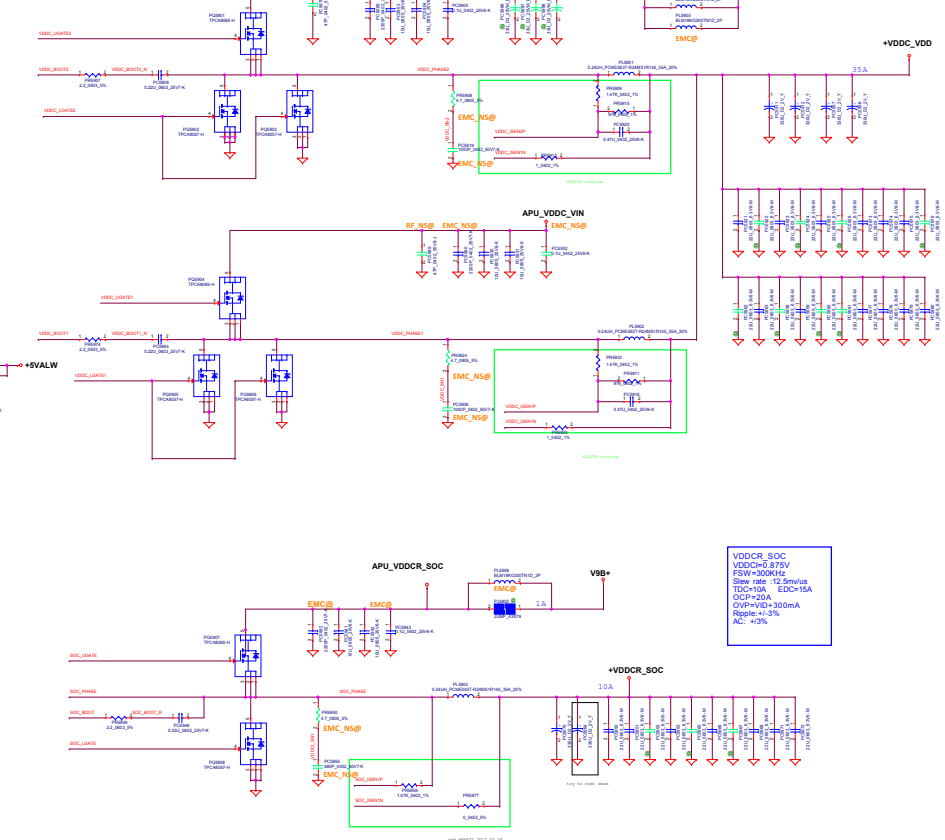
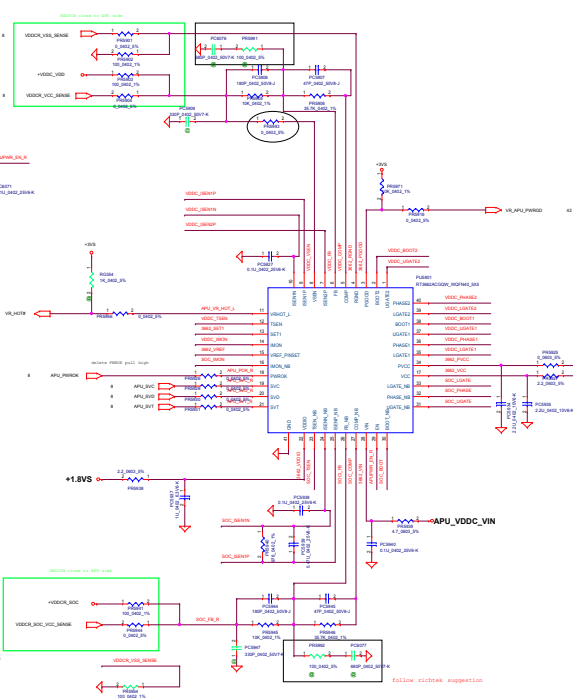
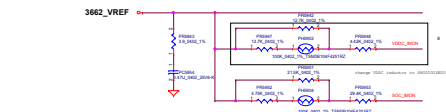
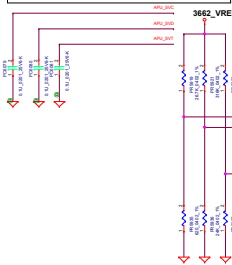




change VDDP enable to EC\_CN3

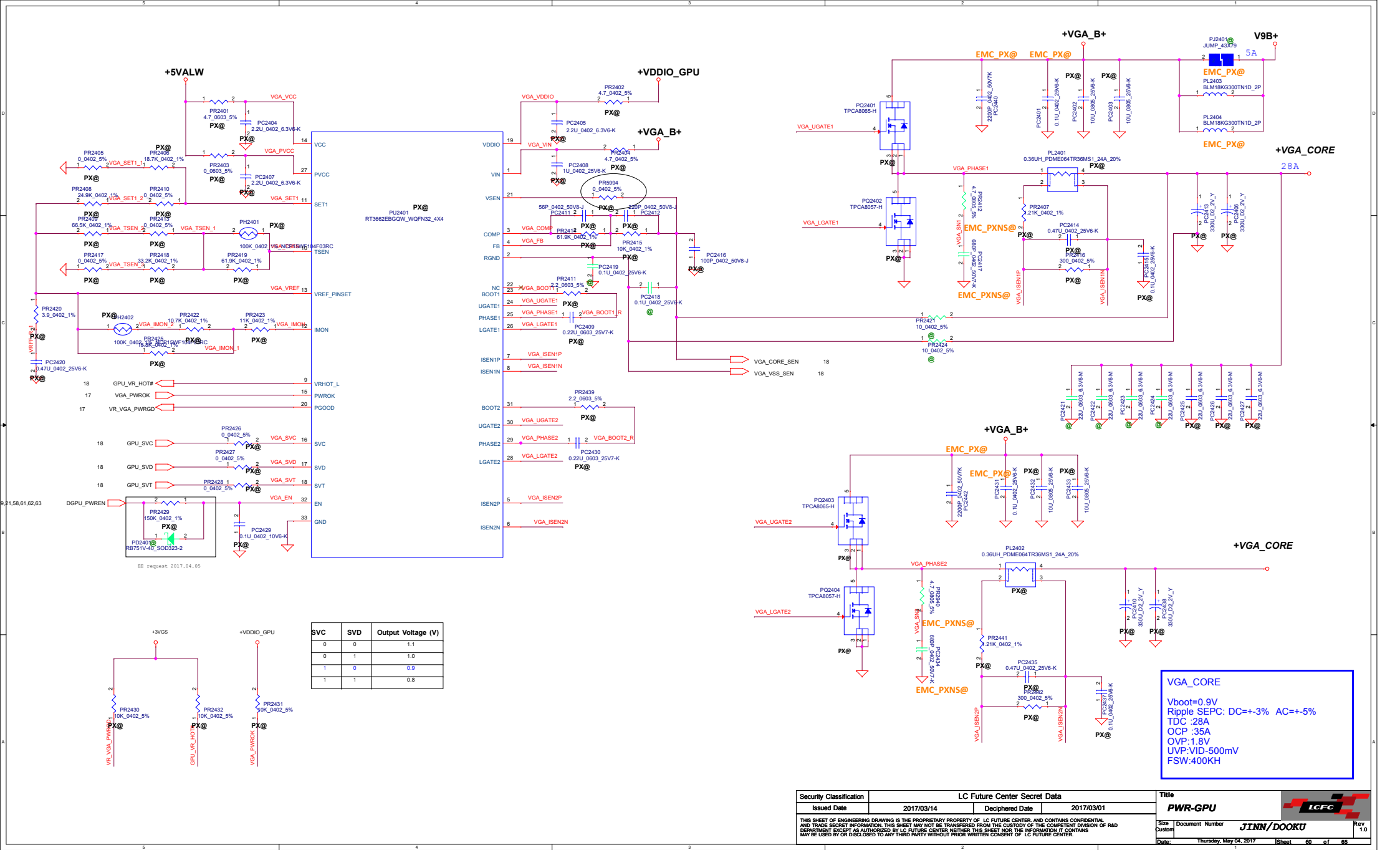


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Issued Date	2017/03/14	Deciphered Date	2017/03/01	PWR-SYSTEM			
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				Date Thursday, May 04, 2017		Rev 1.0	

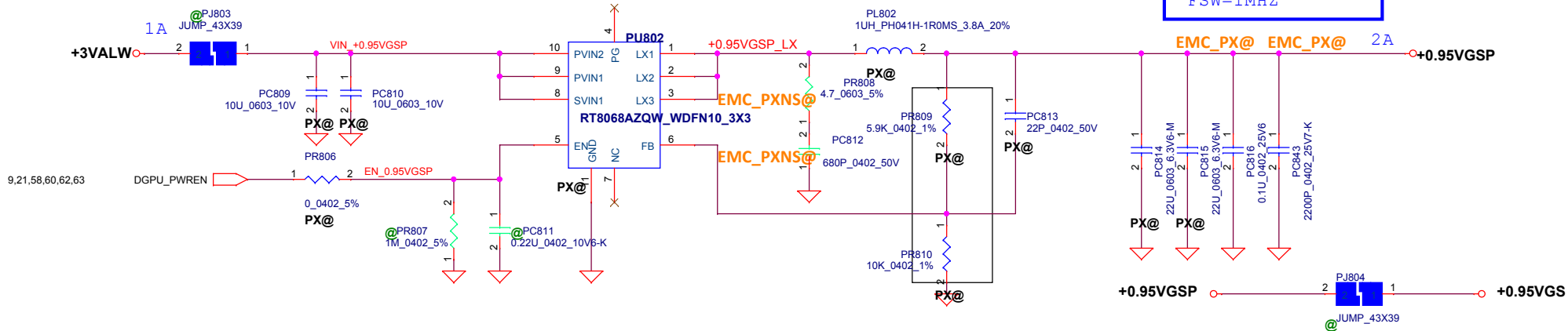


GPU\_VDDC  
FSW=300KHz  
Slew rate:12.5mV/us  
TDC=35A EDC=45A  
OCP=60A  
OVP=VID+300mV  
Load Line=0.6mohm  
Ripple: +/-20mV  
MAX AC: VID\_VDDC +120mV  
MIN AC: VID\_VDDC -80mV


VDDCR\_SOC  
VDDCI=0.875V  
FSW=300KHz  
Slew rate :12.5mv/us  
TDC=10A EDC=15A  
OCP=20A  
OVP=VID+300mA  
Ripple: +/-3%  
AC: +/-3%

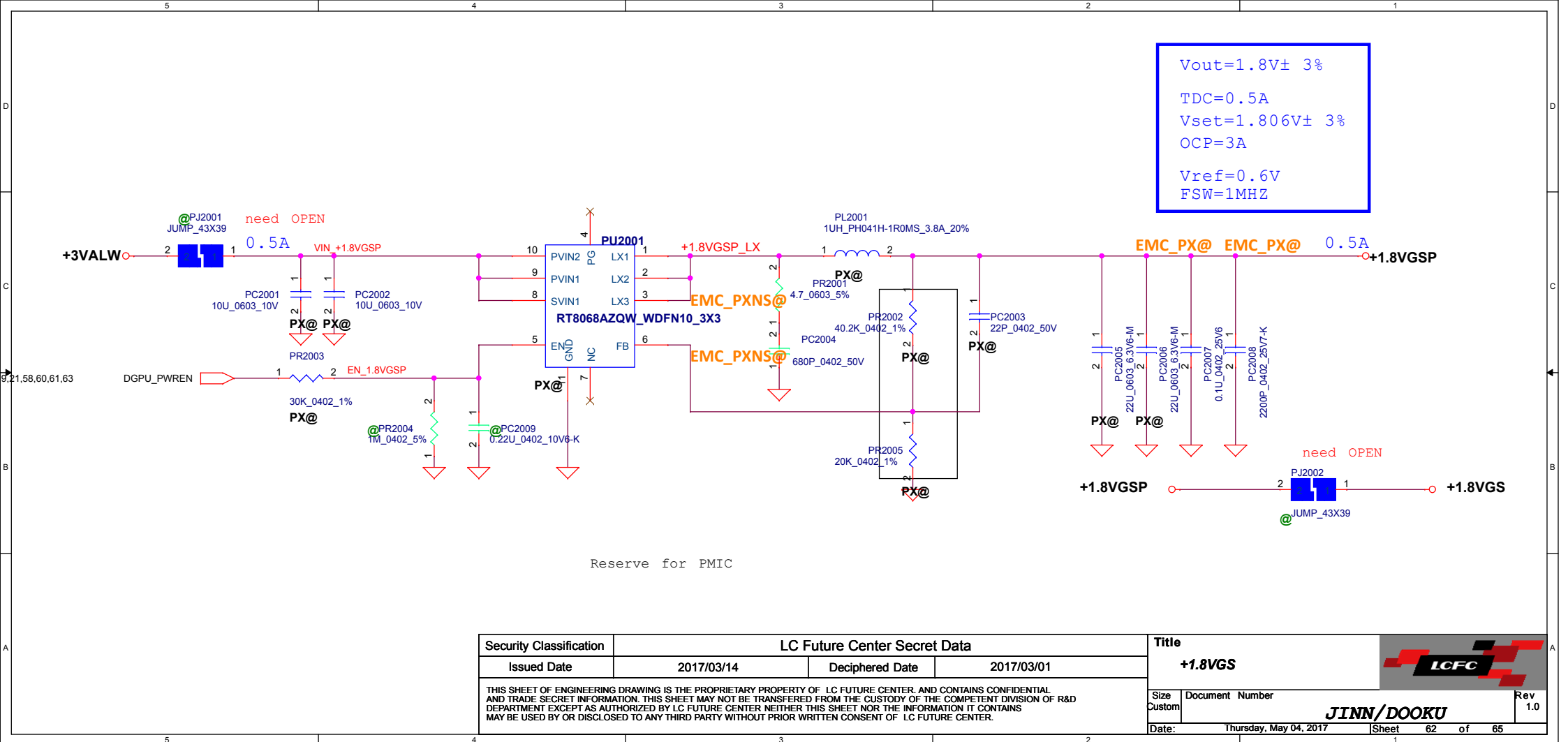


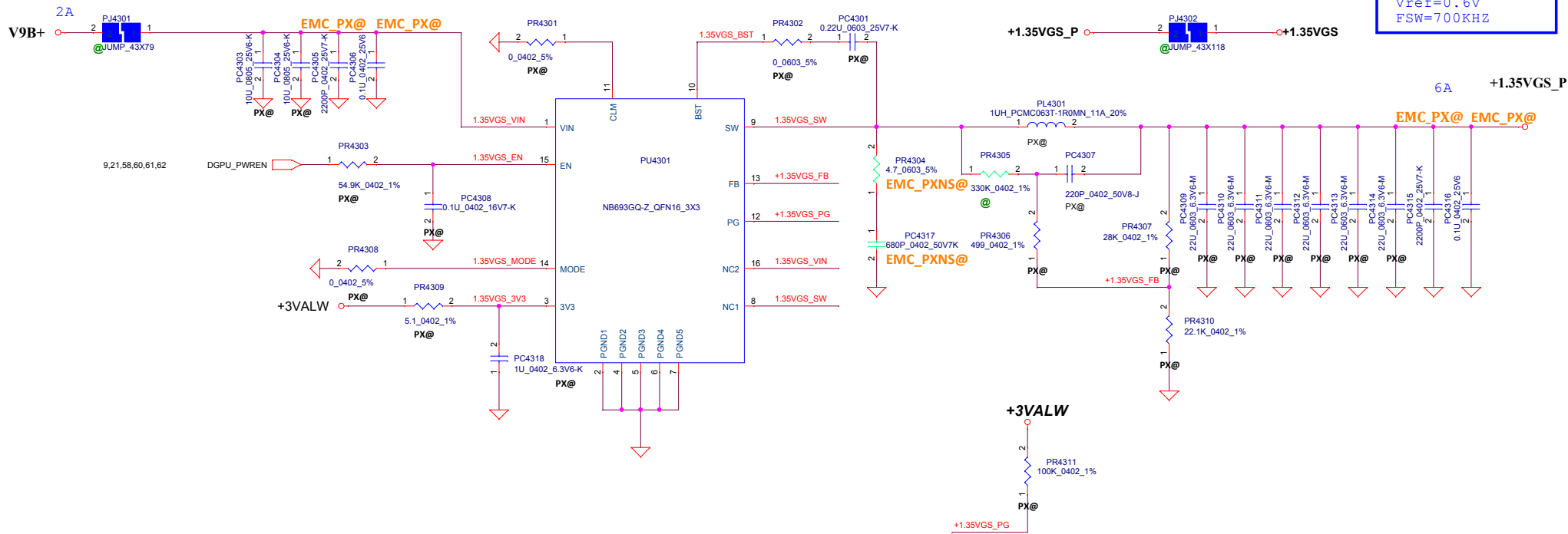
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Issued Date	2017/03/14	Deciphered Date	2017/03/01	PWR-GPU	
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				Date	Thursday, May 04, 2017
				Sheet	60 of 65



Vout=0.95V± 3%  
 TDC=2A  
 Vset=0.954V± 3%  
 OCP=3A  
 Vref=0.6V  
 FSW=1MHZ

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Size		Document Number		JINN/DOOKU		Rev
Custom						1.0
Date:		Thursday, May 04, 2017		Sheet 61 of 65		





Vout=1.35V± 3%  
TDC=6A  
Vset=1.36V± 3%  
OCP=8.5A  
Vref=0.6V  
FSW=700KHZ

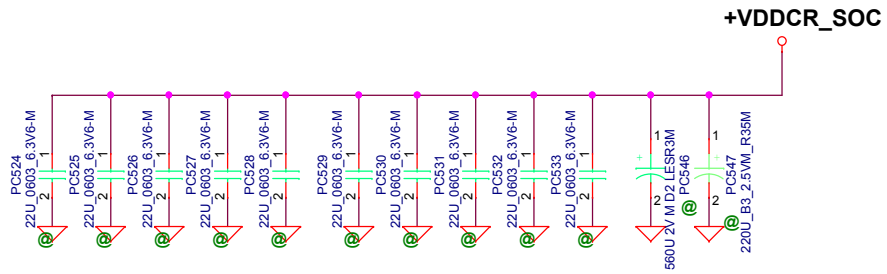
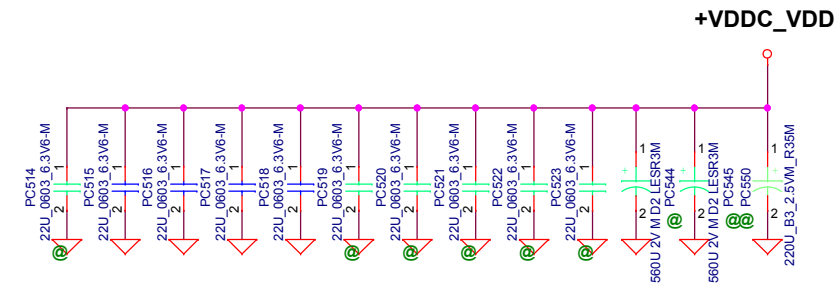
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