

CPU Architecture

LAB2 preparation report

VHDL part2

Sequential code and Behavioral modeling

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1. Aim of the Laboratory

- Obtaining skills in VHDL part2 code, which contains Sequential code and Behavioral modeling.
- Obtaining basic skills in ModelSim (multi-language HDL simulation environment).
- Knowledge in digital systems design.
- Proper analysis and understanding of architecture design.

2. System Design definition

In this laboratory you will design a synchronous digital system which detects valid sub series for a given condition value (see table 1). The system block diagram is depicted in figure 1. You are required to design the whole system and make a test bench for testing.

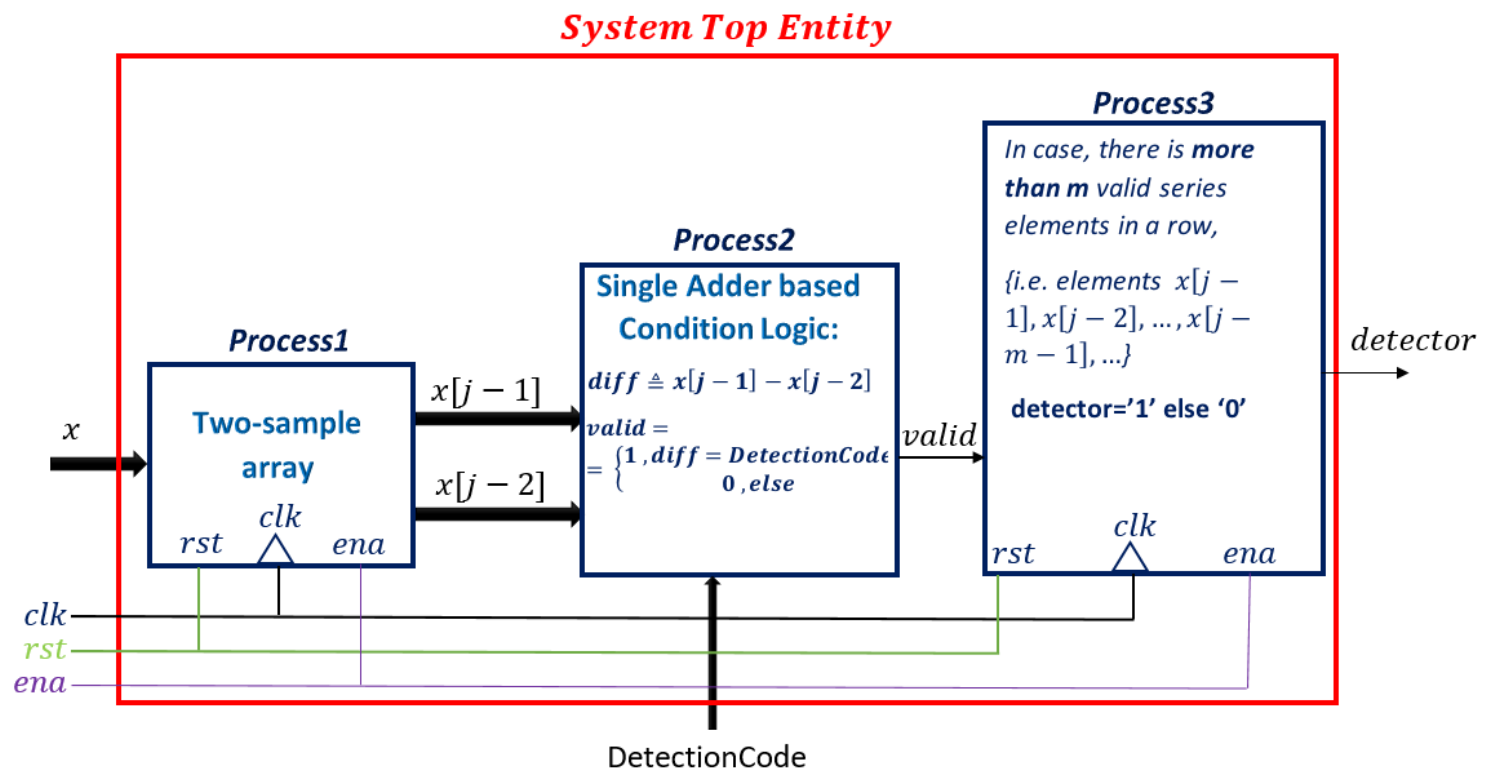
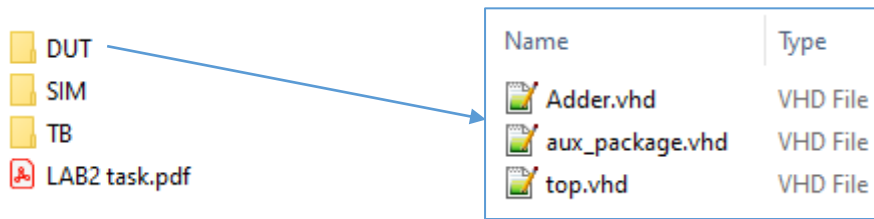


Figure 1 : System structure

<i>DetectionCode</i>	<i>Condition</i>
0	$x[j-1] - x[j-2] = 1$
1	$x[j-1] - x[j-2] = 2$
2	$x[j-1] - x[j-2] = 3$
3	$x[j-1] - x[j-2] = 4$

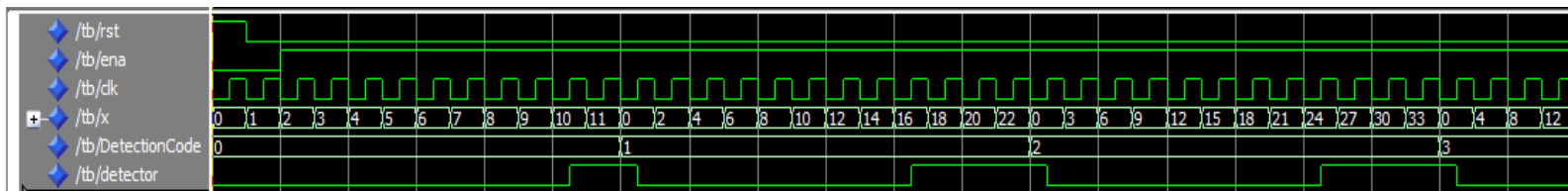
Table 1: cond value

- The Top Level design must be Structural (*your DUT must contain the exact next three *.vhd files*).

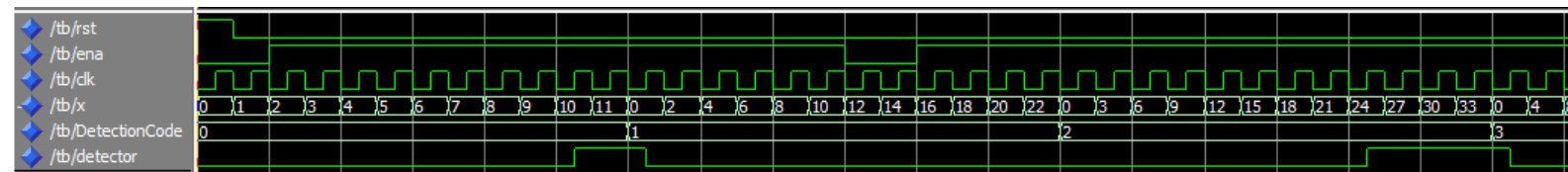


- The Top Level design modeling can be Behavioral except the **Adder** based condition check module (single instantiation only of **Adder.vhd**). The main reason of this constraint is to minimize HW.
- Note:** in the given the next three files that you must use in your project: top.vhd, aux_package.vhd, Adder.vhd (you can only add your code to **top.vhd** file; you are not allowed to erase anything).
- The submitted project must be compiled using the given **tb1.vhd, tb2.vhd** files (otherwise the submitted project will be considered as a failure).
- The submitted assignments get through copy checking machine, in this case, both sides' assignments will be disqualified.
- Examples:**

tb_1 timing diagram



tb_2 timing diagram



tb_3 timing diagram

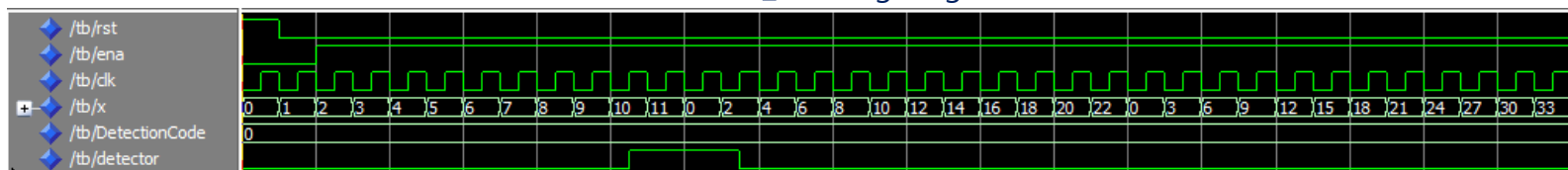
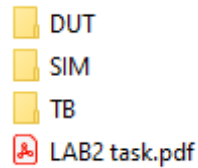
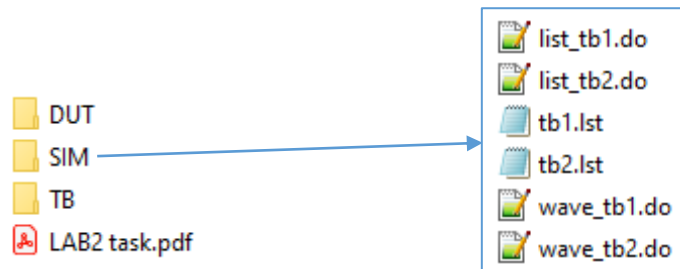


Figure 2: examples using waveforms

In addition, you are given two test bench files *tb1.vhd*, *tb2.vhd* (in TB folder) and their associate do and list files (in SIM folder).

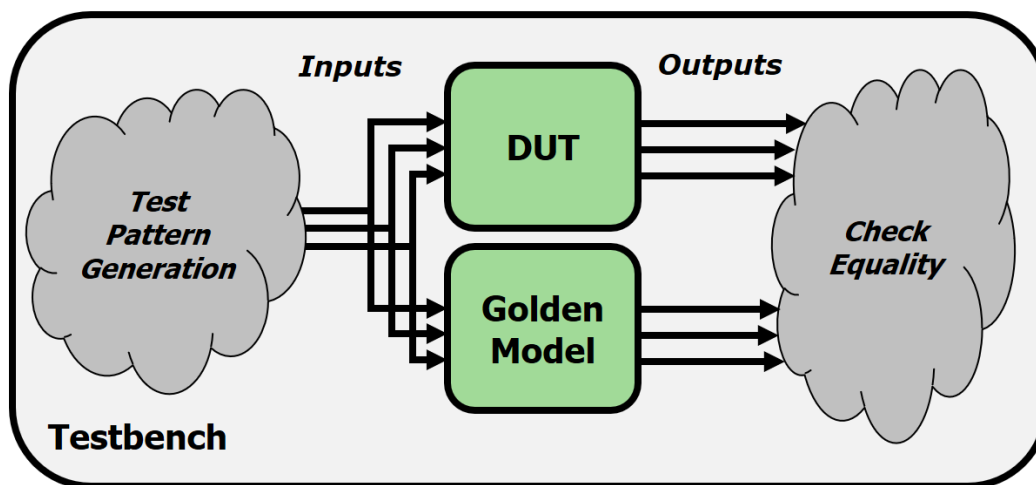


In order to use golden model based functional verification, you are given [TextDiff](#) application (download and double click the *TextDiff.exe* file) in order to compare your developing design results to the golden model results as part of design developing chain.



Automatic Testbench

The DUT **output** is compared against the **golden model**



Note: in comparison between the given *tb1.lst*, *tb2.lst* files and yours, you should ignore the *delta cycle* column

3. Test and Timing:

- Design a test bench, which tests all the system.
- Analyze the results by zooming on the important transactions in the waveforms. Explain these (input/output/internal signals of the system).
- You are welcome to use the Internet also as reference.
- The timing of the system will be ideal (means a functional simulation).

4. Requirements

- a. The design must be well commented.
- b. **Important:** For each of two submodules:
 - Graphical description (a square with ports going in and out) and short descriptions.
- c. Elaborated analysis and wave forms:
 - Remove irrelevant signals.
 - Zoom on regions of interest.
 - Draw clouds on the waveform with explanations of what is happening (Figure 4).
 - Change the waveform colors in ModelSim for clear documentation (Tools->Edit Preferences->Wave Windows).
- d. A ZIP file in the form of **id1_id2.zip** (where id1 and id2 are the identification number of the submitters, and $id1 < id2$) *must be upload to Moodle only by student with id1* (any of these rules violation disqualify the task submission).
- e. The **ZIP** file will contain (*only the exact next sub folders*):

Directory	Contains	Comments
DUT	Project VHDL files	Only VHDL files of DUT , excluding test bench Note: your project files must be well compiled without errors as a basic condition before submission
TB	VHDL files that are used for test bench	A single presentative <i>tb.vhd</i> (your version) of system top verification
SIM	DO files of <u>wave</u> and <u>list</u> forms	Do files for <i>tb.vhd</i> (your version) of system top verification
DOC	Project documentation	Readme.txt and pre2.pdf report file

Table 2: Directory Structure

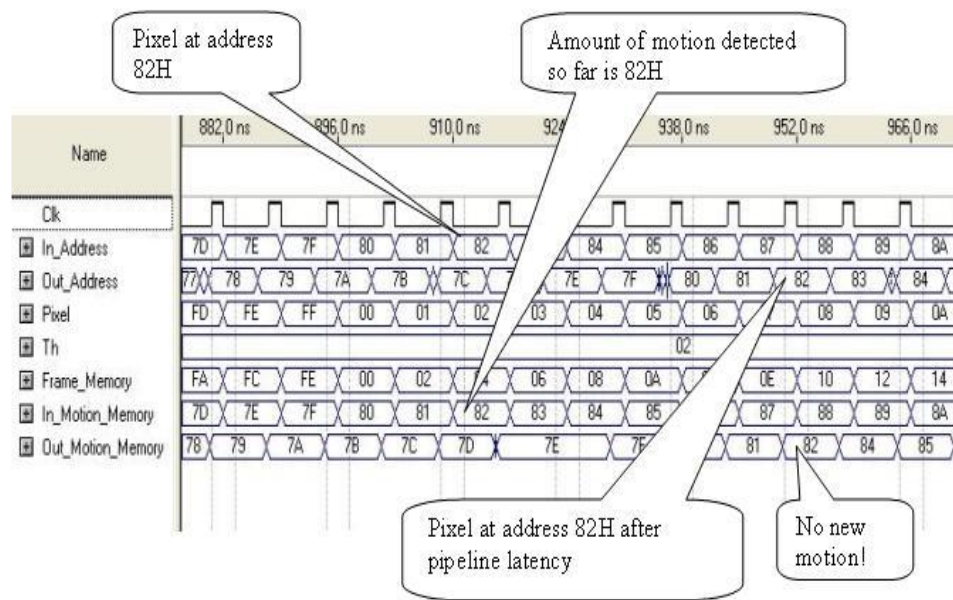


Figure 3: Clouds over the waveform example

5. Grading Policy

Weight	Task	Description
10%	Documentation	The "clear" way in which you presented the requirements and the analysis and conclusions on the work you've done
90%	Analysis and Test	The correct analysis of the system (under the requirements)

Table 1 : Grading

Under the above policies you'll be also evaluated using common sense:

- Your files will be compiled and checked, the system must work.
- Your design and architecture must be intelligent, minimal, effective and well organized.

For a late submission, the penalty is 2

