CPU Architecture

LAB3 assignment

Digital System Design with VHDL

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1. Aim of the Task:

- System design using concurrent and sequential logic principles using advanced Simulation methods (based on material given in LAB1 and LAB2 tasks).
- Controller design based on methodology of Control and Datapath separation.
- Preparation for LAB4 task – FPGA based design synthesis of the given design.
- Proper analysis and understanding of architecture design.

2. Assignment definition:

In this task, you are required to design a controller-based processing machine in order to run a given program code. The preparation material for this lab has been learned until lecture five and includes in addition to the self-leaning material given on a subjects of FSM methodology design and advanced functional verification.

3. Controller based system:

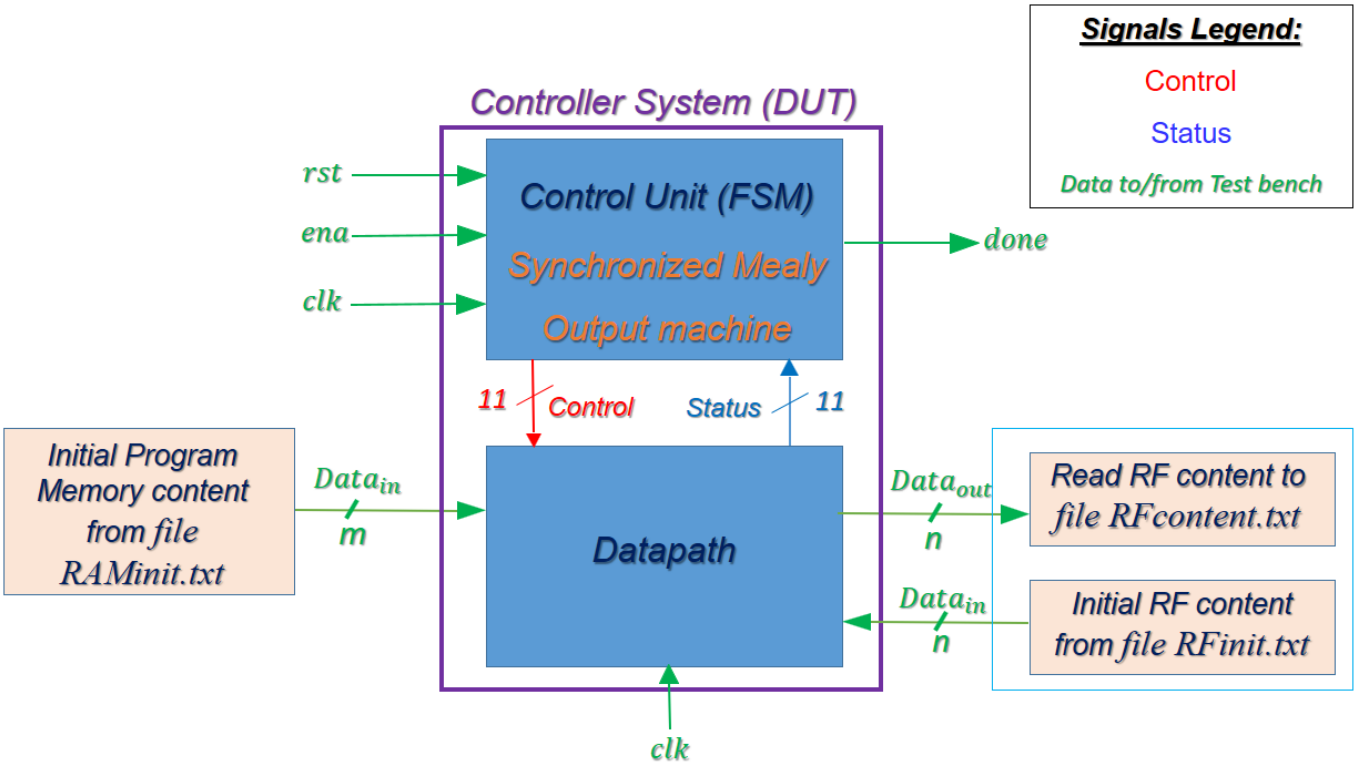


Figure 1: Overall DUT structure

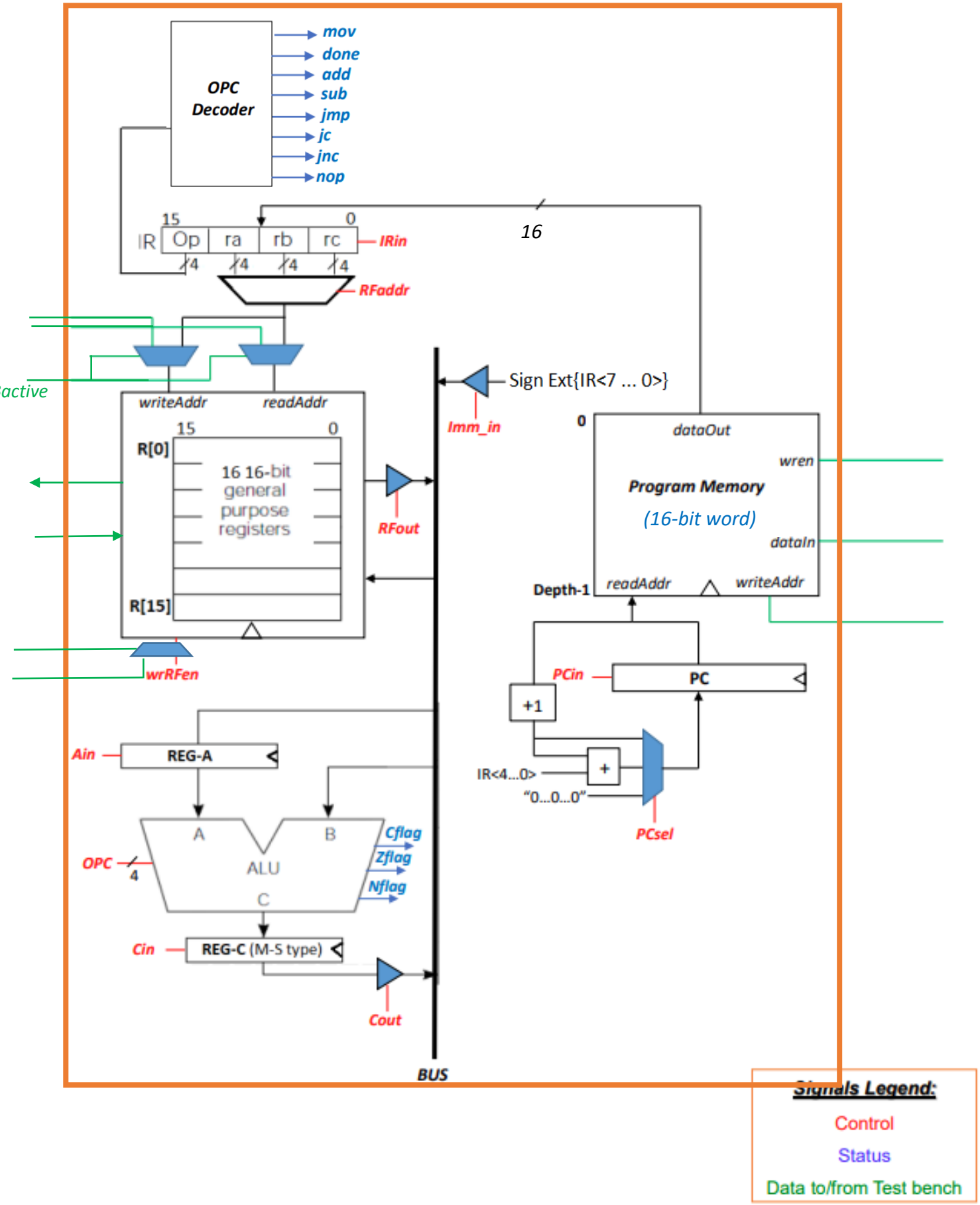


Figure 2: Datapath structure

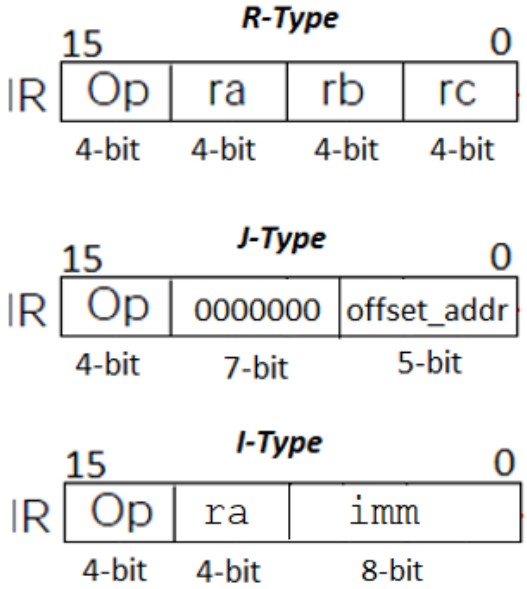


Figure 3: Instruction Formats

Instruction Format	Decimal value	OPC	Instruction	Explanation
R-Type	0	0000	add ra,rb,rc	R[ra]<=R[rb]+R[rc]
	1	0001	sub ra,rb,rc	R[ra]<=R[rb]-R[rc]
	2	0010	nop	R[0]<=R[0]+R[0]
	3	0011	*unused*	
J-Type	4	0100	jmp offset_addr	PC<=PC+1+offset_addr
	5	0101	jc offset_addr	If(Cflag==1) PC<=PC+1+offset_addr
	6	0110	jnc offset_addr	If(Cflag==0) PC<=PC+1+offset_addr
	7	0111	*unused*	
I-Type	8	1000	mov ra,imm	R[ra]<=imm
	9	1001	done	It signals to TB that RF's content is ready to be read

Table 1 : controller ISA

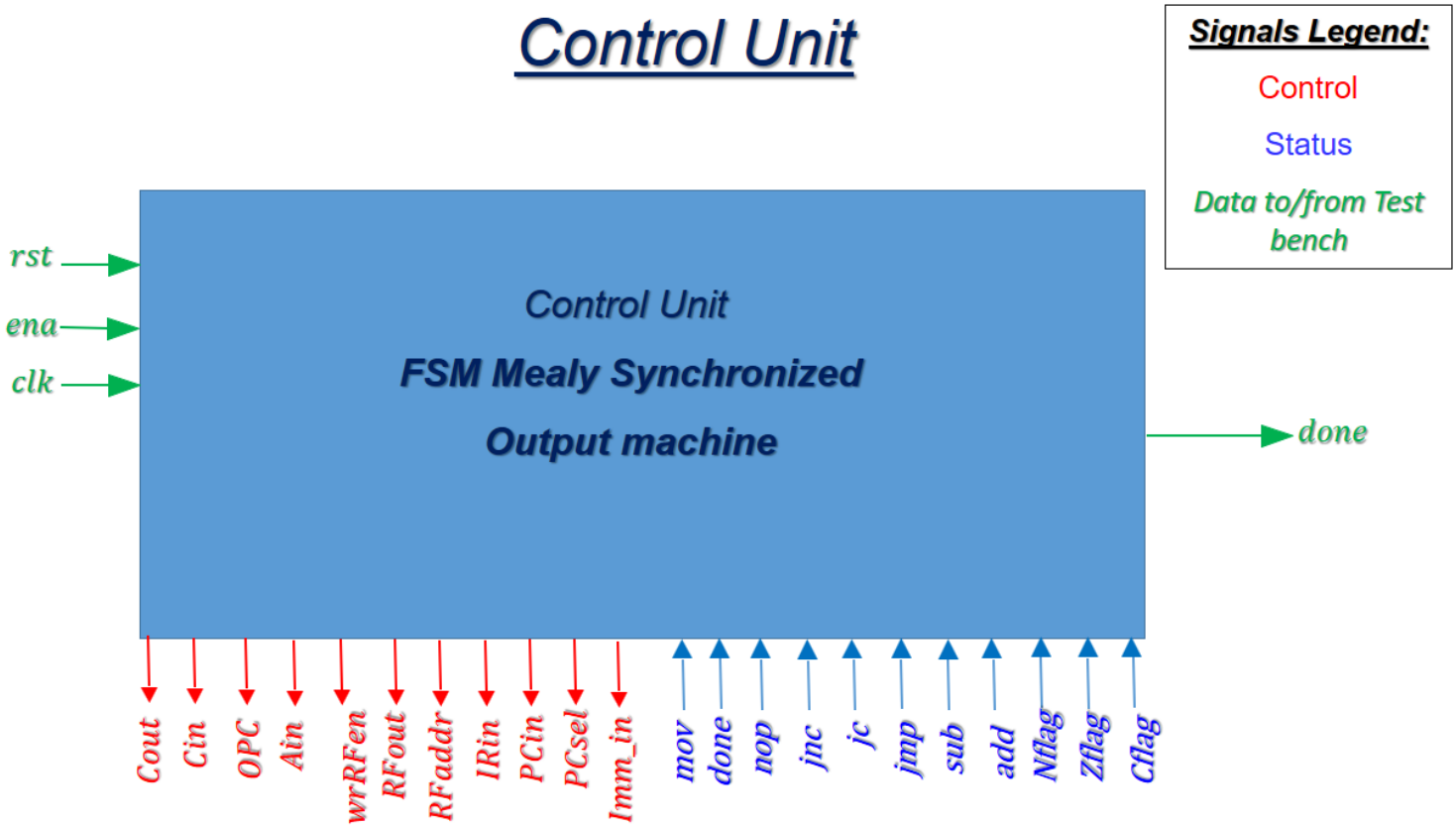


Figure 4: Control unit structure

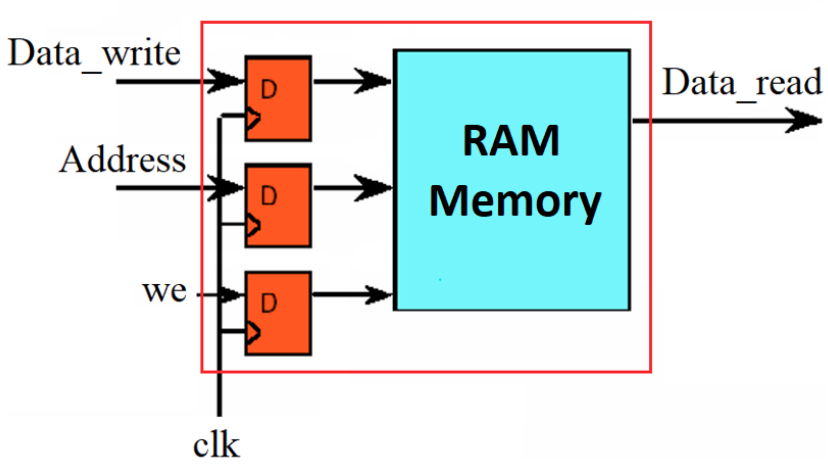
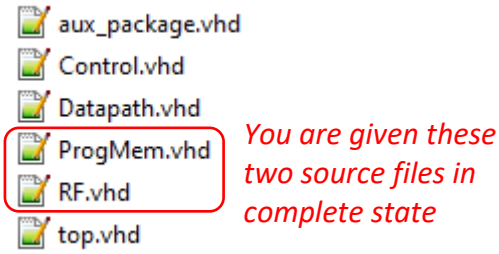


Figure 5: Single Port RAM with unregistered output (this structure used for Register File and Program Memory given VHDL code)

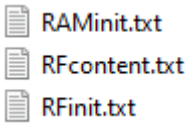
- The given files that you must use in your project:



  - ✓ You must use the listed above source files, you are required to fill them up yourself**.**
  - ✓ You can add additional VHDL source code files.
  - ✓ Other entities can be designed and modeled behaviorally, structurally, etc.

4. File based simulation of DUT:

- As depicted in figure 1, in order to simulate the DUT systemly we use file based simulation.
- Two Input and one Output files structure (according the above given figure at clause 3):



5. Running Code Example:

Assembly code

```
1  mov r1,1
2  add r2,r2,r13
3  add r3,r4,r9
4  sub r6,r2,r3
5  jc  2
6  add r6,r1,r0
7  jmp 1
8  add r6,r0,r0
9  done
10 nop
11 jmp -2
```

Equivalent Pseudo code

```
if(R[2]+R[13] >= R[4]+R[9])
    R[6]=0;
else
    R[6]=1;

loop_forever;
```

RAMinit.txt - Notepad

File Edit Format View Help

```
8101
022D
0349
1623
5002
0610
4001
0600
9000
2000
4FFE
```

RFinit.txt - Notepad

File Edit Format View Help

```
0000
0001
0002
0003
0004
0005
0006
0007
0008
0009
000A
000B
000C
000D
000E
000F
```

RFcontent.txt - Notepad

File Edit Format View Help

```
0000
0001
000F
000D
0004
0005
0000
0007
0008
0009
000A
000B
000C
000D
000E
000F
```

Updated values after program run

6. Requirements:

1. The design must be well commented.
2. Elaborated analysis and wave forms:
   - Remove irrelevant signals.
   - Zoom on regions of interest.
   - Draw clouds on the waveform with explanations of what is happening (Figure 4).
   - Change the waveform colors in ModelSim for clear documentation **(Tools->Edit Preferences->Wave Windows).**
3. A ZIP file in the form of **id1_id2.zip** (where id1 and id2 are the identification number of the submitters, and id1 < id2) *must be upload to Moodle only by student with id1* (any of these rules violation disqualifies the task submission).
4. The **ZIP** file will contain (***only the exact next sub folders***):

Directory	Contains	Comments
DUT	Project VHDL files	**Only VHDL files of DUT**, excluding test bench **Note: your project files must be well compiled without errors as a basic condition before submission**
TB	VHDL files that are used for test bench	One **tb.vhd** for the Datapath One **tb.vhd** for the Control unit One **tb.vhd** for the overall DUT
SIM	ModelSim DO files (wave, list)	One **tb.vhd** for the Datapath One **tb.vhd** for the Control unit One **tb.vhd** for the overall DUT (with Datatpath and Control unit signals included)
DOC	Project documentation	• ***readme.txt*** (list of the DUT **.vhd* files with their brief functional description) • ***pre3.pdf*** (report file that includes brief explanation of the top module with its wave diagrams as shown in figure 4) • ***designGraph.pdf*** *(*elaborated FSM graph of your DUT)

Table 2: Directory Structure

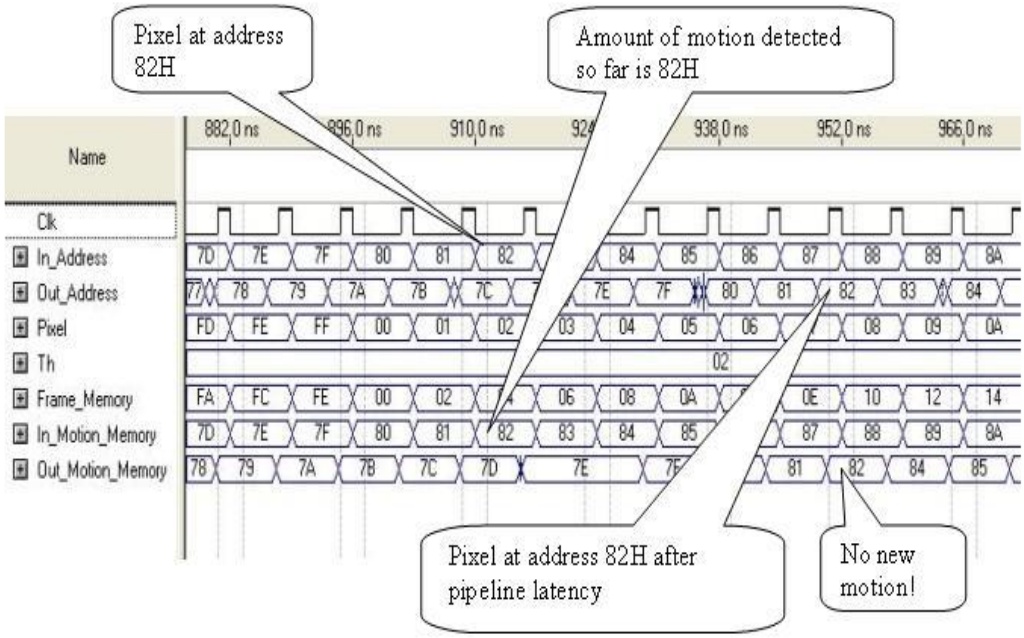


Figure 4: Clouds over the waveform example

7. Grading Policy

Weight	Task	Description
10%	Documentation	The "clear" way in which you presented the requirements and the analysis and conclusions on the work you've done
90%	Analysis and Test	The correct analysis of the system (under the LAB3 SEAT requirements)

Table 3: Grading

Under the above policies you'll be also evaluated using common sense:

- Your files will be compiled and checked, the system must work.
- Your design and architecture must be intelligent, minimal, effective and well organized.