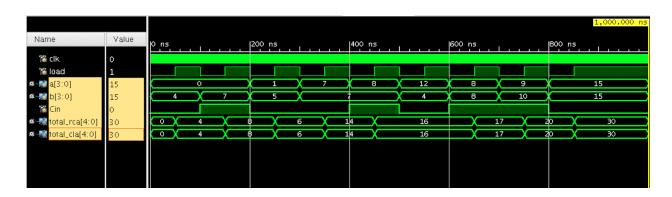
Lab5 - Adders

Colby Janecka CDJ2326 Telang ~ Wed. 12-1

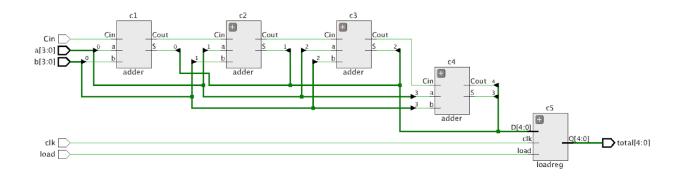
Table of Test Case Sums:

а	b	Cin	sum	Cout
0000	0000	0	0000	0
0000	0001	1	0010	0
0001	0101	0	0110	0
0111	0111	0	1110	0
1000	0111	1	0000	1
1100	0100	0	0000	1
1000	1000	1	0001	1
1001	1010	1	0100	1
1111	1111	0	1110	1

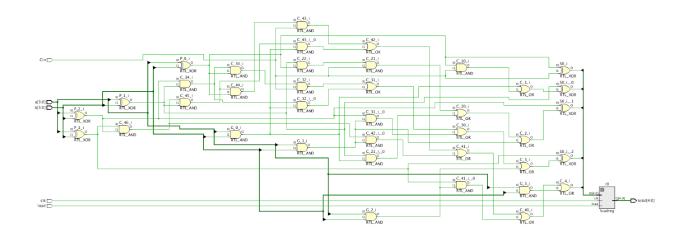
Waveform of Both Adders:



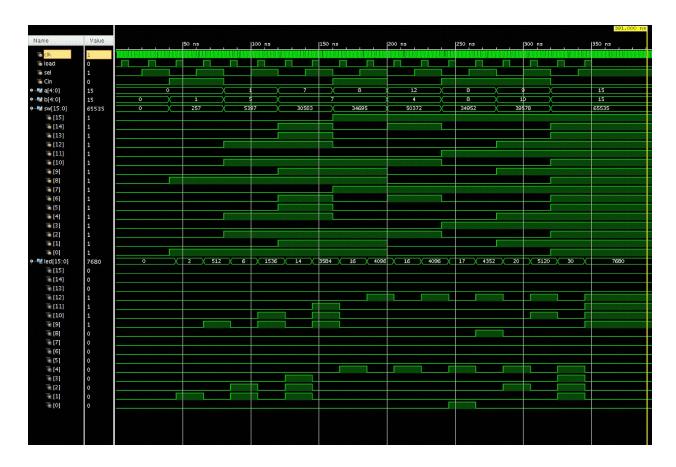
RCA Schematic:



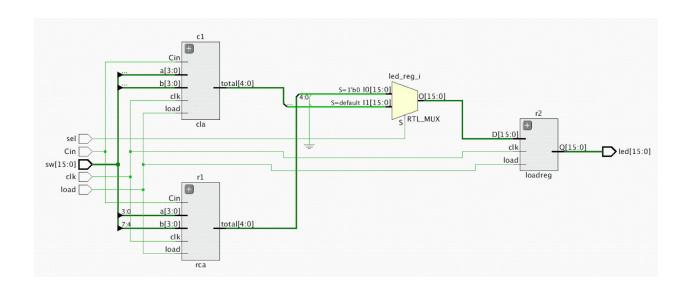
CLA Schematic:



Waveform of Datapath:



Datapath Schematic:



Linux Server Verification Proof:

Part A:

```
hiplandic@Colbys-MacBoo... ssh-Y cjanecka@kamek.ec... cjanecka@mario:/home/e...

System books directory is /home/ecelrc/students/mtemel/acl2/books
Relocation warnings:

Stub file: ..../../../../mtemel/acl2/books/misc/assert.cert
relocated to: ..../../../mtemel/acl2/books/std/testing/assert.cert
is included by:

..../../../mtemel/acl2/books/centaur/bitops/part-select.cert
..../../../mtemel/acl2/books/centaur/depgraph/invert.cert
..../../../mtemel/acl2/books/centaur/depgraph/invert.cert
...././../mtemel/acl2/books/centaur/vl/util/locations.cert
....//.//mtemel/acl2/books/centaur/vl/util/print.cert
....////mtemel/acl2/books/centaur/vl/util/print.cert
....////mtemel/acl2/books/centaur/vl/util/print.cert
..../////mtemel/acl2/books/contaur/vl/util/print.cert
..../////mtemel/acl2/books/doc/autolink.cert
....///////mtemel/acl2/books/doc/autolink.cert
....////////mtemel/acl2/books/doc/autolink.cert
....////////mtemel/acl2/books/doc/preprocess.cert

Making /home/ecelrc/students/cjanecka/EE316L/Lab5/Lab5_PartA/Lab5_PartA.srcs/sources_1/new/lab5
test-a.cert on 20-Apr-2020 14:82:56

Built /home/ecelrc/students/cjanecka/EE316L/Lab5/Lab5_PartA/Lab5_PartA.srcs/sources_1/new/lab5
test-a.cert (142.945*
```

Part B:

Part C:

Checkout Questions:

1. Calculate the critical path of the RCA and CLA given that an XOR gate uses 6 um² of area and has 3ns delay, an AND gate uses 4um² of area and has 3ns delay, and an OR gate uses 4 um² of area and has 2 ns delay. Use the schematics generated from Vivado.

```
RCA: Cout = 2 AND gates + 3 OR gates = 2*3ns + 3*2ns = 12ns

Sum = 3 XOR gates = 3 * 3ns = 9ns

Total = 4 * Cout + Sum = 4*12 + 9 = 57ns

CLA: Total = 2 OR gates + 1 AND gate + 1 XOR gate

Total = 2 * 2ns + 3ns + 3ns

Total = 10ns
```

2. Why does the load register used in the datapath require a clock?

Because the load register takes some propagation time to store the input bits in the internal flip flops, using the clock will ensure that it has the required time to do this before changing the input lines.

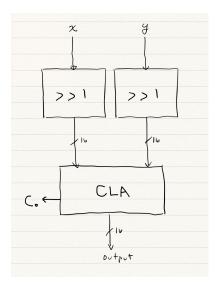
3. In 10 words or less, how would you change your load register module so that it loaded when btnC was both pressed and released?

Change contents of always@(posedge clk) to always@(load).

4. In 20 words or less, why is multiplexing useful in datapath components?

It simplifies control and manipulation of large amounts of bits, useful for data storage.

5. Without using any logic gates or other components except one single CLA with 16-bit inputs a and b, draw the datapath circuit that would calculate the average of two 16-bit values x and y, truncated to the nearest integer.



6. Suppose I instantiated a subtractor, multiplier, and divider into your datapath such that it outputs into the same load register as your RCA and CLA. How many more buttons would you have to use to accommodate my additions?

If there are 5 different possible input values, and you need n input lines for 2^n values, then you would need at least 3 ($2^3 = 8$) buttons total.