Cole Maxwell (25017014): ECE 658

Lab 2: Design of a Bitslice Accumulator

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**Step 1: Truth Table**

* Full adder

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **A** | **CIN** | **RST** | **FF Current State** | **D** | **COUT** |
| 0 | 0 | 0 | 0 |  |  |
| 0 | 0 | 0 | 1 |  |  |
| 0 | 0 | 1 | 0 |  |  |
| 0 | 0 | 1 | 1 |  |  |
| 0 | 1 | 0 | 0 |  |  |
| 0 | 1 | 0 | 1 |  |  |
| 0 | 1 | 1 | 0 |  |  |
| 0 | 1 | 1 | 1 |  |  |
| 1 | 0 | 0 | 0 |  |  |
| 1 | 0 | 0 | 1 |  |  |
| 1 | 0 | 1 | 0 |  |  |
| 1 | 0 | 1 | 1 |  |  |
| 1 | 1 | 0 | 0 |  |  |
| 1 | 1 | 0 | 1 |  |  |
| 1 | 1 | 1 | 0 |  |  |
| 1 | 1 | 1 | 1 |  |  |

**Step 2: Create Schematic**

**Step 3: Check Functionality of Schematic**

**Step 4: Determine Maximum Clock Frequency**

**Step 5: Power**

**Step 6: Layout**