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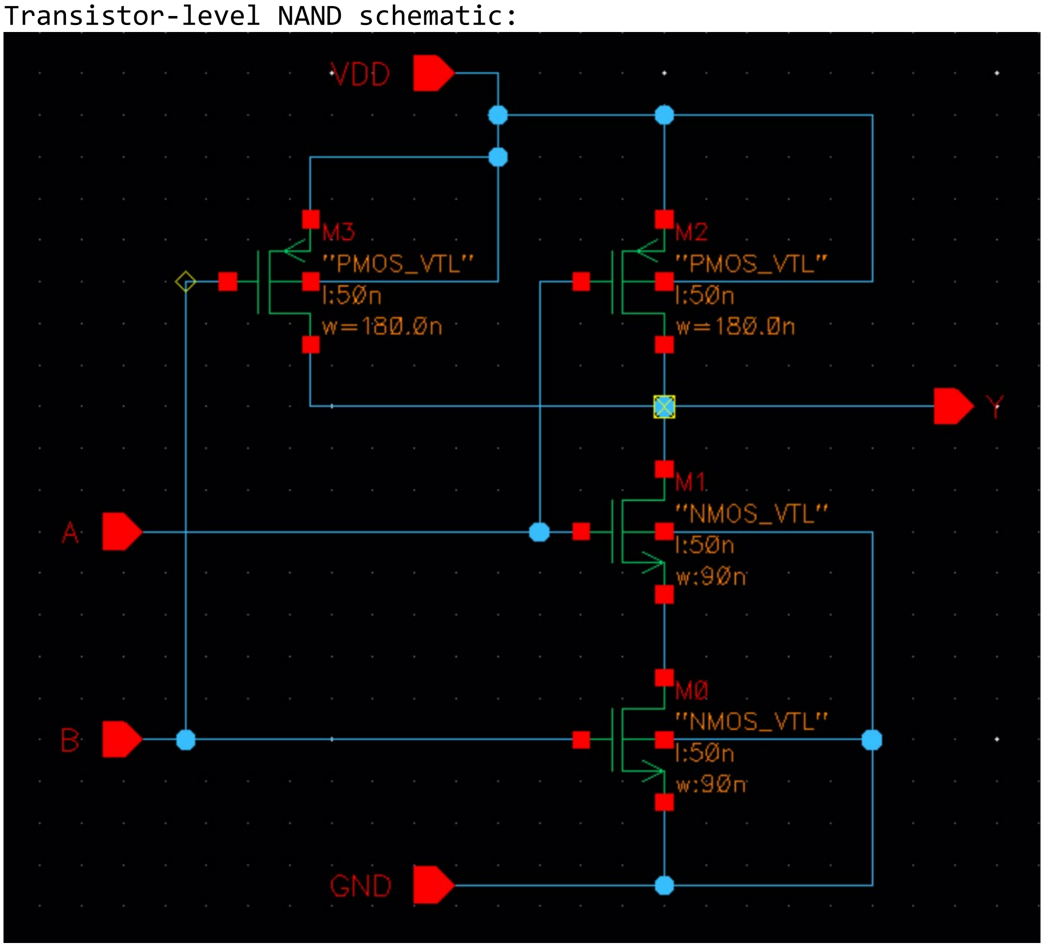
Lab 1: Design and Analysis of CMOS Multiplexer
September 28, 2020

Step 1: Truth Table

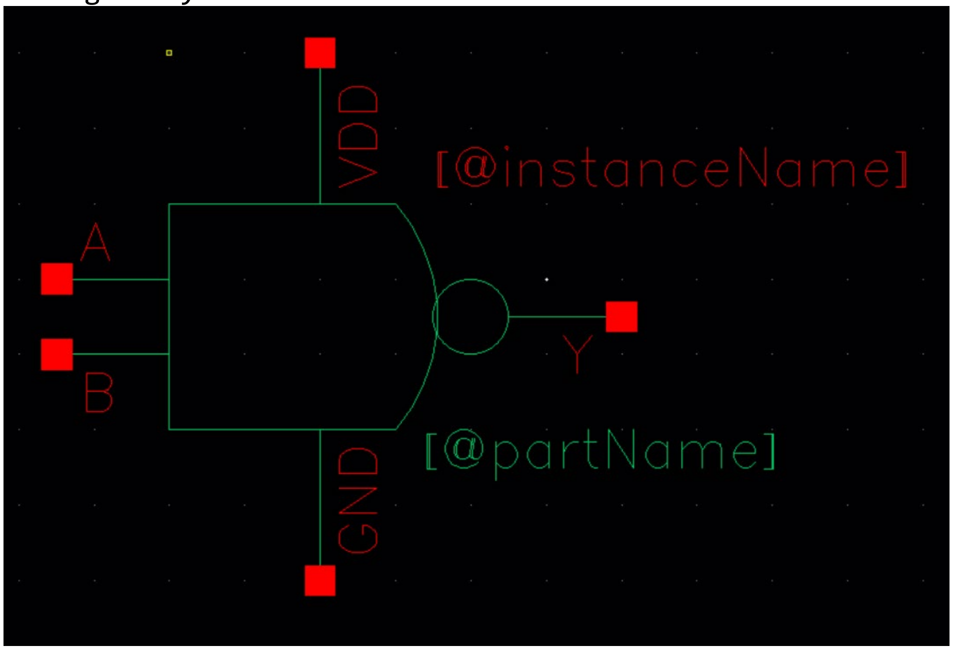
2:1 multiplexor
- When S = 0, Y = A; when S = 1, Y = B

S	B	A	Y
0	0	0	**0**
0	0	1	**1**
0	1	0	**0**
0	1	1	**1**
1	0	0	**0**
1	0	1	**0**
1	1	0	**1**
1	1	1	**1**

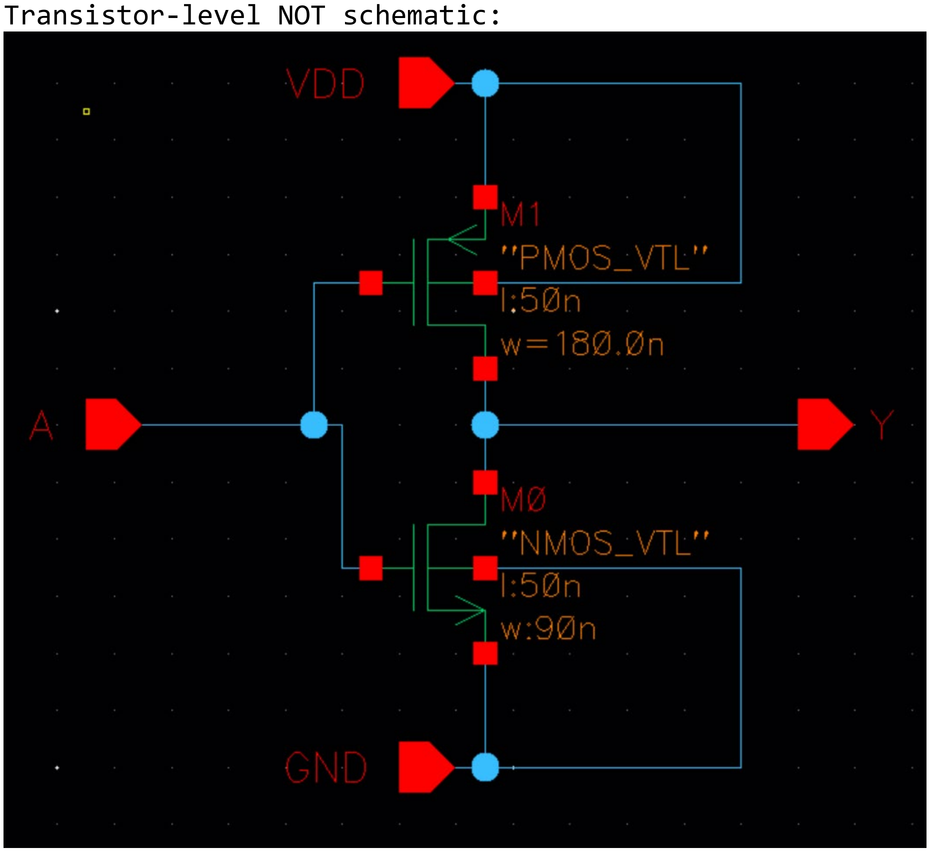
Step 2: Create Schematic
Transistor-level NAND schematic:



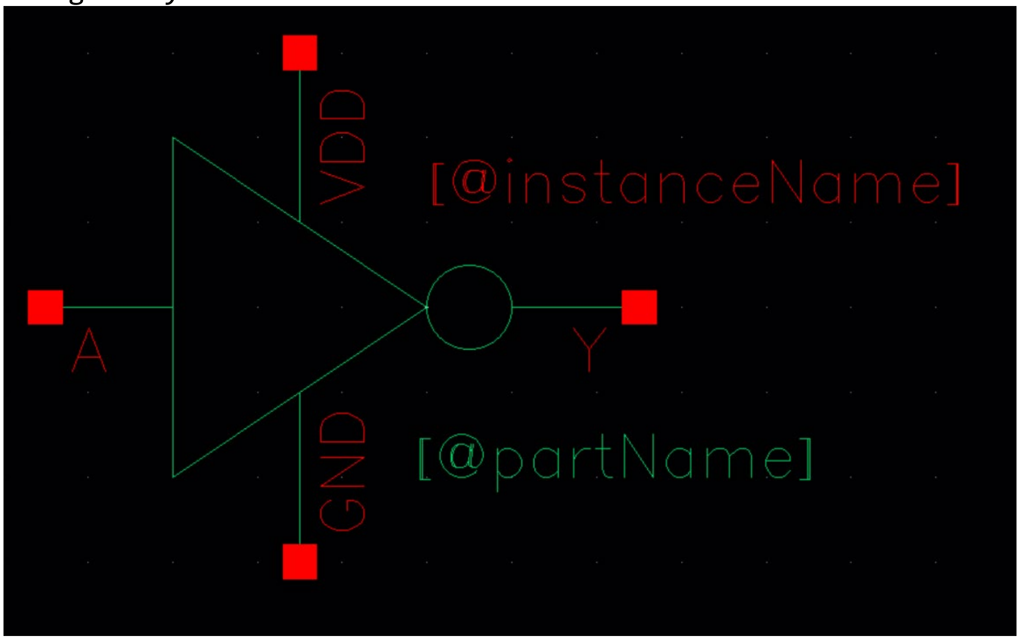
NAND gate symbol:



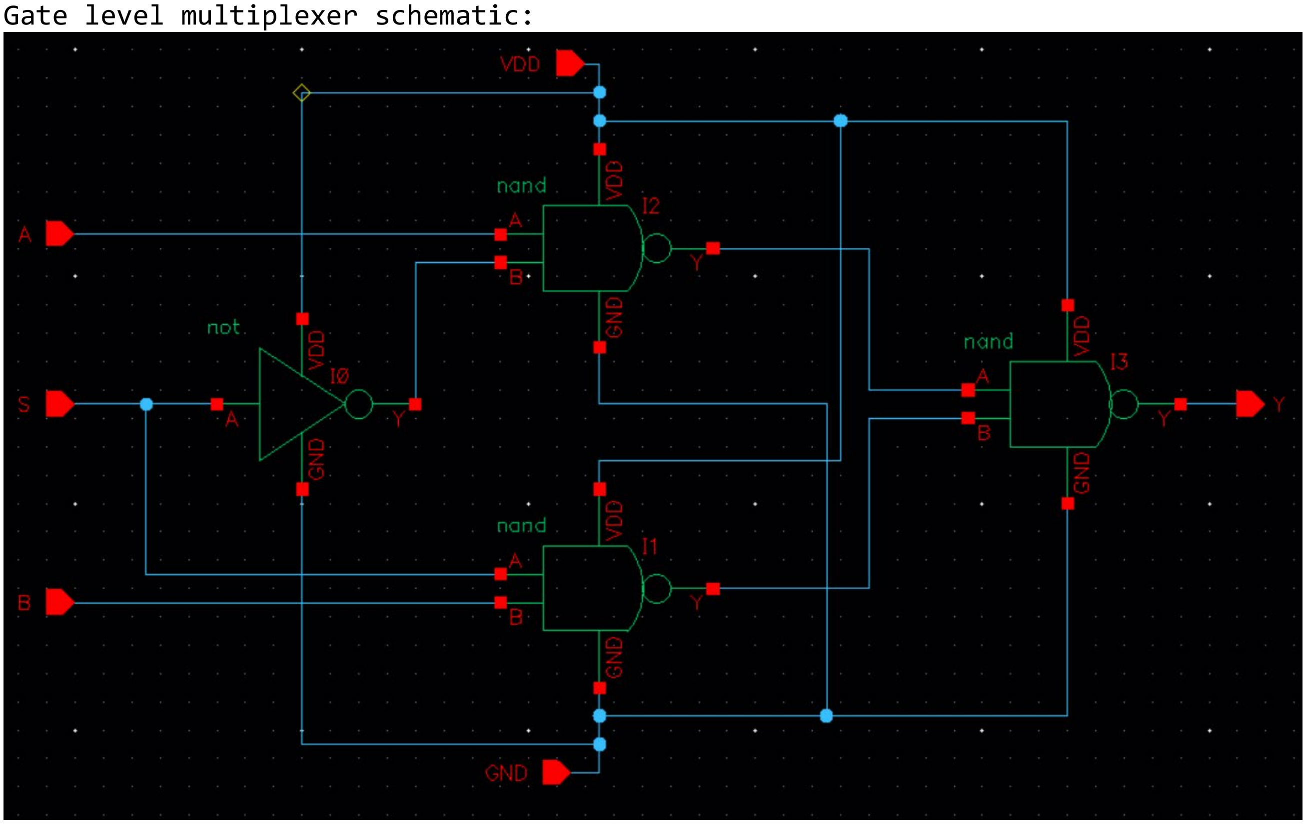
Transistor-level NOT schematic:



NOT gate symbol:



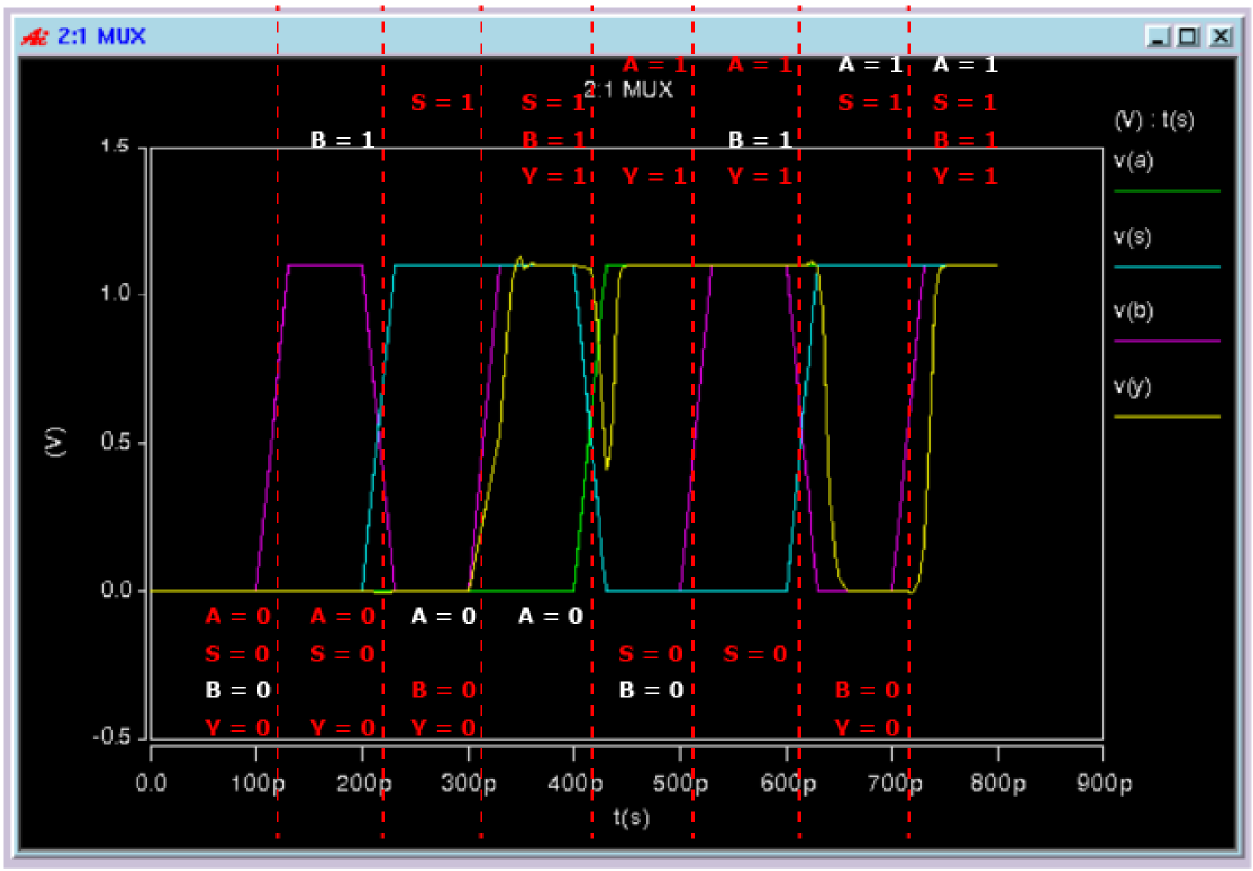
Gate level multiplexer schematic:



Step 3: Check Functionality of Schematic

The graph below demonstrates the function of the 2:1 mux. The simulation is separated into 8 segments, denoted by the vertical red dotted lines. In each stage, the applicable signal values are also shown in red. The graph shows that the value of the select bit chooses whether A or B is reflected in the output.

- When select (S) = 0, the output (Y) matches the value of A.
- When select (S) = 1, the output (Y) matches the value of B.



Step 4: Worst-Case Transitions

The table below displays all patterns in which a transition on a single input causes a transition in the output. The critical transitions and their measurements are highlighted in orange.

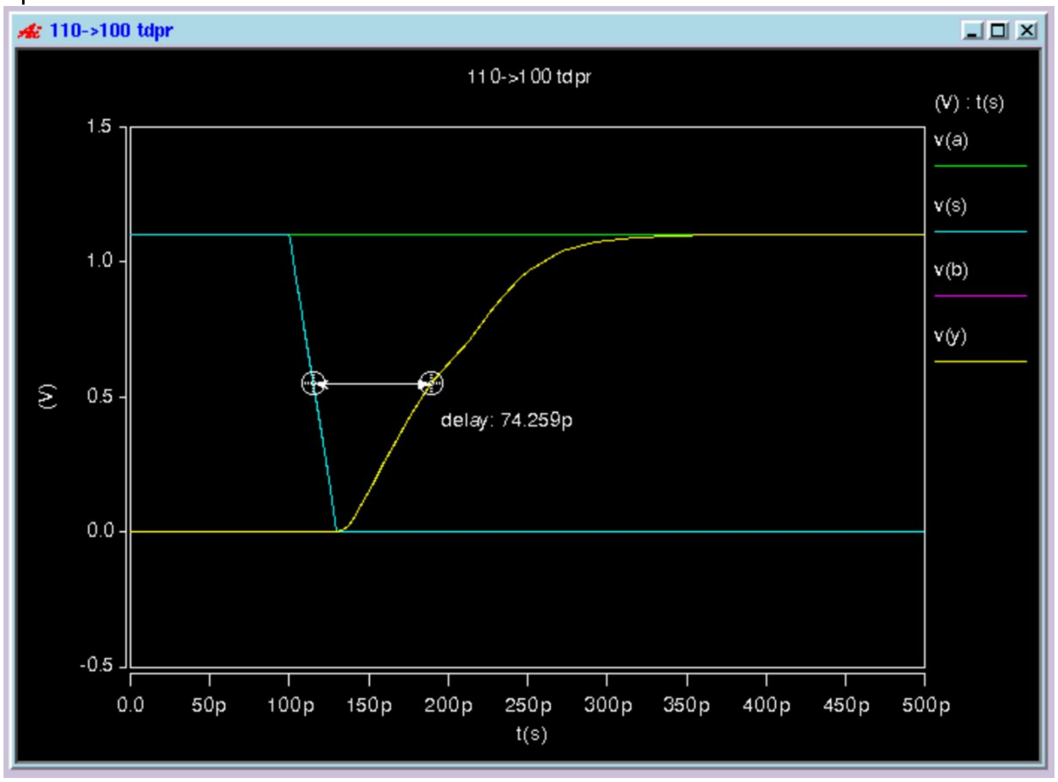
Input transition	Output transition	tpdf	tpdr	tf	tr
000 -> 100	0 -> 1		1.8697E-11		7.6695E-12
100 -> 000	1 -> 0	1.5802E-11		9.0407E-12	
001 -> 101	0 -> 1		1.7751E-11		7.5015E-12
101 -> 001	**1 -> 0**	1.3744E-11		**9.9648E-12**	
011 -> 001	**1 -> 0**	1.4609E-11		**1.0116E-11**	
001 -> 011	0 -> 1		1.8899E-11		8.3493E-12
110 -> 100	**0 -> 1**		**2.0560E-11**		7.0845E-12
100 -> 110	**1 -> 0**	**2.3768E-11**		8.7714E-12	
111 -> 110	1 -> 0	1.6473E-11		9.7874E-12	
110 -> 111	0 -> 1		1.8667E-11		8.6699E-12
010 -> 011	**0 -> 1**		1.9013E-11		**8.9685E-12**
011 -> 010	1 -> 0	1.5954E-11		8.9995E-12	

Step 5: Performance Analysis with Loading

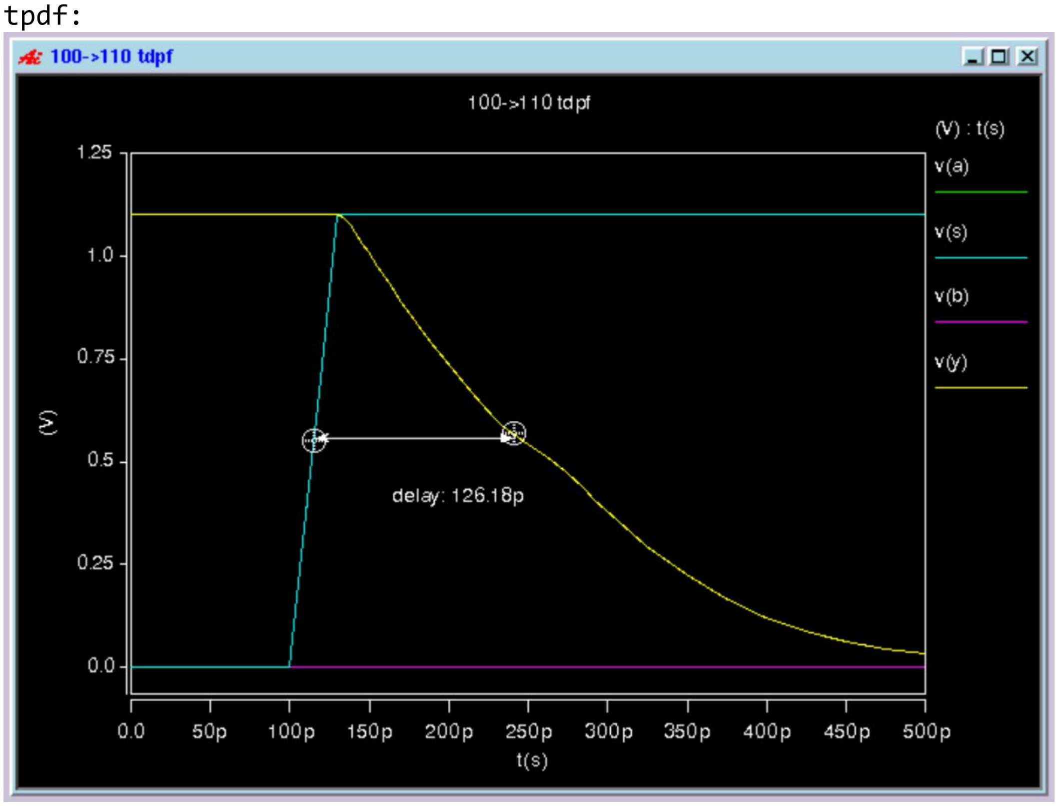
measure	tpdr	tpdf	tr	tf	Pstat	Pdyn
transition	110->100	100->110	010->011	011->001	000->000	000->111
val step 5	7.4247E-11	1.3190E-10	8.0232E-11	1.7970E-10	3.1527E-07	7.2952E-04
val step 6	4.6978E-11	7.9968E-11	5.0040E-11	1.0892E-10	2.0552E-06	4.5778E-03
val step 8	9.5030E-11	1.5312E-10	8.9606E-11	1.9334E-10	3.0964E-07	7.1405E-04

Simulation waveforms:

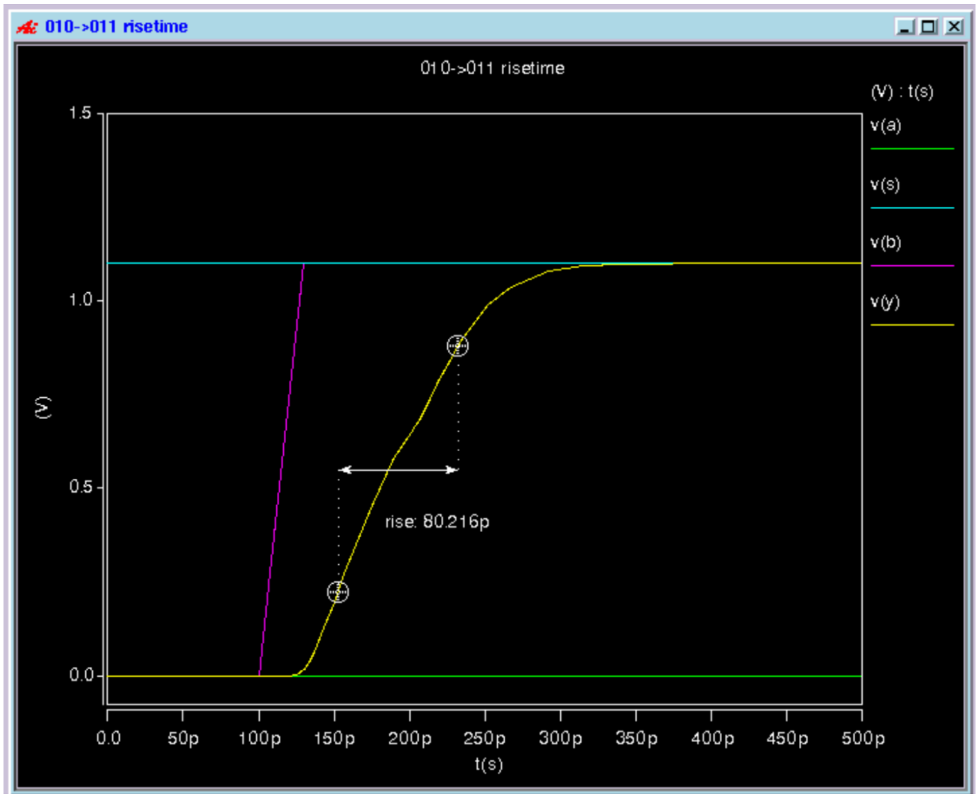
tpdr:



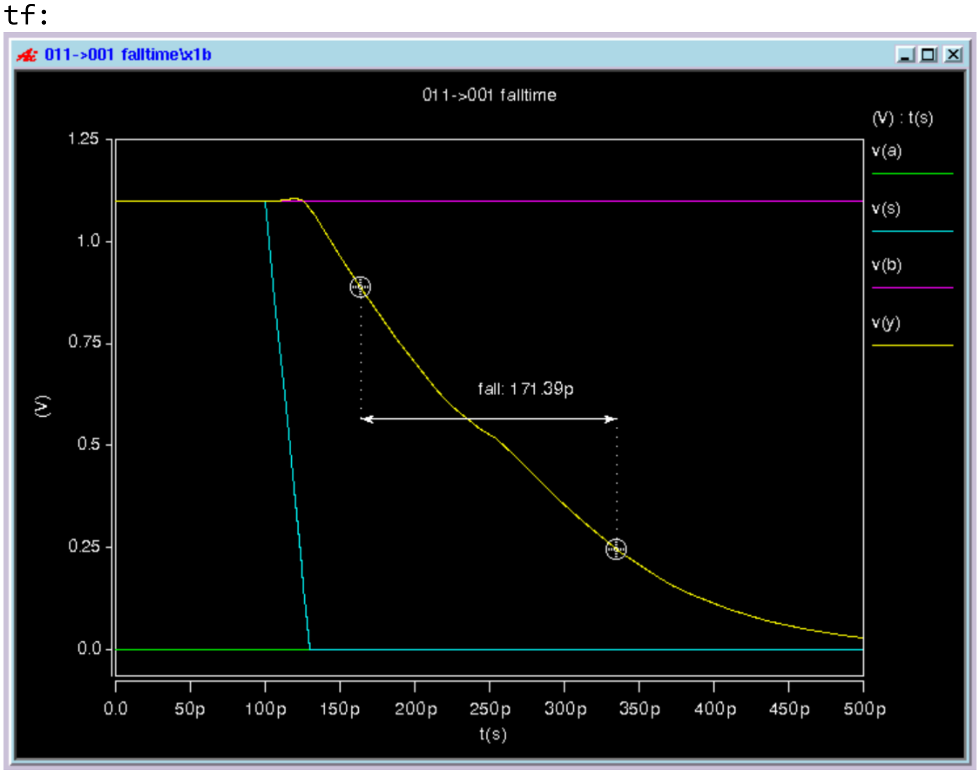
tpdf:



tr:


010->011 risetime
010->011 risetime
(V) : t(s)
v(a)
v(s)
v(b)
v(y)
1.5
1.0
0.5
0.0
(V)
rise: 80.216p
0.0
50p
100p
150p
200p
250p
300p
350p
400p
450p
500p
t(s)

tf:


011->001 falltime\x1b
011->001 falltime
(V) : t(s)
v(a)
v(s)
v(b)
v(y)
1.25
1.0
0.75
0.5
0.25
0.0
(V)
fall: 171.39p
0.0
50p
100p
150p
200p
250p
300p
350p
400p
450p
500p
t(s)

Difference between step 5 and step 4 measurements:

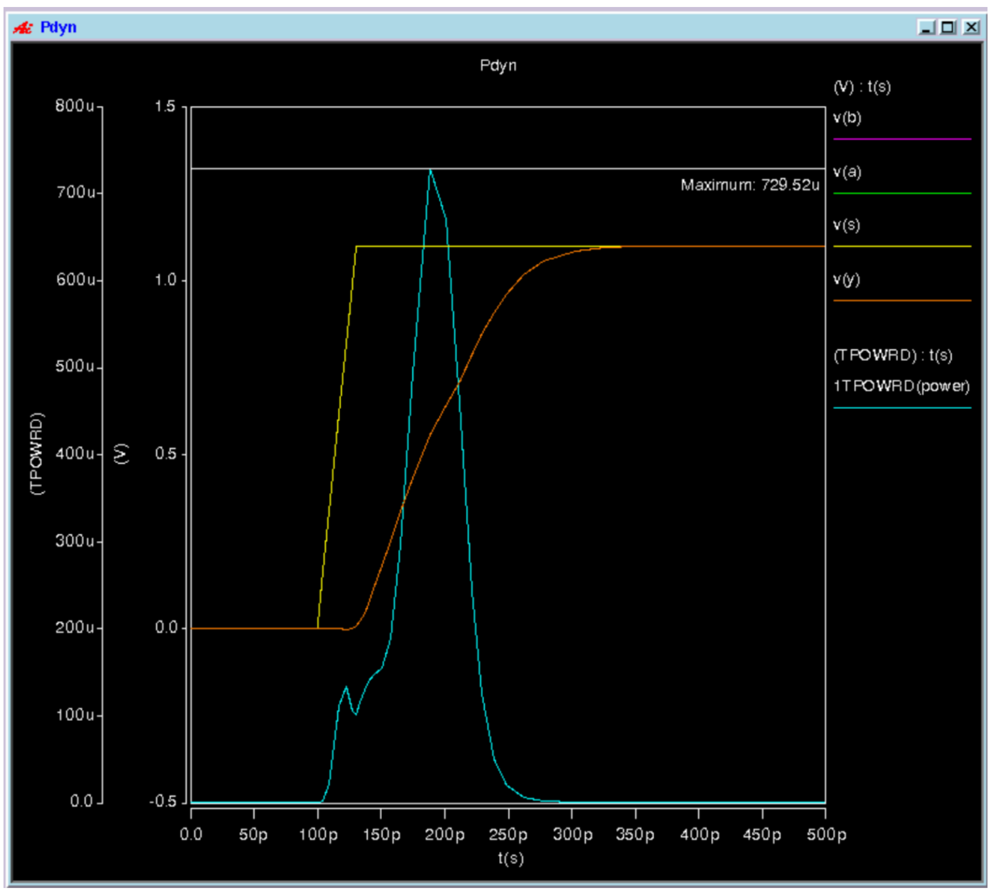
The measurements in step 5 are larger than the same measurements in step 4 due to the capacitive load generated by the 16 inverters and 7fF lumped wire capacitance.

Static power:

Pstat was determined in HSPICE with *.MEASURE tran avgpower AVG power from=1ps to=500ps* to measure the power while the inputs and outputs were not switching during the 000->000 transition.

Peak dynamic power:

Pdyn was determined in HSPICE with *.MEASURE tran peakpower MAX power from=1ps to=500ps* to measure the maximum power during the 000->111 transition. It is also plotted in Cscope, and the value is highlighted in the following graph.



Step 6: Resizing

Modified transistor sizes:

PMOS W = 180.0n * 6 = **1080n**
NMOS W = 90.0n * 6 = **540n**

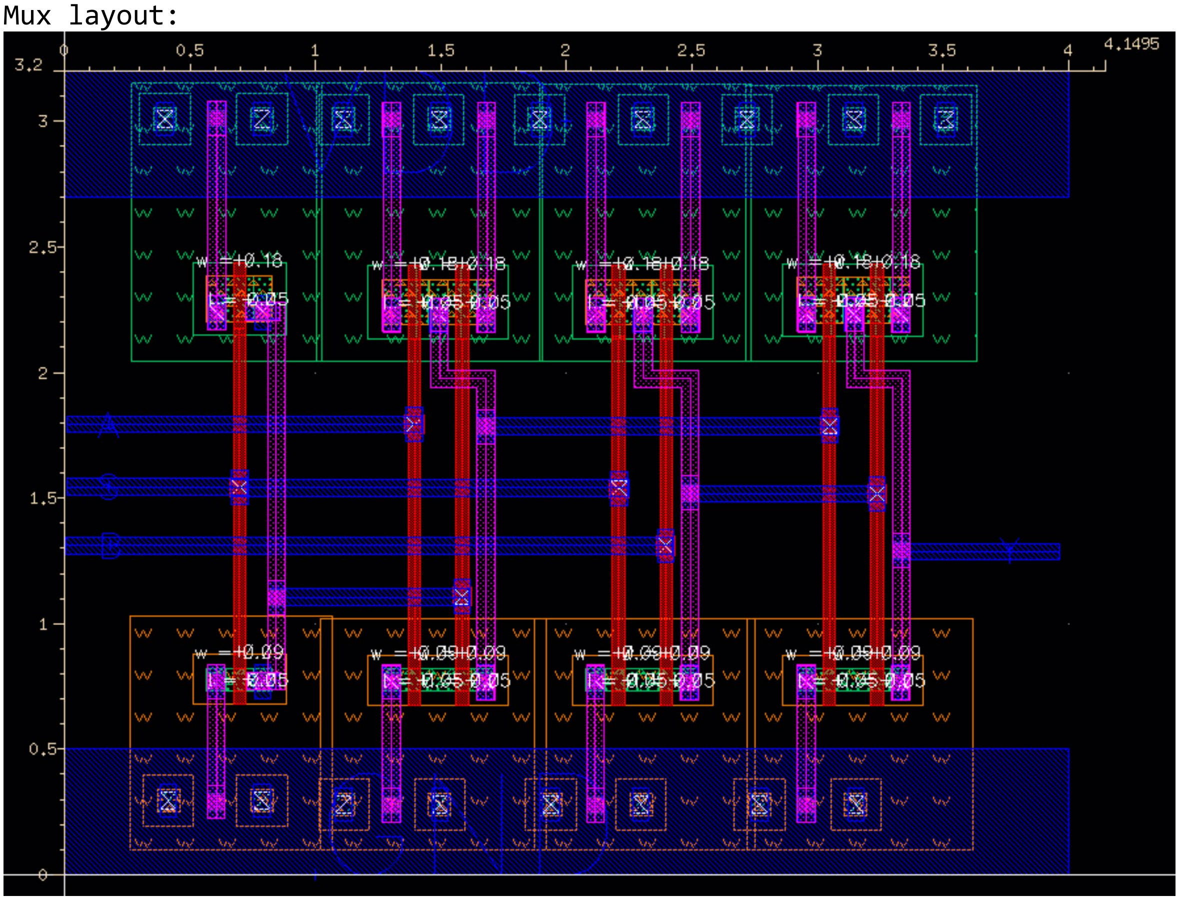
Measurements:
For measurements, see table from step 5, row “val step 6”.

Differences between step 5 and step 6 results:

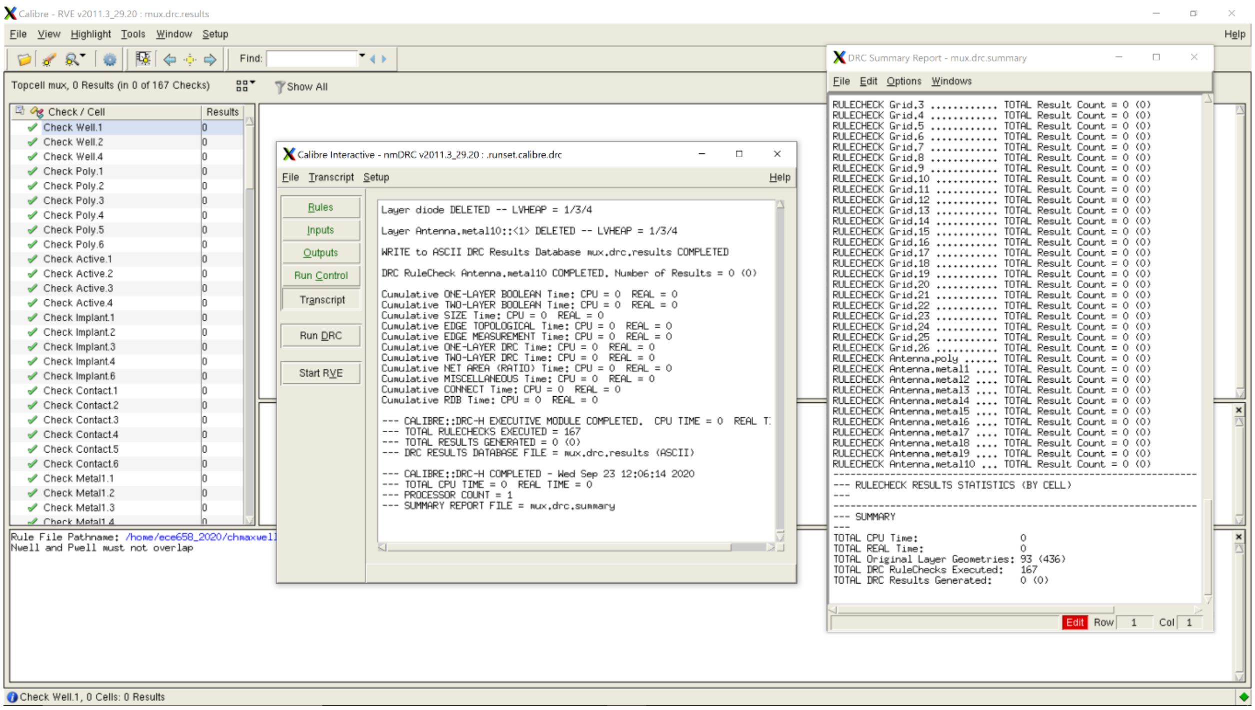
Increasing the width of the transistors by a factor of 6 improves switching time, as tpdr, tpdf, tr, and tf all decreased compared to step 5. However, this causes an increase in static and dynamic power consumption, as Pstat increased from 3.1527E-07 to 1.3592E-06, and Pdyn increased from 7.2952E-04 to 2.9930E-03. Generally, increasing the width of the transistors increases capacitance, which improves delay times, but requires more power.

Step 7: Layout

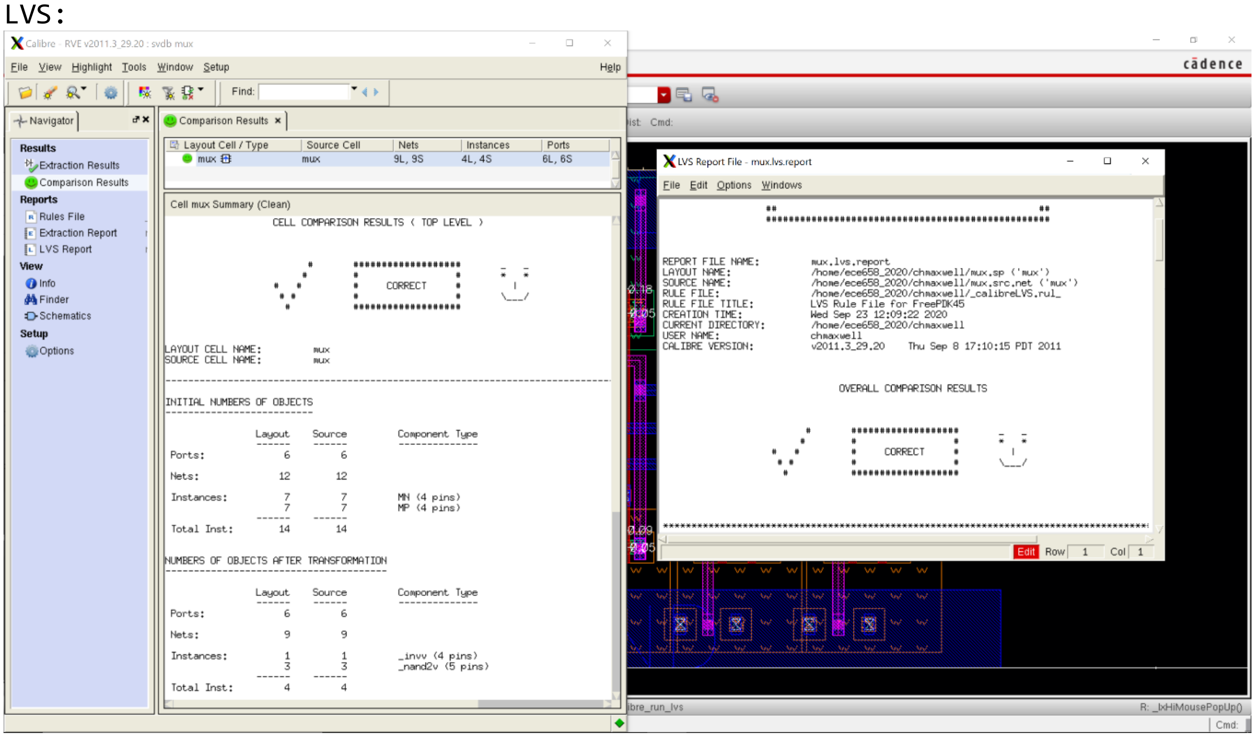
Mux layout:



DRC:



LVS:

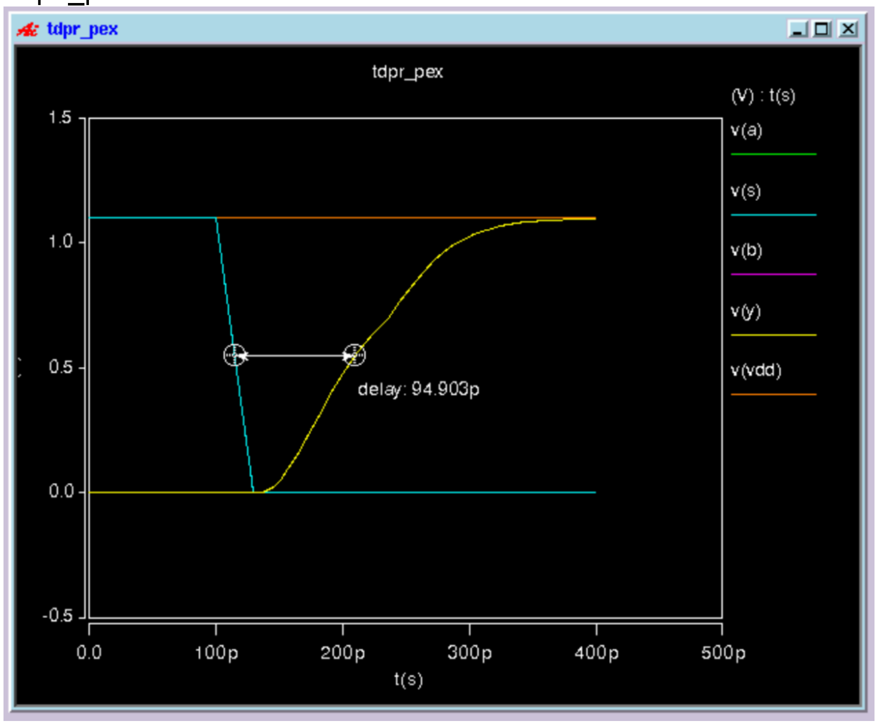


Step 8: Parasitics Extraction

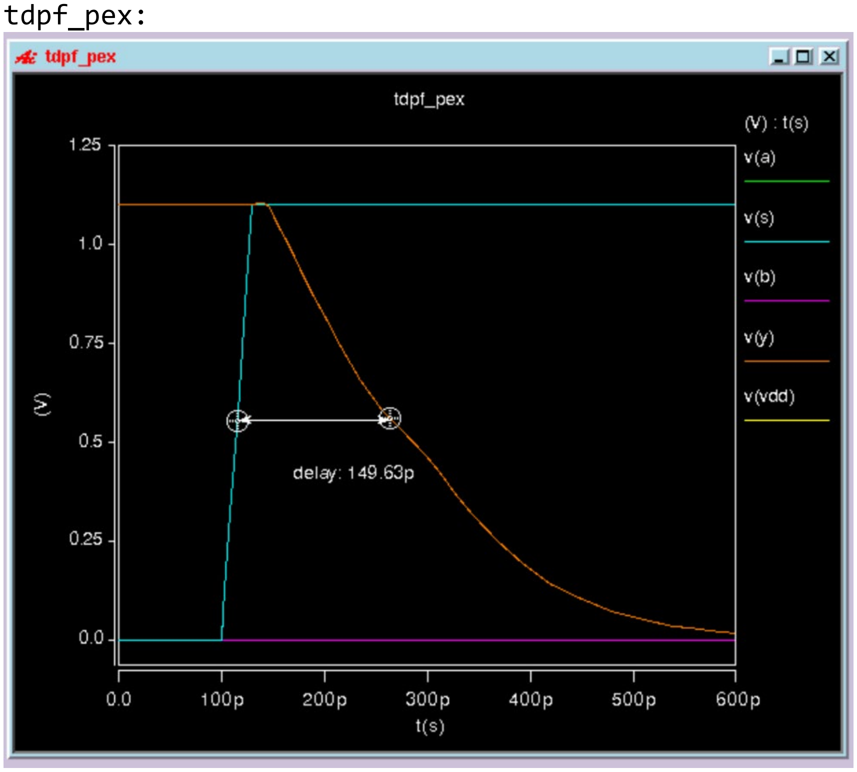
Measurements:

For measurements, see table from step 5, row "val step 8"

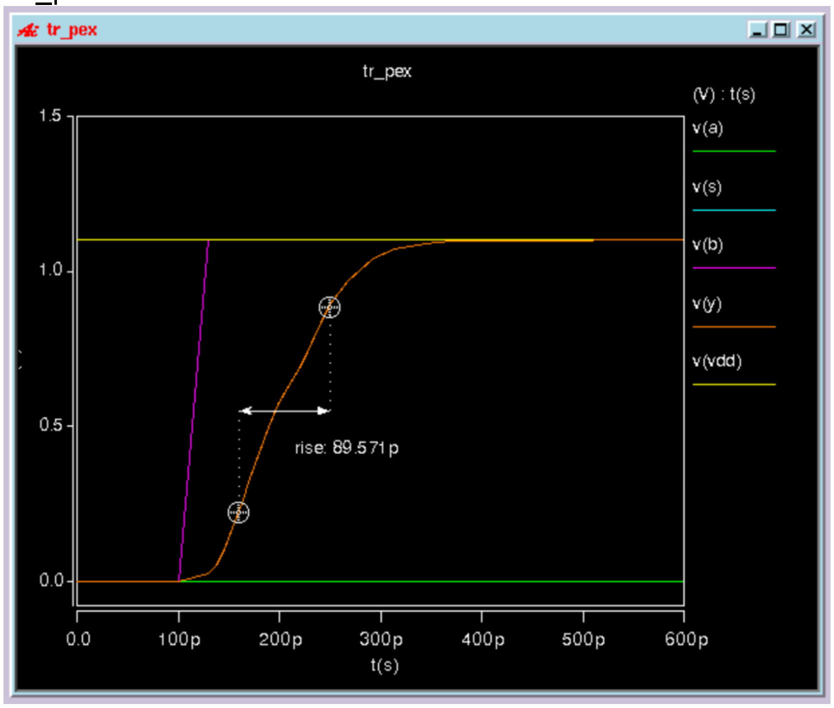
tdpr_pex:



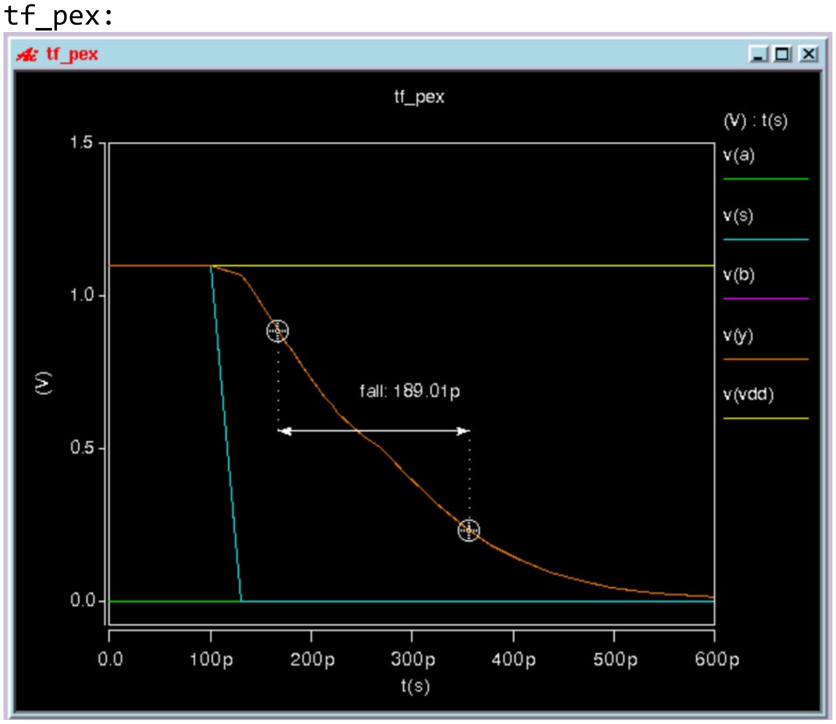
tdpf_pex:



tr_pex:



tf_pex:

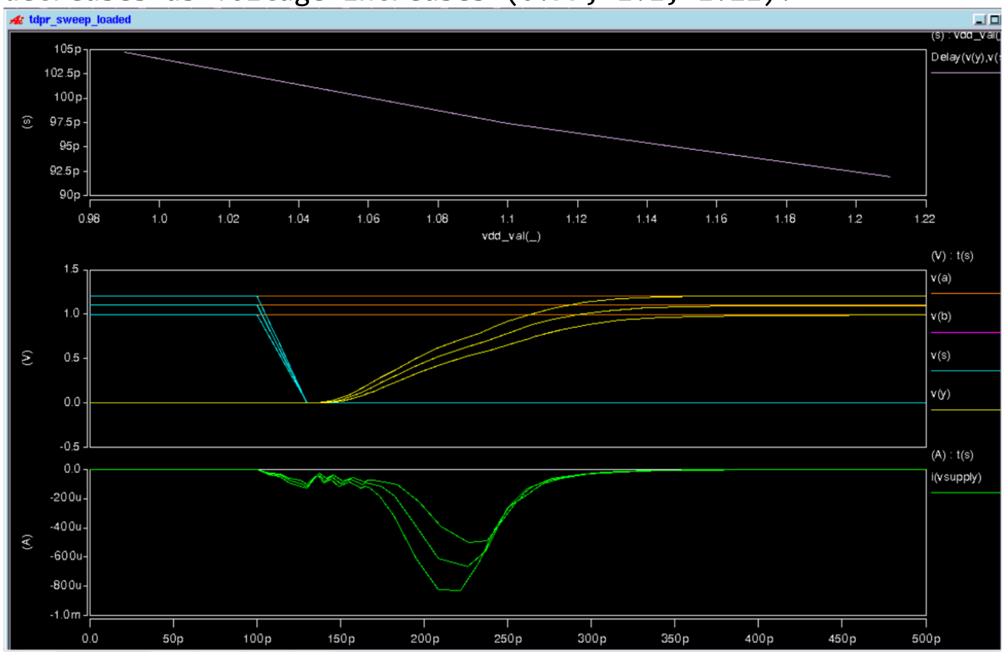


The simulation shows that parasitics cause performance delay times to increase, since tdpr, tdpf, tr, and tf are greater in step 8 than in step 5. While parasitics appear to have less of an effect on performance delay than does resizing transistors, parasitics are still significant.

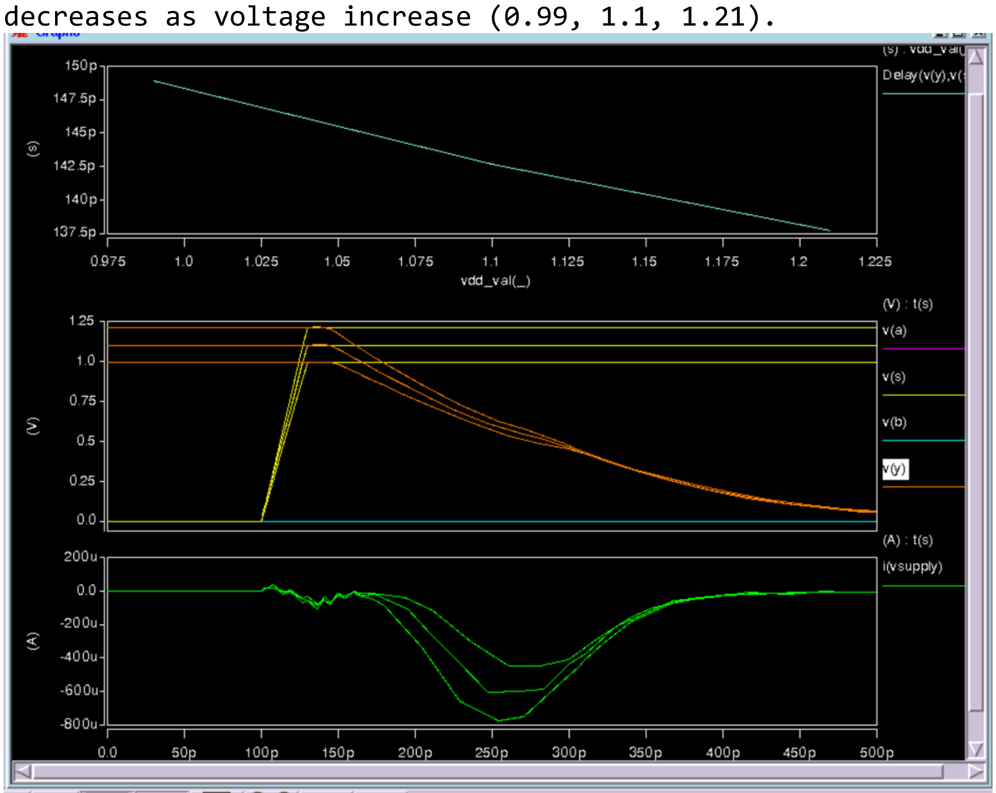
Step 9: Characterizing your Design

Step 9a:

Tpdr with changes in supply voltage. The top graph shows that delay time decreases as voltage increases (0.99, 1.1, 1.21).

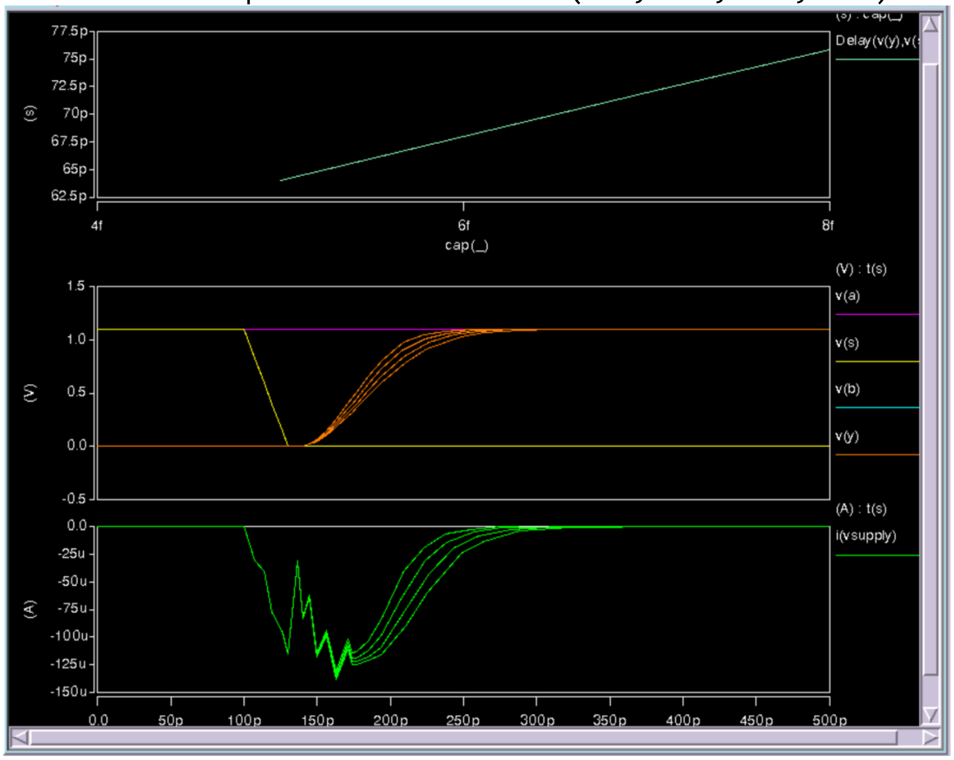


Tpdr with changes in supply voltage. The top graph shows that delay time decreases as voltage increase (0.99, 1.1, 1.21).

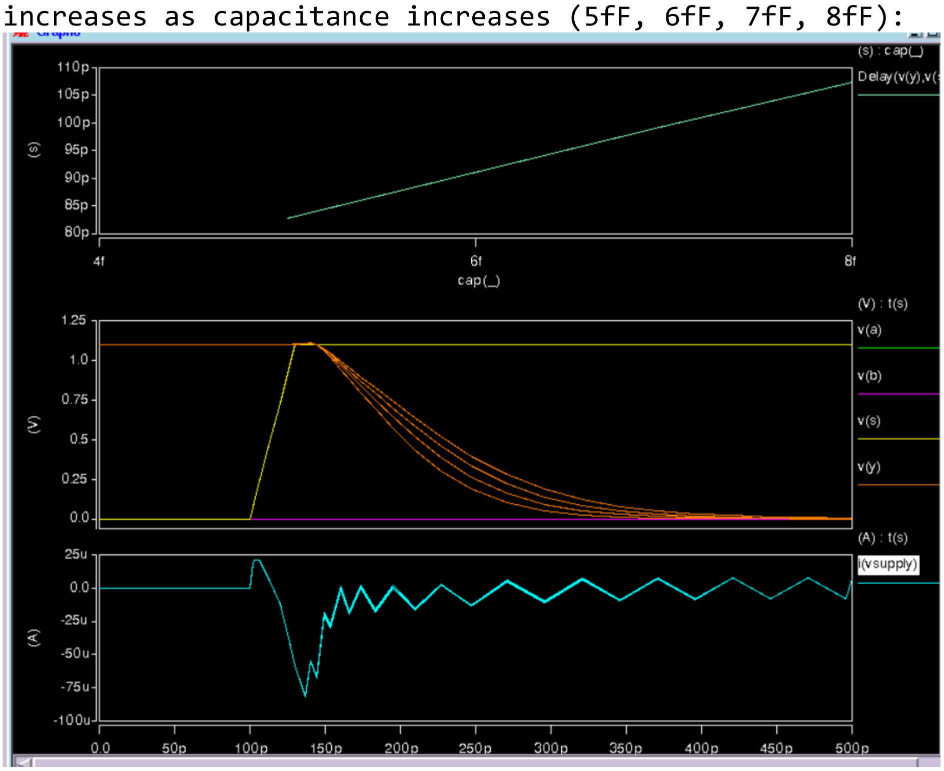


Step 9b:

Tpdr with changes in load capacitance. The top graph shows that delay time increases as capacitance increases (5fF, 6fF, 7fF, 8fF):



Tpdf with changes in load capacitance. The top graph shows that delay time increases as capacitance increases (5fF, 6fF, 7fF, 8fF):



Estimation of inverter cap and Cpermicron:

The following table shows the 4 delay measurements and their averages for tdpr and tpdf when the netlist is loaded with the 16 inverters and 7fF load.

Measurement	tpdr w/ inv	tpdf w/ inv
1	1.0467E-10	1.6231E-10
2	9.7390E-11	1.5225E-10
3	9.1856E-11	1.4653E-10
Average w/ inverters	**9.797e-11**	**1.537e-10**

Next, this table shows the 4 delay measurements and their averages for tdpr and tpdf when the 16 inverters are removed and the 7fF load is varied.

Measurement	Tpdr w/o inv	Tpfr w/o inv
1	6.4003E-11	8.2804E-11
2	6.7970E-11	9.1113E-11
3	7.1924E-11	9.9487E-11
4	7.5819E-11	1.0775E-10
Average w/o inverters	**6.993e-11**	**9.529e-11**

From here, we subtract the without-inverter averages from the with-inverter averages to determine the total amount of capacitance that was resulting from the inverters.

Then, we divide by 16 to find the load per inverter.

And finally, we divide the load per inverter by the combined length of the PMOS and NMOS inverters to determine Cpermicron in each case.

	tdpr	tdpf
Avg w inv	9.797E-11	1.537E-10
-	-	-
Avg w/o inv	6.993E-11	9.529E-11
=	=	=
Total load from 16 inverters	2.804E-11	5.841E-11
/ 16	/16	/16
=	=	=
Inverter cap estimation	**1.7525E-12**	**3.650625E-12**
/ length of CMOS transistors	/ 100um	/ 100um
=	=	=
Cpermicron	**17.525 fF per um**	**36.50625 fF per um**