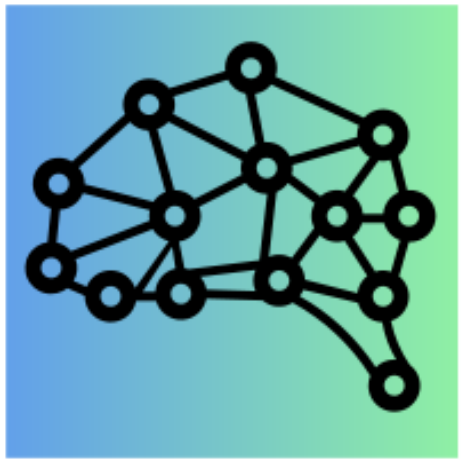

TIDENet

TinyML Image Detection on the Edge with Neural Networks

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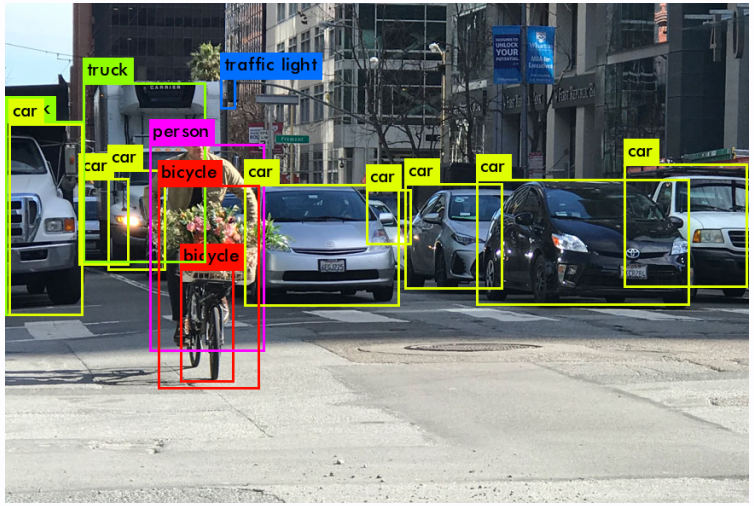
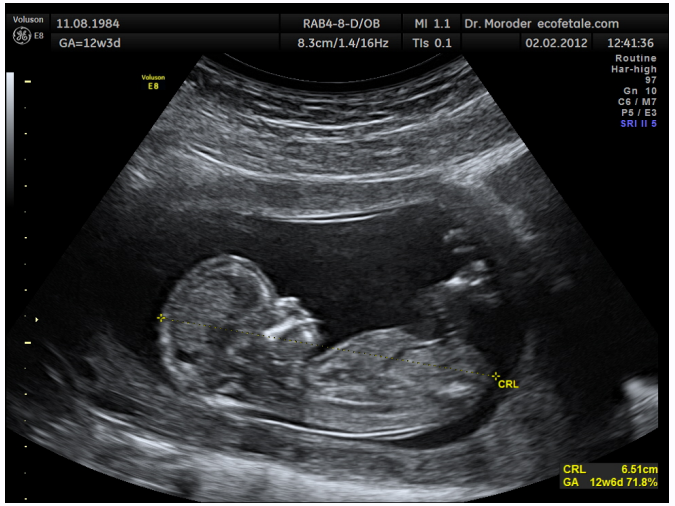
ASICs for real-time ML inference on images

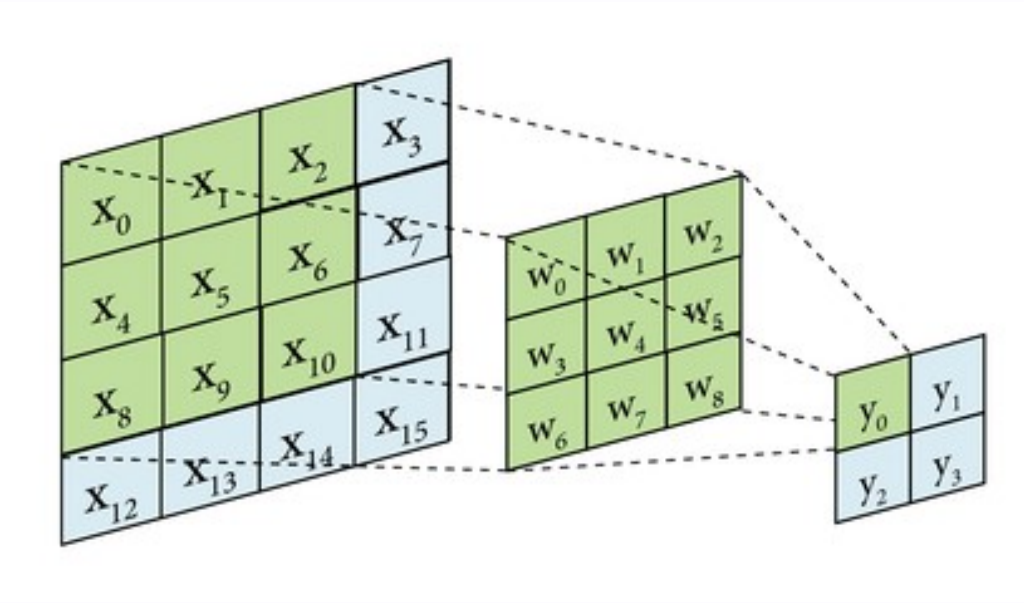
- Facial recognition (ex. security camera)
- Self-driving cars
- Medical image analysis



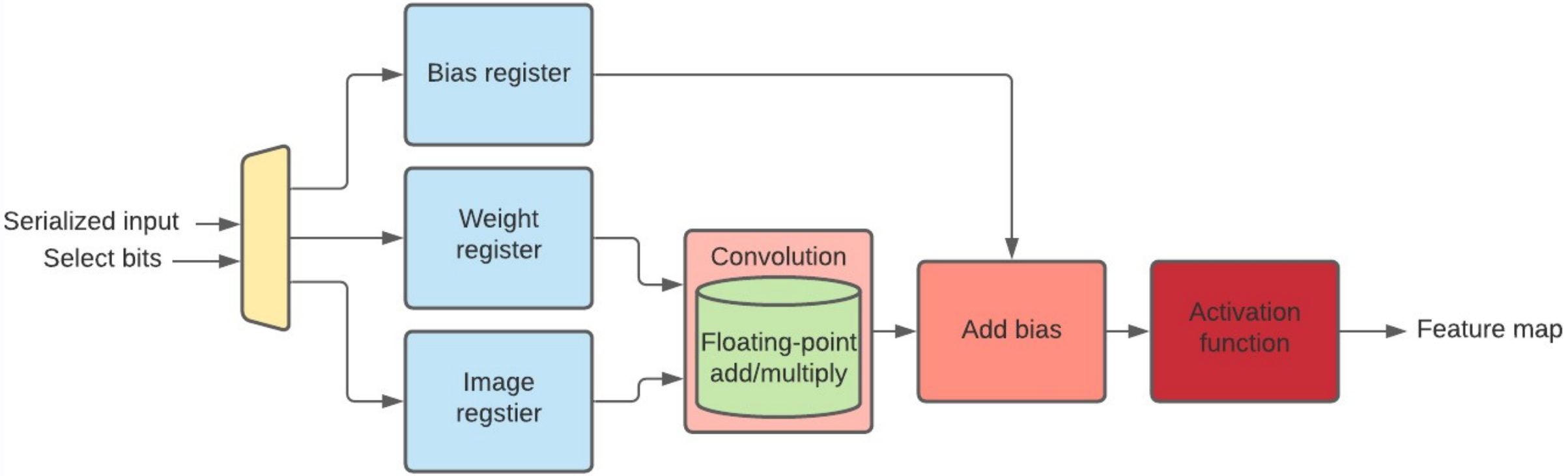


Convolutional NNs

- Pixel location matters
- Very common



Hardware diagram



Design goals

- Run a single convolutional layer on an ASIC
- Demonstrate advantages over DNNWeaver on FPGA

Workflow

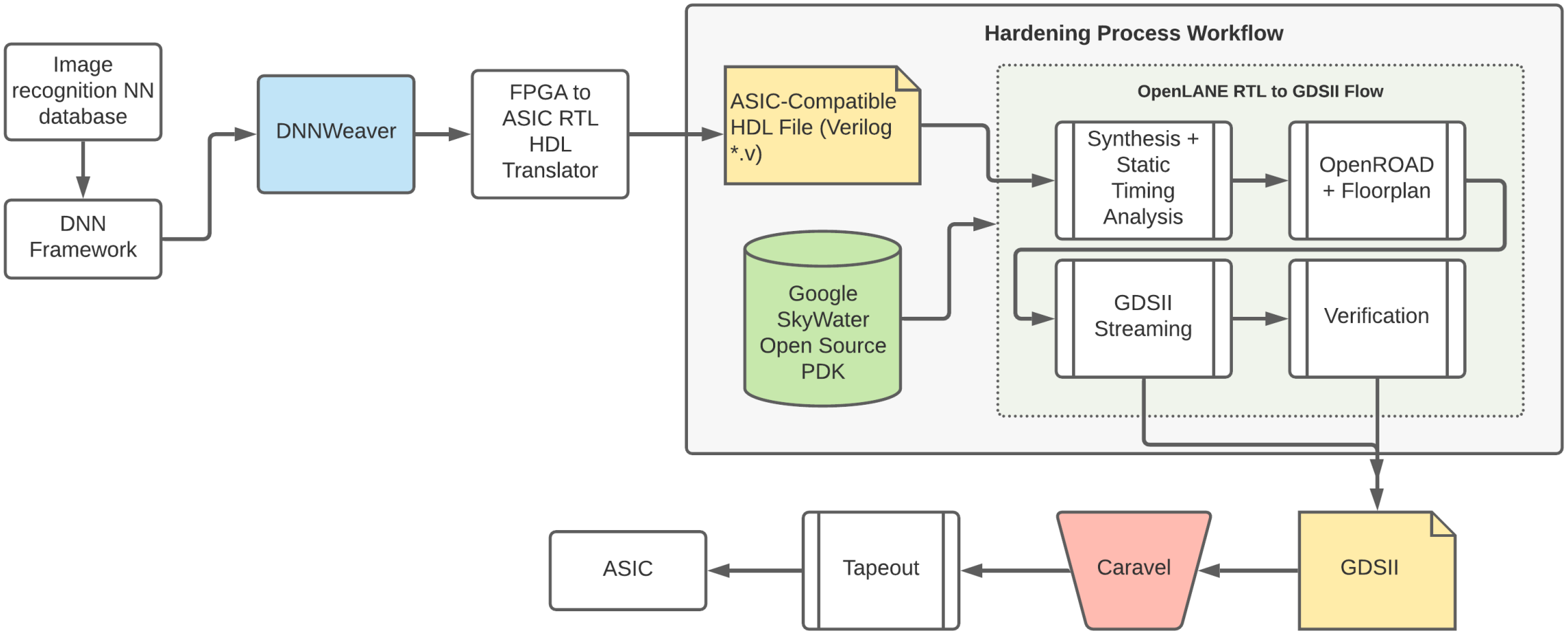


Image recognition NN database
DNN Framework
DNNWeaver
FPGA to ASIC RTL HDL Translator
Hardening Process Workflow
ASIC-Compatible HDL File (Verilog *.v)
Google SkyWater Open Source PDK
OpenLANE RTL to GDSII Flow
Synthesis + Static Timing Analysis
OpenROAD + Floorplan
GDSII Streaming
Verification
GDSII
Caravel
Tapeout
ASIC

Working with Caravel

- Hardened sample project and SHA3-256 from shuttle
- Gained familiarity with the OpenLane config file

Current status

- Writing HDL (Verilog) for use with OpenLANE/Caravel stack (OpenROAD, etc)
  - Implementing convolution and bias
  - Making registers

Upcoming challenges

- Efficient use of IO and memory
- Implementing floating-point operations*

Merging projects

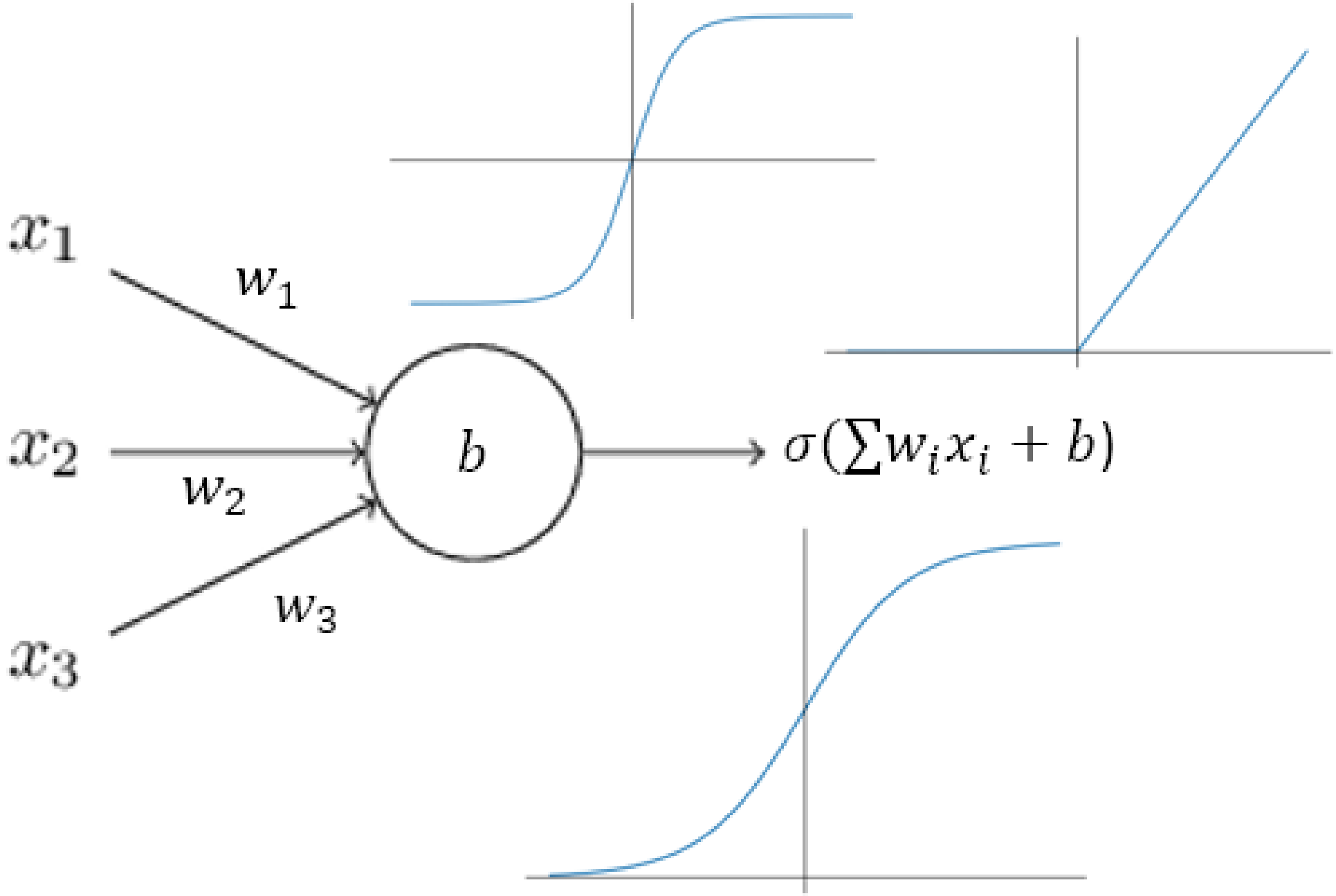
References

http://cctvtechworld.blogspot.com/2018/03/facial-recognition-will-soon-be-part-of.html

https://towardsdatascience.com/yolo-you-only-look-once-17f9280a47b0

https://commons.wikimedia.org/wiki/File:CRL_Crown_rump_length_12_weeks_ecografia_Dr._Wolfgang_Moroder.jpg

https://www.researchgate.net/figure/Example-of-a-discrete-convolution-a-and-equivalent-transposed-convolution-operation-b_fig2_321719286


x_1
w_1
x_2
w_2
b
$\sigma(\sum w_i x_i + b)$
w_3
x_3