PTAT Current Drivers for Neural Stimulation

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***Abstract*—Overview of the design decisions for a PTAT current source and sink using 65nm TSMC PDK technology.**

I. Introduction

THE complete system for neural stimulation is described in this report. Driver electronics must minimize loading effects due to the high-impedance of an implantable neural electrodes. This writeup discusses the method and implementation of maximum output impedance drivers, on the order of Gigaohms (GΩ).

A. Objective

Continuing the design for the neural stimulation, a current source driver is designed including layout for all devices, and a physical switch. The accuracy of the current source is verified by integrating the positive and negative current pulses. Most of the difficulty of this project was incorporating multiple components together and ensuring there is minimal charge discrepancy between them.

B. Top Level Schematic

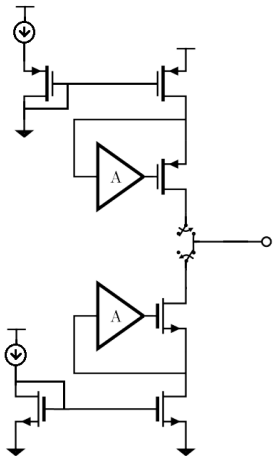

Fig. 1: Source and Sink Drivers with Gain-Boost

II. Design

The gain boosted cascode is applied to both the source and sink drivers. PMOS devices are implemented in the source driver and NMOS devices in the sink driver. The source operates from V_{DD} to the electrode voltage and the sink operates from the electrode voltage to ground. The theoretical R_{out} is defined as

$$R_{out} \approx [g_{m2} r_{01} r_{02} A_1] = 13.7G\Omega$$

The simulated R_{out} values are discussed in the results section.

A. Amplifier Stability

The frequency analysis of the amplifiers are included. In order to achieve stability, they are compensated with $500fF$ capacitors. The amplifiers are tuned so that they provide approximately the same gain and both achieve slightly greater than 60 degrees of phase margin. The response operates very close to a critically damped system, resulting in small overshoot and settling time. The sink driver has poles at approximately 20kHz and 200MHz and the source driver has poles at approximately 9kHz and 90MHz.

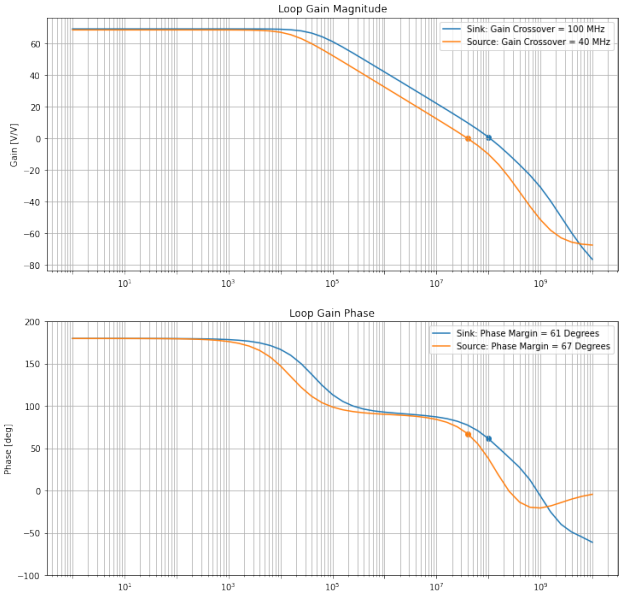

Fig. 2: Current Sink Driver Stability

B. Telescopic PMOS Differential Pair

The ideal gain for a differential telescopic amp is

$$A_v = g_{m1}(g_{m2} r_{04} r_{05} || g_{m6} r_{06} r_{07}) = 4288.$$

The measured gain is 3810, which accounts for the losses due to the tail current source and non-ideality.

Name	Device	W	L	g_m	r_{out}
M0	nch	5.3u	933n	304.8u	83.08K
M2	nch	9.81u	786.4n	460.2u	94.52K
M4	pch	4u	935n	137.2u	502.2K
M5	pch	4u	930n	138.9u	779.2K
M6	pch	14u	880n	141.2u	509.9K
M7	pch	14u	880n	142.3u	939.1K
M8	nch	14u	880n	142.7u	939.0K
M9	nch	14u	880n	442.6u	900.8K
M10	nch	4u	880n	137.1u	499.5K
M11	nch	4u	880n	137.0u	499.6K
M20	nch	4u	600n	151.7u	161.1K

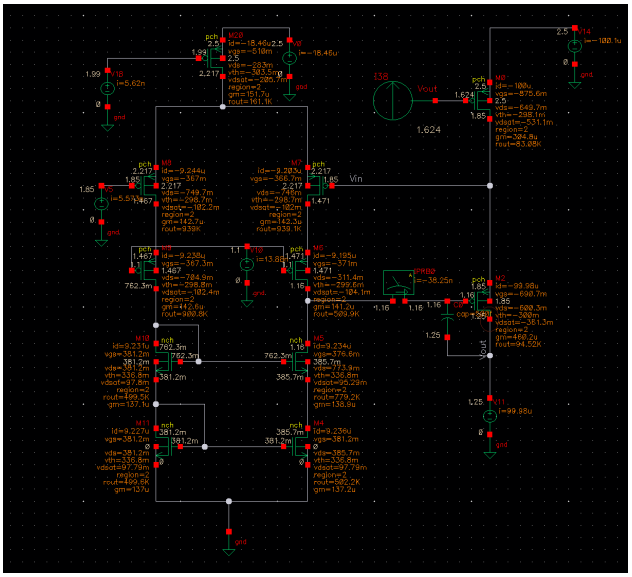

Fig. 3: Source Driver DC Operating Point

The source amplifier was originally designed to use the telescopic NMOS differential amp from the sink driver. The goal was to simplify and reuse as many components as possible. However, the dc input voltage ultimately resulted in a design change. The NMOS differential input has to be large enough to keep the bottom cascode in saturation such that the input voltage is at least $V_{DD}/2 + V_{DSat,Cas}$. The telescopic amplifier also must support several V_{DSat} from $V_{in} - V_{gs}$. This bias requirement is very difficult to achieve. Thus, our driver design implements a PMOS differential telescopic amplifier which supports all the device requirements.

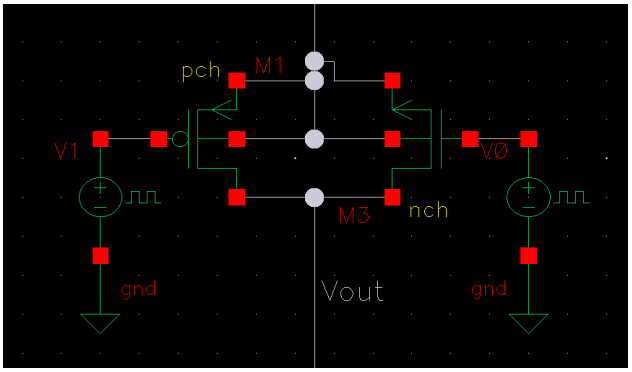

Fig. 4: Source Driver Switch

III. Results

The total output resistance of the source driver is 8.28GΩ with a current of $99.79\mu A$. This is very close to the updated sink output resistance of 8.32GΩ with a current of $99.88\mu A$. Ideally, we want the two drivers to match as close as possible in current and resistance so that the electrode sees no difference between the charge taken and deposited. This solution prioritizes matching the source and sink drivers rather than achieving marginally improved gain and/or resistance in a single driver.

The electrode waveform of the full solution including physical switches is provided. The resulting waveforms show the precise work of our design and demonstrate very low variance between peaks. In the first plot, the voltage waveform reaches it's steady state after a single period and has a very predictable swing every following period. The second plot shows the simulated current pulses. We came close to reaching our $100\mu A$ target, however it was limited by the non-ideal switch we placed in there both allowing some current to pass when the switch was off and limiting the voltage at the cascode. Lastly, the integral of the current is shown to evaluate the amount of charge deposited and withdrawn from the electrode. The charge balance is calculated by taking the difference of two points that are one period apart. Thus, we determined that we had a very low charge discrepancy and this is also discussed in the conclusion.

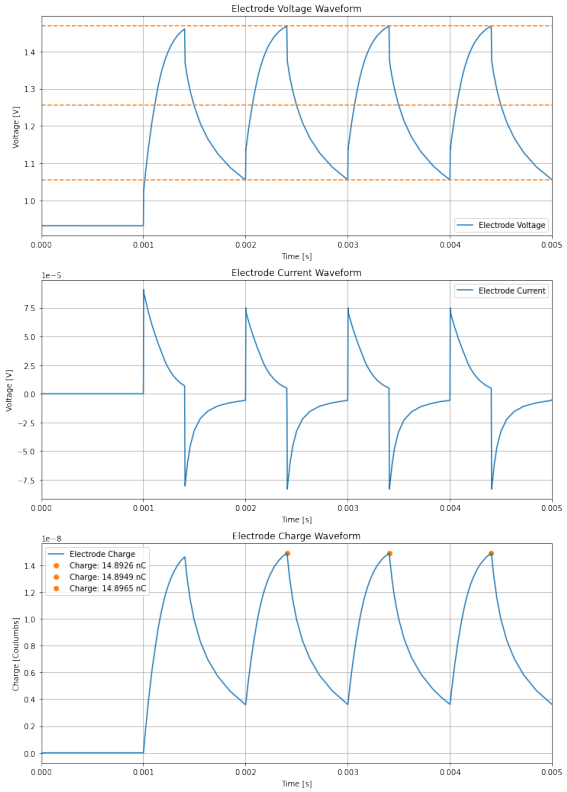

Fig. 5: Electrode Waveforms

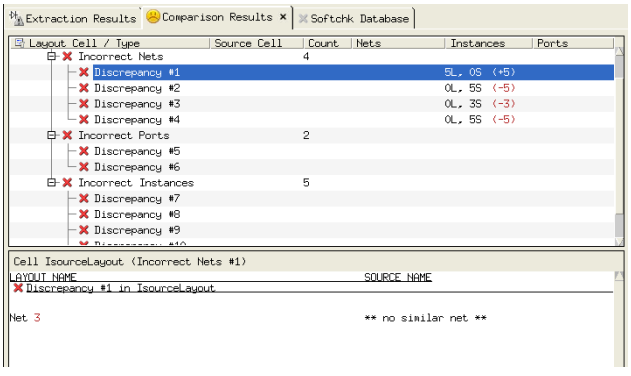

Fig. 6: LVS: Incorrect Nets

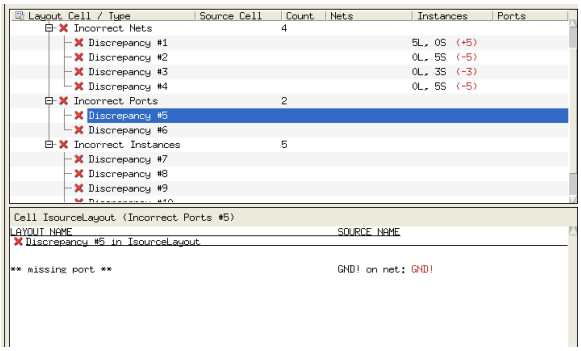

Fig. 7: LVS: Missing Ports

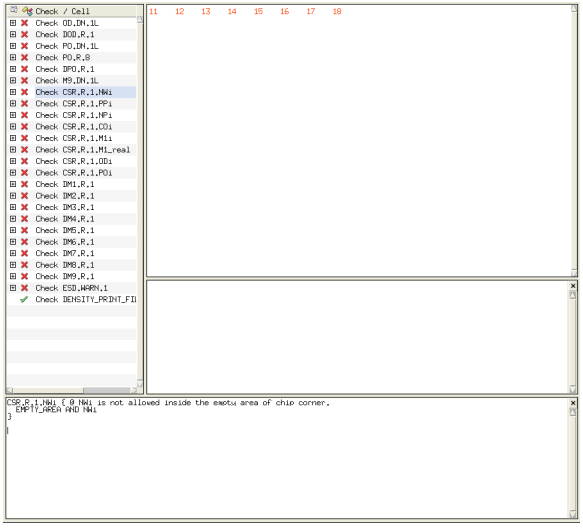

Fig. 8: DRC: Empty Area and NWi

We were unable to achieve a perfect match from our schematic to the layout as seen in the LVS report. Most of the error messages were resolved, however, there are a few that couldn't be determined even with additional resources. Some of these errors are provided in *V. Additional Figures*.

For example, the LVS report lists that *net3* is not matched to our schematic, however, there is no *net3* on our schematic or layout. It also generated an error for not including our stability capacitor and stability test circuit, but it's unclear how to add those. Additionally, there was no GND! and PTAT IO pins despite there being both pins and labels for each.

The output from the DRC program is provided in Figure 8. The report shows many failed checks, with a lot of errors being related to the same thing. Similar to layout CAD project 3, we fixed all of the errors pertaining to sizing, n and p doped regions, oxide overlaps, contact sizes, etc. In the end, we were left with the following errors that we were unable to solve despite multiple attempts. Most remaining problems relate to chip space issues and missing layers that we did not recognize and are still unable to identify. We are unsure if they would create problems in fabrication or if they are harmless errors like we had at the end of CAD 3.

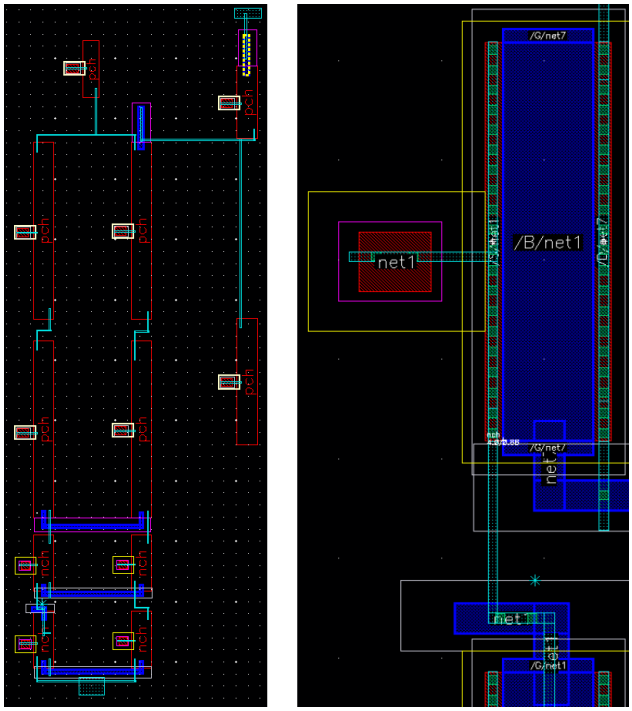

Fig. 9: Source Driver Layout

IV. Conclusion

The final result of our design is shown in the table below. Total power consumption was large because the design doesn't reuse currents and required a lot of power in the mirroring current sources. Total area used was also large because we were seeking to optimize the resistance of our source and sink by increasing Rout. To achieve the desired Rout, the current in the amplifiers is decreased. Additionally, L is increased to reduce the lambda term. This resulted in the scaling of both the W and L of the transistors.

The simulated charge mismatch was very close to zero and continued to decrease the longer the simulation ran. The charge difference between pulses was calculated as 1.6pC. The charge waveform shows approximately 11nC swing on the electrode charge and equates to nearly 0.015% error. The Voltage swing came out to be quite low. This was a result of using 1.85V and 0.6V as the two bias voltages of our op amps. In order for the devices to stay in saturation the voltage at the electrode needs to be larger than $0.6V + V_{DSat,Cas} + V_{DSat,Switch}$ and lower than $1.85V - V_{DSat,Cas} - V_{DSat,Switch}$ this calculates to our waveform swinging from about 1.05V to 1.45V.

In summary, the final design achieved a stable response and very good matching between sink and source currents on the electrode. However, it should be iterated to reduce power consumption and total area used.

If we had more time, we would have liked to place our focus on developing a more advanced switch to interface with the electrode. The switch in this design created problems by reducing our voltage swing and inhibiting current to the electrode. With more time, we could have created a more advanced switch that left less of an impact on our final current waveform.

Power Consumption	Transistor Areas	Charge Mismatch	Voltage Supply	Voltage Output Swing
0.62mW	$436\mu m^2$	$1.6pC$	2.5V	0.41V

V. Additional Figures

```
DM1.R.1 { @ DM1 is a must. The DM1 CAD layer (TSMC default, 31;1 for DM1) must be different from the M1 CAD layer.
  CHIPx NOT INTERACT DUM1
}
```

Fig. 10: Error Message: DM1.R.1

```
PO.DN.1L { @ Min. POLY density across full chip >= 14%
  DENSITY ALL_POLY CHIP < PO_DN_1_L INSIDE OF LAYER CHIPx PRINT PO.DN.1L.density
  [ AREA(ALL_POLY)/AREA(CHIP) ]
}
```

Fig. 11: Error Message: P0.DN.1L

	W	**L**	**Area**				
Source Driver							
M0	5.30E-06	9.35E-07	4.96E-12		PMOS Cascode		
M2	9.81E-06	9.30E-07	9.12E-12		1.25V*99.79uA	0.0001247375	
M4	4.00E-06	8.80E-07	3.52E-12				
M5	4.00E-06	8.80E-07	3.52E-12				
M6	1.40E-05	8.80E-07	1.23E-11		PMOS Op Amp		
M7	1.40E-05	8.80E-07	1.23E-11		2.5V * 18.46uA	0.000046175	
M8	1.40E-05	8.80E-07	1.23E-11				
M9	1.40E-05	8.80E-07	1.23E-11				
M10	4.00E-06	8.80E-07	3.52E-12				
M11	4.00E-06	8.80E-07	3.52E-12				
M20	4.00E-06	6.00E-07	2.40E-12				
		Sum	7.98E-11				
Source PTAT					Source PTAT		
M0	6.00E-06	1.30E-06	7.80E-12		2.5V * 82.49uA	0.000206225	
M1	6.00E-06	1.30E-06	7.80E-12				
M3	6.00E-06	1.30E-06	7.80E-12				
M21	6.00E-06	1.30E-06	7.80E-12				
R1		298 Ohms			Sum of Source Driver + PTAT		
Q0	5.00E-06	5.00E-06	2.50E-11		1.86E+02		
Q1 (n=2)	5.00E-06	5.00E-06	5.00E-11				
		Sum	1.06E-10				
Sink Driver							
M4	1.20E-05	7.50E-07	9.00E-12		NMOS Op Amp		
M5	1.20E-05	7.50E-07	9.00E-12		2.5V * 35.23uA	0.000088075	
M6	9.00E-06	7.50E-07	6.75E-12				
M7	9.00E-06	7.50E-07	6.75E-12				
M8	9.00E-06	7.50E-07	6.75E-12				
M9	9.00E-06	7.50E-07	6.75E-12				
M10	1.20E-05	7.50E-07	9.00E-12				
M11	1.20E-05	7.50E-07	9.00E-12				
M18	2.00E-06	2.00E-07	4.00E-13				
M19	1.58E-06	6.00E-07	9.45E-13				
M20	2.00E-06	1.40E-06	2.80E-12				
		Sum	6.71E-11				
Sink PTAT							
Q1	5.00E-06	5.00E-06	2.50E-11		Sink PTAT		
Q2 (n=2)	5.00E-06	5.00E-06	5.00E-11		2.5V * 63.4uA	0.0001585	
M0	2.00E-06	1.40E-06	2.80E-12				
M1	2.00E-06	1.40E-06	2.80E-12				
M2	2.00E-06	1.40E-06	2.80E-12				
M3	2.00E-06	1.40E-06	2.80E-12				
M4	2.00E-06	1.40E-06	2.80E-12				
R1		4.60E+04					
		Sum	8.90E-11			Total Power Consumed (W)	
		SUM	4.36E-10			0.0006237125	0.6237125

Fig. 12: Transistor Summary