**Submission Instructions:**

Please strictly follow Assignment 1 instructions**.**

**Assignment Instructions:**

Use binary (or hex) and fill out the tables below.

Assume that the contents of register $Ri is 3\*i (e.g., register 20 contains 60). Use N/A for non-applicable

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Instruction Fetch:**  IR 🡸 IM[PC]  PC 🡸 PC+4;  Branch 🡨 0  Jump 🡨 0 // **only for the J inst.**  A 🡸 PC  **Instruction Decode:**  CLU 🡸 IR[31:26]  Read\_Register\_1 🡸 IR[25:21] // &Rs  Read\_Register\_2 🡸 IR[20:16] // &Rt  Write\_Register 🡸 IR[15:11] // &Rd  C 🡸 A // PC+4  D 🡸 RF[IR[25:21]] // \*Rs  E 🡸 RF[IR[20:16]] // \*Rt  F 🡸 SE[IR[15:0]] // Sign extended constant (immediate)  G 🡸 IR[20:16] // &Rt  H 🡸 IR[15:11] // &Rd  X 🡸 IR[25-0] // **only for the j inst.** | 0x12341234 start: lw $t1, 200 ($t0)  ori $s0, $s1, -2  j start  bne $s0, $s1, start  sw $s1, 400 ($s0)  xor $a3, $a1, $a2   |  |  | | --- | --- | | IR[31:26] | ‘R-type’ | | IR[25:21] | ‘00101’ | | IR[20:16] | ‘00110’ | | IR[15:11] | ‘00111’ | | IR[10:6] | 000000 | | IR[5:0] | ‘xor’ |  |  |  | | --- | --- | | IR[31:26] | ‘j’ instruction | | IR[25:20] | 0x08D048D |  |  |  |  |  |  | | --- | --- | --- | --- | --- | | IR[31:26] | ‘ori’ | ‘lw’ | ‘sw’ | ‘bne’ | | IR[25:21] | ‘10001’ | ‘01000’ | ‘10000’ | ‘10000’ | | IR[20:16] | 10000 | ‘01001 | 10001 | 10001 | | IR[15:0] | -2 | 200 | 400 | -4 | |

|  |  |
| --- | --- |
| xor | bne |
| **IF**  IR 🡸 ‘R-Type’  Branch 🡨 0  PC 🡸  A 🡸 0x1234124C  **ID**  CLU 🡸 000000  RR\_1 🡸 5  RR\_2 🡸 6  WR 🡸 7  C 🡸 A  D 🡸 10  E 🡸 12  F 🡸  G 🡸 6  H 🡸7 | **IF**  IR 🡸 ‘I-Type’  Branch 🡨 0  PC 🡸  A 🡸 0x12341244  **ID**  CLU 🡸 000101  RR\_1 🡸 16  RR\_2 🡸 17  WR 🡸  C 🡸 A  D 🡸 16  E 🡸 17  F 🡸 -4  G 🡸 17  H 🡸 |

|  |  |
| --- | --- |
| lw | sw |
| **IF**  IR 🡸 ‘I-Type’  Branch 🡨 0  PC 🡸  A 🡸 0x12341234  **ID**  CLU 🡸 100011  RR\_1 🡸 8  RR\_2 🡸 9  WR 🡸  C 🡸 A  D 🡸 16  E 🡸 18  F 🡸 -2  G 🡸 9  H 🡸 | **IF**  IR 🡸 ‘I-Type’  Branch 🡨 0  PC 🡸  A 🡸 0x12341248  **ID**  CLU 🡸 101011  RR\_1 🡸 16  RR\_2 🡸 17  WR 🡸  C 🡸 A  D 🡸 16  E 🡸 17  F 🡸 400  G 🡸 17  H 🡸 |

|  |  |
| --- | --- |
| ori | j |
| **IF**  IR 🡸 ‘I-type’  Branch 🡨 0  PC 🡸  A 🡸 0x12341238  **ID**  CLU 🡸 001101  RR\_1 🡸 8  RR\_2 🡸 9  WR 🡸  C 🡸 A  D 🡸  E 🡸  F 🡸 -2  G 🡸 9  H 🡸 | **IF**  IR 🡸 ‘J-type’  Branch 🡨 0  Jump 🡨1  PC 🡸  A 🡸 0x12341240  **ID**  CLU 🡸 000010  RR\_1 🡸  RR\_2 🡸  WR 🡸  C 🡸  D 🡸  E 🡸  F 🡸  G 🡸  H 🡸  X 🡸0x08D048D |