**EEL 4712C - Digital Design**

**Lab Report**

Due one week after regular lab completion.   
Delay penalty: 10% per week, maximum 20%

Cut-off date for submission: 2 weeks after deadline

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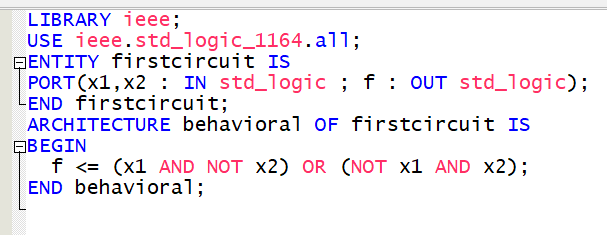
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**Prelab Report**

**Prelab Questions**

* Put all the answers to the prelab questions. These may be scanned using your phone or scanner. Not all prelabs have prelab questions.

**Prelab Design and Implementation**



**Reflection**

* **I was primarily stumped by the programmer device section of the tutorial. I followed all instructions during the installation process including installing the USB Blaster Driver. After troubleshooting, I still cannot program my device.**

**Prelab Homework**

* **Tutorials**
* **VHDL Syntax and Coding Questions**
  1. **A\_123, A123\_, c1\_\_c2, and1**
  2. **All are equivalent**
  3. **False**
  4. **A sequential statement happens in a sequential order, while concurrent happens all at the same time.**
  5. **Defining circuit:**
     + ENTITY firstcircuit IS
     + PORT(A,B,C,D : IN std\_logic ; G : OUT std\_logic);
     + END firstcircuit;
     + ARCHITECTURE behavioral OF firstcircuit IS
     + BEGIN
     + E <= A AND B;
     + F <= C OR E;
     + G <= D AND F;
     + END behavioral;
  6. X3 must be added to the list
  7. Truth Table

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| x1 | x3 | x2 | C | A | B | D | f |
| F | F | F | F | T | T | T | F |
| F | F | T | F | T | F | T | F |
| F | T | F | T | F | T | T | T |
| F | T | T | T | F | F | F | F |
| T | F | F | T | T | T | T | T |
| T | F | T | T | T | F | T | T |
| T | T | F | T | F | T | T | T |
| T | T | T | T | F | F | F | F |