**EEL 4712C - Digital Design**

**Lab Report**

Due one week after regular lab completion.   
Delay penalty: 10% per week, maximum 20%

Cut-off date for submission: 2 weeks after deadline

Cole Rottenberg

11062528

**Prelab Report**

**Prelab Questions**

* Put all the answers to the prelab questions. These may be scanned using your phone or scanner. Not all prelabs have prelab questions.

**Prelab Design and Implementation**

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**Reflection**

**Prelab Homework**

* **VHDL Syntax and Coding Questions**
  1. **A\_123, A123\_, c1\_\_c2, and1**
  2. **All are equivalent**
  3. **False**
  4. **A sequential statement happens in a sequential order, while concurrent happens all at the same time.**
  5. **Defining circuit:**
     + ENTITY firstcircuit IS
     + PORT(A,B,C,D : IN std\_logic ; G : OUT std\_logic);
     + END firstcircuit;
     + ARCHITECTURE behavioral OF firstcircuit IS
     + BEGIN
     + E <= A AND B;
     + F <= C OR E;
     + G <= D AND F;
     + END behavioral;

**Postlab Report**

**Problem Statement:**

* Provide a short informal description of the lab’s goals (From the lab assignment).
* If required, specify the system to design.
  + Define the inputs.
  + Define the outputs.
  + Define the function of your system.
* This section should be 1-2 paragraphs long.

**Design:**

* Describe the design decisions you made.
  + What components did you use?
  + What signals did you use to connect the components?
  + What algorithms were used.
* Code segment or block diagram may be used for illustrative purposes.
* Explain your design choices (pros/cons).
* Any designs made in the prelab should also be covered but more briefly.
* This section should be 1-2 paragraphs long.

**Implementation:**

* Describe your implementation process.
* Code segments or pictures may be used for illustrative purposes.
* What time did you need to complete your design?
* This section should be 1-2 paragraphs long.

**Testing:**

* Describe how you tested your design.
* Did everything work as expected?
  + Did the inputs match the expected outputs?
  + Special cases.
* Include if possible, timing diagram of photograph/video of the system.

**Conclusions:**

* Summarize in one paragraph, the work you did, the success and problems you encountered and how to improve next in the future.
* This section should be 1paragraph long.

**Appendix**

* Include all postlab code, screenshots, pictures, and simulations here. **All simulations must be annotated**. All figures must be captioned. Code should be commented on a fair amount.