Chapter 10

Lab 10 - Final Project

10.1 Objective

The objective of the final project is to bring together concepts taught in previous labs in to a single circuit.

10.2 Materials

- Laptop with LTSpice
- Analog Discovery
- Breadboard
- Wiring kit
- Lab parts kit with TLV272 and LM393P
- Speakers with 3.5mm connector

10.3 Introduction

The nature of the lab will be different to accommodate the final project. With a total score that accounts for 20% of the entire lab grade, the final project is required to pass the course. There is no quiz for the final project and the breakdown is as follows:

- 20% Pre-lab
- 40% In-lab Demonstration (This includes building your final circuit on a provided printed circuit board)
- 40% Write up

The pre-lab simply requires a working spice schematic with the correct outputs, this is much simpler than it sounds. Source files for the spice simulation are available on Canvas under the Labs folder, Jingle4.wav and Jingle19.wav. The wav files can be imported in to LTspice using the following instructions, `http://www.linear.com/solutions/6087`. The final simulation, the simulation that's submitted to Canvas, must use the Jingle19.wav file and a transient simulation that's 19 seconds long (.tran 19). Because of the total time to complete the simulation, several minutes, a shorted file has been provided, Jingle4.wav, which runs for four seconds.

Failure to complete the pre-lab will result in a zero for 20% of the final project and being barred from the first lab sessions. A student will not however receive a zero for the entire lap project.

Lab sessions for the final project will span two weeks and exist purely for the student to demo their working breadboard circuit using the in-lab speakers and connector. Because there isn't enough connectors or speakers for students to take them home, both items must remain in the lab. The deadline to have a circuit checked off is approximately the end of the second lab session. Students are not allowed to demo their circuit during lab sessions that are not their own or during office hours.

The write up for the project is also different, see the template in the files section, and the due time for the final report will be announced in Canvas.

10.3.1 Audio Amplifier

The final project is a basic audio amplifier with a block diagram shown below in Figure 10.1. A simple jingle with a small amplitude, mV, and a large DC offset, 0.5 V, will serve as the input. The system functions as follows.

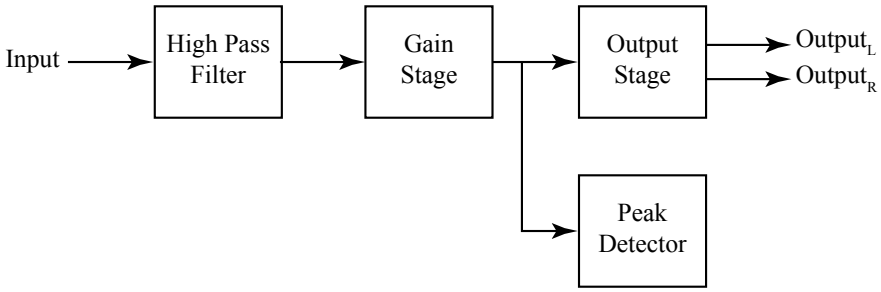

Figure 10.1: Audio amplifier block diagram.

- The high pass filter removes the DC offset from the jingle, effectively AC coupling the signal in to the system.
- A gain stage is used to amplify the jingle to a range of volts from mV so that it can be heard from the speakers.

State	LED 1	LED 2
Input < Threshold 1 and 2	Off	Off
Threshold 1 < Input < Threshold 2	On	Off
Threshold 1 and 2 < Input	On	On

Table 10.1: Different states for the peak detector

- An output stage must buffer the output to the speakers, the outputs do not need to be offset in phase.
- A peak detector is also required in order to indicate when the output is in the right range, defined by two thresholds. When the output passes the first threshold (LED 1 turns on), the output is operating in the normal linear range with an output on the order of Volts, and the second threshold (LED 2 turns on), where the output is about to start clipping. See the different LED states in Table 10.1. Note that this is a slight variation on the circuit used in the diode lab.

10.3.2 Recommendations

A few words on some of the individual sections.

- As always, you're limited to the components in your lab kit, not the Digilent student kit, choose your values wisely.
- Choose the 3 dB frequency of the high pass filter carefully. The audio band is 20 Hz to 20 kHz and a 3 dB frequency in the kHz will attenuate (weaken/shrink) important parts of the jingle. Good rule of thumb is if you are over 1 KHz then you are too high. However don't choose it too low, aim for higher than 50 Hz.
- The required gain is high, and amplification should occur in two stages. One stage will have a fixed gain. This will be your active high pass filter, both accomplishing the needed filtering and providing gain. The next stage will be another amplifer with variable gain (using a potentiometer as the input resistor). This will allow for a variable voltage on the output signal.
- The output stage should be trivial.
- Choose the voltage thresholds for the peak detector so that at a reasonable gain, one LED is always on and the other only turns on when the output starts, or is about to start, to clip or distort.
- Use of the active high pass filter for your first stage eliminates the loading effect.

- The circuit should pass a demo using sine wave (10 mV amplitude, 1 KHz, 0.5 V DC offset) as input and the peak detection circuit's Threshold 1 and Threshold 2 voltages should be 1 V and 4 V. Both LED should be off when the input is <1 V, one LED on when the input is between 1 V and 4 V for OPAMP's linear range operation, then both LEDs should be on when the input is >4 V to indicate OPAMP's output is getting into saturation range. The comparator's input configuration is different than Lab 8's, don't copy it directly.
- Output stage should have two buffers (for channels L and R).
- After you finish the demo and verification of your final project circuits, you need to continue to perform more measurement using scope, spectrum analyzer and network analyzer functions. Follow the file "Final Project Write Up Template" to complete your final report.
- Due time for the final report will be announced in Canvas.

And some more general advice.

- Build everything in LTspice before doing any work on a breadboard.
- The spice simulation of the 19 second jingle file will take a long time, several minutes. The 4 second jingle will also take a few minutes. Start instead with a 10 mV amplitude 1 kHz sine wave with a 0.5 V DC offset and a transient simulation of 1m (.tran 1m). Once you have that working, start using the jingle files.
- Use virtual net nodes instead of making various +5 V and -5 V supplies.
- All of the active components are powered by +5 V and -5 V supplies.
- When it's time to build the circuit on a breadboard, build the circuit in a linear fashion. The input should start at one end with the output at the other, don't make it a maze.
- Use color coded wires to make debugging easier and avoid creating extra nodes whenever possible. The more nodes in the circuit, the less likely it's going to work.
- Build stages one at a time to confirm that they're working as opposed to building everything at once and then trying to debug everything at once.
- Complete both the prelab and the first demo of the project in the first week, there's a test the second week and it's better to simply get these out of the way. During the second week you will also need to make time to solder the parts from the project on to a provided PCB for the final demo.
- Once you've demoed your circuit, don't take it apart, you'll still need it for items in the write up. It is recommended to complete all measurements required by the write up before soldering to the PCB.

10.4 Pre-Lab Requirements

This following must be completed and submitted to Canvas by the start of lab.

1. Image of the spice schematic and a plot of the input and all subsequent outputs (outputs of each individual stage) for a transient simulation for Jingle19 submitted to Canvas. Include the plot of the output and a circuit schematic, nothing else. The schematic and plot should be appropriately labeled. Images that are unclear or vague will receive little to no points. Your plot must include the following in **different plot planes**: input voltage, output of the high pass filter, output of the variable gain amplifier, output of the buffer stage (at least one), and the current of both LEDs. The gain doesn't need to be high enough to induce clipping in order to show that both LEDs turn on but the first LED should turn on.

10.5 In-Lab Requirements

Unlike previous labs, the final project lab spans two weeks (two lab sessions). The final project in-lab portion is only complete once a student has demoed a working circuit on both the breadboard and on a fully soldered PCB (printed circuit board, this will be provided). There are two steps to demonstrating a circuit is working:

1. Using an input of a 10 mV amplitude sine wave with a 0.5 V DC offset, demonstrate that that the output can be varied and the peak detectors functions properly.

2. Using the 19 second jingle file as an input, demonstrate that the output can be heard on both speakers and the peak detector functions properly.

A student can demonstrate their working circuit during either of the two lab sessions, but only in their lab session, not during another lab session or office hours. There are a limited number of connectors and speakers, they will only be handed out to a student once they have demonstrated the first step of the required demonstration.

10.5.1 Wavegen Settings and Speakers

In order to play the sound file, Jingle19.wav, it must be imported in to the Wavegen's player. Instead of simple, choose play from the pulldown. Click import and then select the Jingle19.wav file. You'll be given a list of options and a plot of the signal, leave the settings to their default and select ok. Hit run to start the jingle playing.

The 3.5mm connector has three right angle pins soldered to it which allow it to be used with a breadboard. The center pin is ground and the other two pins connect to a speaker. Because the outputs are simply buffered, there's no need for a distinction between left and right.

10.6 Write Up

The write up is also different for the lab project, it takes the form of a formal report. See the template for details. The write up due time will be posted to Canvas, and is typically due around the end of the semester.