

# EEL 4712C - Digital Design: Lab Report 2

Cole Rottenberg  
11062528

February 18<sup>th</sup>, 2024

```
1 — This is a test VHDL code block
2 library IEEE;
3 use IEEE.STD_LOGIC_1164.ALL;
4 use IEEE.STD_LOGIC_ARITH.ALL;
5
6 entity test is
7     Port ( a : in   STD_LOGIC;
8           b : in   STD_LOGIC;
9           c : out  STD_LOGIC);
10 end test;
```

Listing 1: Test VHDL Code

## Prelab Report

### Prelab Questions

#### Demo:

1. Using the provided top\_level.vhd, the 7-segment display entity you created in Lab 0, and the provided fsm.vhdp synthesize your circuit.
2. In Quartus, assign pins to the inputs (switches & buttons) and outputs (LEDs) such that the correct outputs are displayed on the 7-segment display.
3. Show your TA the RTL viewer showing the properly synthesized datapath.
4. Once the everything is working, show a TA the correct output for  $\text{Fib}(11) = 89$ .

Prelab Design and Implementation

Reflection

Prelab Homework

**Postlab Report**

Problem Statement

Design

Implementation

Testing

Conclusions

Appendix