EEL 4712C - Digital Design: Lab Report 2

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```vhdl
-- This is a test VHDL code block
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;

entity test is
    Port ( a : in  STD_LOGIC;
           b : in  STD_LOGIC;
           c : out  STD_LOGIC);
end test;
```

Listing 1: Test VHDL Code

Prelab Report

Prelab Questions

Demo:

1. Using the provided top_level.vhd, the 7-segment display entity you created in Lab 0, and the provided fsm.vhdp synthesize your circuit.
2. In Quartus, assign pins to the inputs (switches buttons) and outputs (LEDs) such that the correct outputs are displayed on the 7-segment display.
3. Show your TA the RTL viewer showing the properly synthesized datapath.
4. Once the everything is working, show a TA the correct output for Fib(11) = 89.