# EEL 4712C - Digital Design: Lab Report

Cole Rottenberg

11062528

Due Date

```vhdl
1  -- This is a test VHDL code block
2  library IEEE;
3  use IEEE.STD_LOGIC_1164.ALL;
4  use IEEE.STD_LOGIC_ARITH.ALL;
5
6  entity test is
7      Port ( a : in   STD_LOGIC;
8             b : in   STD_LOGIC;
9             c : out   STD_LOGIC);
10 end test;
```

Listing 1: Test VHDL Code

# Prelab Report

## Prelab Questions

## Prelab Design and Implementation

## Reflection

## Prelab Homework

# Postlab Report

## Problem Statement

## Design

## Implementation

## Testing

## Conclusions

# Appendix